

16Mb (1M x 16 bit) U t RAM

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Document Title

1Mx16 bit Multiplexed Uni-Transistor Random Access Memory

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial - Design target	December 19, 2006	Preliminary
0.1	Revised - Updated package dimension	Januayr 11, 2007	Preliminary

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K1B1616B8B

UtRAM

1M x 16 bit Multiplexed Uni-Transistor CMOS RAM

GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need bigger & faster memory capacity to handle the multi-media data. SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market. UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature. K1B1616B8B is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous read and asynchronous write), the NOR flash like synchronous operation (synchronous burst read and asynchronous write) and the fully synchronous operation (synchronous burst read and synchronous burst write). These three operation modes are defined through the mode register setting. The device also supports the special features for the standby power saving. Those are the Partial Array Refresh(PAR) mode, Deep Power Down(DPD) mode and internal TCSR (Temperature Compensated Self Refresh). The optimization of output drive strength is possible through the mode register setting to adjust for the different data loadings. Through this drive strength optimization, the device can minimize the noise generated on the data bus during read operation.

FEATURES

- Process technology: CMOS
- Organization: 1M x 16 bit
- Multiplexed Address and Data bus
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports MRS (Mode Register Set)
 - Software set up
- Supports power saving modes
 - PAR (Partial Array Refresh)
 - DPD (Deep Power Down)
 - Internal TCSR (Temperature Compensated Self Refresh)
- Supports driver strength optimization
- K1B1616B8B supports
 - Asynchronous read/ Asynchronous write
 - Synchronous burst read / Asynchronous write
 - Synchronous burst read / Synchronous burst write
- Synchronous burst operation
 - Max. clock frequency : 104MHz
 - Fixed and Variable read latency
 - 4 / 8 / 16 / 32 and Continuous burst
 - Wrap / No-wrap
 - Latency : 4(Variable) @ 104MHz
3(Variable) @ 80MHz
2(Variable) @ 66MHz
- Burst stop
- Burst read suspend
- Burst write data masking

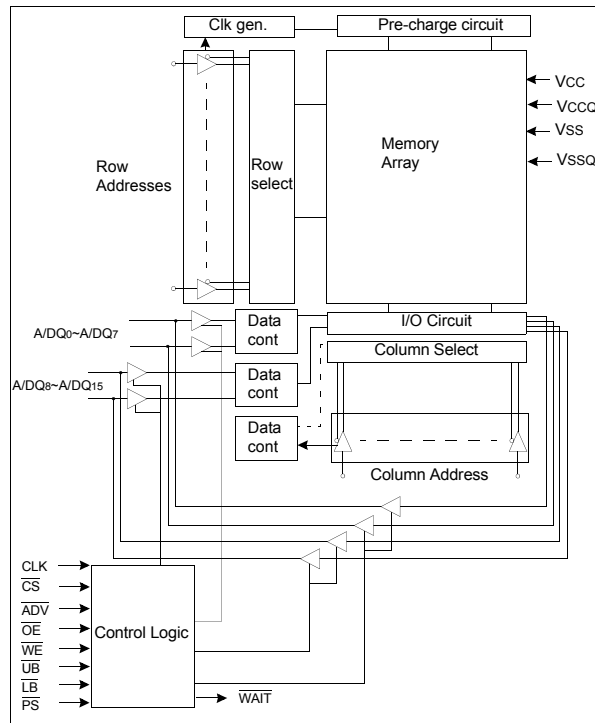
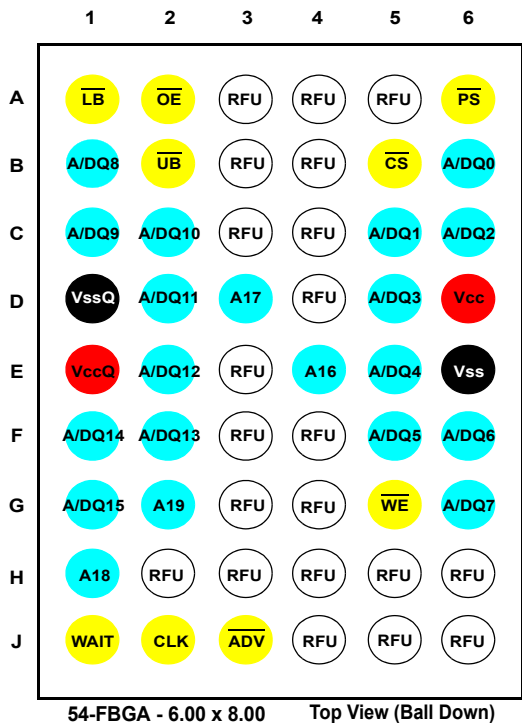
PRODUCT FAMILY

Product Family	Operating Mode ¹⁾	Operating Temp.	Vcc Range	Speed	Current Consumption	
					Standby (I _{sb1} , Max.)	Operating (I _{cc2} , Max.)
K1B1616B8B-I	Mode 1 Mode 2 Mode 3	Industrial(-40~85°C)	1.7~1.95V	104MHz	TBD < 85°C TBD < 40°C	TBD

1) Mode 1: Asynchronous read/ Asynchronous write
 Mode 2: Synchronous burst read/ Asynchronous write
 Mode 3: Synchronous burst read/ Synchronous burst write

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PIN DESCRIPTIONS & FUNCTION BLOCK DIAGRAM



TERMINOLOGY DESCRIPTION

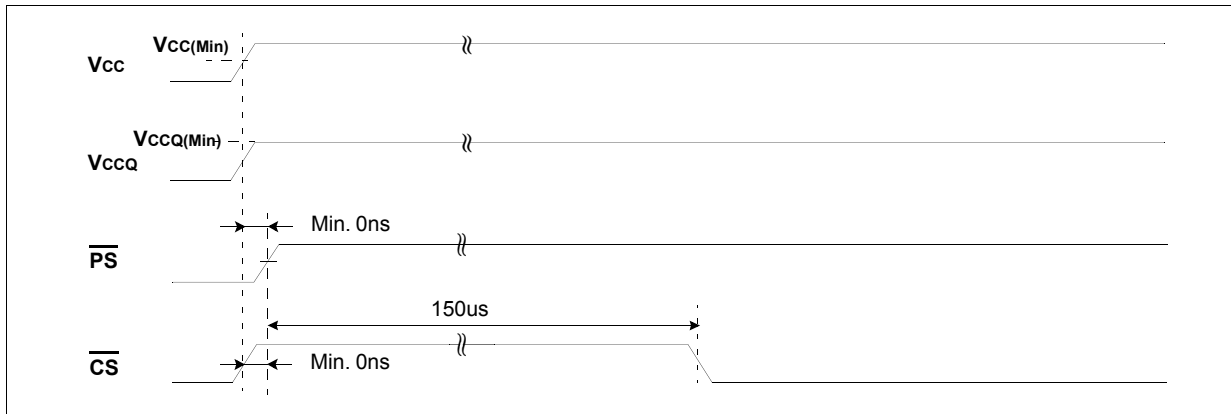
Name	Function	Type	Description
CLK	Clock	Input	Synchronizes the memory to the system operating frequency during synchronous operations. Commands are referenced to CLK.
ADV	Address Valid	Input	Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV during asynchronous READ and WRITE operations.
PS	Mode Register set	Input	PS low enables either PAR or DPD to be set.
CS	Chip Select	Input	CS low enables the chip to be active CS high disables the chip and puts it into standby mode or deep power down mode.
OE	Output Enable	Input	Enables the output buffers when LOW. when OE is HIGH, the output buffers are disabled.
WE	Write Enable	Input	WE low enables the chip to start writing the data
LB	Lower Byte (I/O0~7)	Input	UB (LB) low enables upper byte (lower byte) to allow data Input/output from I/O buffers.
UB	Upper Byte (I/O8~15)	Input	
A16~A19	Address 16 ~ Address 19	Input	Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles.
A/DQ0~A/DQ15	Address and Data Inputs / Outputs	Input/Output	Address and Data I/Os: These pins are multiplexed address/ data bus.
Vcc	Voltage Source	Power	Device Power supply. Power supply for device core operation.
VccQ	I/O Voltage Source	Power	I/O Power supply. Power supply for input/output buffers.
Vss	Ground Source	GND	Ground for device core operation
VssQ	I/O Ground Source	GND	Ground for input/output buffers
WAIT	Valid Data Indicator	Output	The WAIT signal is output signal indicating the status of the data on the bus whether or not it is valid. WAIT is asserted when a burst crosses a word-line boundary. WAIT is asserted and should be ignored during asynchronous mode operations.

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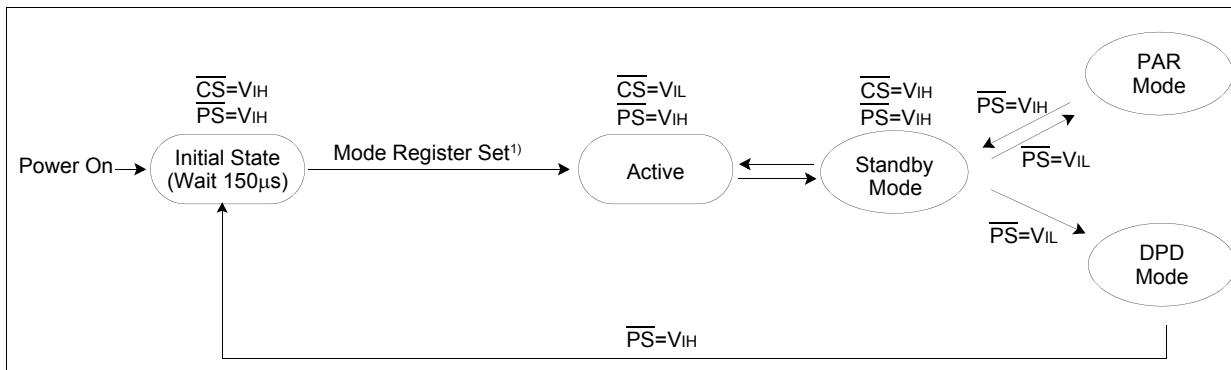
UtRAM

POWER UP SEQUENCE

After V_{CC} and V_{CCQ} reach minimum operating voltage(1.7V), drive \overline{CS} High first and then drive \overline{PS} High. Then the device gets into the Power Up mode. Wait for minimum 150 μ s to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence. Mode1 (Asynchronous read/ Asynchronous write) is set up after power up, but this mode is not always guaranteed.



MODE STATE MACHINE



1) Refer to MRS(Mode Register Set).

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to VCCQ+0.3V	V
Power supply voltage relative to Vss	VCC, VCCQ	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	VCC	1.7	1.8	1.95	V
Power supply voltage(I/O)	VCCQ	1.7	1.8	1.95	V
Ground	Vss, VSSQ	0	0	0	V
Input high voltage	V _{IH}	VCCQ-0.4	-	VCCQ+0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.

2. Overshoot: VCCQ+1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.

3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit		
Input Leakage Current	I _{LI}	V _{IN} =Vss to VCCQ	-1	-	1	μA		
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{PS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =Vss to VCCQ	-1	-	1	μA		
Average Operating Current(Async)	I _{CC2} ⁶⁾	Cycle time=70ns, I _{IO} =0mA ⁴⁾ , 100% duty, $\overline{CS}=V_{IL}$, $\overline{PS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	TBD	mA		
Average Operating Current(Sync)	I _{CC3}	Burst Length 4, Latency 5, 80MHz, I _{IO} =0mA ⁴⁾ , Address transition 1 time, $\overline{CS}=V_{IL}$, $\overline{PS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	TBD	mA		
Output Low Voltage	V _{OL}	I _{OL} =0.1mA	-	-	0.2	V		
Output High Voltage	V _{OH}	I _{OH} =-0.1mA	1.4	-	-	V		
Standby Current(CMOS)	I _{SB1} ¹⁾	$\overline{CS} \geq VCCQ-0.2V$, $\overline{PS} \geq VCCQ-0.2V$, Other inputs=Vss or VCCQ (Toggle is not	< 40°C	-	-	TBD	μA	
			< 85°C	-	-	TBD	μA	
Partial Refresh Current	I _{SBP} ²⁾	$\overline{PS} \leq 0.2V$, $\overline{CS} \geq VCCQ-0.2V$, Other inputs=Vss or VCCQ (Toggle is not allowed) ⁵⁾	< 40°C	1/2 Block	-	-	TBD	μA
				1/4 Block	-	-	TBD	
			< 85°C	1/2 Block	-	-	TBD	μA
				1/4 Block	-	-	TBD	
Deep Power Down Current	I _{SD}	$\overline{PS} \leq 0.2V$, $\overline{CS} \geq VCCQ-0.2V$, Other inputs=Vss or VCCQ (Toggle is not allowed) ⁵⁾	< 85°C	-	-	TBD	μA	

1. I_{SB1} is measured after 60ms after \overline{CS} high. CLK should be fixed at high or at Low.

2. Full Array Partial Refresh Current(I_{SBP}) is same as Standby Current(I_{SB1}).

3. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle below 40°C.

4. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

5. V_{IN}=0V; all inputs should not be toggle.

6. Clock should not be inserted between \overline{ADV} low and \overline{WE} low during Write operation.

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UtRAM

MRS (MODE REGISTER SET)

The mode registers store the values for the various modes to make UtRAM suitable for a various applications through MRS. The mode registers have lots of fields and each field consists of several options. Refer to the Table below for detailed Mode Register Setting. A19 addresses are "Don't care" in Mode Register Setting.

MRS CODE

MRS code consists of 12 categories and several options in each category. RARS, PARA, PAR and DPD are related to power saving, BL, WC, Latency, Wrap, WP, MS and IL are related to bus operation and DS is related to device output impedance.

Mode Register Setting according to field of function

Address	A18	A17~A16	A/DQ15~A/DQ14	A/DQ13	A/DQ12	A/DQ11~A/DQ9	A/DQ8	A/DQ7~A/DQ5	A/DQ4	A/DQ3	A/DQ2	A/DQ1~A/DQ0
Function	IL	DS	MS	WP	Wrap	Latency	WC	BL	DPD	PAR	PARA	PARS

Initial Latency		Driver Strength				Mode Select				
A18	IL	A17	A16	DS	A/DQ15	A/DQ14	MS			
0	Fixed	0	0	Full Drive	0	0	Mode 1 (Async. Read / Async. Write)			
1	Variable	0	1	1/2 Drive	0	1	Mode 2 (Sync. Burst Read / Async. Write)			
		1	0	1/4 Drive	1	0	Mode 3 (Sync. Burst Read / Sync. Burst Write)			

WAIT Polarity		Wrap		Latency Count				Wait Configuration		Burst Length			
A/DQ13	WP ¹⁾	A/DQ12	Wrap	A/DQ11	A/DQ10	A/DQ9	Latency	A/DQ8	WC	A/DQ7	A/DQ6	A/DQ5	BL
0	Low Enable	0	Wrap	1	0	0	2	0	One clock prior	0	1	0	4 word
1	High Enable	1	No-Wrap	0	0	0	3	1	At data	0	1	1	8 word
				0	0	1	4			1	0	0	16 word
				0	1	0	5			1	0	1	32 word
				0	1	1	6			1	1	1	Continuous ²⁾
				1	0	1	7						
				1	1	0	8						
			9										

Deep Power Down		Partial Array Refresh		PAR Array		PAR Size		
A/DQ4	DPD	A/DQ3	PAR	A/DQ2	PARA	A/DQ1	A/DQ0	PARS
0	DPD Enable	0	PAR Enable	0	Bottom Array	0	0	Full Array
1	DPD Disable	1	PAR Disable	1	Top Array	1	0	1/2 Array
						1	1	1/4 Array

[Note]

- A19 addresses are "Don't care" & reserved for future use.

- The modes are set automatically to default modes which are Async. Read and Async. Write/ DPD disable / PAR disable after power up or DPD exit.

- Mode Change Rules.

Mode1(2) to Mode3 : 1 dummy write(to any address with any data) is necessary before setting Mode3

* Dummy write: Dummy write timing is just the same with normal write timing. It is necessary because 'Late write' is applied to Asynchronous write as in Mode1(2).

* Late write: The data that is latched in previous write cycle is written in the address that is also latched in previous write cycle when Write starts. And current data and address are latched when Write ends. (WE high or CS high, whichever comes first)

Mode3 to Mode1(2) : 1 dummy write is necessary before setting Mode1(2)

* Dummy write: The data and the address should be the same with those which are used during Mode1(2) to Mode3 transition.

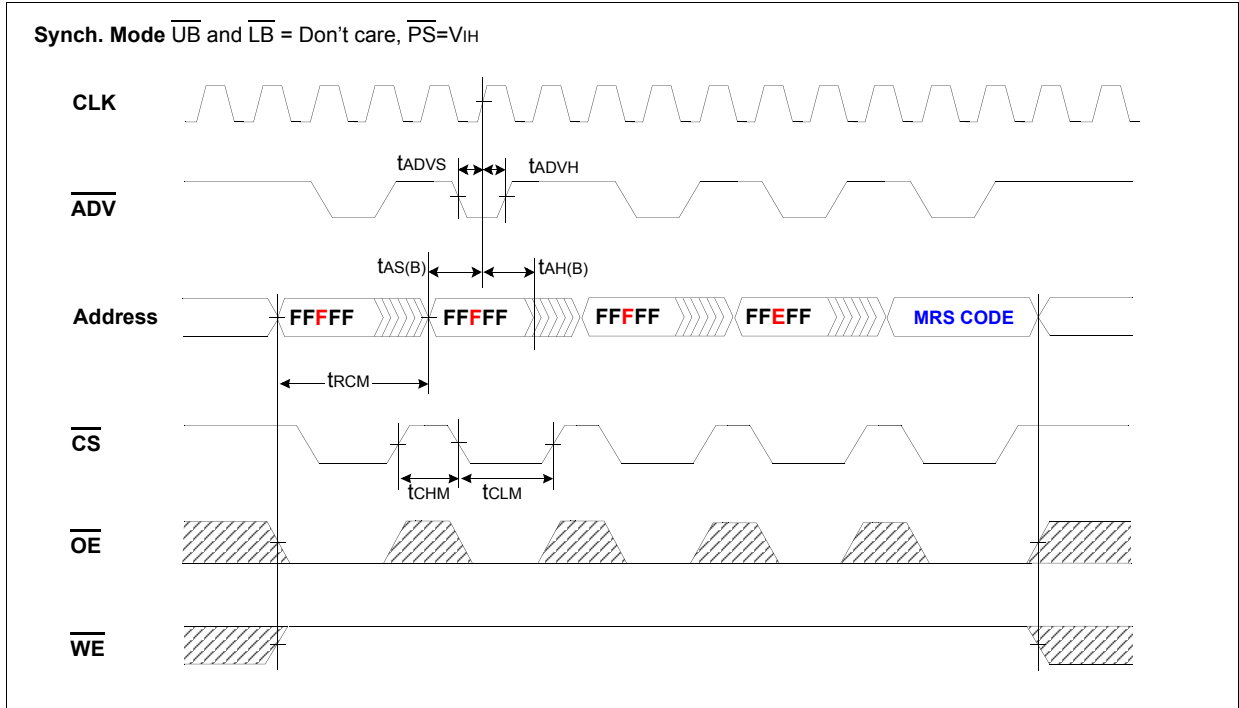
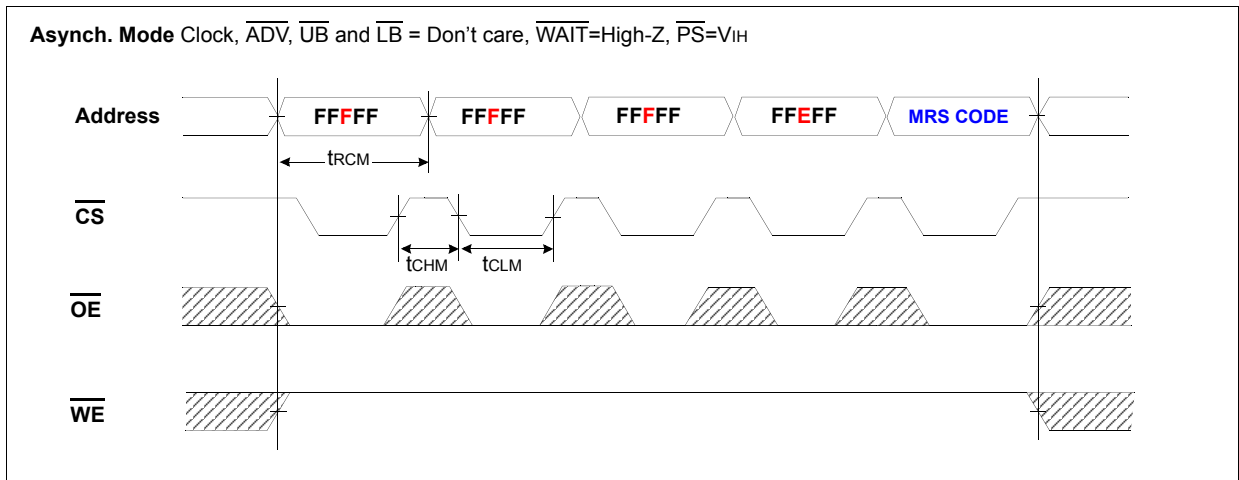
1) WP[0]: The data is available when $\overline{\text{WAIT}}$ signal is High. All the timings in this spec are illustrated based on this mode.

WP[1]: The data is available when WAIT signal is Low.

2) Refresh command will be denied during continuous operation. $\overline{\text{CS}}$ low should not be longer than tBC(max. 2.5us)

MRS TIMING WAVEFORM (SOFTWARE)

Software MRS timing consists of 5 Read cycles. Each cycle is normal Read cycle. \overline{CS} pin should be toggling between cycles. 1st, 2nd and 3rd cycle should be FFFF(h), 4th cycle should be FFEFF(h) and 5th cycle should be MRS code



Note) Above timing and address condition should not be used in the normal operation. The above condition should be used only for the mode register setting purpose.

AC CHARACTERISTICS

Parameter List	Symbol	Min	Max	Units	Parameter List	Symbol	Min	Max	Units
\overline{ADV} setup time to clock	tADVS	3	-	ns	Read cycle time	tRCM	70	-	ns
\overline{ADV} hold time from clock	tADVH	2	-	ns	\overline{CS} high time	tCHM	10	-	ns
Address setup time to clock	tAS(B)	3	-	ns	\overline{CS} low time	tCLM	60	-	ns
Address hold time from clock	tAH(B)	2	-	ns					

PAR (Partial Array Refresh) mode A/DQ[3]~A/DQ[0]

User can select half array, a fourth array as active memory array. The active memory array is periodically refreshed(data stored), whereas the disabled array is not going to be refreshed and so the previously stored data will be invalid. When re-enabling additional portions of the array, the new portions are available immediately upon writing to the MRS.

PAR mode execution;

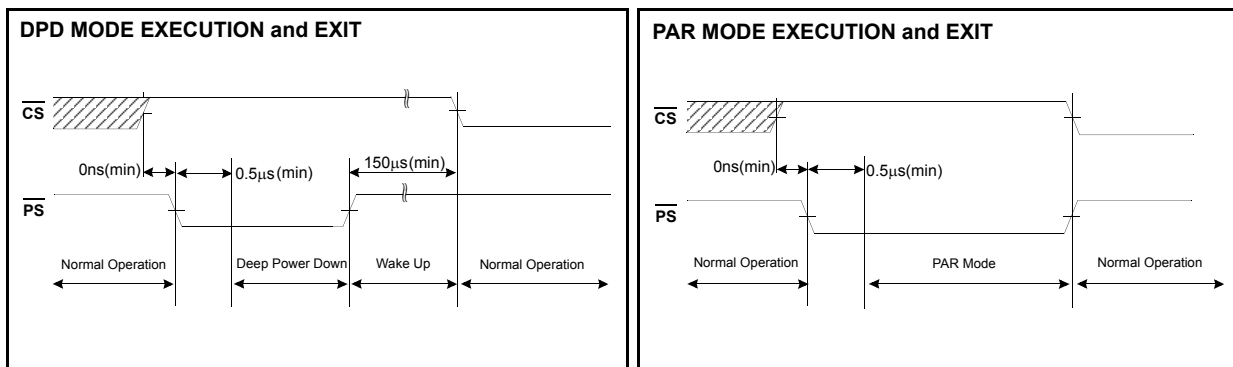
- 1) Mode Register Setting into PAR enable(A/DQ3=0)
DPD enabled setting(A/DQ4=0) has higher priority to PAR enabled setting(A/DQ3=0). A/DQ4=1 is necessary to use PAR mode.
 - 2) PAR mode Enter; keep \overline{PS} signal at V_{IL} for longer than 0.5 μ s during standby mode (Mode Register: A/DQ4=1 & A/DQ3=0).
 - 3) PAR mode Exit; The device returns to the standby mode when \overline{PS} signal goes to V_{IH} during PAR mode.
- * Mode register values are not changed after the device has been to PAR mode.

DPD (Deep Power Down) mode A/DQ[4]

The deep power down mode disables all the refresh related activities. This mode can be used when the system needs to save power. The data become invalid when DPD mode is executed.

DPD mode execution ;

- 1) Mode Register Setting into DPD enable(A/DQ4=0)
 - 2) DPD mode Enter; keep \overline{PS} signal at V_{IL} for more than 0.5 μ s during standby mode (Mode Register: A/DQ4=0).
 - 3) DPD mode Exit; The device returns to initial State when \overline{PS} signal goes to V_{IH} during DPD mode. Wake up sequence is needed for the device to do normal operation.
- * Mode register values are initialized to default value after the device has been to DPD mode.
Default modes are Async. Read and Async. Write / DPD disable / PAR disable.



STANDBY MODE CHARACTERISTICS

Power Mode	Address (Bottom Array) ²⁾	Address (Top Array) ²⁾	Memory Cell Data	Standby ³⁾ (ISB1, <40°C)	Standby ³⁾ (ISB1, <85°C)	Wait Time(µs)
Standby(Full Array)	00000h ~ FFFFFh	00000h ~ FFFFFh	Valid ¹⁾	TBD	TBD	0
Partial Refresh(1/2 Block)	00000h ~ 7FFFFh	80000h ~ FFFFFh	Valid ¹⁾	TBD	TBD	0
Partial Refresh(1/4 Block)	00000h ~ 3FFFFh	C0000h ~ FFFFFh	Valid ¹⁾	TBD	TBD	0
Deep Power Down	00000h ~ FFFFFh		Invalid	TBD	TBD	150

1. Only the data in the selected blocks are valid
2. PAR Array can be selected through Mode Register Set
3. Standby mode is supposed to be set up after at least one active operation after power up.
ISB1 is measured after 60ms from the time when standby mode is set up.

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Burst Length A/DQ[7]~A/DQ[5] & Wrap A/DQ[12]

The device supports 4 word, 8 word, 16 word, 32 word and Continuous burst read or write. and Wrap & No-Wrap are supported for Burst sequence.

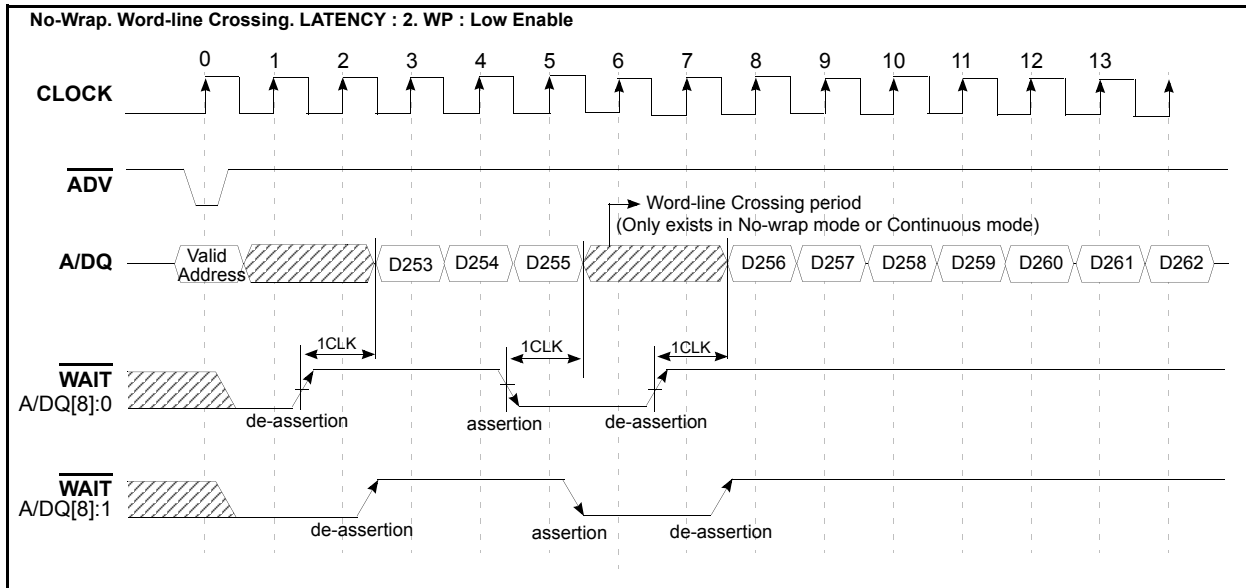
Burst Address Sequence(Decimal)					
Mode	Start	4 word	8 word	16 word	32 word
WRAP	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31 - 0
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31 - 0 - 1
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31- 0 - 1 - 2
	~		~	~	~
	7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7 - 8 - 9 - 10 - 11 - 12 ~ 2 - 3 - 4 - 5 - 6
	~		~	~	~
	15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20 ~ 10- 11- 12- 13- 14
~				~	
31				31- 0 - 1 - 2 - 3 - 4 ~ 25-26-27-28-29-30	
No-WRAP	0	0-1-2-3	0- 1- 2- 3- 4- 5- 6- 7	0- 1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-4	1- 2- 3- 4- 5- 6- 7- 8	1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31-32
	2	2-3-4-5	2- 3- 4- 5- 6- 7- 8- 9	2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31-32-33
	3	3-4-5-6	3- 4- 5- 6- 7- 8- 9-10	3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17-18	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31-32-33-34
	~		~	~	~
	7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7 - 8 - 9 - 10-11-12 ~ 33-34-35-36-37-38
	~		~	~	~
	15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-18-19-20 ~ 41-42-43-44-45-46
~				~	
31				31-32-33-34-35-36 ~ 57-58-59-60-61-62	

1. Continuous Burst mode needs to meet tBC(max. 2.5us) parameter.

WAIT Configuration A/DQ[8] & WAIT Polarity A/DQ[13]

The WAIT signal is output signal indicating the status of the data on the bus whether or not it is valid. WAIT configuration is to decide the timing when WAIT asserts or desserts. WAIT asserts (or desserts) one clock prior to the data when A/DQ8 is set to 0. (WAIT asserts (or desserts) at data clock when A/DQ8 is set to 1). WAIT polarity is to decide the WAIT signal level at which data is valid or invalid. Data is valid if WAIT signal is high when A/DQ13 is set to 0. (Data is valid if WAIT signal is low when A/DQ13 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; A/DQ[13]:0 and A/DQ[8]:0.

Below timing shows WAIT signal's movement when word boundary crossing happens in No-wrap mode.



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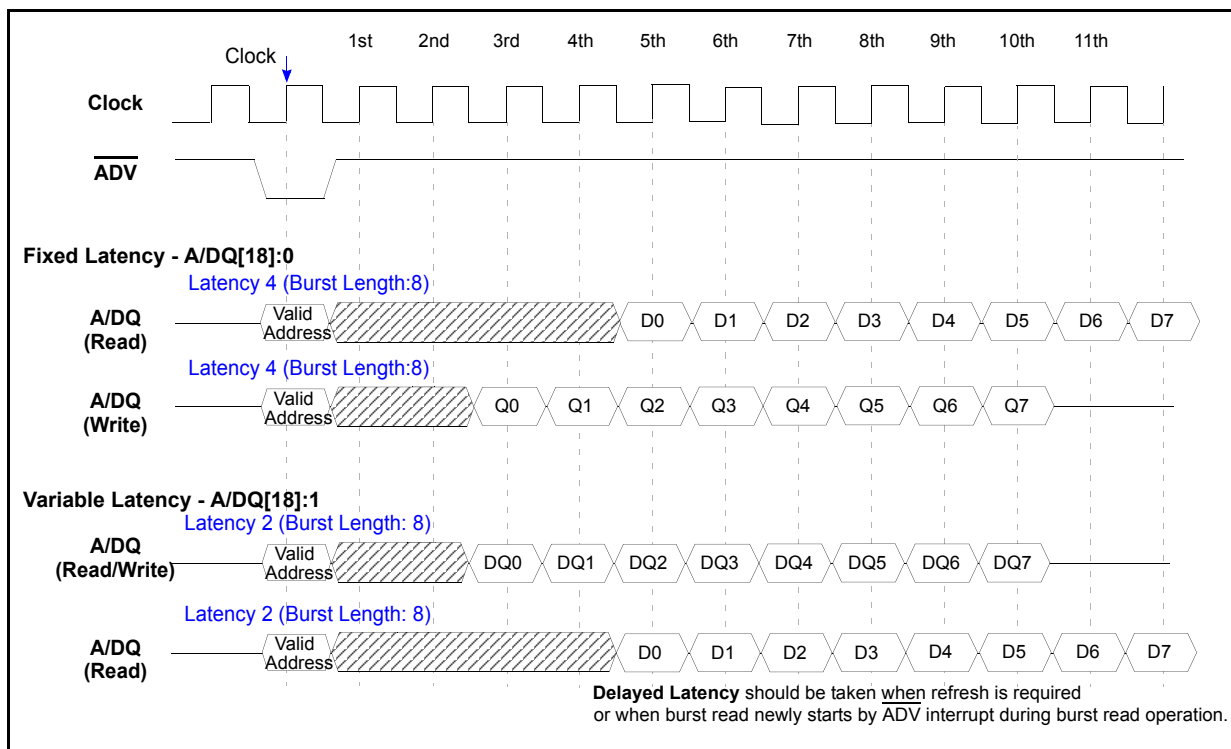
UtRAM

Latency A/DQ[11]~A/DQ[9]

The Latency stands for the number of clocks before the first data available from the burst command.

Item	Upto 66MHz		Upto 80MHz		Upto 104MHz	
	Fixed	Variable	Fixed	Variable	Fixed	Variable
Latency Set(A/DQ11:A/DQ10:A/DQ9)	4(0:0:1)	2(1:0:0)	5(0:1:0)	3(0:0:0)	7(1:0:1)	4(0:0:1)
Read Latency(min)	4	2 / 4 ¹⁾	5	3 / 5 ¹⁾	7	4 / 7 ¹⁾
1st Read data fetch clock	5th	3rd / 5th ¹⁾	6th	4th / 6th ¹⁾	8th	5th / 8th ¹⁾
Write Latency(min)	2	2	3	3	4	4
1st Write data loading clock	3rd	3rd	4th	4th	5th	5th

1) Delayed Latency should be taken when refresh is required or when burst read newly starts by ADV interrupt during burst read operation.



Driver Strength A/DQ[17]~A/DQ[16]

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength.

Driver Strength	Full	1 / 2	1 / 4
IMPEDANCE(typ.)	40Ω	90Ω	150Ω

1. Impedance values are typical values, not 100% tested.

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OPERATION MODE (A/DQ[15]~A/DQ[14])

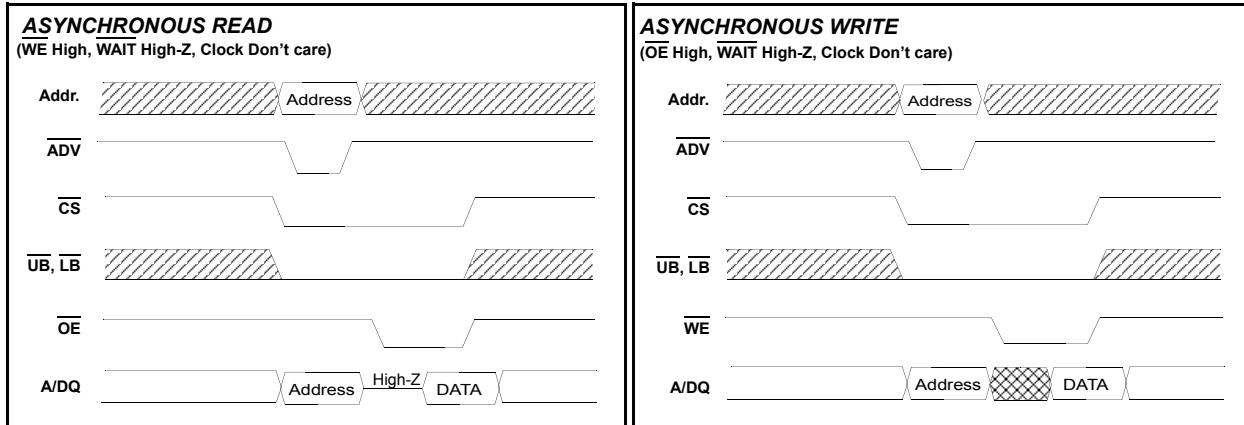
MODE1. ASYNCHRONOUS READ / ASYNCHRONOUS WRITE MODE

Asynchronous read operation

Asynchronous read operation starts when \overline{CS} , \overline{OE} and \overline{UB} or \overline{LB} are asserted. First data come out after random access time(t_{AA}) \overline{PS} and \overline{WE} should be de-asserted during read operation. Clock is don't care during read operation and \overline{WAIT} is Hi-Z.

Asynchronous write operation

Asynchronous write operation starts when \overline{CS} , \overline{WE} and \overline{UB} or \overline{LB} are asserted. \overline{PS} and should be de-asserted during write operation. Clock, \overline{OE} are don't care during write operation and \overline{WAIT} signal is Hi-Z.



FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	\overline{ADV}	A/DQ0~15	A16 ~ A19	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	X ¹⁾	Deselected	Standby
L	H	H	X ¹⁾	X ¹⁾	H	High-Z	X ¹⁾	Output Disabled	Active
L	X ¹⁾	X ¹⁾	H	H	X ¹⁾	High-Z	X ¹⁾	Output Disabled	Active
L	H	H	H	H		Add. Input	Add. Input	Address Input	Active
L	L	H	L	H	H	Dout	X ¹⁾	Lower Byte Read	Active
L	L	H	H	L	H	Dout	X ¹⁾	Upper Byte Read	Active
L	L	H	L	L	H	Dout	X ¹⁾	Word Read	Active
L	H	L	L	H	H	Din	X ¹⁾	Lower Byte Write	Active
L	H	L	H	L	H	Din	X ¹⁾	Upper Byte Write	Active
L	H	L	L	L	H	Din	X ¹⁾	Word Write	Active

1. X means "Don't care". X should be low or high state.
2. In asynchronous mode, Clock is ignored. Clock should be low or high state.
3. \overline{WAIT} pin is High-Z in Asynchronous mode.

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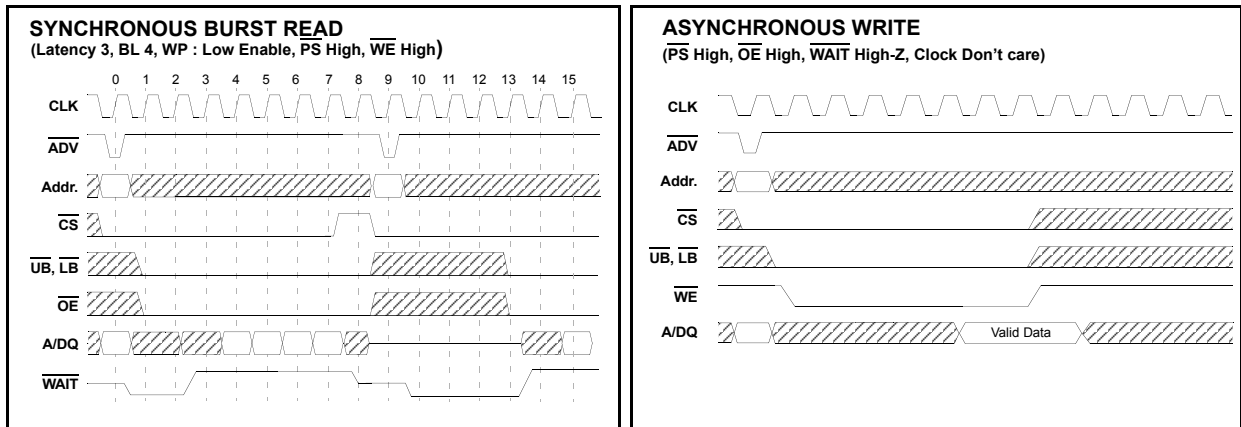
MODE2. SYNCHRONOUS BURST READ / ASYNCHRONOUS WRITE MODE

Synchronous Burst Read Operation

Burst Read command is implemented when \overline{ADV} is detected low at clock rising edge. \overline{WE} should be de-asserted during Burst read, Burst operation re-starts whenever \overline{ADV} is detected low at clock rising edge even in the middle of operation. Variable latency allows the UTRAM to be configured for minimum latency at high frequencies, but the controller must monitor \overline{WAIT} to detect any conflict with refresh cycles.

Asynchronous Write Operation

Asynchronous write operation starts when \overline{CS} , \overline{WE} and \overline{UB} or \overline{LB} are asserted. \overline{PS} and should be de-asserted during write operation. Clock, \overline{OE} are don't care during write operation and \overline{WAIT} signal is Hi-Z.



FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{PS}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	A/DQ0~7	A/DQ8~15	CLK	\overline{ADV}	Mode	Power
H	H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	X ¹⁾	Deselected	Standby
H	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	X ¹⁾	Deselected	PAR
L	H	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	H	Output Disabled	Active
L	H	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	X ¹⁾	H	Output Disabled	Active
L	H	X ¹⁾	H	X ¹⁾	X ¹⁾	Address	Address			Read Command	Active
L	H	L	H	L	H	Dout	High-Z		H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout		H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout		H	Word Read	Active
L	H	H	L	L	H	Din	High-Z	X ¹⁾	H	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	X ¹⁾	H	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	X ¹⁾	H	Word Write	Active

1. X means "Don't care". X should be low or high state.

2. \overline{WAIT} is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for \overline{WAIT} pin function.

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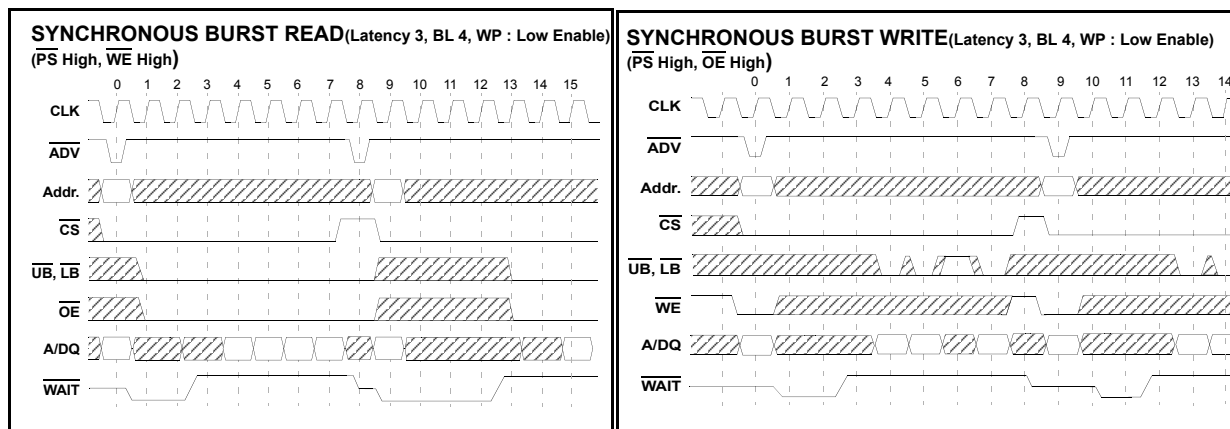
MODE3. SYNCHRONOUS BURST READ / SYNCHRONOUS BURST WRITE MODE

Synchronous Burst Read Operation

Burst Read command is implemented when \overline{ADV} is detected low at clock rising edge. \overline{WE} should be de-asserted during Burst read, Burst Read operation re-starts whenever \overline{ADV} is detected low at clock rising edge even in the middle of Burst Read operation. Variable latency allows the UTRAM to be configured for minimum latency at high frequencies, but the controller must monitor \overline{WAIT} to detect any conflict with refresh cycles.

Synchronous Burst Write Operation

Burst Write command is implemented when \overline{ADV} & \overline{WE} are detected low at clock rising edge. Burst Write operation re-starts whenever \overline{ADV} is detected low at clock rising edge even in the middle of Burst Write operation. Write operations always use fixed latency.



FUNCTIONAL DESCRIPTION

CS	PS	OE	WE	LB	UB	I/O0~7	I/O8~15	CLK	ADV	Mode	Power
H	H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	X ¹⁾	Deselected	Standby
H	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	X ¹⁾	Deselected	PAR
L	H	H	H	X ¹⁾	X ¹⁾	High-Z	High-Z	X ¹⁾	H	Output Disabled	Active
L	H	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	X ¹⁾	H	Output Disabled	Active
L	H	X ¹⁾	H	X ¹⁾	X ¹⁾	High-Z	High-Z	⌋	⌋	Read Command	Active
L	H	L	H	L	H	Dout	High-Z	⌋	H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	⌋	H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	⌋	H	Word Read	Active
L	H	X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	High-Z	⌋	⌋	Write Command	Active
L	H	H	X ¹⁾	L	H	Din	High-Z	⌋	H	Lower Byte Write	Active
L	H	H	X ¹⁾	H	L	High-Z	Din	⌋	H	Upper Byte Write	Active
L	H	H	X ¹⁾	L	L	Din	Din	⌋	H	Word Write	Active

1. X means "Don't care". X should be low or high state.

2. /WAIT is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for /WAIT pin function.

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MODE 1 AC OPERATING CONDITIONS (ASYNCH. READ / ASYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V

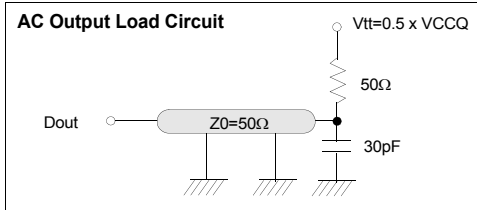
Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V_{CCQ}

Output load: CL=30pF

V_{CC}: 1.7V~1.95V

T_A: -40°C~85°C



AC CHARACTERISTICS

Parameter List		Symbol	Speed		Units
			Min	Max	
Common	\overline{CS} High Pulse Width	t _{CSHP(A)}	10	-	ns
	Address Set-up Time to \overline{ADV} Rising	t _{AS(A)}	7	-	ns
	Address Hold Time from \overline{ADV} Rising	t _{AH(A)}	3	-	ns
	\overline{ADV} Pulse Width Low	t _{VP}	7	-	ns
Asynch. Read	Address Access Time	t _{AA}	-	70	ns
	\overline{ADV} Access Time	t _{AA\overline{DV}}	-	70	ns
	\overline{CS} Setup Time to \overline{ADV} Rising	t _{CS(A)}	5	-	ns
	Chip Select to Output	t _{CO}	-	70	ns
	Output Enable to Valid Output	t _{OE}	-	20	ns
	\overline{UB} , \overline{LB} Access Time	t _{BA}	-	20	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t _{CHZ}	0	10	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	t _{BHZ}	0	10	ns
	Output Disable to High-Z Output	t _{OHZ}	0	10	ns
	\overline{ADV} High to \overline{OE} Low	t _{ADVOE}	5	-	ns
Asynch. Write	\overline{ADV} Setup to end of Write	t _{VS}	70	-	ns
	Chip Select to End of Write	t _{CW}	60	-	ns
	Address Valid to End of Write	t _{AW}	60	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	t _{BW}	60	-	ns
	Write Pulse Width	t _{WP}	55 ¹⁾	-	ns
	Write Recovery Time	t _{WR}	0	-	ns
	Data to Write Time Overlap	t _{DW}	20	-	ns
	Data Hold from Write Time	t _{DH}	0	-	ns
	\overline{CS} Low to \overline{ADV} High	t _{CVS}	7	-	ns
	\overline{ADV} High to \overline{WE} Low	t _{ADVWE}	5	-	ns

1. t_{WP}(min)=70ns for continuous write without CS toggling longer than 2.5us

2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5

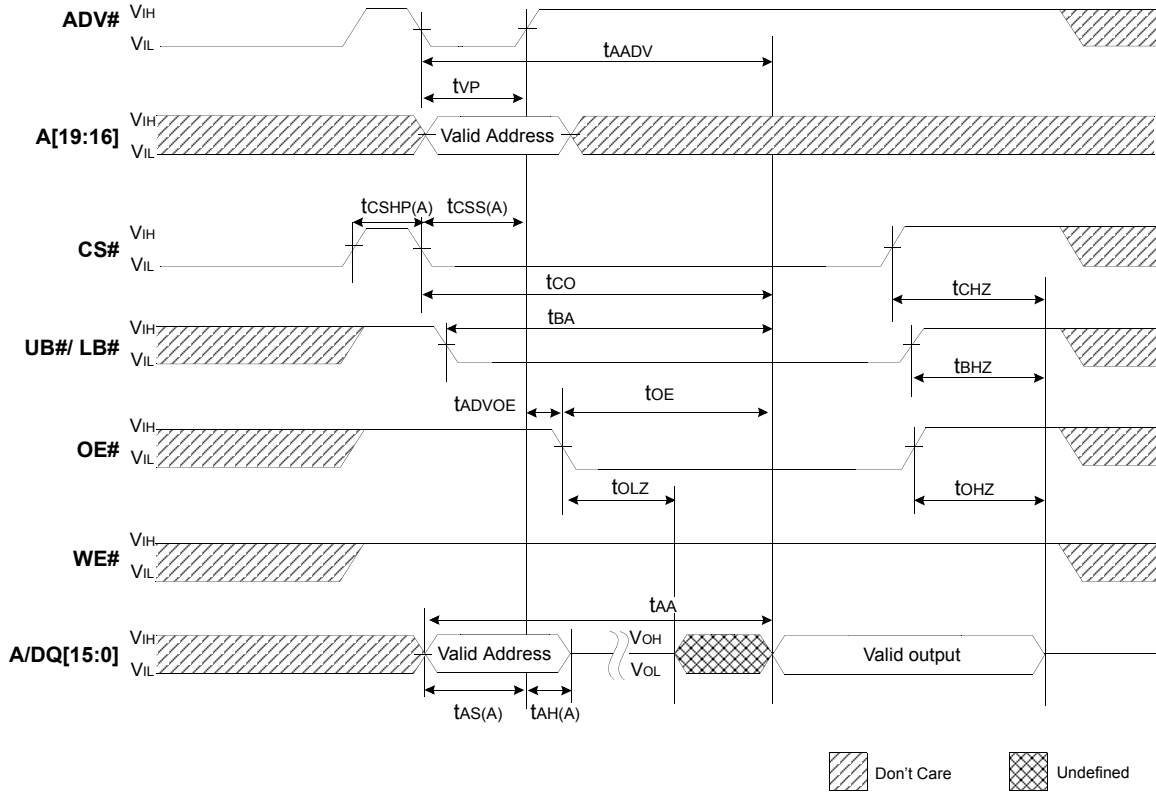
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

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TIMING WAVEFORMS (ASYNCH. READ / ASYNCH. WRITE)

Asynch. READ

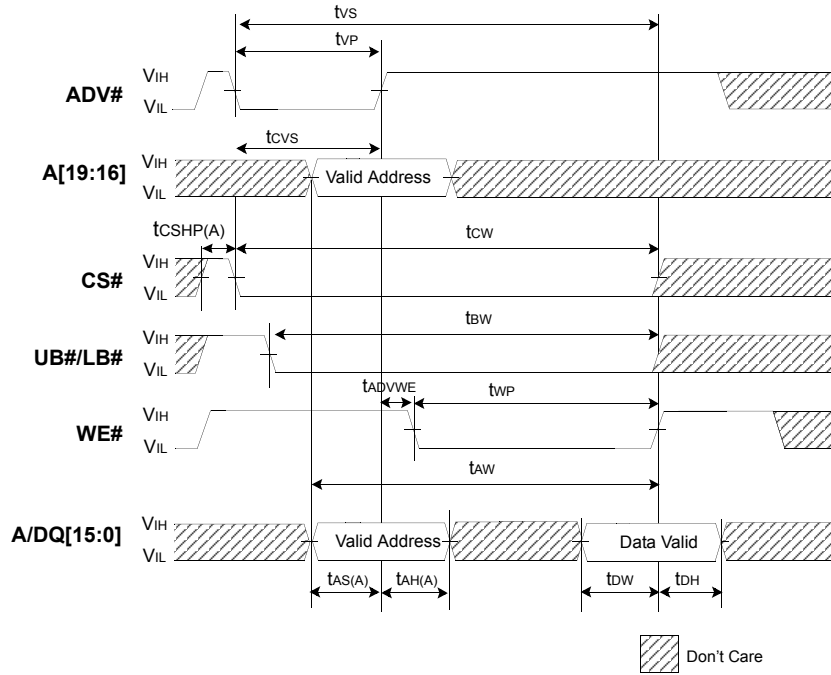
(PS=VIH, WE=VIH, WAIT=High-Z)



1. tCHZ and tOHZ are defined as the time when the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. In asynchronous read cycle, Clock is ignored.

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Asynchronous WRITE



Notes:

1. The end of the WRITE cycle is controlled by CE#, UB#/LB#, or WE#, whichever de-asserts first.

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UtRAM

MODE 2 AC OPERATING CONDITIONS (SYNCH. READ / ASYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V_{CCQ}-0.2V

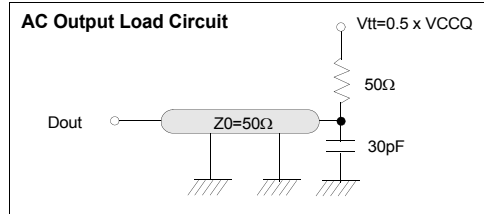
Input rising and falling time: 1ns

Input and output reference voltage: 0.5 x V_{CCQ}

Output load: CL=30pF

V_{CC}: 1.7V~1.95V

T_A: -40°C~85°C



AC CHARACTERISTICS

Parameter List	Symbol	66MHz		80MHz		104MHz		Units
		Min	Max	Min	Max	Min	Max	
Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
Burst Cycle Time	t _{BC}	-	2500	-	2500	-	2500	ns
Address Set-up Time to clock	t _{AS(B)}	5	-	4	-	3	-	ns
Address Hold Time from clock	t _{AH(B)}	2	-	2	-	2	-	ns
ADV Setup Time to clock	t _{ADVS}	5	-	4	-	3	-	ns
ADV Hold Time from clock	t _{ADVH}	2	-	2	-	2	-	ns
CS Setup Time to clock	t _{CSS(B)}	5	-	4	-	3	-	ns
CS High to ADV Low (Burst Stop)	t _{BSADV¹⁾}	0	-	0	-	0	-	ns
CS Low Hold Time from Clock(Burst Stop)	t _{CSSLH}	2	-	2	-	2	-	ns
CS High Pulse Width	t _{CSSH}	5	-	5	-	5	-	ns
CS Low to WAIT Low	t _{WL}	-	7.5	-	7.5	-	7.5	ns
Clock to WAIT High	t _{WH}	-	11	-	9	-	7	ns
CS High to WAIT High-Z	t _{WZ}	-	10	-	10	-	10	ns
UB, LB Low to End of Latency Clock	t _{BEL}	20	-	20	-	20	-	ns
OE Low to End of Latency Clock	t _{OEL}	20	-	20	-	20	-	ns
UB, LB Low to Low-Z Output	t _{B LZ}	5	-	5	-	5	-	ns
OE Low to Low-Z Output	t _{O LZ}	5	-	5	-	5	-	ns
Clock Rising to Data Output	t _{CD}	-	11	-	9	-	7	ns
Output Hold from clock	t _{OH(B)}	3	-	3	-	3	-	ns
Burst End Clock to Output High-Z	t _{HZ}	-	10	-	10	-	10	ns
CS High to Output High-Z	t _{CHZ}	-	10	-	10	-	10	ns
OE High to Output High-Z	t _{OHZ}	-	10	-	10	-	10	ns
UB, LB High to Output High-Z	t _{BHZ}	-	10	-	10	-	10	ns
ADV# high to OE# Low	t _{ADVO}	5	-	4	-	3	-	ns

1. Refresh can not be implemented when t_{BSADV} is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for t_{BSADV}.

2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5

3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

Parameter List	Symbol	Speed		Units
		Min	Max	
Write Cycle Time	t _{WC}	70	-	ns
Chip Select to End of Write	t _{CW}	60	-	ns
ADV Minimum Low Pulse Width	t _{ADV}	5	-	ns
Address Set-up Time to ADV Rising	t _{AS(A)}	5	-	ns
Address Hold Time from ADV Rising	t _{AH(A)}	3	-	ns
CS Setup Time to ADV Rising	t _{CSS(A)}	5	-	ns
Address Valid to End of Write	t _{AW}	60	-	ns
UB, LB Valid to End of Write	t _{BW}	60	-	ns
Write Pulse Width	t _{WP}	55 ¹⁾	-	ns
Write Recovery Time	t _{WR}	0	-	ns
Data to Write Time Overlap	t _{DW}	20	-	ns
Data Hold from Write Time	t _{DH}	0	-	ns
ADV# HIGH to WE# LOW	t _{ADVWE}	5	-	ns

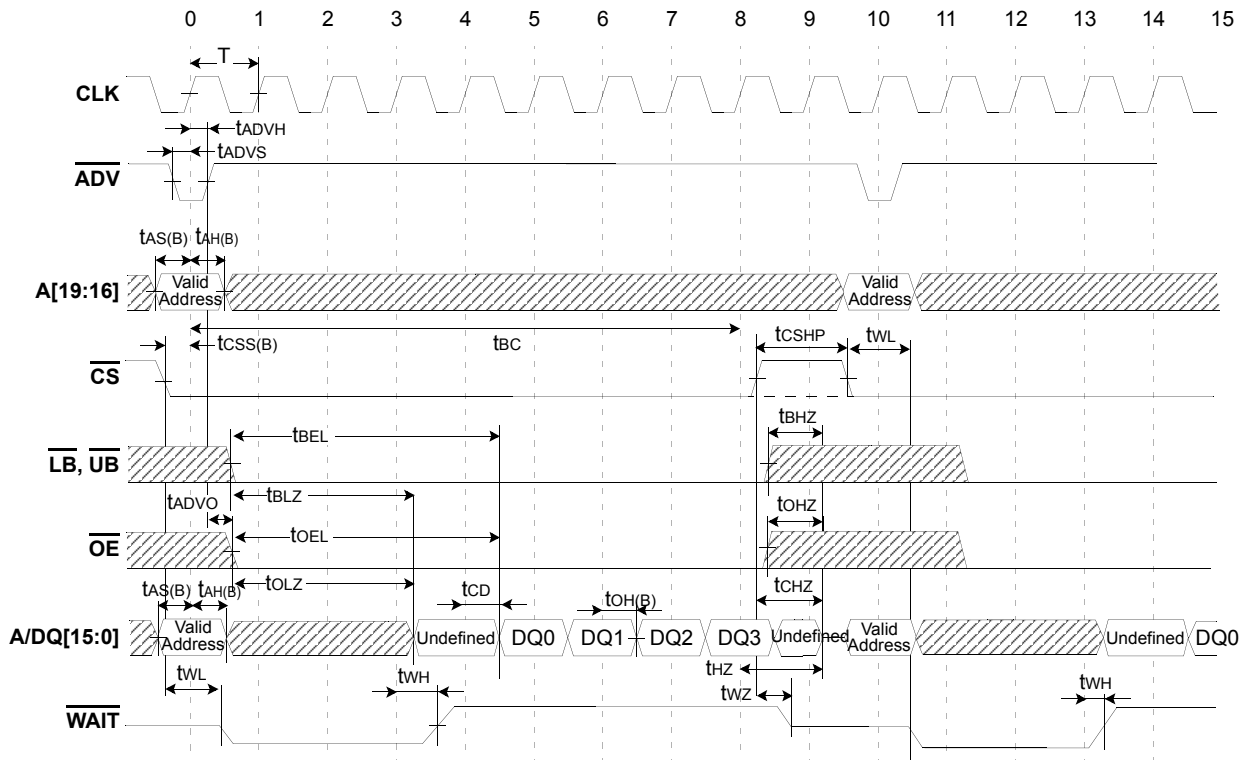
1. t_{WP}(min)=70ns for continuous write longer than 2.5us without CS toggling.

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TIMING WAVEFORMS (SYNCH. READ / SYNCH. WRITE)

Burst READ - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. /WAIT Low(tWL) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by \overline{CS} high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5 μ s)

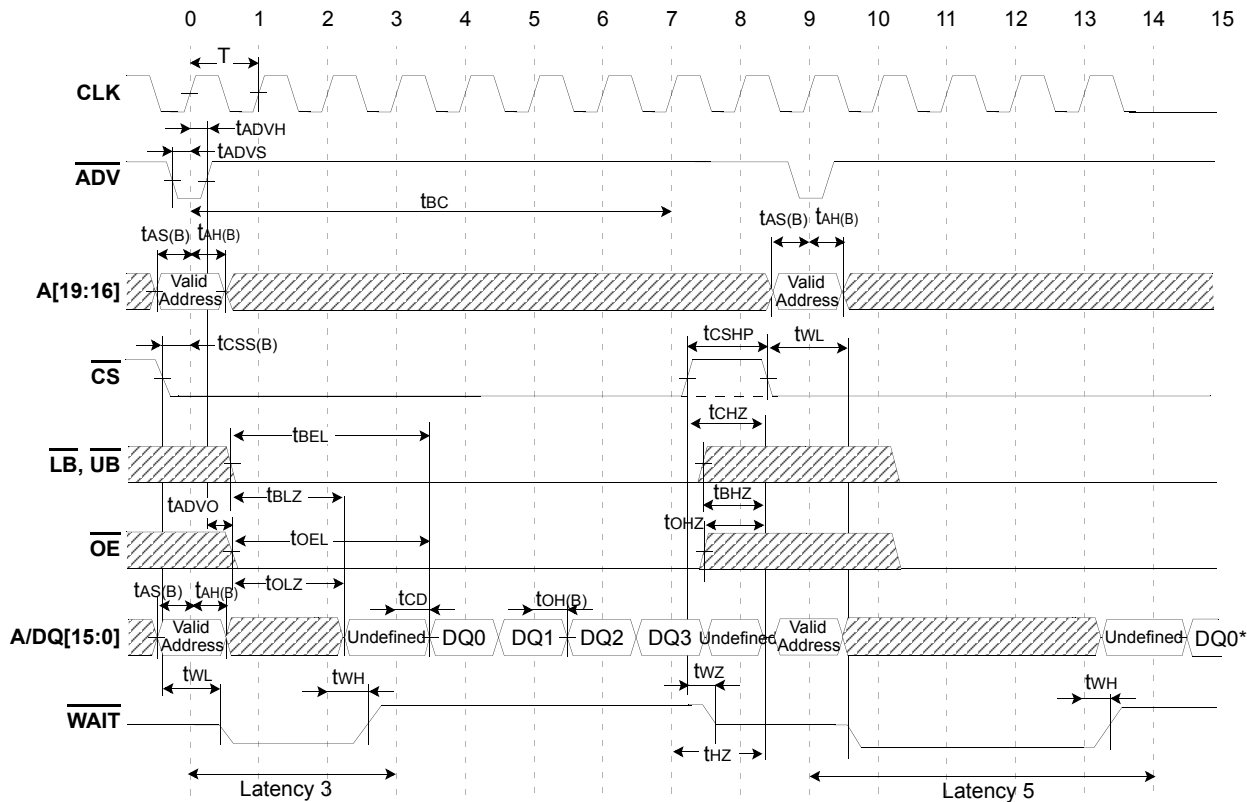
AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tcSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

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Burst READ - Variable Latency

(PS=VIH, WE=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5µs).

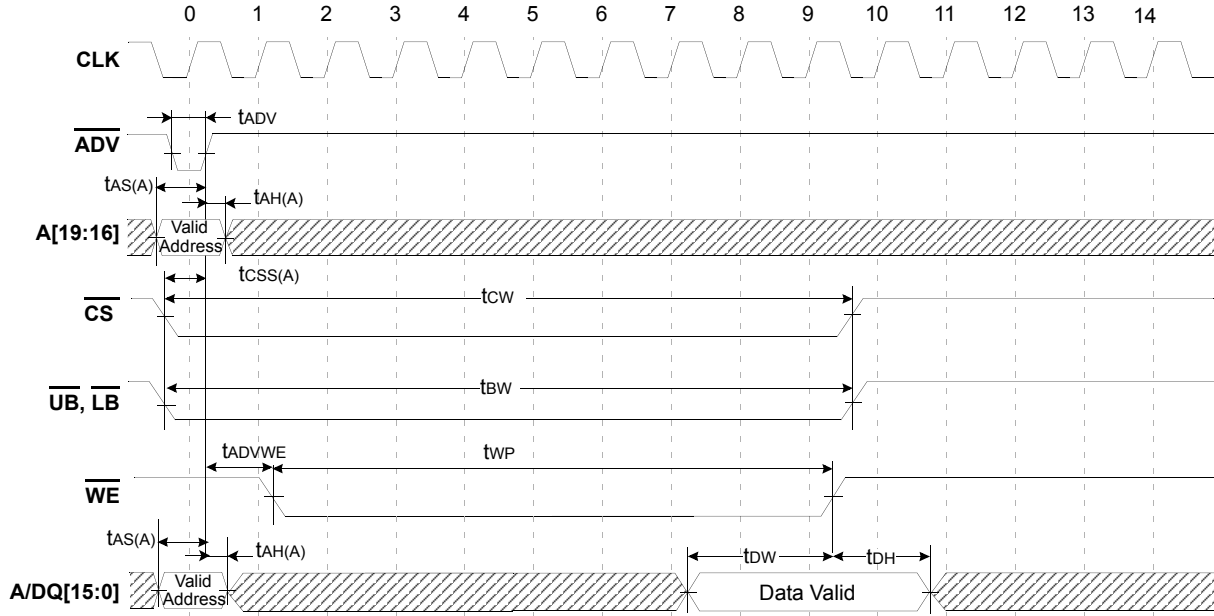
AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

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Asynch. WRITE

(PS=VIH, OE=VIH, WAIT=High-Z)

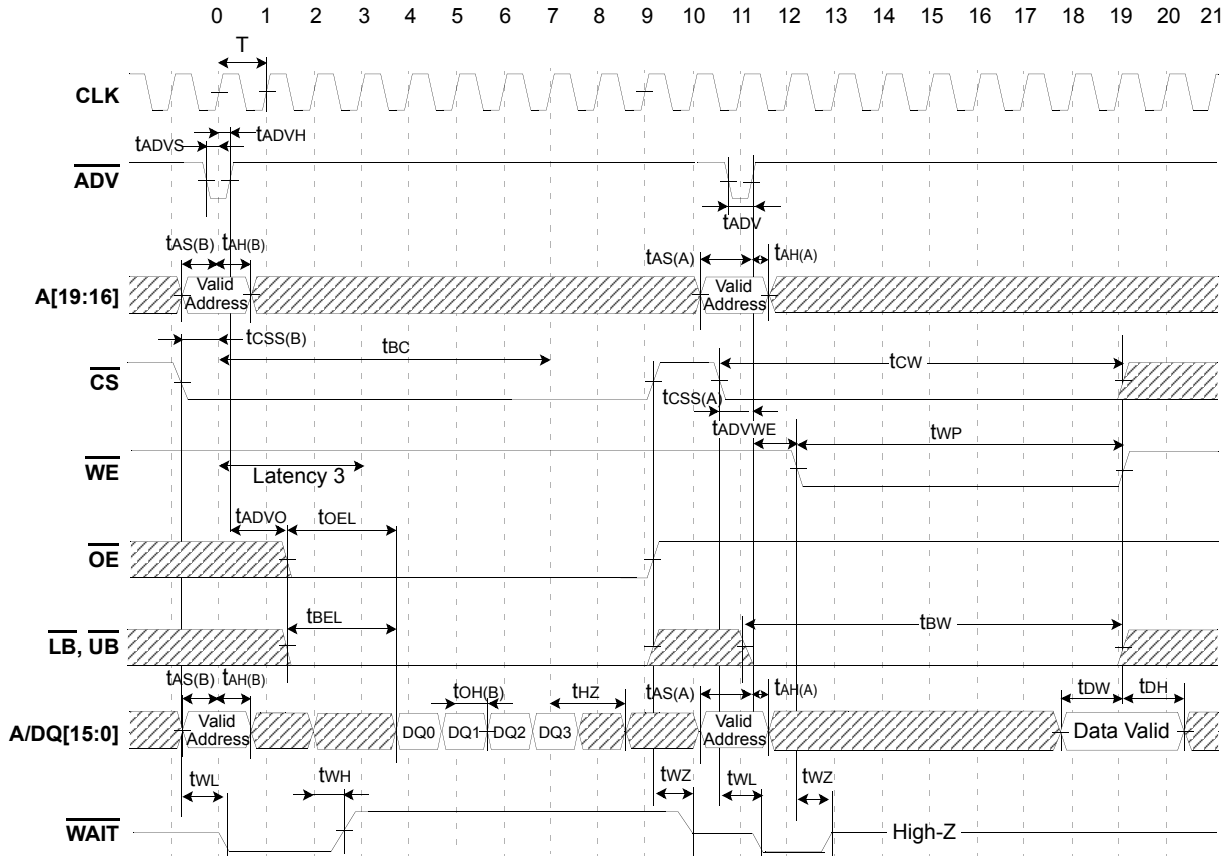


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U1RAM

Burst READ followed by Asynch. WRITE

(PS=VIH, WAIT=High-Z, Variable Latency=3)

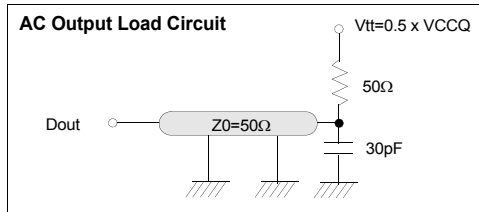


1. A write occurs during the overlap(t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for word operation. A write ends at the earliest transition when CS goes high or WE goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{AW} is measured from the address valid to the end of write. In this address latch type write timing, t_{WC} is same as t_{AW} .
3. t_{CW} is measured from the \overline{CS} going low to the end of write.
4. t_{W} is measured from the \overline{UB} and \overline{LB} going low to the end of write.

MODE3. AC OPERATING CONDITIONS (SYNCH. READ / SYNCH. WRITE)

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
 Input pulse level: 0.2 to Vcc-0.2V
 Input rising and falling time: 1ns
 Input and output reference voltage: 0.5 x Vcc
 Output load: CL=30pF
 Vcc:1.7V~1.95V
 TA: -40°C~85°C



AC CHARACTERISTICS

Parameter List	Symbol	66MHz		80MHz		104MHz		Units	
		Min	Max	Min	Max	Min	Max		
Burst Operation (Common)	Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
	Burst Cycle Time	tBC	-	2500	-	2500	-	2500	ns
	Address Set-up Time to clock	tAS(B)	5	-	4	-	3	-	ns
	Address Hold Time from clock	tAH(B)	2	-	2	-	2	-	ns
	\overline{ADV} Setup Time to clock	tADVS	5	-	4	-	3	-	ns
	\overline{ADV} Hold Time from clock	tADVH	2	-	2	-	2	-	ns
	\overline{CS} Setup Time to clock	tCSS(B)	5	-	4	-	3	-	ns
	\overline{CS} High to New \overline{ADV} Low (Burst Stop)	tBSADV	0	-	0	-	0	-	ns
	\overline{CS} Low Hold Time from Clock(Burst Stop)	tCSLH	2	-	2	-	2	-	ns
	\overline{CS} High Pulse Width	tCSHP	5	-	5	-	5	-	ns
	\overline{CS} Low to \overline{WAIT} Low	tWL	-	7.5	-	7.5	-	7.5	ns
	Clock to \overline{WAIT} High	tWH	-	11	-	9	-	7	ns
\overline{CS} High to \overline{WAIT} High-Z	tWZ	-	10	-	10	-	10	ns	
Burst Read Operation	$\overline{UB}, \overline{LB}$ Low to End of Latency Clock	tBEL	20	-	20	-	20	-	ns
	\overline{OE} Low to End of Latency Clock	toEL	20	-	20	-	20	-	ns
	$\overline{UB}, \overline{LB}$ Low to Low-Z Output	tBLZ	5	-	5	-	5	-	ns
	\overline{OE} Low to Low-Z Output	toLZ	5	-	5	-	5	-	ns
	Clock Rising to Data Output	tCD	-	11	-	9	-	7	ns
	Output Hold from clock	tOH(B)	3	-	3	-	3	-	ns
	Burst End Clock to Output High-Z	tHZ	-	10	-	10	-	10	ns
	\overline{CS} High to Output High-Z	tCHZ	-	10	-	10	-	10	ns
	\overline{OE} High to Output High-Z	toHZ	-	10	-	10	-	10	ns
	$\overline{UB}, \overline{LB}$ High to Output High-Z	tBHZ	-	10	-	10	-	10	ns
\overline{ADV} high to \overline{OE} Low	tADVO	5	-	4	-	3	-	ns	

1. Refresh can not be implemented when tBSADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBSADV.
2. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either VOH or VOL.

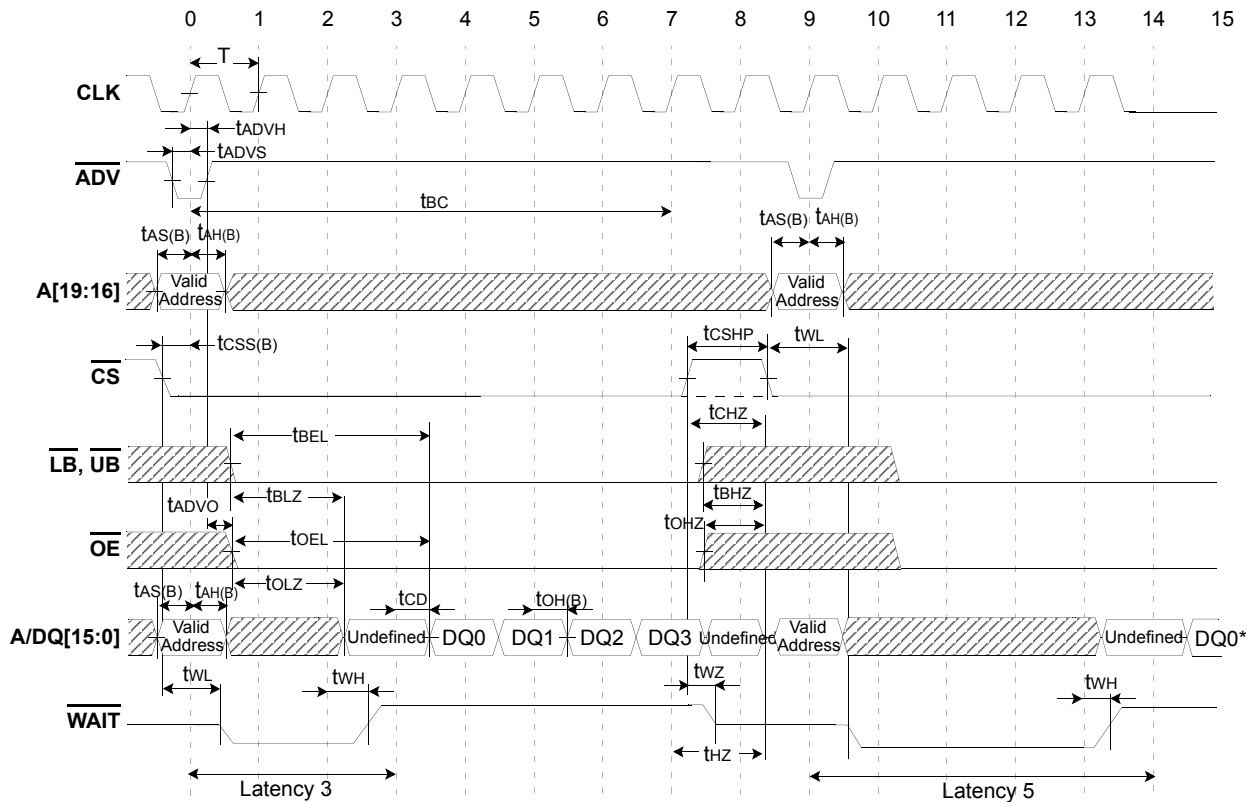
Burst Write Operation	\overline{WE} Set-up Time to Clock	tWES	5	-	4	-	3	-	ns
	\overline{WE} Hold Time from Clock	tWEH	2	-	2	-	2	-	ns
	$\overline{UB}, \overline{LB}$ Set-up Time to Clock	tBS	5	-	4	-	3	-	ns
	Burst End clock to New \overline{ADV} Low	tBEADV	0	-	0	-	0	-	ns
	$\overline{UB}, \overline{LB}$ Hold Time from Clock	tBH	2	-	2	-	2	-	ns
	Byte Masking Set-up Time to Clock	tBMS	5	-	4	-	3	-	ns
	Byte Masking Hold Time from Clock	tBMH	2	-	2	-	2	-	ns
	Write Data Set-up Time to Clock	tDS	5	-	4	-	3	-	ns
Write Data Hold Time from Clock	tDHC	2	-	2	-	2	-	ns	

1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.

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Burst READ - Variable Latency

(PS=VIH, WE=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5µs).

AC CHARACTERISTICS

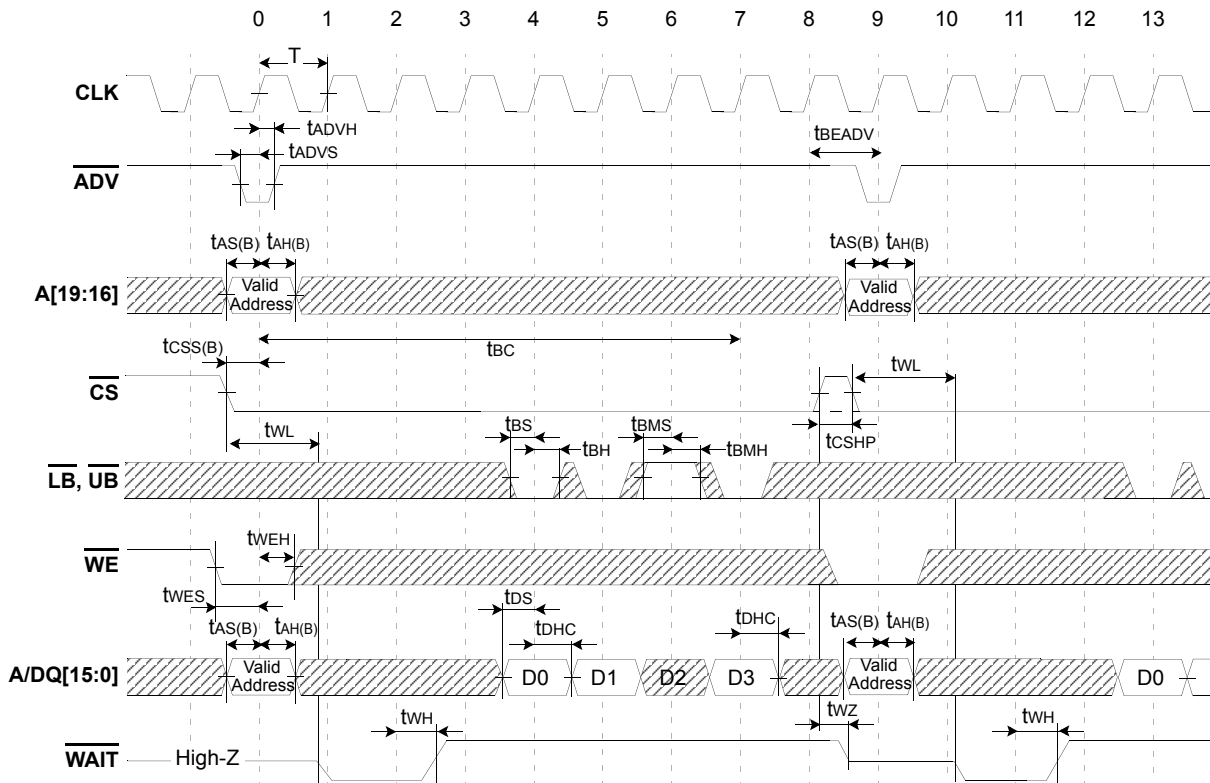
Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	3	-	3	-	3	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns	tADVO	5	-	4	-	3	-	ns

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Burst WRITE

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
/WAIT High(tWH) : Data available(driven by Latency-1 clock)
/WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5μs)

AC CHARACTERISTICS

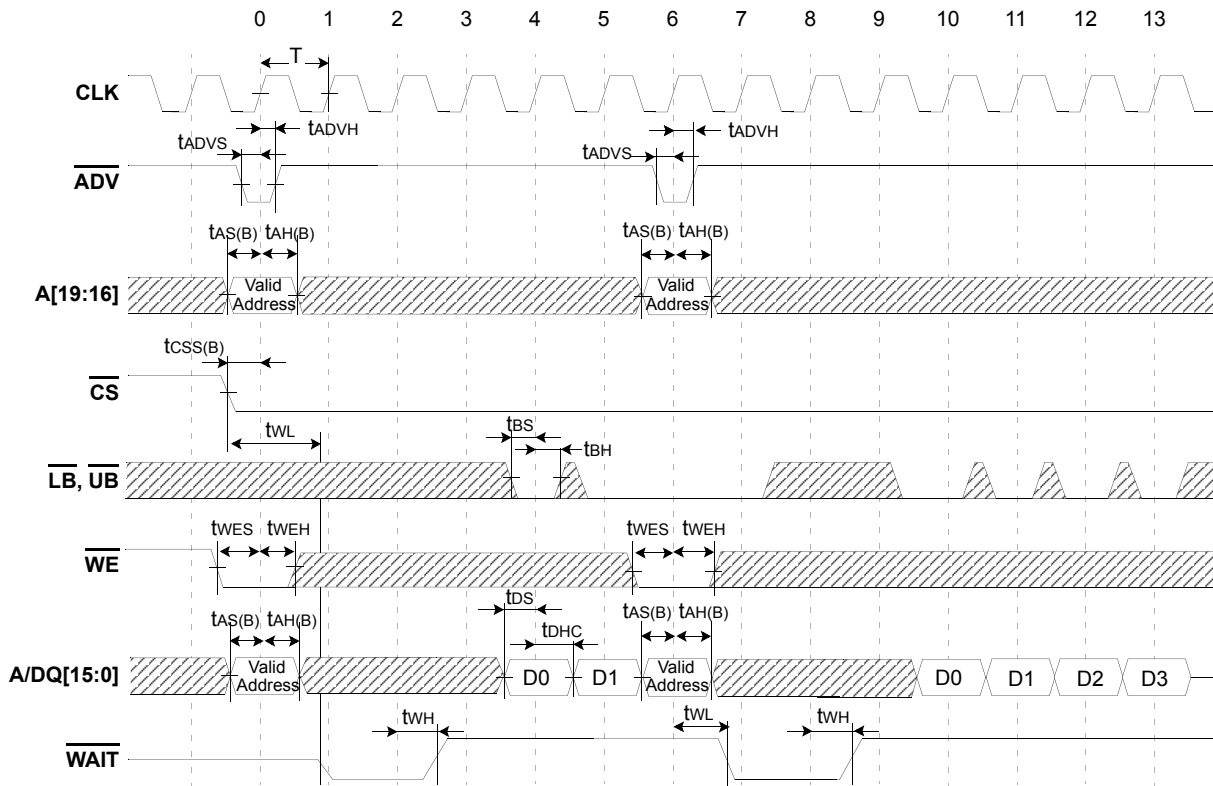
Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	3	-	3	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	tWZ	-	10	-	10	-	10	ns
tWES	5	-	4	-	3	-	ns								
tWEH	2	-	2	-	2	-	ns								

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UtRAM

Burst WRITE (ADV PULSE Interrupt)

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



- Multiple clock risings are allowed during low \overline{ADV} period. The data starts after set Latency from the last clock rising.
- \overline{WAIT} Low (t_{WL}): Data not available (driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 \overline{WAIT} High (t_{WH}): Data available (driven by Latency-1 clock)
 \overline{WAIT} High-Z (t_{WZ}): Data don't care (driven by \overline{CS} high going edge)
- Burst interrupt is allowable after the first data word written.

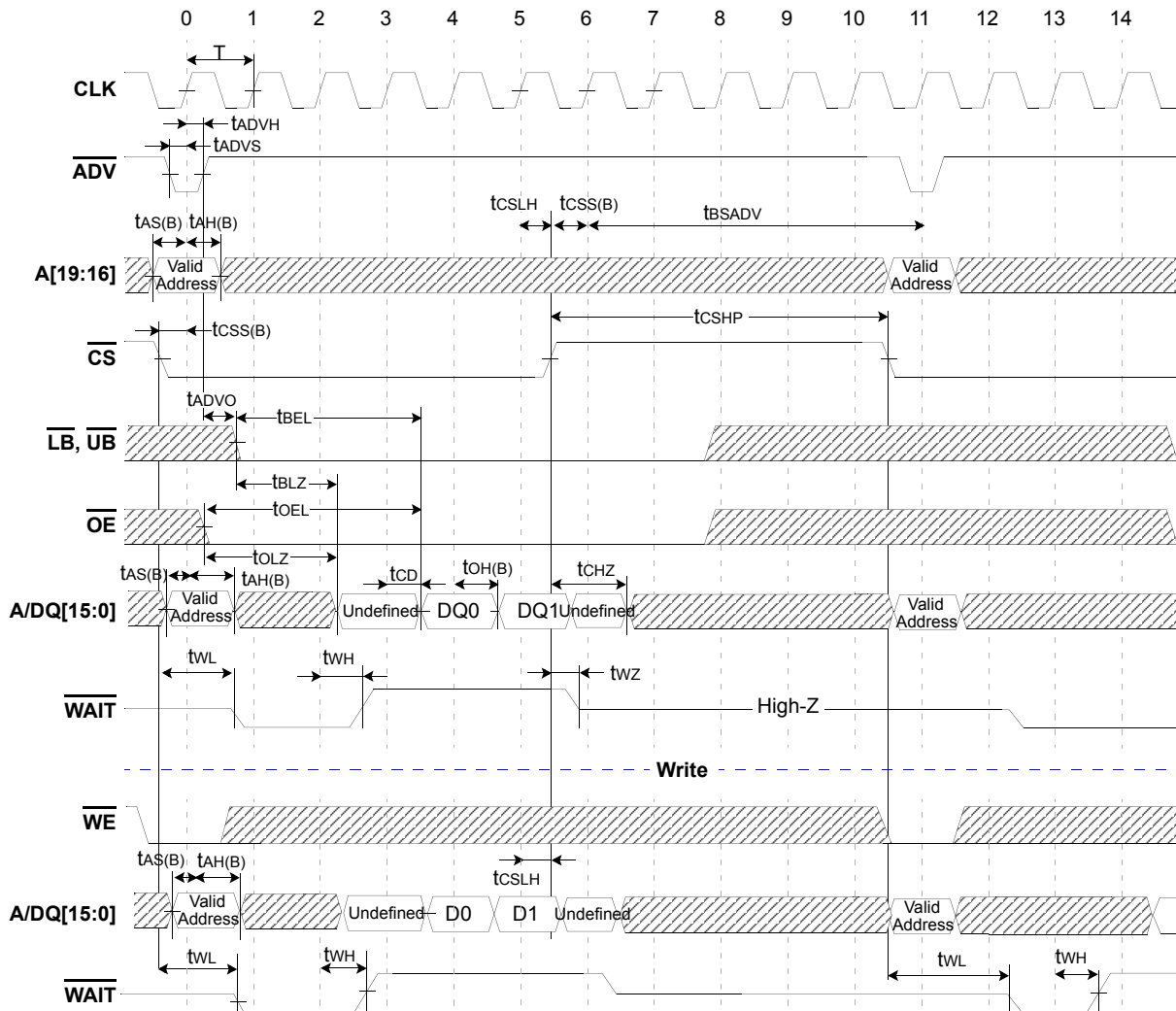
AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
t_{CSHP}	5	-	5	-	5	-	ns	t_{DS}	5	-	4	-	3	-	ns
t_{BS}	5	-	4	-	3	-	ns	t_{DHC}	2	-	2	-	2	-	ns
t_{BH}	2	-	2	-	2	-	ns	t_{WL}	-	7.5	-	7.5	-	7.5	ns
t_{BMS}	5	-	4	-	3	-	ns	t_{WH}	-	11	-	9	-	7	ns
t_{BMH}	2	-	2	-	2	-	ns	t_{WZ}	-	10	-	10	-	10	ns
t_{WES}	5	-	4	-	3	-	ns								
t_{WEH}	2	-	2	-	2	-	ns								

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Burst READ STOP & Burst WRITE STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)

AC CHARACTERISTICS

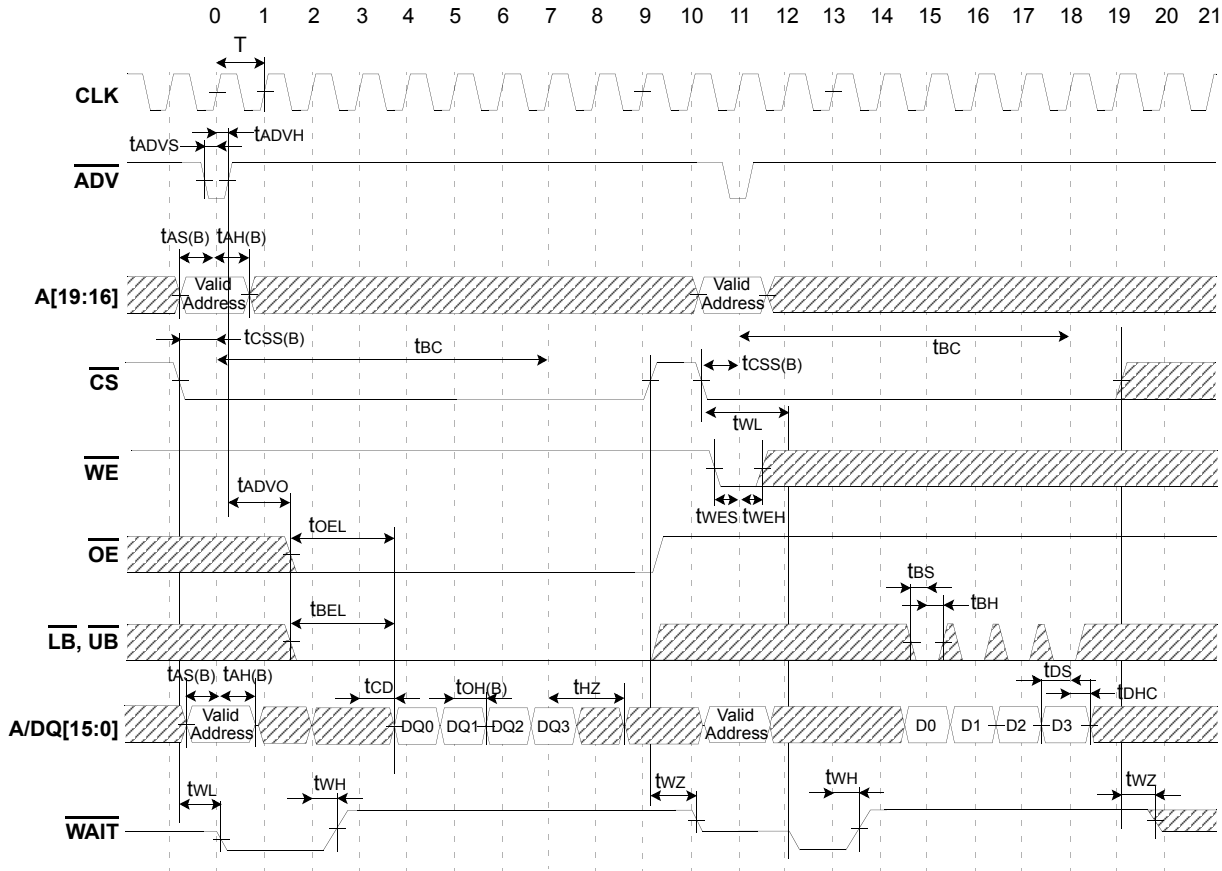
Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	5	-	4	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	tWZ	-	10	-	10	-	10	ns
tWES	5	-	4	-	3	-	ns	tBSADV	-	0	-	0	-	0	ns
tWEH	2	-	2	-	2	-	ns	tOH(B)	3	-	3	-	3	-	ns

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UtRAM

Burst READ followed by Burst WRITE

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

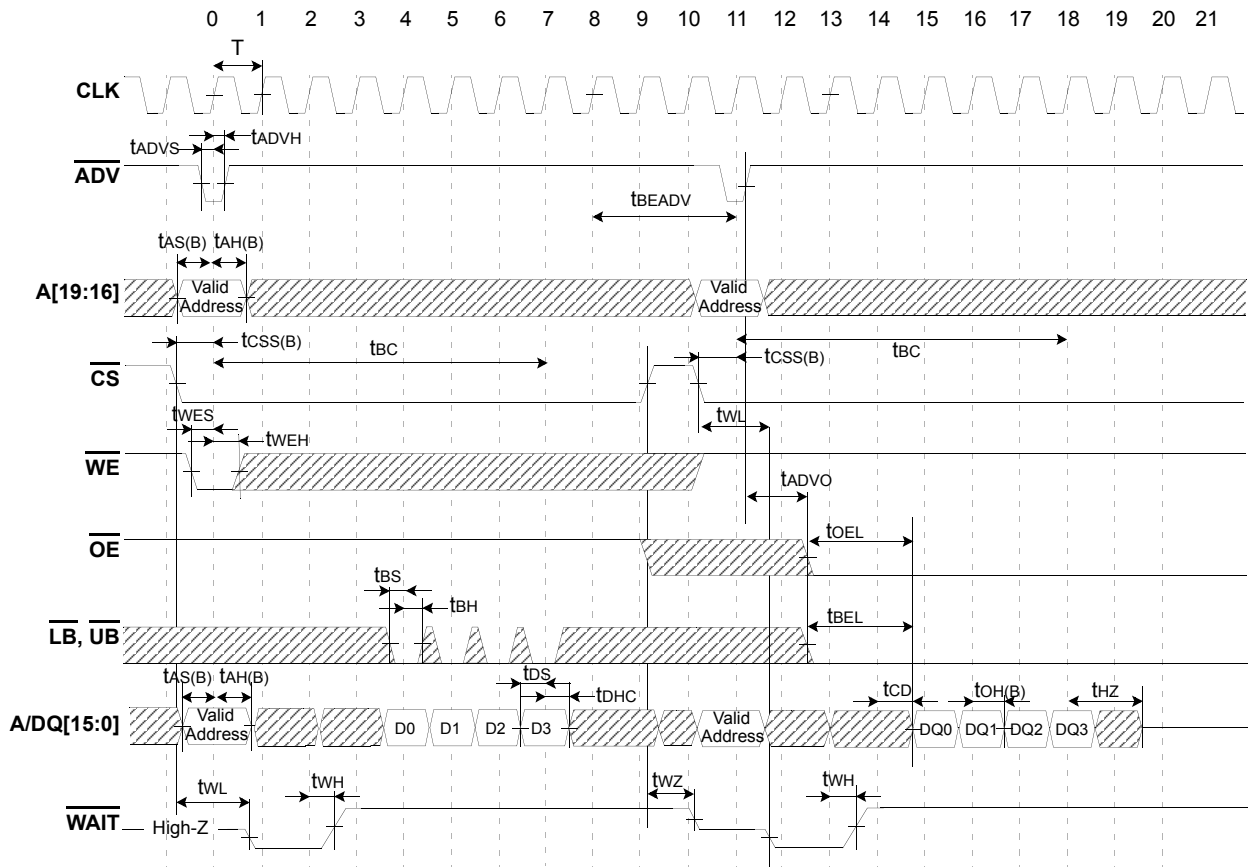


1. /WAIT Low(t_{WL}) : Data not available(driven by \overline{CS} low going edge or \overline{ADV} low going edge)
 /WAIT High(t_{WH}) : Data available(driven by Latency-1 clock)
 /WAIT High-Z(t_{WZ}) : Data don't care(driven by \overline{CS} high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than t_{BC} (2.5 μ s)

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Burst WRITE followed by Burst READ

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



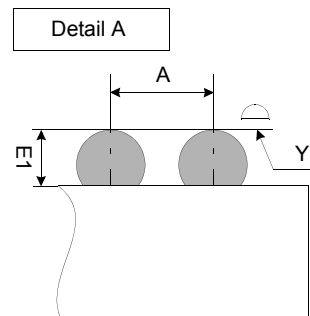
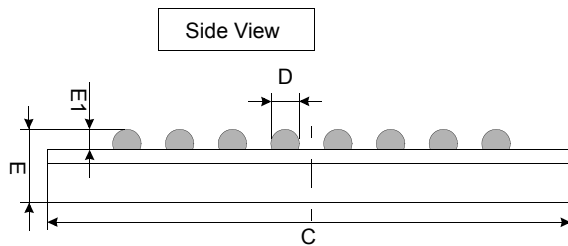
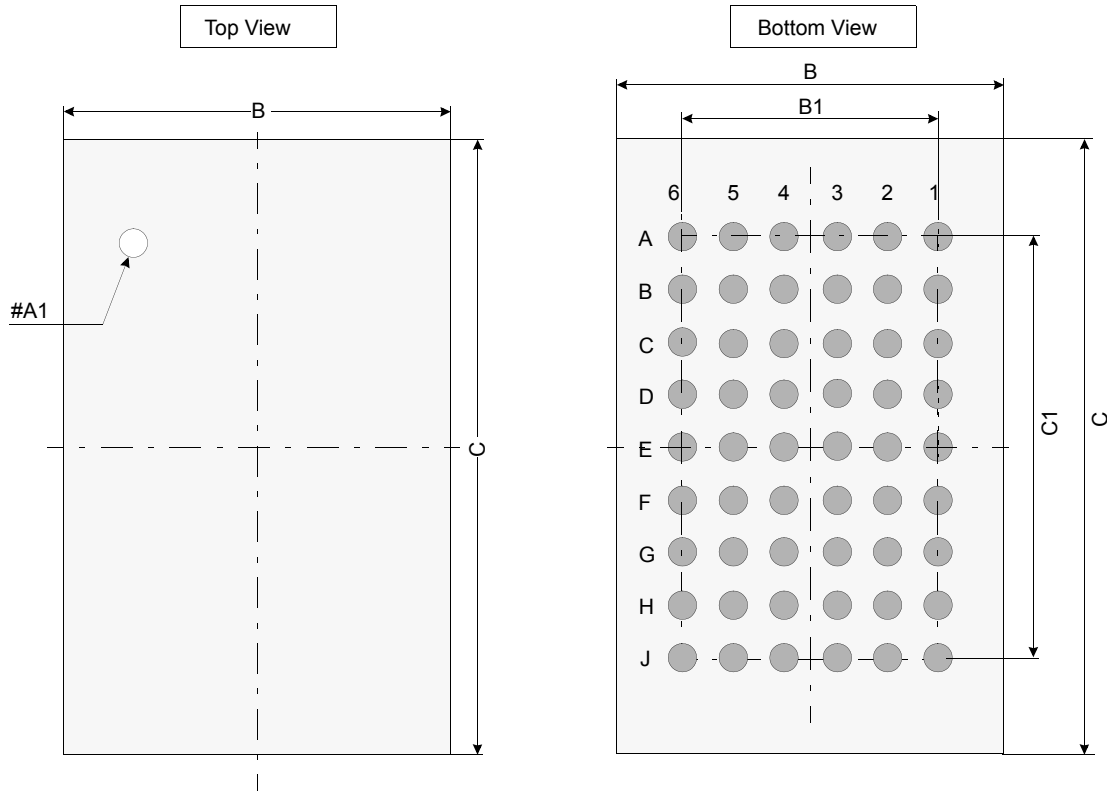
1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)
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 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than (tBC)2.5μs.

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PACKAGE DIMENSION

54 BALL FINE PITCH BGA(0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

Notes.

1. Ball counts: 54(9 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are ± 0.050 unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity