

## **32Mb (2M x 16 bit) U $t$ RAM**

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**K1B3216BDE**

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**Document Title**

**2Mx16 bit Synchronous Burst Uni-Transistor Random Access Memory**

**Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Date</u></b>	<b><u>Remark</u></b>
0.0	Initial - Design Target	Mar.28,2007	Preliminary

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# K1B3216BDE

## 2M x 16 bit Synchronous Burst Uni-Transistor CMOS RAM

### GENERAL DESCRIPTION

The world is moving into the mobile multi-media era and therefore the mobile handsets need bigger & faster memory capacity to handle the multi-media data. SAMSUNG's UtRAM products are designed to meet all the request from the various customers who want to cope with the fast growing mobile market. UtRAM is the perfect solution for the mobile market with its low cost, high density and high performance feature. K1B3216BDE is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports the traditional SRAM like asynchronous operation (asynchronous page read and asynchronous write) the NOR flash like synchronous operation (synchronous burst read and asynchronous write) and the fully synchronous operation (synchronous burst read and synchronous burst write). These three operation modes are defined through the mode register setting. The device also supports the special features for the standby power saving like internal TCSR (Temperature Compensated Self Refresh). The optimization of output drive strength is possible through the mode register setting to adjust for the different data loadings. Through this drive strength optimization, the device can minimize the noise generated on the data bus during read operation.

### FEATURES

- Process technology: CMOS
- Organization: 2M x 16 bit
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports MRS (Mode Register Set)
  - PS pin set up
  - Software set up
- Supports power saving modes
  - Internal TCSR (Temperature Compensated Self Refresh)
- Supports driver strength optimization
- K1B3216BDE supports
  - Asynchronous read / Asynchronous write
  - Synchronous burst read/ Asynchronous write
  - Synchronous burst read / Synchronous burst write
- Synchronous burst operation
  - Max. clock frequency : 104MHz
  - Fixed and Variable read latency
  - 4 / 8 / 16 / 32 and Continuous burst
  - Wrap / No-wrap
  - Latency : 4(Variable) @ 104MHz  
 3(Variable) @ 80MHz  
 2(Variable) @ 66MHz
  - Burst stop
  - Burst read suspend
  - Burst write data masking

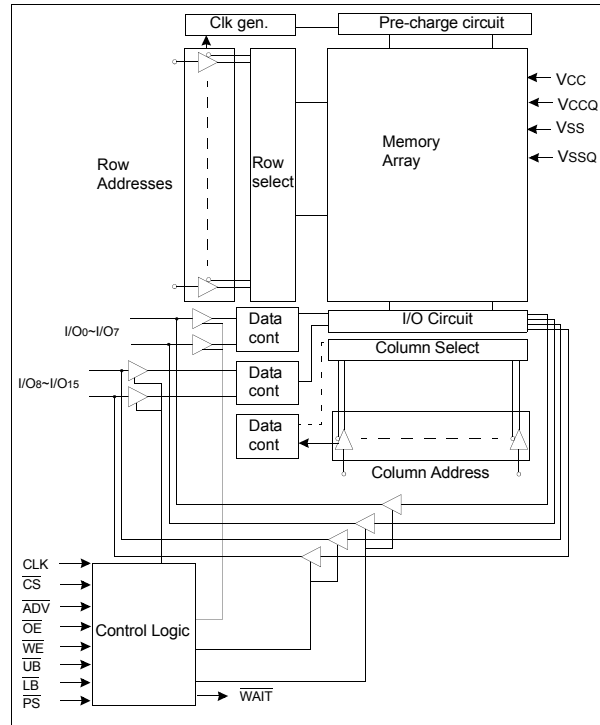
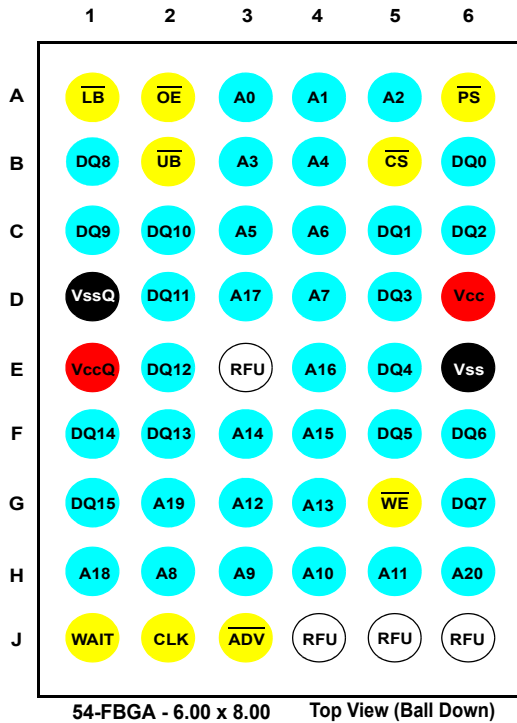
### PRODUCT FAMILY

Product Family	Operating Mode <sup>1)</sup>	Operating Temp.	Vcc Range	Speed	Current Consumption	
					Standby (I <sub>SB1</sub> , Max.)	Operating (I <sub>CC2P</sub> , Max.)
K1B3216BDE-I	Mode 1 Mode 2 Mode 3	Industrial(-40~85°C)	1.7~1.95V	104MHz	120µA	35mA

1) Mode1 : Asynchronous read / Asynchronous write  
 Mode2 : Synchronous burst read / Asynchronous write  
 Mode3 : Synchronous burst read / Synchronous burst write

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## PIN DESCRIPTIONS & FUNCTION BLOCK DIAGRAM



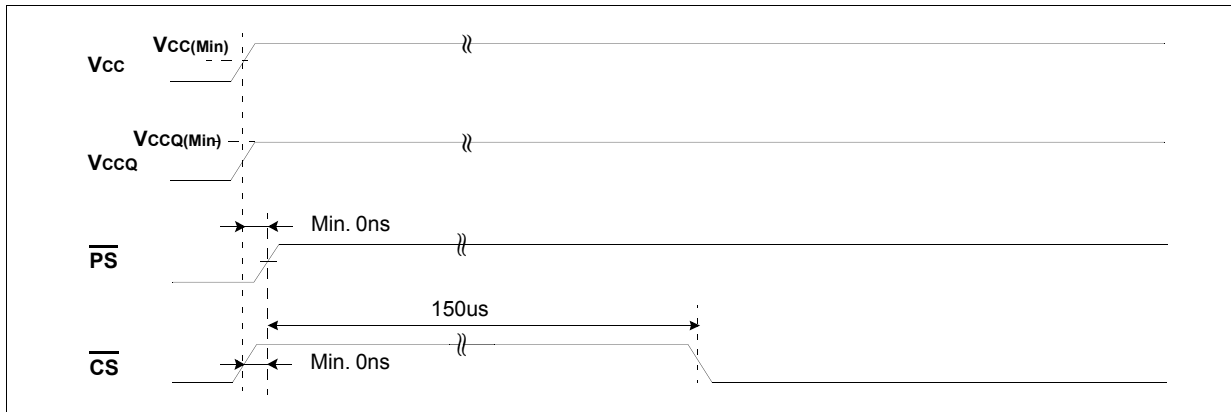
## TERMINOLOGY DESCRIPTION

Name	Function	Type	Description
CLK	Clock	Input	Synchronizes the memory to the system operating frequency during synchronous operations. Commands are referenced to CLK.
ADV	Address Valid	Input	Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV during asynchronous READ and WRITE operations.
PS	Power Saving	Input	PS low enables Mode Register to be set
CS	Chip Select	Input	CS low enables the chip to be active CS high disables the chip and puts it into standby mode or deep power down mode.
OE	Output Enable	Input	Enables the output buffers when LOW. when OE is HIGH, the output buffers are disabled.
WE	Write Enable	Input	WE low enables the chip to start writing the data
LB	Lower Byte (I/O0~7)	Input	UB (LB) low enables upper byte (lower byte) to allow data Input/output from I/O buffers.
UB	Upper Byte (I/O8~15)	Input	
A0~A20	Address 0 ~ Address 20	Input	Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles.
I/O0~I/O15	Data Inputs / Outputs	Input/Output	Depending on UB or LB status, word(16-bit, UB & LB low) data, upper byte(8-bit, UB low & LB high) data or lower byte(8-bit, LB low & UB high) data is loaded
VCC	Voltage Source	Power	Device Power supply. Power supply for device core operation.
VCCQ	I/O Voltage Source	Power	I/O Power supply. Power supply for input/output buffers.
VSS	Ground Source	GND	Ground for device operation
VSSQ	I/O Ground Source	GND	Ground for Input/Output buffers
WAIT	Valid Data Indicator	Output	The WAIT signal is output signal indicating the status of the data on the bus whether or not it is valid. WAIT is asserted when a burst crosses a word-line boundary. WAIT is asserted and should be ignored during asynchronous and page mode operations.

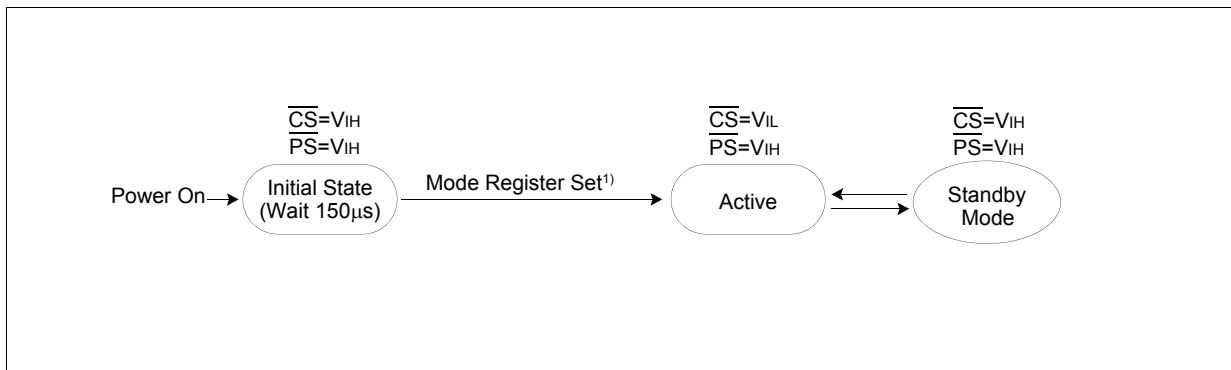
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## POWER UP SEQUENCE

After  $V_{CC}$  and  $V_{CCQ}$  reach minimum operating voltage(1.7V), drive  $\overline{CS}$  High first and then drive  $\overline{PS}$  High. Then the device gets into the Power Up mode. Wait for minimum 150 $\mu$ s to get into the normal operation mode. During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence. MODE1(Asynchronous Read / Asynchronous Write) is set up after power up, but this mode is not always guaranteed.



## MODE STATE MACHINE



1) Refer to MRS(Mode Register Set).

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## ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.2 to V <sub>CCQ</sub> +0.3V	V
Power supply voltage relative to Vss	V <sub>CC</sub> , V <sub>CCQ</sub>	-0.2 to 2.5V	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	T <sub>A</sub>	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V <sub>CC</sub>	1.7	1.8	1.95	V
Power supply voltage(I/O)	V <sub>CCQ</sub>	1.7	1.8	1.95	V
Ground	V <sub>SS</sub> , V <sub>SSQ</sub>	0	0	0	V
Input high voltage	V <sub>IH</sub>	V <sub>CCQ</sub> -0.4	-	V <sub>CCQ</sub> +0.2 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	-0.2 <sup>3)</sup>	-	0.4	V

1. T<sub>A</sub>=-40 to 85°C, otherwise specified.

2. Overshoot: V<sub>CCQ</sub>+1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.

3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

## CAPACITANCE (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CCQ</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ , $\overline{PS}=V_{IH}$ , $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CCQ</sub>	-1	-	1	μA	
Average Operating Current(Async)	I <sub>CC2</sub>	Cycle time=70ns, I <sub>IO</sub> =0mA <sup>4)</sup> , 100% duty, $\overline{CS}=V_{IL}$ , $\overline{PS}=V_{IH}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	35	mA	
	I <sub>CC2P</sub>	Cycle time=t <sub>RC</sub> +3t <sub>PC</sub> , I <sub>IO</sub> =0mA <sup>4)</sup> , 100% duty, $\overline{CS}=V_{IL}$ , $\overline{PS}=V_{IH}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	35	mA	
Average Operating Current(Sync)	I <sub>CC3</sub>	Burst Length 4, Latency 5, 104MHz, I <sub>IO</sub> =0mA <sup>4)</sup> , Address transition 1 time, $\overline{CS}=V_{IL}$ , $\overline{PS}=V_{IH}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	-	35	mA	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =0.1mA	-	-	0.2	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-0.1mA	1.4	-	-	V	
Standby Current(CMOS)	I <sub>SB1</sub> <sup>1)</sup>	$\overline{CS} \geq V_{CCQ}-0.2V$ , $\overline{PS} \geq V_{CCQ}-0.2V$ , Other inputs=V <sub>SS</sub> or V <sub>CCQ</sub> (Toggle is not allowed) <sup>5)</sup>	< 40°C	-	-	100	μA
			< 85°C	-	-	120	μA

1. I<sub>SB1</sub> is measured after 60ms after CS high. CLK should be fixed at high or at Low.

2. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize refresh cycle below 40°C.

3. I<sub>IO</sub>=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

4. V<sub>IN</sub>=0V; all inputs should not be toggle.

5. Clock should not be inserted between ADV low and  $\overline{WE}$  low during Write operation.

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## MRS (MODE REGISTER SET)

The mode registers store the values for the various modes to make UtRAM suitable for a various applications through MRS. There are two ways to perform MRS. One is PS pin MRS and the other is Software MRS. The mode registers have lots of fields and each field consists of several options. Refer to the Table below for detailed Mode Register Setting. A19~A20 addresses are "Don't care" in Mode Register Setting.

### MRS CODE

MRS code consists of 12 categories and several options in each category. BL, WC, Latency, Wrap, WP, MS and IL are related to bus operation and DS is related to device output impedance.

#### Mode Register Setting according to field of function

Address	A18	A17~A16	A15~A14	A13	A12	A11~A9	A8	A7~A5
Function	IL	DS	MS	WP	Wrap	Latency	WC	BL

Initial Latency		Driver Strength			Mode Select				
A18	IL	A17	A16	DS	A15	A14	MS <sup>1)</sup>		
0	Fixed	0	0	Full Drive	0	0	Mode 1(Async. 4 Page Read / Async. Write)		
1	Variable	0	1	1/2 Drive	0	1	Mode 2(Sync. Burst Read / Async. Write)		
		1	0	1/4 Drive	1	0	Mode 3(Sync. Burst Read / Sync. Burst Write)		

WAIT Polarity		Wrap		Latency Count				Wait Configuration		Burst Length			
A13	WP <sup>1)</sup>	A12	Wrap	A11	A10	A9	Latency	A8	WC	A7	A6	A5	BL
0	Low Enable	0	Wrap	1	0	0	2	0	One clock prior	0	1	0	4 word
1	High Enable	1	No-Wrap	0	0	0	3	1	At data	0	1	1	8 word
				0	0	1	4			1	0	0	16 word
				0	1	0	5			1	0	1	32 word
				0	1	1	6			1	1	1	Continuous <sup>2)</sup>
				1	0	1	7						
				1	1	0	8						
				1	1	1	9						

[Note]

- A0~A4, A19~A20 addresses are "Don't care" & reserved for future use.
- The modes are set automatically to default modes which are 4 Page Read and Asynchronous Write after power up.

- Mode Change Rules.

Mode1 to Mode2 (or vice-versa) : No limitation

Mode1 to Mode3 : 1 dummy write(to any address with any data) is necessary before setting Mode3

\* Dummy write: Dummy write timing is just the same with normal write timing. It is necessary because 'Late write' is applied to Asynchronous write as in Mode1.

\* Late write: The data that is latched in previous write cycle is written in the address that is also latched in previous write cycle when Write starts. And current data and address are latched when Write ends. (WE high or CS high, whichever comes first)

Mode3 to Mode1 : 1 dummy write is necessary before setting Mode1

\* Dummy write: The data and the address should be the same with those which are used during Mode1 to Mode3 transition.

1) WP[0]: The data is available when  $\overline{\text{WAIT}}$  signal is High. All the timings in this spec are illustrated based on this mode.

WP[1]: The data is available when  $\overline{\text{WAIT}}$  signal is Low.

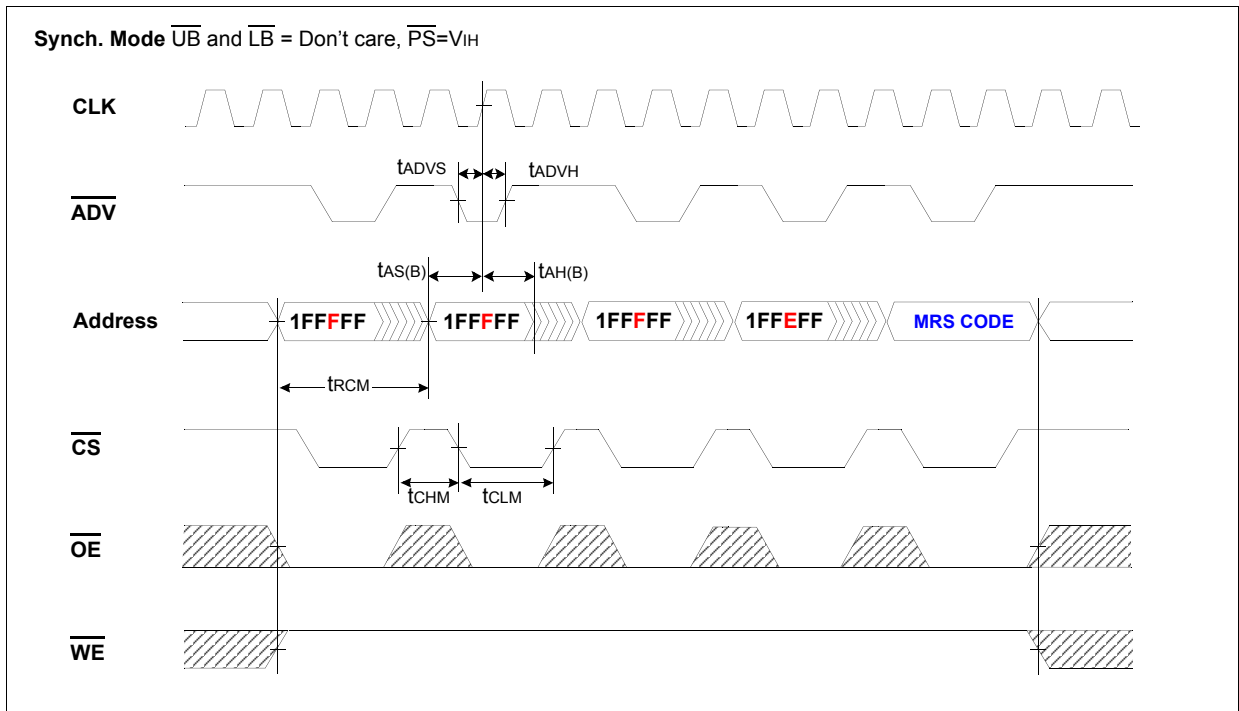
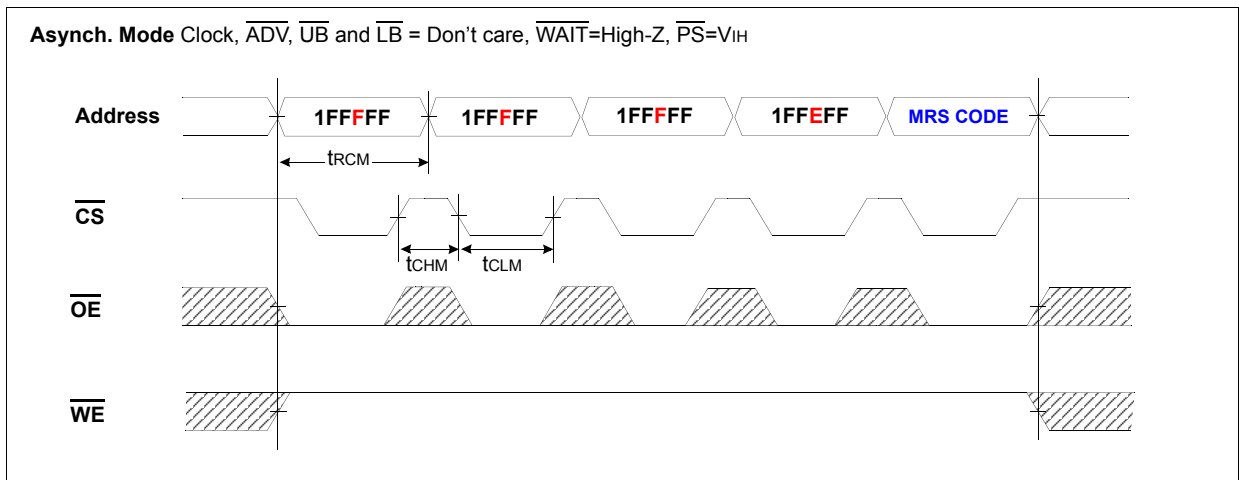
2) Refresh command will be denied during continuous operation.  $\overline{\text{CS}}$  low should not be longer than tBC(max. 2.5us)



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## MRS TIMING WAVEFORM (SOFTWARE)

Software MRS timing consists of 5 Read cycles. Each cycle is normal Read cycle.  $\overline{CS}$  pin should be toggling between cycles. 1st, 2nd and 3rd cycle should be 1FFFFF(h), 4th cycle should be 1FFEFF(h) and 5th cycle should be MRS code



Note) Above timing and address condition should not be used in the normal operation. The above condition should be used only for the mode register setting purpose.

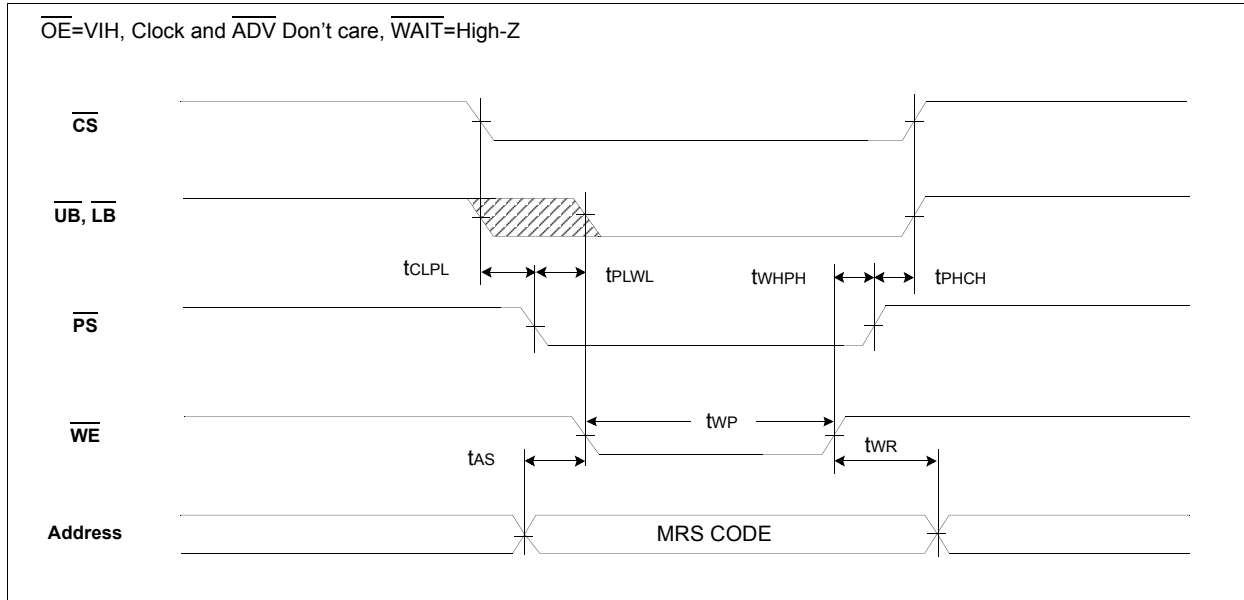
## AC CHARACTERISTICS

Parameter List	Symbol	Min	Max	Units	Parameter List	Symbol	Min	Max	Units
$\overline{ADV}$ setup time to clock	tADVS	3	-	ns	Read cycle time	tRCM	70	-	ns
$\overline{ADV}$ hold time from clock	tADVH	2	-	ns	$\overline{CS}$ high time	tCHM	10	-	ns
Address setup time to clock	tAS(B)	3	-	ns	$\overline{CS}$ low time	tCLM	60	-	ns
Address hold time from clock	tAH(B)	2	-	ns					

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### MRS TIMING WAVEFORM ( $\overline{PS}$ Pin)

MRS can be implemented using by  $\overline{PS}$  pin. Serial assertion of control signals of  $\overline{CS}$ ,  $\overline{UB}$  &  $\overline{LB}$ ,  $\overline{PS}$  and  $\overline{WE}$  will get the device to be ready for MRS. MRS CODE should be set up before  $\overline{WE}$  low and keep the CODE until one of those control signals deserts. MRS terminates when one of those control signals deserts. Clock &  $\overline{ADV}$  are don't care in Asynchronous mode.



### AC CHARACTERISTICS

	Parameter List	Symbol	Speed		Units
			Min	Max	
MRS	$\overline{CS}$ Low to $\overline{PS}$ Low	tCLPL	0	-	ns
	$\overline{PS}$ Low to $\overline{WE}$ Low	tPLWL	0	-	ns
	$\overline{WE}$ High to $\overline{PS}$ High	tWHPH	0	-	ns
	$\overline{PS}$ High to $\overline{CS}$ High	tPHCH	0	-	ns

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## Burst Length [A7~A5] & Wrap [A12]

The device supports 4 word, 8 word, 16 word, 32 word and Continuous burst read or write. and Wrap & No-Wrap are supported for Burst sequence.

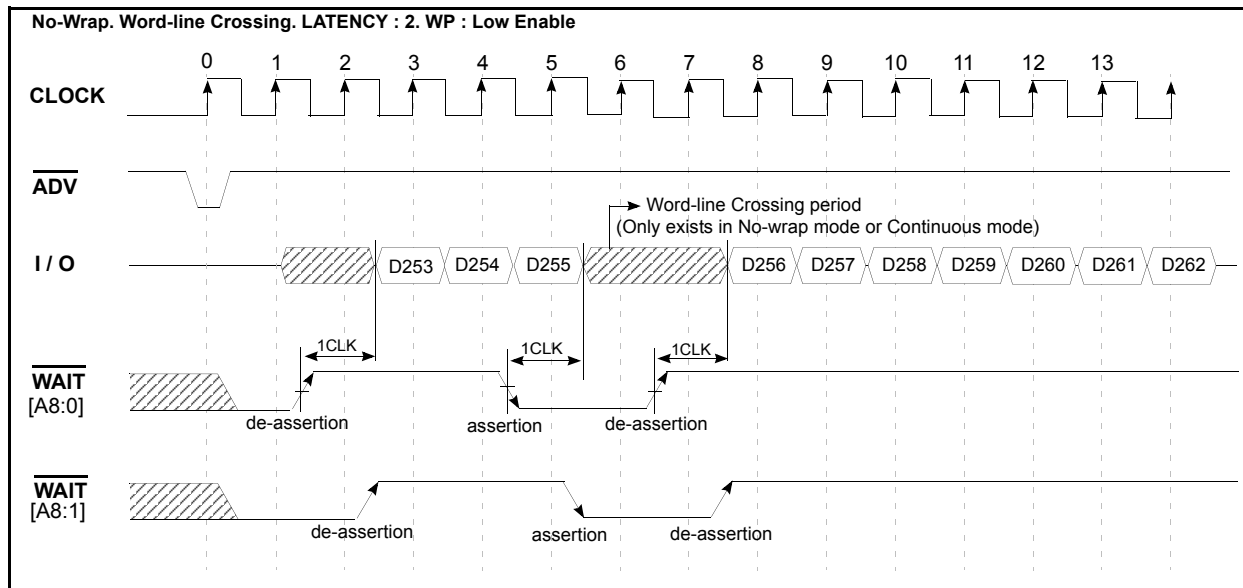
Burst Address Sequence(Decimal)					
Mode	Start	4 word	8 word	16 word	32 word
WRAP	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31 - 0
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31 - 0 - 1
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31- 0 - 1 - 2
	~		~	~	~
	7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7 - 8 - 9 - 10 - 11 - 12 ~ 2 - 3 - 4 - 5 - 6
	~		~	~	~
	15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20 ~ 10- 11- 12- 13- 14
~				~	
31				31- 0 - 1 - 2 - 3 - 4 ~ 25-26-27-28-29-30	
No-WRAP	0	0-1-2-3	0- 1- 2- 3- 4- 5- 6- 7	0- 1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15	0 - 1 - 2 - 3 - 4 - 5 ~ 26-27-28-29-30-31
	1	1-2-3-4	1- 2- 3- 4- 5- 6- 7- 8	1- 2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16	1 - 2 - 3 - 4 - 5 - 6 ~ 27-28-29-30-31-32
	2	2-3-4-5	2- 3- 4- 5- 6- 7- 8- 9	2- 3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17	2 - 3 - 4 - 5 - 6 - 7 ~ 28-29-30-31-32-33
	3	3-4-5-6	3- 4- 5- 6- 7- 8- 9-10	3- 4- 5- 6- 7- 8- 9- 10- 11- 12-13-14-15-16-17-18	3 - 4 - 5 - 6 - 7 - 8 ~ 29-30-31-32-33-34
	~		~	~	~
	7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	7 - 8 - 9 - 10-11-12 ~ 33-34-35-36-37-38
	~		~	~	~
	15			15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	15-16-17-18-19-20 ~ 41-42-43-44-45-46
~				~	
31				31-32-33-34-35-36 ~ 57-58-59-60-61-62	

1. Continuous Burst mode needs to meet tBC(max. 2.5us) parameter.

## WAIT Configuration [A8] & WAIT Polarity [A13]

The WAIT signal is output signal indicating the status of the data on the bus whether or not it is valid. WAIT configuration is to decide the timing when WAIT asserts or deserts. WAIT asserts (or deserts) one clock prior to the data when A8 is set to 0. (WAIT asserts (or deserts) at data clock when A8 is set to 1). WAIT polarity is to decide the WAIT signal level at which data is valid or invalid. Data is valid if WAIT signal is high when A13 is set to 0. (Data is valid if WAIT signal is low when A13 is set to 1). All the timing diagrams in this SPEC are illustrated based on following setup; [A13 : 0] and [A8 : 0].

Below timing shows WAIT signal's movement when word boundary crossing happens in No-wrap mode.



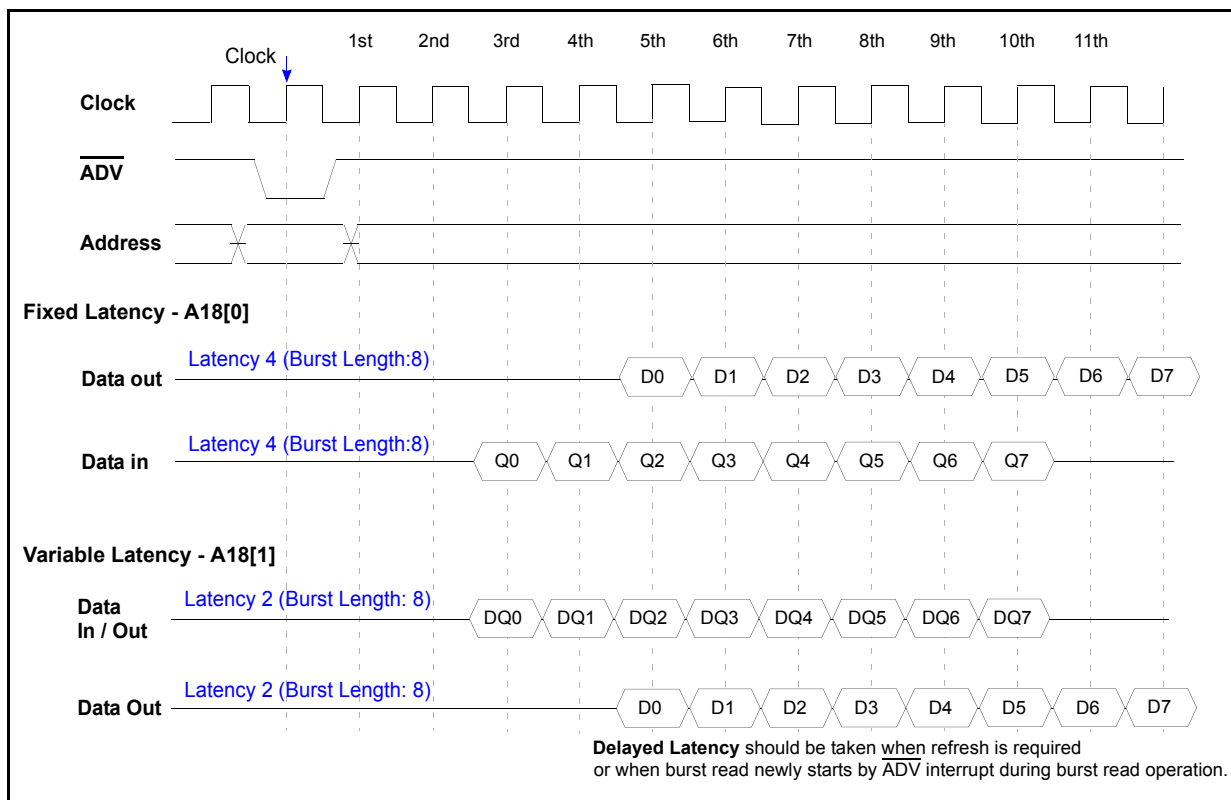
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## Latency [A11~A9]

The Latency stands for the number of clocks before the first data available from the burst command.

Item	Upto 66MHz		Upto 80MHz		Upto 104MHz	
	Fixed	Variable	Fixed	Variable	Fixed	Variable
Latency Set(A11:A10:A9)	4(0:0:1)	2(1:0:0)	5(0:1:0)	3(0:0:0)	7(1:0:1)	4(0:0:1)
Read Latency(min)	4	2 / 4 <sup>1)</sup>	5	3 / 5 <sup>1)</sup>	7	4 / 7 <sup>1)</sup>
1st Read data fetch clock	5th	3rd / 5th <sup>1)</sup>	6th	4th / 6th <sup>1)</sup>	8th	5th / 8th <sup>1)</sup>
Write Latency(min)	2	2	3	3	4	4
1st Write data loading clock	3rd	3rd	4th	4th	5th	5th

1) Delayed Latency should be taken when refresh is required or when burst read newly starts by ADV interrupt during burst read operation.



## Driver Strength [A17~A16]

The optimization of output driver strength is possible to adjust for the different data loadings. The device can minimize the noise generated on the data bus during read operation. The device supports full, 1/2 and 1/4 driver strength. The device's default mode is 1/2 driver strength.

Driver Strength	Full	1 / 2	1 / 4
IMPEDANCE(typ.)	40Ω	90Ω	150Ω

1. Impedance values are typical values, not 100% tested.

# K1B3216BDE

## OPERATION MODE [A15~A14]

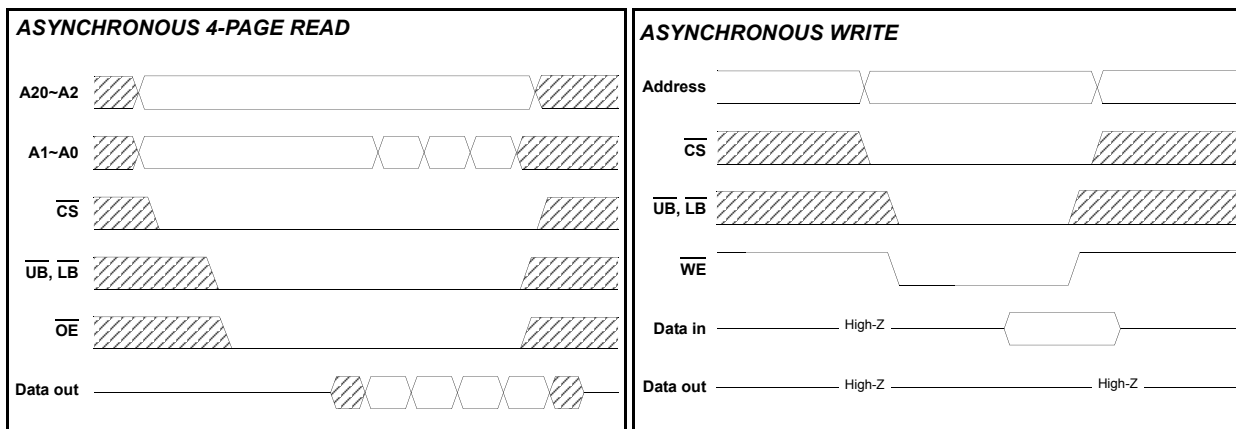
### MODE1. ASYNCHRONOUS READ / ASYNCHRONOUS WRITE MODE

#### Asynchronous read operation

Asynchronous read operation starts when  $\overline{CS}$ ,  $\overline{OE}$  and  $\overline{UB}$  or  $\overline{LB}$  are asserted. First data come out after random access time( $t_{AA}$ ) but second, third and fourth data come out after page access time( $t_{PA}$ ) when using the page addresses (A0, A1).  $\overline{PS}$  and  $\overline{WE}$  should be de-asserted during read operation. Clock,  $\overline{ADV}$  are don't care during read operation and  $\overline{WAIT}$  is Hi-Z.

#### Asynchronous write operation

Asynchronous write operation starts when  $\overline{CS}$ ,  $\overline{WE}$  and  $\overline{UB}$  or  $\overline{LB}$  are asserted.  $\overline{PS}$  and should be de-asserted during write operation. Clock,  $\overline{OE}$ ,  $\overline{ADV}$  are don't care during write operation and  $\overline{WAIT}$  signal is Hi-Z.



### FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{PS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	Mode	Power
H	H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Deselected	Standby
L	H	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	Output Disabled	Active
L	H	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	H	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	Word Write	Active

1. X means "Don't care". X should be low or high state.
2. In asynchronous mode, Clock and  $\overline{ADV}$  are ignored. Clock and  $\overline{ADV}$  should be low or high state.
3.  $\overline{WAIT}$  pin is High-Z in Asynchronous mode.

# K1B3216BDE

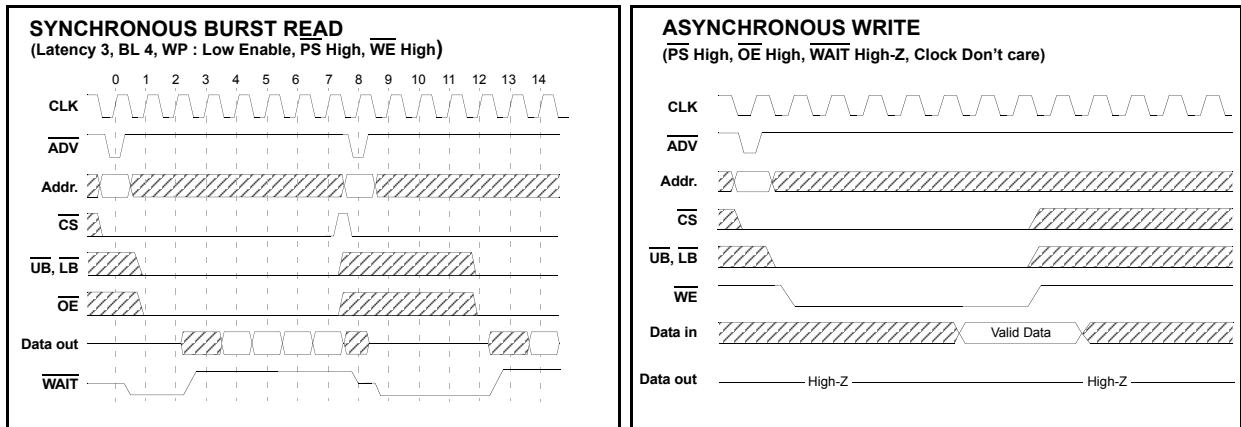
## MODE2. SYNCHRONOUS BURST READ / ASYNCHRONOUS WRITE MODE

### Synchronous Burst Read Operation

Burst Read command is implemented when  $\overline{ADV}$  is detected low at clock rising edge.  $\overline{WE}$  should be de-asserted during Burst read, Burst operation re-starts whenever  $\overline{ADV}$  is detected low at clock rising edge even in the middle of operation. Variable latency allows the U1RAM to be configured for minimum latency at high frequencies, but the controller must monitor  $\overline{WAIT}$  to detect any conflict with refresh cycles.

### Asynchronous Write Operation

Asynchronous write operation starts when  $\overline{CS}$ ,  $\overline{WE}$  and  $\overline{UB}$  or  $\overline{LB}$  are asserted.  $\overline{PS}$  and should be de-asserted during write operation. Clock,  $\overline{OE}$ ,  $\overline{ADV}$  are don't care during write operation and  $\overline{WAIT}$  signal is Hi-Z.



### FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{PS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	X <sup>1)</sup>	X <sup>1)</sup>	Deselected	Standby
L	H	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	X <sup>1)</sup>	H	Output Disabled	Active
L	H	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	X <sup>1)</sup>	H	Output Disabled	Active
L	H	X <sup>1)</sup>	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z			Read Command	Active
L	H	L	H	L	H	Dout	High-Z		H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout		H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout		H	Word Read	Active
L	H	H	L	L	H	Din	High-Z	X <sup>1)</sup>		Lower Byte Write	Active
L	H	H	L	H	L	High-Z	Din	X <sup>1)</sup>		Upper Byte Write	Active
L	H	H	L	L	L	Din	Din	X <sup>1)</sup>		Word Write	Active

1. X means "Don't care". X should be low or high state.  
 2.  $\overline{WAIT}$  is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for  $\overline{WAIT}$  pin function.

# K1B3216BDE

## MODE3. SYNCHRONOUS BURST READ / SYNCHRONOUS BURST WRITE MODE

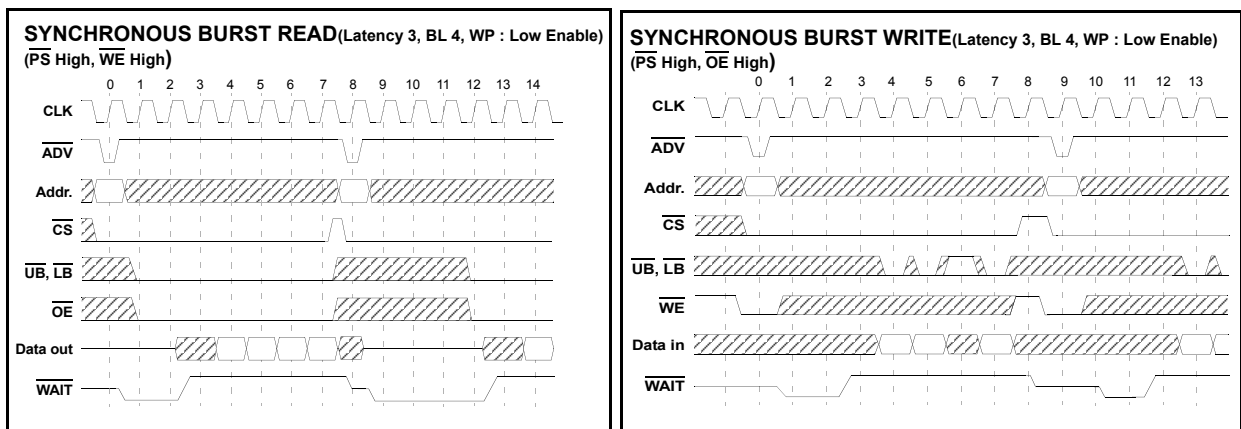
### Synchronous Burst Read Operation

Burst Read command is implemented when  $\overline{ADV}$  is detected low at clock rising edge.  $\overline{WE}$  should be de-asserted during Burst read, Burst Read operation re-starts whenever  $\overline{ADV}$  is detected low at clock rising edge even in the middle of Burst Read operation. Variable latency allows the UTRAM to be configured for minimum latency at high frequencies, but the controller must monitor  $\overline{WAIT}$  to detect any conflict with refresh cycles.

### Synchronous Burst Write Operation

Burst Write command is implemented when  $\overline{ADV}$  &  $\overline{WE}$  are detected low at clock rising edge. Burst Write operation re-starts whenever  $\overline{ADV}$  is detected low at clock rising edge even in the middle of Burst Write operation.

Write operations always use fixed latency.



### FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{PS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O0~7	I/O8~15	CLK	$\overline{ADV}$	Mode	Power
H	H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	X <sup>1)</sup>	X <sup>1)</sup>	Deselected	Standby
L	H	H	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	X <sup>1)</sup>	H	Output Disabled	Active
L	H	X <sup>1)</sup>	X <sup>1)</sup>	H	H	High-Z	High-Z	X <sup>1)</sup>	H	Output Disabled	Active
L	H	X <sup>1)</sup>	H	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	⌋	⌋	Read Command	Active
L	H	L	H	L	H	Dout	High-Z	⌋	H	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	⌋	H	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	⌋	H	Word Read	Active
L	H	X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	High-Z	⌋	⌋	Write Command	Active
L	H	H	X <sup>1)</sup>	L	H	Din	High-Z	⌋	H	Lower Byte Write	Active
L	H	H	X <sup>1)</sup>	H	L	High-Z	Din	⌋	H	Upper Byte Write	Active
L	H	H	X <sup>1)</sup>	L	L	Din	Din	⌋	H	Word Write	Active
L	L	H	L	L	L	High-Z	High-Z	⌋	⌋	Mode Register Set	Active

1. X means "Don't care". X should be low or high state.

2.  $\overline{WAIT}$  is device output signal so does not have any affect to the mode definition. Please refer to each timing diagram for  $\overline{WAIT}$  pin function.

# K1B3216BDE

## MODE 1 AC OPERATING CONDITIONS (ASYNCH. READ / ASYNCH. WRITE)

### TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V<sub>CCQ</sub>-0.2V

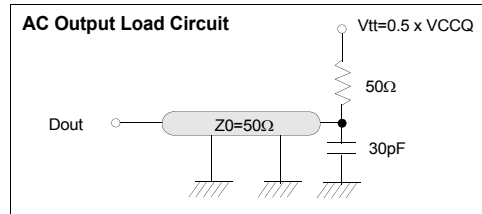
Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V<sub>CCQ</sub>

Output load: CL=30pF

V<sub>CC</sub>: 1.7V~1.95V

T<sub>A</sub>: -40°C~85°C



### AC CHARACTERISTICS

Parameter List		Symbol	Speed		Units
			Min	Max	
Common	$\overline{CS}$ High Pulse Width	tCSHP(A)	10	-	ns
Asynch. Read	Read Cycle Time	t <sub>RC</sub>	70	-	ns
	Page Read Cycle Time	t <sub>PC</sub>	20	-	ns
	Address Access Time	t <sub>AA</sub>	-	70	ns
	Page Access Time	t <sub>PA</sub>	-	20	ns
	Chip Select to Output	t <sub>CO</sub>	-	70	ns
	Output Enable to Valid Output	t <sub>OE</sub>	-	20	ns
	$\overline{UB}$ , $\overline{LB}$ Access Time	t <sub>BA</sub>	-	20	ns
	Chip Select to Low-Z Output	t <sub>LZ</sub>	10	-	ns
	$\overline{UB}$ , $\overline{LB}$ Enable to Low-Z Output	t <sub>BLZ</sub>	5	-	ns
	Output Enable to Low-Z Output	t <sub>OLZ</sub>	5	-	ns
	Chip Disable to High-Z Output	t <sub>CHZ</sub>	0	10	ns
	$\overline{UB}$ , $\overline{LB}$ Disable to High-Z Output	t <sub>BHZ</sub>	0	10	ns
	Output Disable to High-Z Output	t <sub>OHZ</sub>	0	10	ns
	Output Hold	t <sub>OH</sub>	5	-	ns
Asynch. Write	Write Cycle Time	t <sub>WC</sub>	70	-	ns
	Chip Select to End of Write	t <sub>CW</sub>	60	-	ns
	Address Set-up Time to Beginning of Write	t <sub>AS</sub>	0	-	ns
	Address Valid to End of Write	t <sub>AW</sub>	60	-	ns
	$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	t <sub>BW</sub>	60	-	ns
	Write Pulse Width	t <sub>WP</sub>	55 <sup>1)</sup>	-	ns
	$\overline{WE}$ High Pulse Width	t <sub>WHP</sub>	5	-	ns
	Write Recovery Time	t <sub>WR</sub>	0	-	ns
	Data to Write Time Overlap	t <sub>DW</sub>	20	-	ns
	Data Hold from Write Time	t <sub>DH</sub>	0	-	ns

1. t<sub>WP</sub>(min)=70ns for continuous write without CS toggling longer than 2.5us

2. The High-Z timings measure a 100mV transition from either V<sub>OH</sub> or V<sub>OL</sub> toward V<sub>CCQ</sub> x 0.5

3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V<sub>OH</sub> or V<sub>OL</sub>.

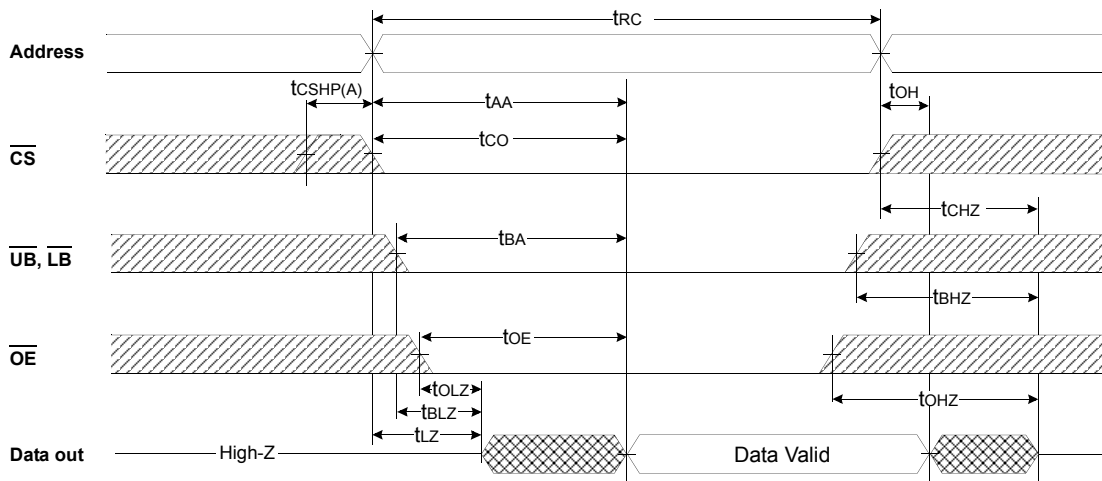


# K1B3216BDE

## TIMING WAVEFORMS (ASYNCH. READ / ASYNCH. WRITE)

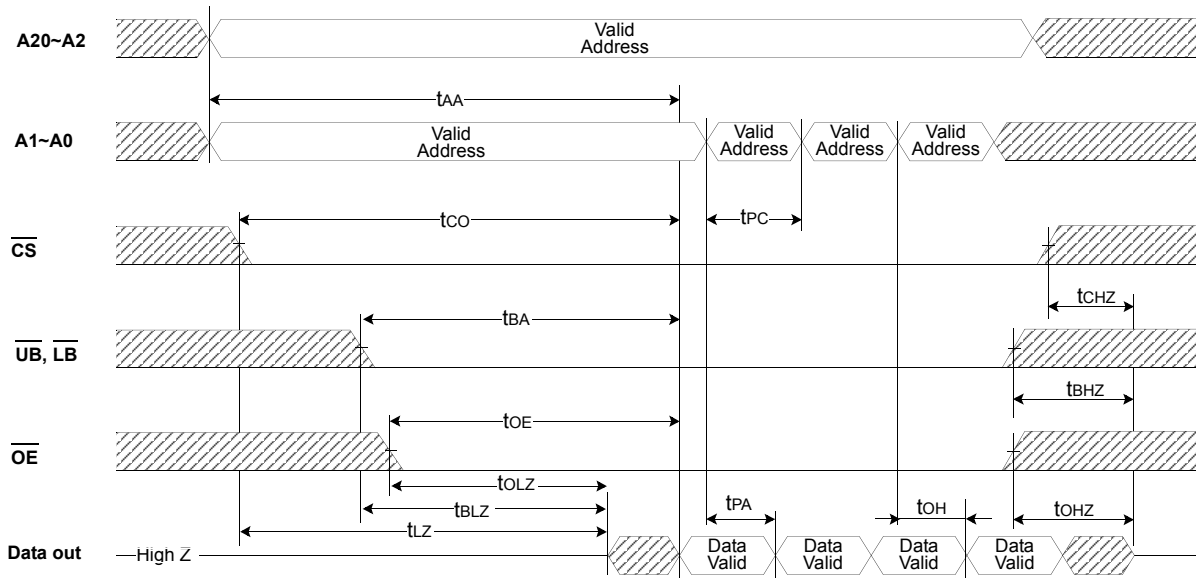
### Asynch. READ

(PS=VIH, WE=VIH, WAIT=High-Z)



### Asynch. PAGE READ

(PS=VIH, WE=VIH, WAIT=High-Z)

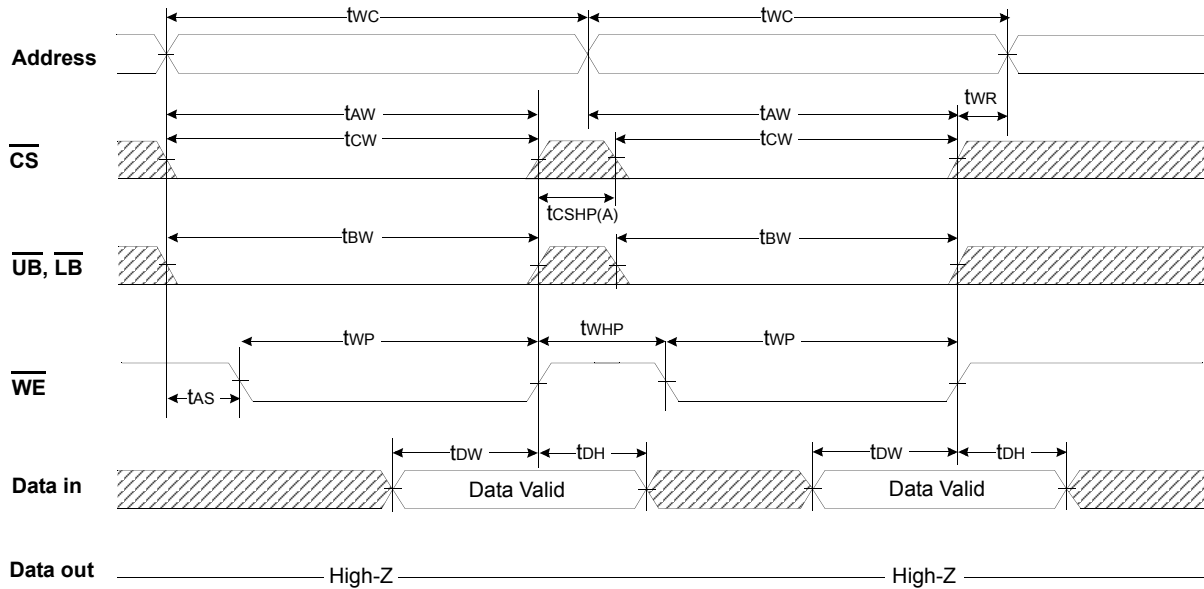


1. tCHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tCHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. In asynchronous read cycle, Clock and ADV signals are ignored.
4. If invalid address signals shorter than min. tRC are continuously repeated for over 2.5us, the device needs a normal read timing(tRC) or needs to sustain standby state for min. tRC at least once in every 2.5us.
5. In asynchronous 4 page read cycle, Clock and ADV signals are ignored.

# K1B3216BDE

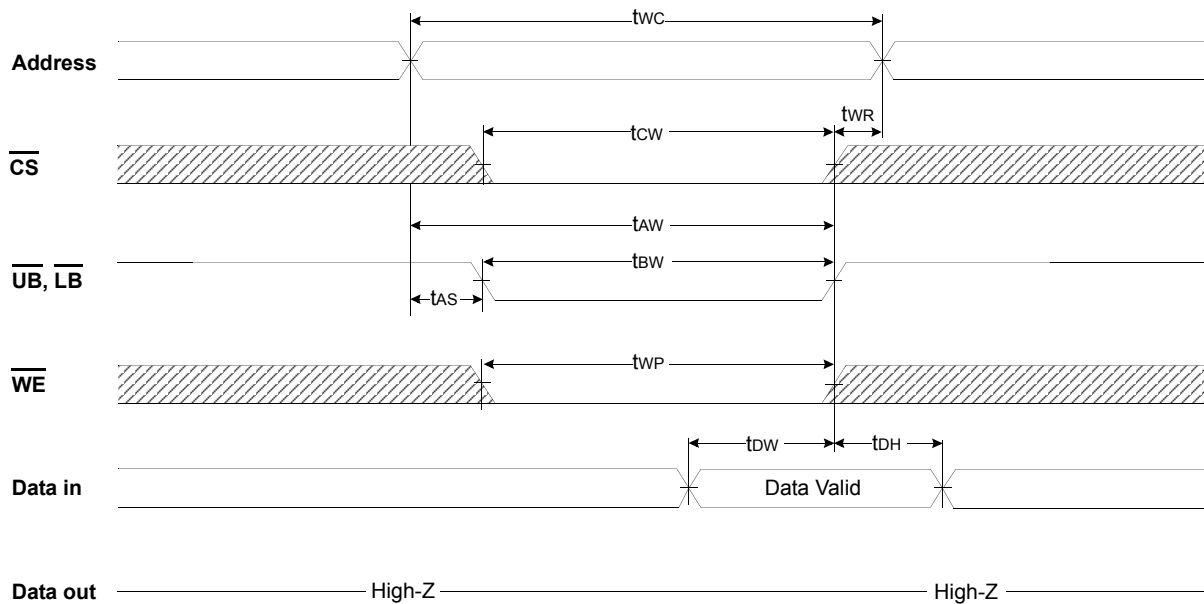
## Asynch. WRITE (1)

(PS=VIH, OE=VIH, WAIT=High-Z, WE Controlled)



## Asynch. WRITE (2)

(PS=VIH, OE=VIH, WAIT=High-Z, UB & LB Controlled)



1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for double byte operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  is applied in case a write ends with  $\overline{CS}$  or  $\overline{WE}$  going high.
5. In asynchronous write cycle, Clock and  $\overline{ADV}$  signals are ignored.
6. Condition for continuous write operation over 15 times :  $t_{WP}(\text{min})=70\text{ns}$

# K1B3216BDE

## MODE 2 AC OPERATING CONDITIONS (SYNCH. READ / ASYNCH. WRITE)

### TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to V<sub>CCQ</sub>-0.2V

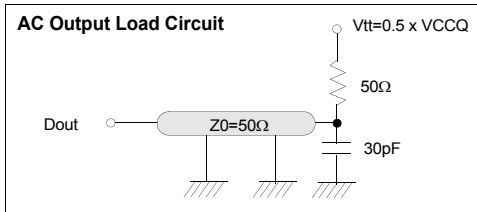
Input rising and falling time: 1ns

Input and output reference voltage: 0.5 x V<sub>CCQ</sub>

Output load: CL=30pF

V<sub>CC</sub>: 1.7V~1.95V

T<sub>A</sub>: -40°C~85°C



### AC CHARACTERISTICS

Parameter List	Symbol	66MHz		80MHz		104MHz		Units
		Min	Max	Min	Max	Min	Max	
Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
Burst Cycle Time	t <sub>BC</sub>	-	2500	-	2500	-	2500	ns
Address Set-up Time to clock	t <sub>AS(B)</sub>	5	-	4	-	3	-	ns
Address Hold Time from clock	t <sub>AH(B)</sub>	2	-	2	-	2	-	ns
ADV Setup Time to clock	t <sub>ADVS</sub>	5	-	4	-	3	-	ns
ADV Hold Time from clock	t <sub>ADVH</sub>	2	-	2	-	2	-	ns
CS Setup Time to clock	t <sub>CSS(B)</sub>	5	-	4	-	3	-	ns
CS High to ADV Low (Burst Stop)	t <sub>BsADV<sup>1)</sup></sub>	0	-	0	-	0	-	ns
CS Low Hold Time from Clock(Burst Stop)	t <sub>CsLH</sub>	2	-	2	-	2	-	ns
CS High Pulse Width	t <sub>CsHP</sub>	5	-	5	-	5	-	ns
CS Low to WAIT Low	t <sub>WL</sub>	-	7.5	-	7.5	-	7.5	ns
Clock to WAIT High	t <sub>WH</sub>	-	11	-	9	-	7	ns
CS High to WAIT High-Z	t <sub>WZ</sub>	-	10	-	10	-	10	ns
UB, LB Low to End of Latency Clock	t <sub>BEL</sub>	20	-	20	-	20	-	ns
OE Low to End of Latency Clock	t <sub>OEL</sub>	20	-	20	-	20	-	ns
UB, LB Low to Low-Z Output	t <sub>B LZ</sub>	5	-	5	-	5	-	ns
OE Low to Low-Z Output	t <sub>O LZ</sub>	5	-	5	-	5	-	ns
Clock Rising to Data Output	t <sub>CD</sub>	-	11	-	9	-	7	ns
Output Hold from clock	t <sub>OH(B)</sub>	2	-	2	-	2	-	ns
Burst End Clock to Output High-Z	t <sub>HZ</sub>	-	10	-	10	-	10	ns
CS High to Output High-Z	t <sub>CHZ</sub>	-	10	-	10	-	10	ns
OE High to Output High-Z	t <sub>OHZ</sub>	-	10	-	10	-	10	ns
UB, LB High to Output High-Z	t <sub>BHZ</sub>	-	10	-	10	-	10	ns

- Refresh can not be implemented when t<sub>BsADV</sub> is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for t<sub>BsADV</sub>.
- The High-Z timings measure a 100mV transition from either V<sub>OH</sub> or V<sub>OL</sub> toward V<sub>CCQ</sub> x 0.5
- The Low-Z timings measure a 100mV transition away from the High-Z level toward either V<sub>OH</sub> or V<sub>OL</sub>.

Parameter List	Symbol	Speed		Units
		Min	Max	
Write Cycle Time	t <sub>WC</sub>	70	-	
Chip Select to End of Write	t <sub>CW</sub>	60	-	ns
ADV Minimum Low Pulse Width	t <sub>ADV</sub>	5	-	ns
Address Set-up Time to Beginning of Write	t <sub>AS</sub>	0	-	ns
Address Set-up Time to ADV Rising	t <sub>AS(A)</sub>	5	-	ns
Address Hold Time from ADV Rising	t <sub>AH(A)</sub>	3	-	ns
CS Setup Time to ADV Rising	t <sub>CSS(A)</sub>	5	-	ns
Address Valid to End of Write	t <sub>AW</sub>	60	-	ns
UB, LB Valid to End of Write	t <sub>BW</sub>	60	-	ns
Write Pulse Width	t <sub>WP</sub>	55 <sup>1)</sup>	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	20	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	ns

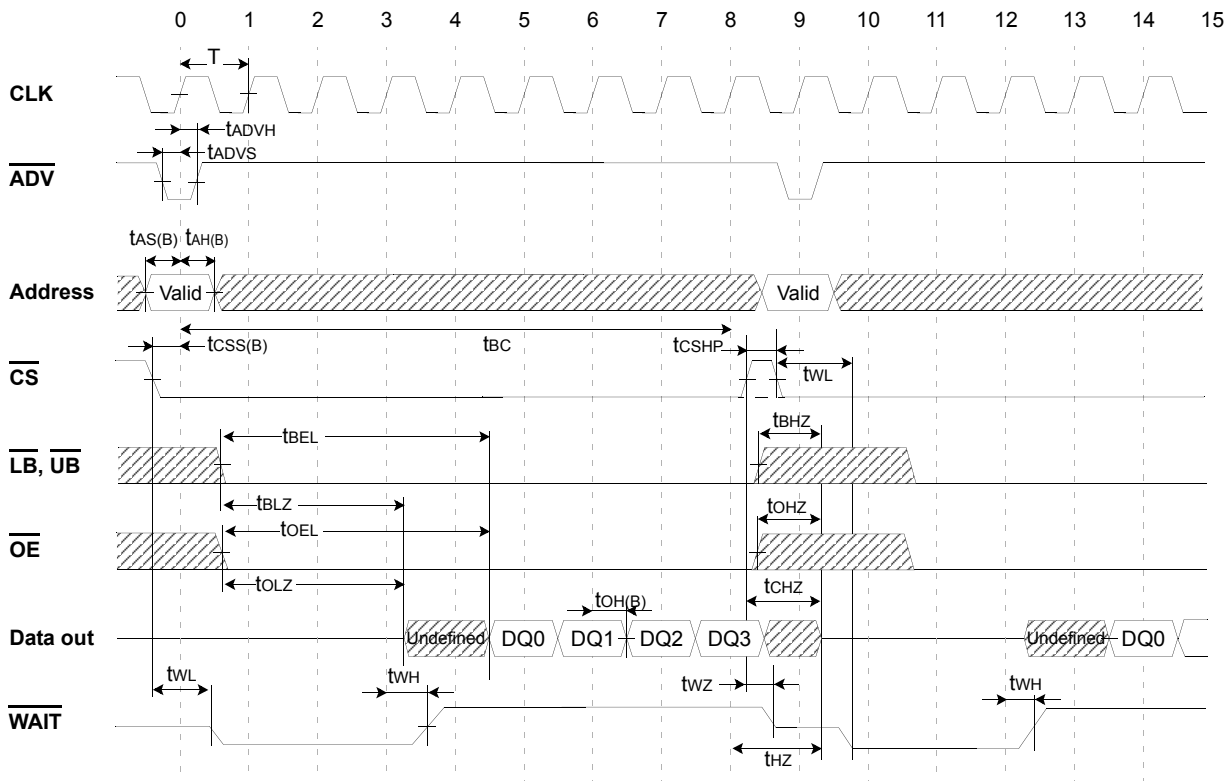
- t<sub>WP</sub>(min)=70ns for continuous write longer than 2.5us without CS toggling.

# K1B3216BDE

## TIMING WAVEFORMS (SYNCH. READ / ASYNCH. WRITE)

### Burst READ - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. /WAIT Low( $t_{WL}$ ) : Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High( $t_{WH}$ ) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z( $t_{WZ}$ ) : Data don't care(driven by  $\overline{CS}$  high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than  $t_{BC}$ (2.5 $\mu$ s)

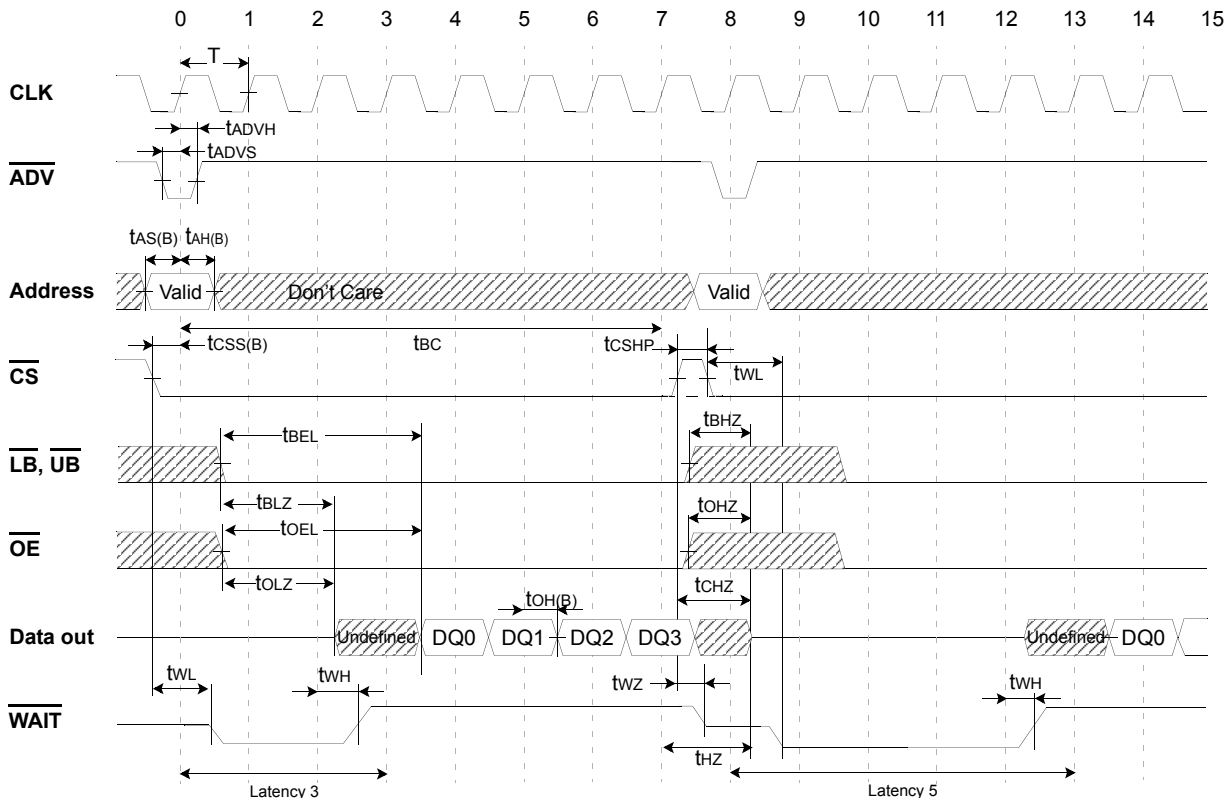
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	t <sub>BLZ</sub>	5	-	5	-	5	-	ns
t <sub>BC</sub>	-	2500	-	2500	-	2500	ns	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
t <sub>ADVS</sub>	5	-	4	-	3	-	ns	t <sub>HZ</sub>	-	10	-	10	-	10	ns
t <sub>ADVH</sub>	2	-	2	-	2	-	ns	t <sub>CHZ</sub>	-	10	-	10	-	10	ns
t <sub>AS(B)</sub>	5	-	4	-	3	-	ns	t <sub>OZH</sub>	-	10	-	10	-	10	ns
t <sub>AH(B)</sub>	2	-	2	-	2	-	ns	t <sub>BHZ</sub>	-	10	-	10	-	10	ns
t <sub>CS(B)</sub>	5	-	4	-	3	-	ns	t <sub>CD</sub>	-	11	-	9	-	7	ns
t <sub>CSHP</sub>	5	-	5	-	5	-	ns	t <sub>OH(B)</sub>	2	-	2	-	2	-	ns
t <sub>BEL</sub>	20	-	20	-	20	-	ns	t <sub>WL</sub>	-	7.5	-	7.5	-	7.5	ns
t <sub>OEL</sub>	20	-	20	-	20	-	ns	t <sub>WH</sub>	-	11	-	9	-	7	ns
t <sub>WZ</sub>	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ - Variable Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=3, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5µs)

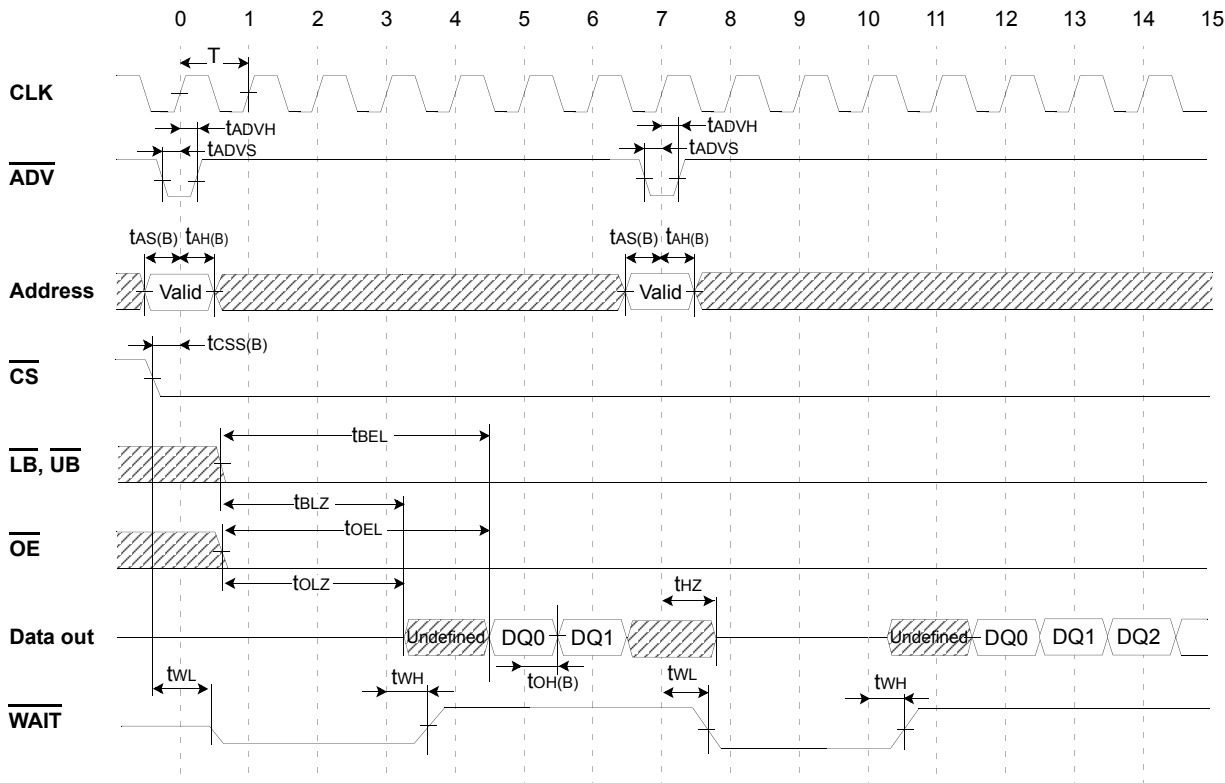
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ ( $\overline{ADV}$ Interrupt) - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. Refresh is blocked during  $\overline{ADV}$  Interrupt Read and continuous Burst Read by  $\overline{ADV}$  interrupt should not be longer than tBC (2.5us)
2. /WAIT Low (tWL) : Data not available (driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High (tWH) : Data available (driven by Latency-1 clock)  
 /WAIT High-Z (tWZ) : Data don't care (driven by  $\overline{CS}$  high going edge)
3. Multiple clock risings are allowed during low  $\overline{ADV}$  period but the First valid data come out after set Latency from the last clock rising.
4. Burst interrupt is allowable after the first data received by controller.

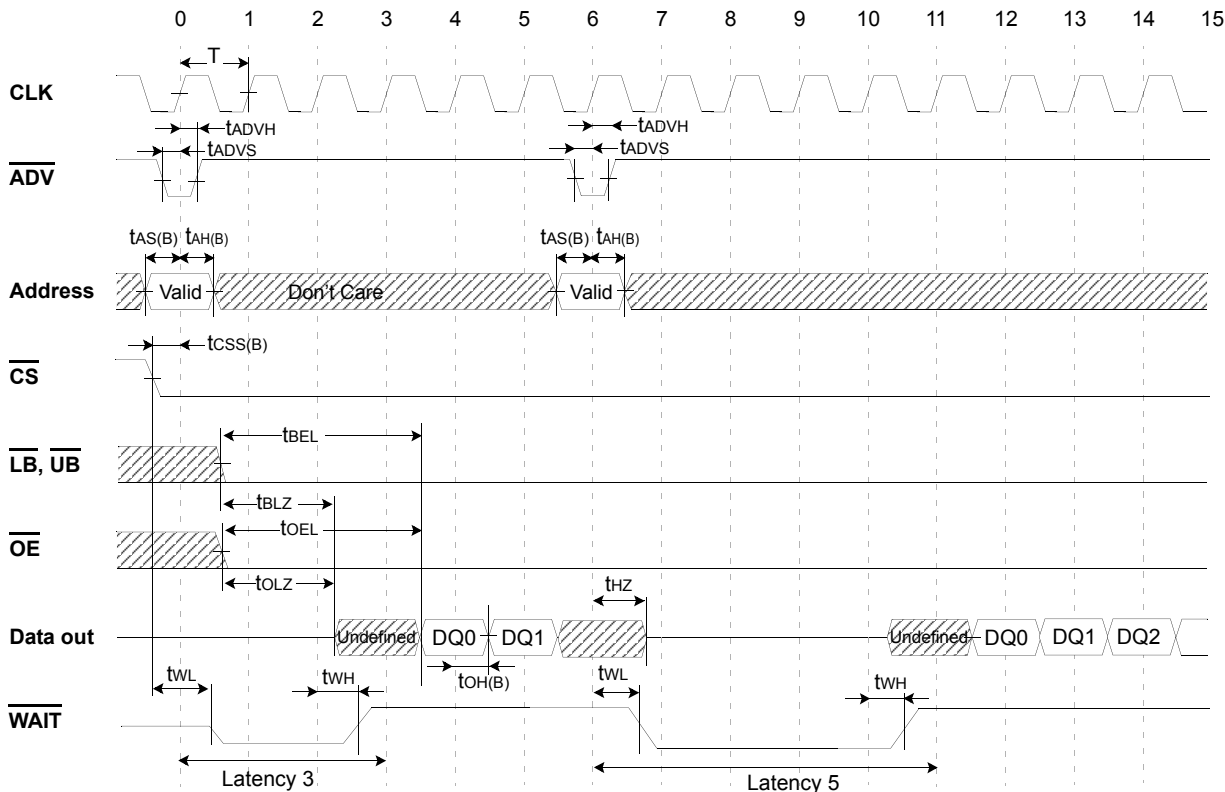
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tcSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tcSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ ( ADV Interrupt) - Variable Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=3, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. Refresh is blocked during ADV Interrupt Read and continuous Burst Read by ADV interrupt should not be longer than tBC (2.5us)
3. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
4. Multiple clock risings are allowed during low ADV period but the First valid data come out after set Latency from the last clock rising.
5. Burst interrupt is allowable after the first data received by controller.

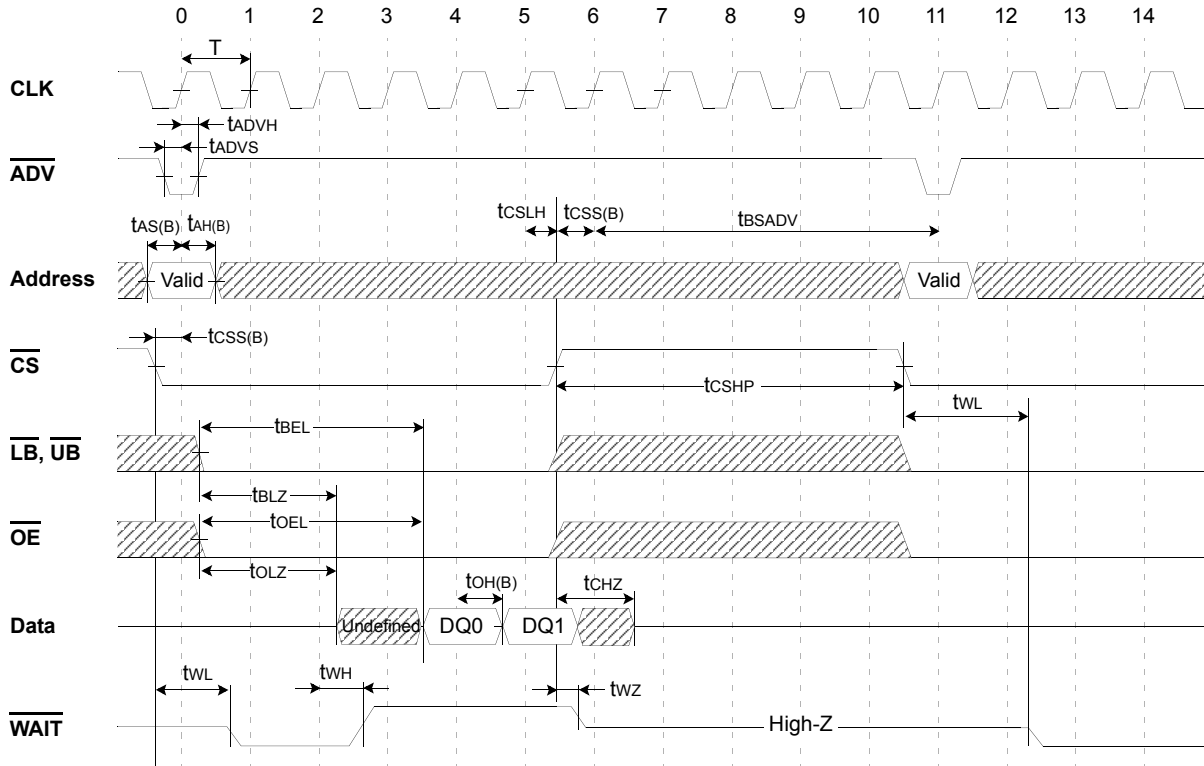
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. /WAIT Low( $t_{WL}$ ) : Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High( $t_{WH}$ ) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z( $t_{WZ}$ ) : Data don't care(driven by  $\overline{CS}$  high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Refresh can not be implemented when  $t_{BSADV}$  is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without  $\overline{CS}$  toggling. To avoid Refresh fail, 13ns for all frequency is needed for  $t_{BSADV}$ .

## AC CHARACTERISTICS

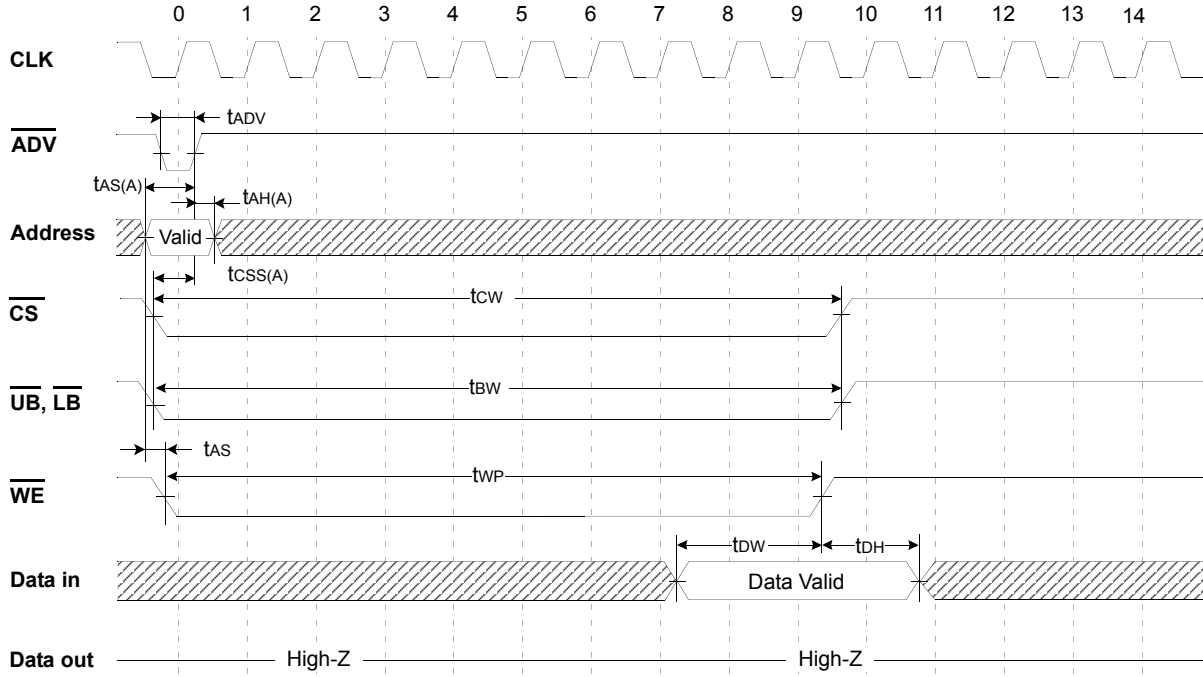
Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
$t_{BSADV}$	0	-	0	-	0	-	ns	$t_{CD}$	-	11	-	9	-	7	ns
$t_{CSLH}$	2	-	2	-	2	-	ns	$t_{OH(B)}$	2	-	2	-	2	-	ns
$t_{CSHP}$	5	-	5	-	5	-	ns	$t_{CHZ}$	-	10	-	10	-	10	ns
$t_{BEL}$	20	-	20	-	20	-	ns	$t_{WL}$	-	7.5	-	7.5	-	7.5	ns
$t_{OEL}$	20	-	20	-	20	-	ns	$t_{WH}$	-	11	-	9	-	7	ns
$t_{BLZ}$	5	-	5	-	5	-	ns	$t_{WZ}$	-	10	-	10	-	10	ns
$t_{OLZ}$	5	-	5	-	5	-	ns								



# K1B3216BDE

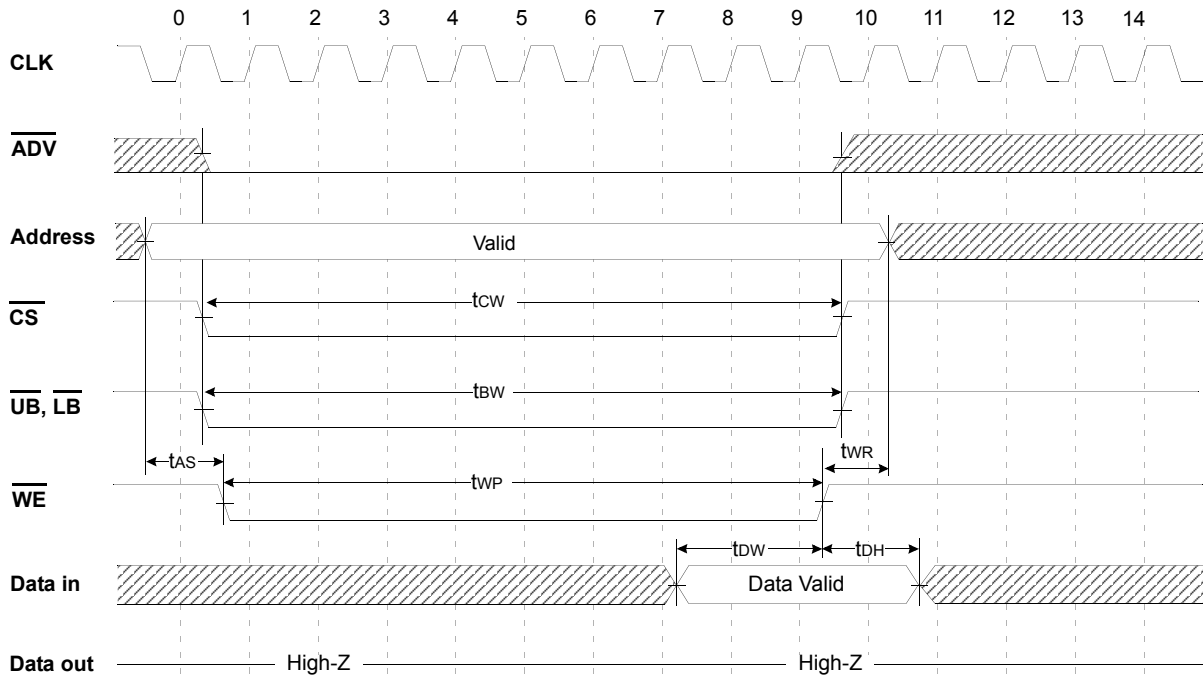
## Asynch. WRITE ( ADV Latch)

(PS=VIH, OE=VIH, WAIT=High-Z)



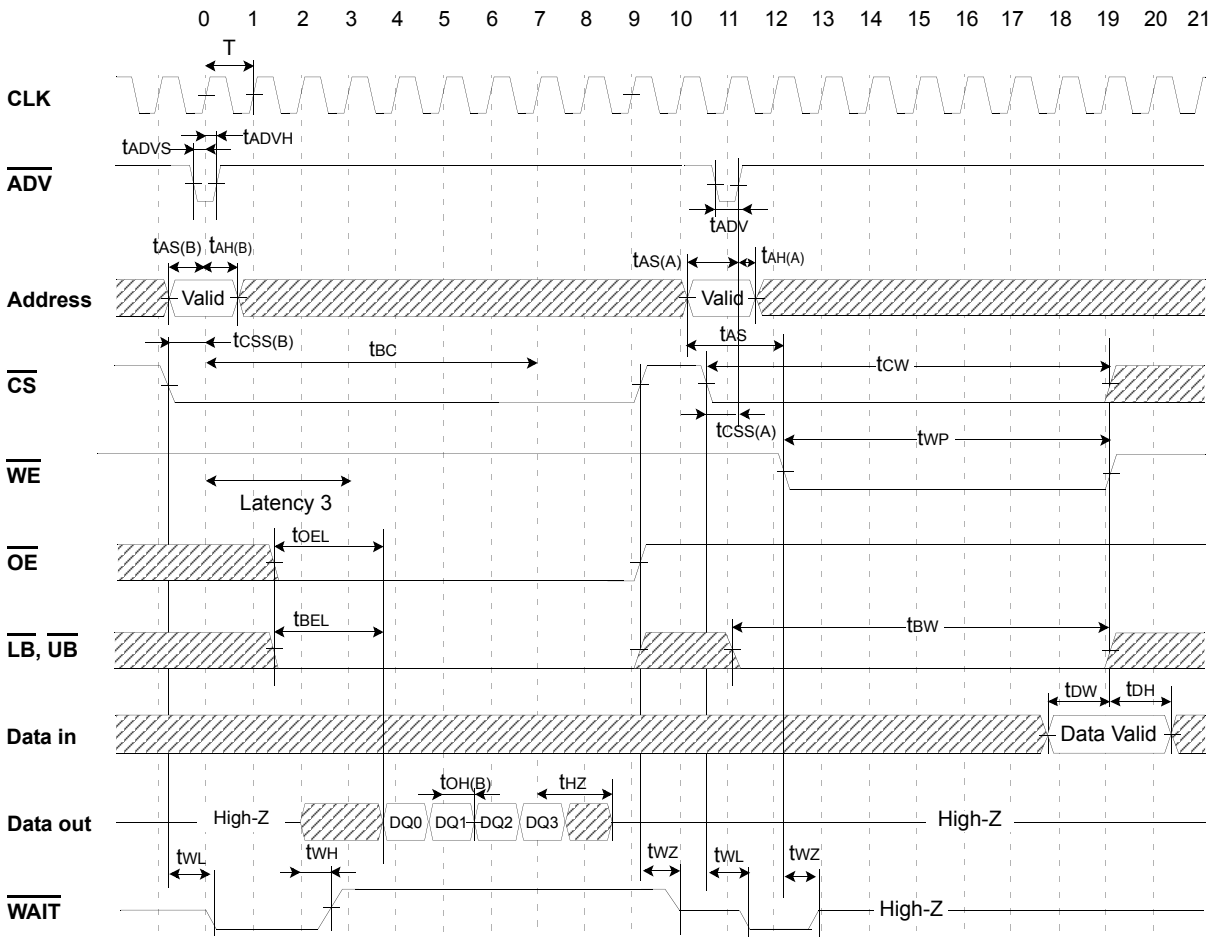
## Asynch. WRITE ( $\overline{ADV}$ Fix Low)

(PS=VIH, OE=VIH, WAIT=High-Z)



**K1B3216BDE**

**Burst READ followed by Asynch. WRITE**  
 (PS=VIH, WAIT=High-Z, Variable Latency=3)

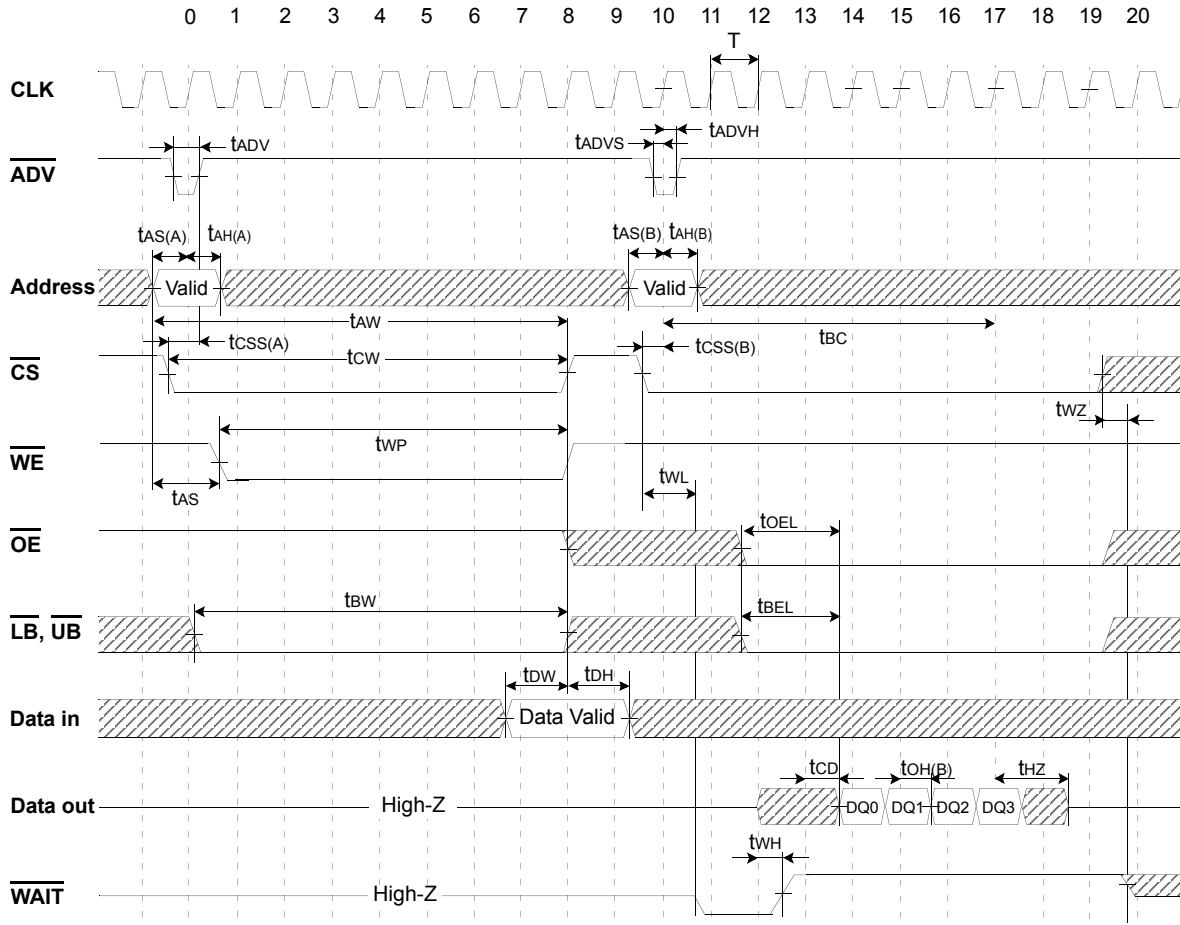


1. A write occurs during the overlap( $t_{WP}$ ) of low  $\overline{CS}$  and low  $\overline{WE}$ . A write begins when  $\overline{CS}$  goes low and  $\overline{WE}$  goes low with asserting  $\overline{UB}$  or  $\overline{LB}$  for single byte operation or simultaneously asserting  $\overline{UB}$  and  $\overline{LB}$  for word operation. A write ends at the earliest transition when  $\overline{CS}$  goes high or  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{BW}$  is measured from the address valid to the end of write. In this address latch type write timing,  $t_{WC}$  is same as  $t_{BW}$ .
3.  $t_{CW}$  is measured from the  $\overline{CS}$  going low to the end of write.
4.  $t_{BW}$  is measured from the  $\overline{UB}$  and  $\overline{LB}$  going low to the end of write.

## K1B3216BDE

### Asynch. WRITE followed by Burst READ

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



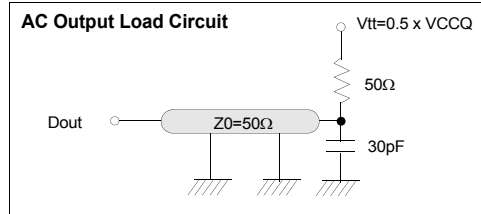
1. /WAIT Low( $t_{WL}$ ) : Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High( $t_{WH}$ ) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z( $t_{WZ}$ ) : Data don't care(driven by  $\overline{CS}$  high going edge)
2. Multiple clock risings are allowed during low  $\overline{ADV}$  period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than  $t_{BC}$ (2.5 $\mu$ s)

# K1B3216BDE

## MODE 3 AC OPERATING CONDITIONS (SYNCH. READ / SYNCH. WRITE)

### TEST CONDITIONS

(Test Load and Test Input/Output Reference)  
 Input pulse level: 0.2 to Vcc-0.2V  
 Input rising and falling time: 1ns  
 Input and output reference voltage: 0.5 x Vcc  
 Output load: CL=30pF  
 Vcc: 1.7V~1.95V  
 TA: -40°C~85°C



### AC CHARACTERISTICS

Parameter List		Symbol	66MHz		80MHz		104MHz		Units
			Min	Max	Min	Max	Min	Max	
Burst Operation (Common)	Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns
	Burst Cycle Time	tBC	-	2500	-	2500	-	2500	ns
	Address Set-up Time to clock	tAS(B)	5	-	4	-	3	-	ns
	Address Hold Time from clock	tAH(B)	2	-	2	-	2	-	ns
	$\overline{ADV}$ Setup Time to clock	tADVS	5	-	4	-	3	-	ns
	$\overline{ADV}$ Hold Time from clock	tADVH	2	-	2	-	2	-	ns
	$\overline{CS}$ Setup Time to clock	tCSS(B)	5	-	4	-	3	-	ns
	$\overline{CS}$ High to New $\overline{ADV}$ Low (Burst Stop)	tBSADV	0	-	0	-	0	-	ns
	$\overline{CS}$ Low Hold Time from Clock(Burst Stop)	tCSLH	2	-	2	-	2	-	ns
	$\overline{CS}$ High Pulse Width	tCSHP	5	-	5	-	5	-	ns
	$\overline{CS}$ Low to $\overline{WAIT}$ Low	tWL	-	7.5	-	7.5	-	7.5	ns
	Clock to $\overline{WAIT}$ High	tWH	-	11	-	9	-	7	ns
$\overline{CS}$ High to $\overline{WAIT}$ High-Z	tWZ	-	10	-	10	-	10	ns	
Burst Read Operation	$\overline{UB}, \overline{LB}$ Low to End of Latency Clock	tBEL	20	-	20	-	20	-	ns
	$\overline{OE}$ Low to End of Latency Clock	toEL	20	-	20	-	20	-	ns
	$\overline{UB}, \overline{LB}$ Low to Low-Z Output	tBLZ	5	-	5	-	5	-	ns
	$\overline{OE}$ Low to Low-Z Output	toLZ	5	-	5	-	5	-	ns
	Clock Rising to Data Output	tCD	-	11	-	9	-	7	ns
	Output Hold from clock	tOH(B)	2	-	2	-	2	-	ns
	Burst End Clock to Output High-Z	tHZ	-	10	-	10	-	10	ns
	$\overline{CS}$ High to Output High-Z	tCHZ	-	10	-	10	-	10	ns
	$\overline{OE}$ High to Output High-Z	toHZ	-	10	-	10	-	10	ns
$\overline{UB}, \overline{LB}$ High to Output High-Z	tBHZ	-	10	-	10	-	10	ns	

1. Refresh can not be implemented when tBSADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBSADV.
2. The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either VOH or VOL.

Burst Write Operation	$\overline{WE}$ Set-up Time to Clock	tWES	5	-	4	-	3	-	ns
	$\overline{WE}$ Hold Time from Clock	tWEH	2	-	2	-	2	-	ns
	$\overline{UB}, \overline{LB}$ Set-up Time to Clock	tBS	5	-	4	-	3	-	ns
	Burst End clock to New $\overline{ADV}$ Low	tBEADV	0	-	0	-	0	-	ns
	$\overline{UB}, \overline{LB}$ Hold Time from Clock	tBH	2	-	2	-	2	-	ns
	Byte Masking Set-up Time to Clock	tBMS	5	-	4	-	3	-	ns
	Byte Masking Hold Time from Clock	tBMH	2	-	2	-	2	-	ns
	Write Data Set-up Time to Clock	tDS	5	-	4	-	3	-	ns
Write Data Hold Time from Clock	tDHC	2	-	2	-	2	-	ns	

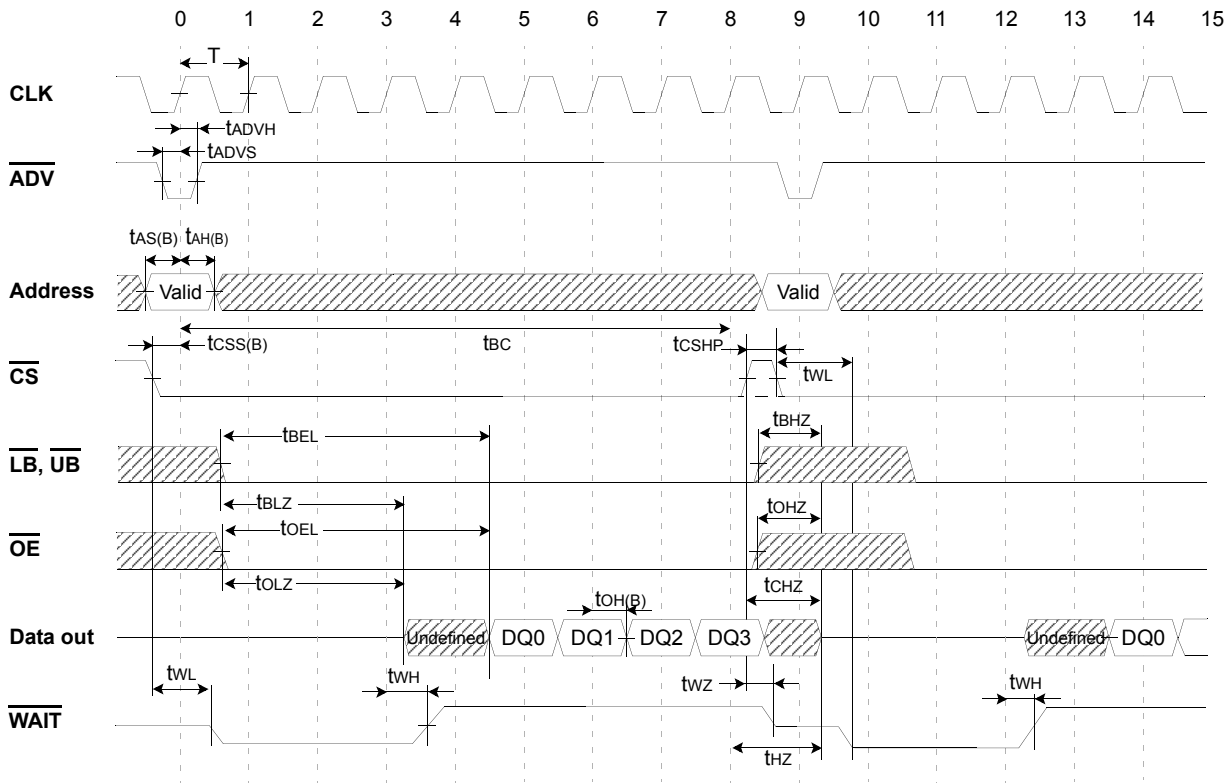
1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.

# K1B3216BDE

## TIMING WAVEFORMS (SYNCH. READ / SYNCH. WRITE)

### Burst READ - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. /WAIT Low( $t_{wL}$ ) : Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High( $t_{wH}$ ) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z( $t_{wZ}$ ) : Data don't care(driven by  $\overline{CS}$  high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than  $t_{BC}$ (2.5 $\mu$ s)

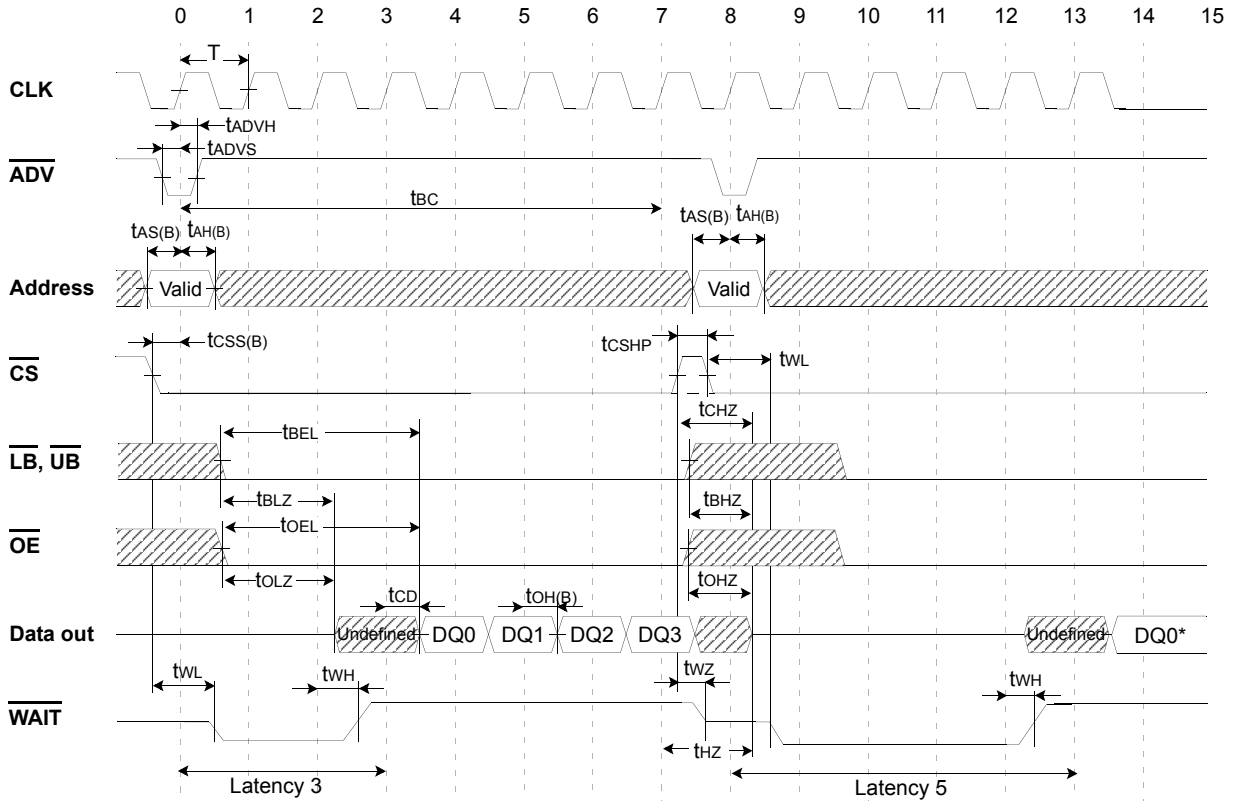
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	toHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tcSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	toH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	twL	-	7.5	-	7.5	-	7.5	ns
toEL	20	-	20	-	20	-	ns	twH	-	11	-	9	-	7	ns
twZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ - Variable Latency

(PS=VIH, WE=VIH, Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Delayed Latency should be taken increased when refresh is required. Refer to Latency Table.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than tBC(2.5μs).

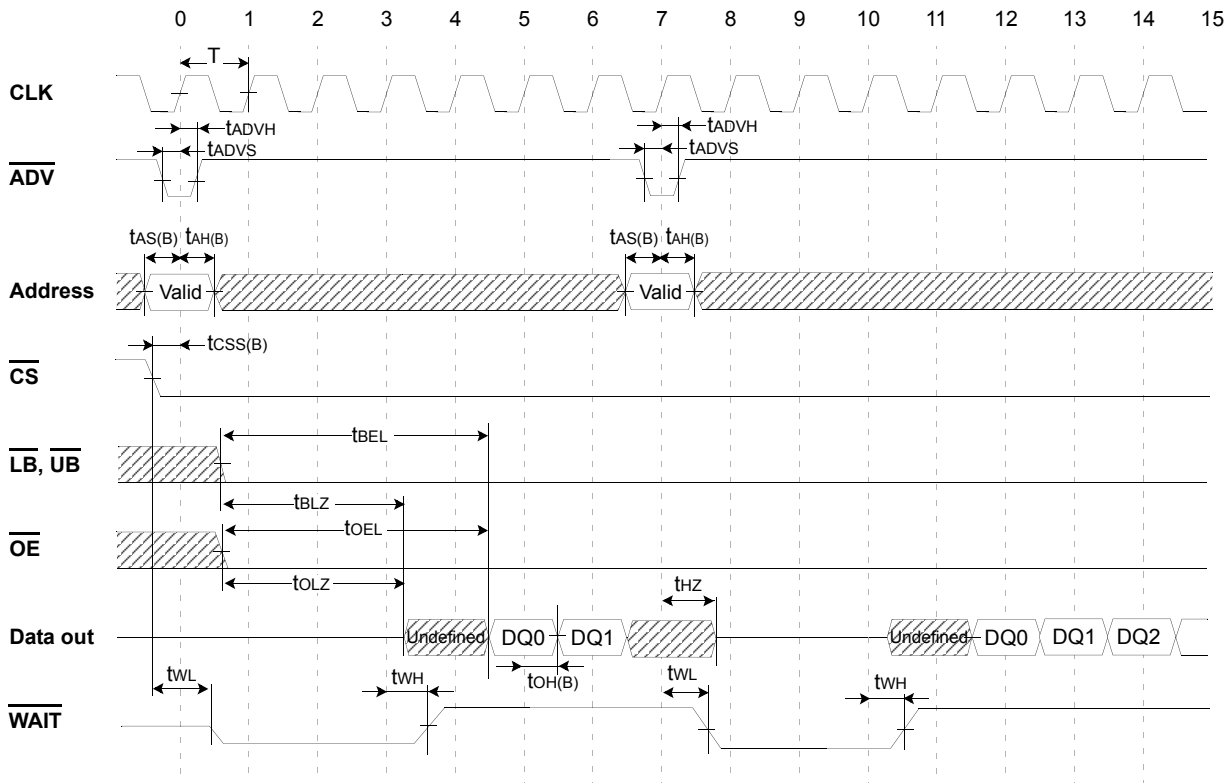
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ ( $\overline{ADV}$ Interrupt) - Fixed Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=4, Burst Length=4, WP=Low enable, WC=one clock prior to the data)



1. Refresh is blocked during  $\overline{ADV}$  Interrupt Read and continuous Burst Read by  $\overline{ADV}$  interrupt should not be longer than tBC (2.5us)
2. /WAIT Low(tWL) : Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by  $\overline{CS}$  high going edge)
3. Multiple clock risings are allowed during low  $\overline{ADV}$  period but the First valid data come out after set Latency from the last clock rising.
4. Burst interrupt is allowable after the first data received by controller.

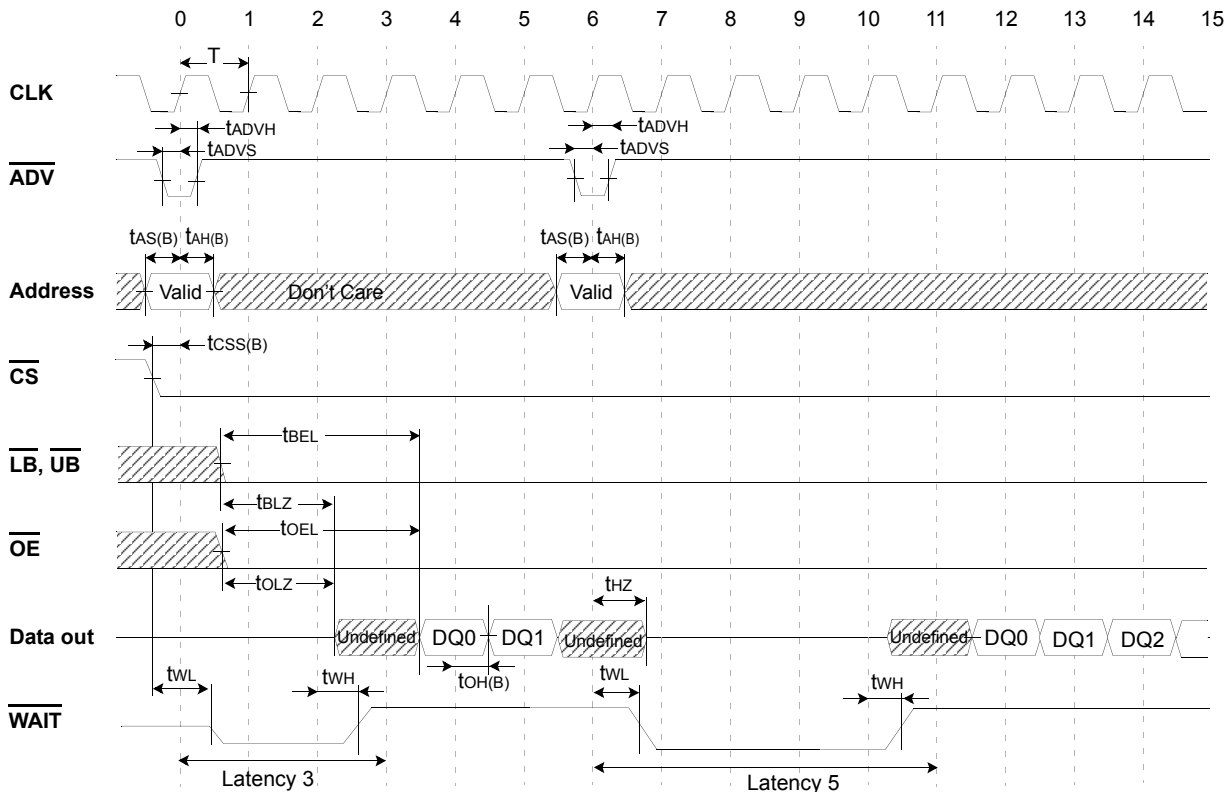
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tcSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tcSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								

# K1B3216BDE

## Burst READ ( ADV Interrupt) - Variable Latency

(PS=VIH, WE=VIH, WAIT=High-Z, Latency=3,Burst Length=4,WP=Low enable, WC=one clock prior to the data)



1. Delayed latency is taken for Burst READ by **ADV** interrupt. Refer to Latency Table.
2. Refresh is blocked during **ADV** Interrupt Read and continuous Burst Read by **ADV** interrupt should not be longer than **tBC**(2.5us)
3. **WAIT** Low(**tWL**) : Data not available(driven by **CS** low going edge or **ADV** low going edge)  
**WAIT** High(**tWH**) : Data available(driven by Latency-1 clock)  
**WAIT** High-Z(**tWZ**) : Data don't care(driven by **CS** high going edge)
4. Multiple clock risings are allowed during low **ADV** period. The data come out after set Latency from the last clock rising.
5. Burst interrupt is allowable after the first data received by controller.

## AC CHARACTERISTICS

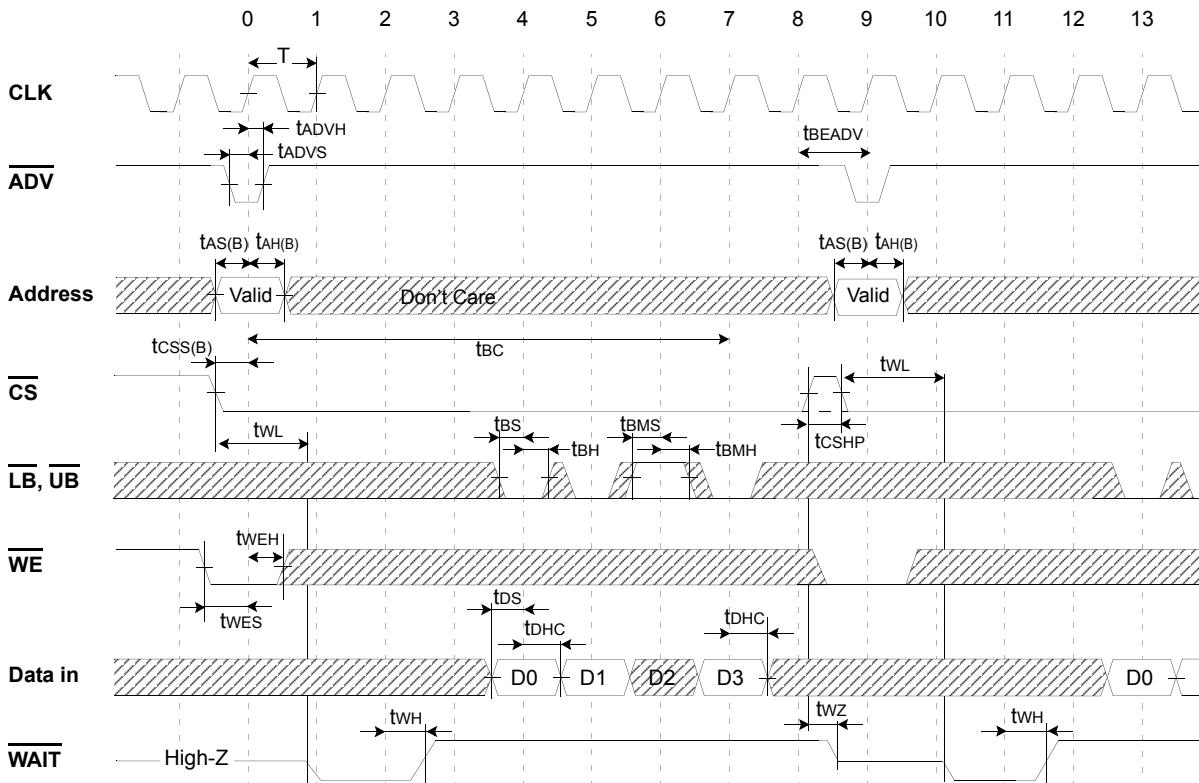
Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
T	15	200	12.5	200	9.6	200	ns	tBLZ	5	-	5	-	5	-	ns
tBC	-	2500	-	2500	-	2500	ns	tOLZ	5	-	5	-	5	-	ns
tADVS	5	-	4	-	3	-	ns	tHZ	-	10	-	10	-	10	ns
tADVH	2	-	2	-	2	-	ns	tCHZ	-	10	-	10	-	10	ns
tAS(B)	5	-	4	-	3	-	ns	tOHZ	-	10	-	10	-	10	ns
tAH(B)	2	-	2	-	2	-	ns	tBHZ	-	10	-	10	-	10	ns
tCSS(B)	5	-	4	-	3	-	ns	tCD	-	11	-	9	-	7	ns
tCSHP	5	-	5	-	5	-	ns	tOH(B)	2	-	2	-	2	-	ns
tBEL	20	-	20	-	20	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tOEL	20	-	20	-	20	-	ns	tWH	-	11	-	9	-	7	ns
tWZ	-	10	-	10	-	10	ns								



# K1B3216BDE

## Burst WRITE

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Refresh can not be implemented when  $t_{BEADV}$  is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for  $t_{BEADV}$ .
2. /WAIT Low( $t_{WL}$ ): Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High( $t_{WH}$ ): Data available(driven by Latency-1 clock)  
 /WAIT High-Z( $t_{WZ}$ ): Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than  $t_{BC}$ (2.5 $\mu$ s)

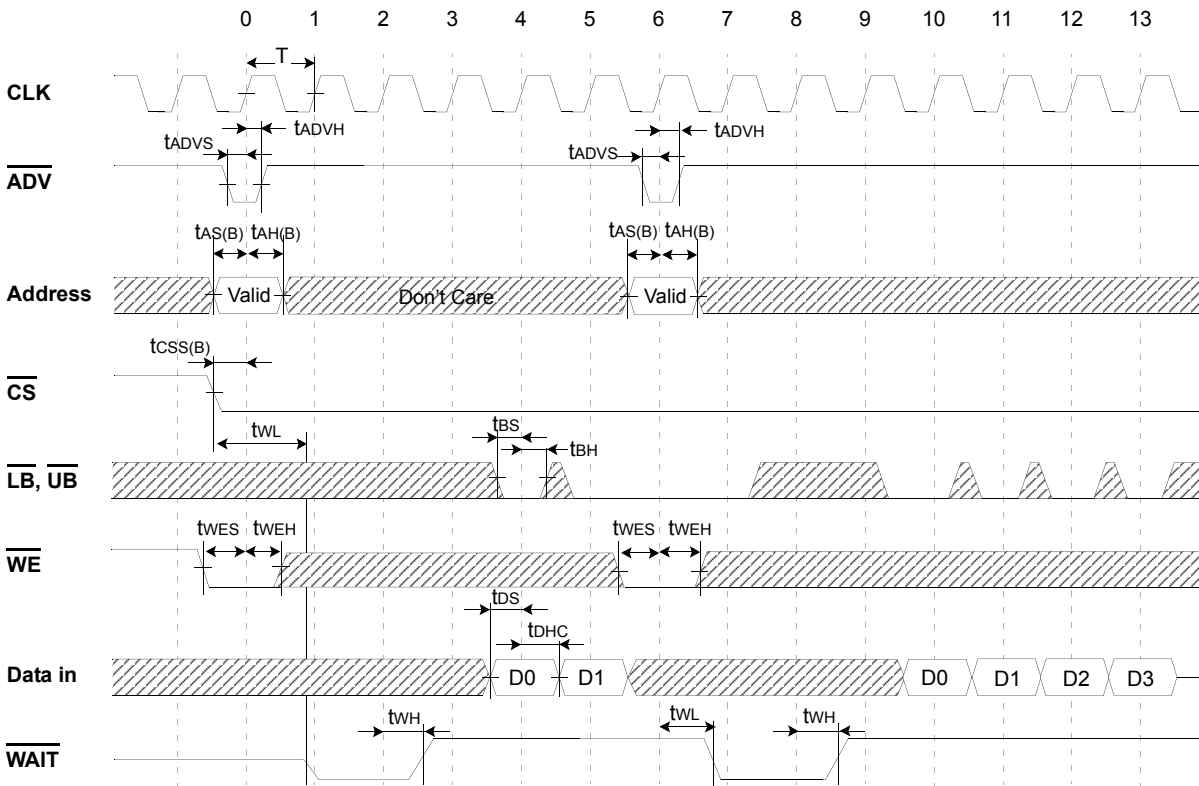
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
$t_{CSHP}$	5	-	5	-	5	-	ns	$t_{DS}$	5	-	4	-	3	-	ns
$t_{BS}$	5	-	4	-	3	-	ns	$t_{DHC}$	2	-	2	-	2	-	ns
$t_{BH}$	2	-	2	-	2	-	ns	$t_{WL}$	-	7.5	-	7.5	-	7.5	ns
$t_{BMS}$	5	-	4	-	3	-	ns	$t_{WH}$	-	11	-	9	-	7	ns
$t_{BMH}$	2	-	2	-	2	-	ns	$t_{WZ}$	-	10	-	10	-	10	ns
$t_{WES}$	5	-	4	-	3	-	ns								
$t_{WEH}$	2	-	2	-	2	-	ns								

# K1B3216BDE

## Burst WRITE (ADV PULSE Interrupt)

(PS=VIH, OE=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



- Multiple clock risings are allowed during low  $\overline{ADV}$  period. The data starts after set Latency from the last clock rising.
- $\overline{WAIT}$  Low( $t_{WL}$ ): Data not available(driven by  $\overline{CS}$  low going edge or  $\overline{ADV}$  low going edge)  
 $\overline{WAIT}$  High( $t_{WH}$ ): Data available(driven by Latency-1 clock)  
 $\overline{WAIT}$  High-Z( $t_{WZ}$ ): Data don't care(driven by  $\overline{CS}$  high going edge)
- Burst interrupt is allowable after the first data word written.

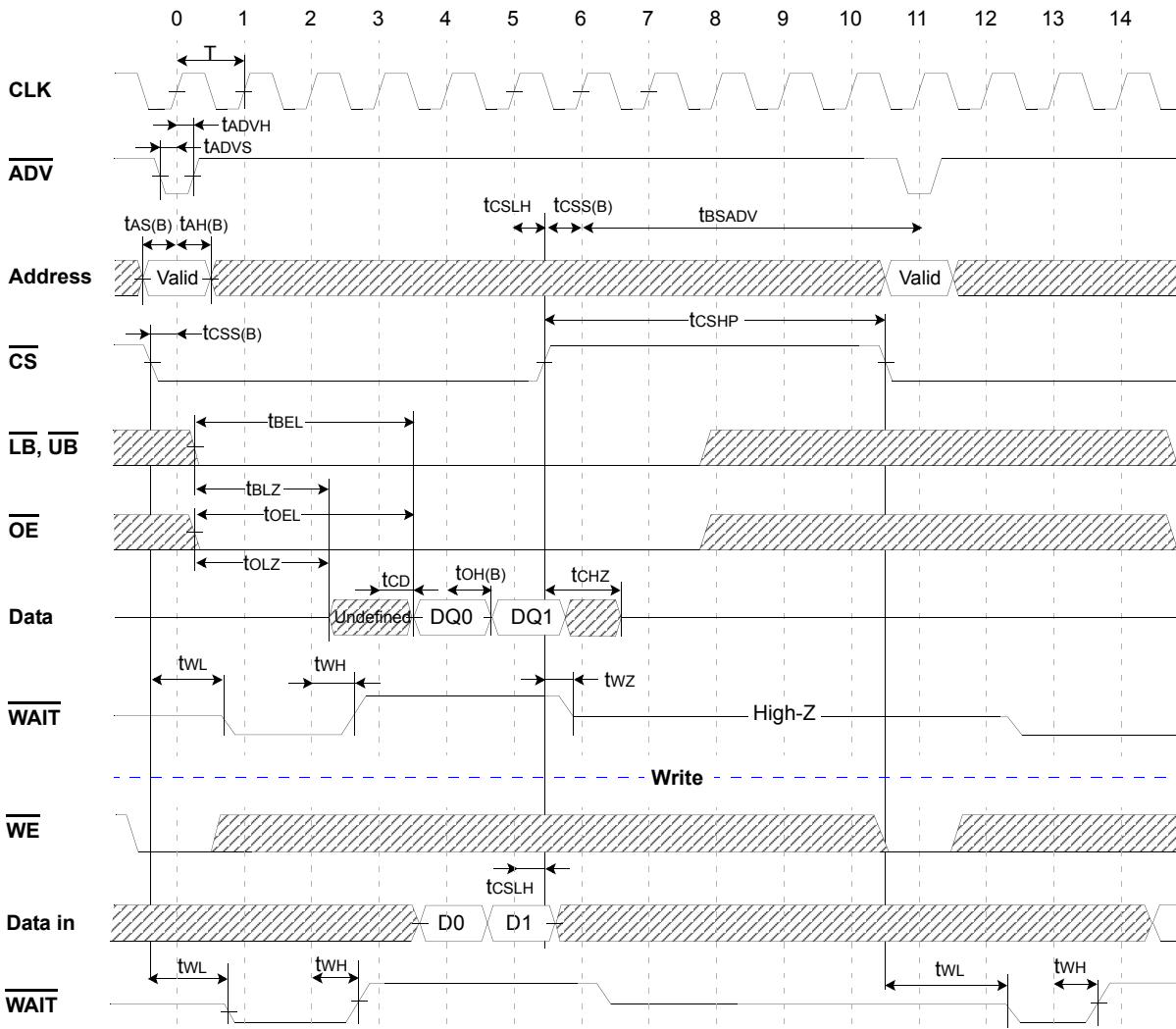
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
$t_{CSHP}$	5	-	5	-	5	-	ns	$t_{DS}$	5	-	4	-	3	-	ns
$t_{BS}$	5	-	4	-	3	-	ns	$t_{DHC}$	2	-	2	-	2	-	ns
$t_{BH}$	2	-	2	-	2	-	ns	$t_{WL}$	-	7.5	-	7.5	-	7.5	ns
$t_{BMS}$	5	-	4	-	3	-	ns	$t_{WH}$	-	11	-	9	-	7	ns
$t_{BMH}$	2	-	2	-	2	-	ns	$t_{WZ}$	-	10	-	10	-	10	ns
$t_{WES}$	5	-	4	-	3	-	ns								
$t_{WEH}$	2	-	2	-	2	-	ns								

# K1B3216BDE

## Burst READ STOP & Burst WRITE STOP

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(twz) : Data don't care(driven by CS high going edge)

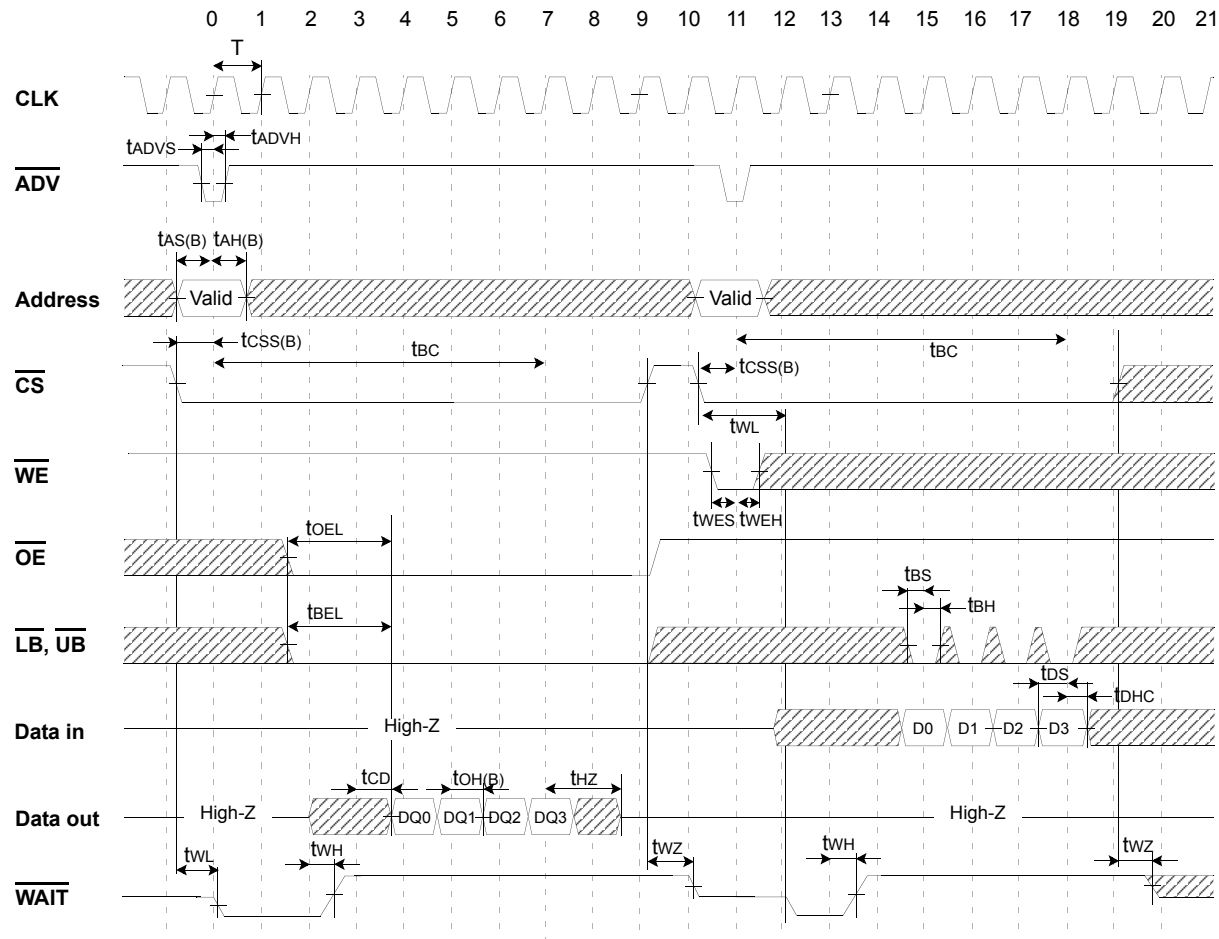
## AC CHARACTERISTICS

Symbol	66MHz		80MHz		104MHz		Units	Symbol	66MHz		80MHz		104MHz		Units
	Min	Max	Min	Max	Min	Max			Min	Max	Min	Max	Min	Max	
tCSHP	5	-	5	-	5	-	ns	tDS	5	-	4	-	3	-	ns
tBS	5	-	4	-	3	-	ns	tDHC	2	-	2	-	2	-	ns
tBH	2	-	2	-	2	-	ns	tWL	-	7.5	-	7.5	-	7.5	ns
tBMS	5	-	4	-	3	-	ns	tWH	-	11	-	9	-	7	ns
tBMH	2	-	2	-	2	-	ns	twz	-	10	-	10	-	10	ns
twES	5	-	4	-	3	-	ns	tBSADV	-	0	-	0	-	0	ns
tWEH	2	-	2	-	2	-	ns	tOH(B)	2	-	2	-	2	-	ns

**K1B3216BDE**

**Burst READ followed by Burst WRITE**

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)

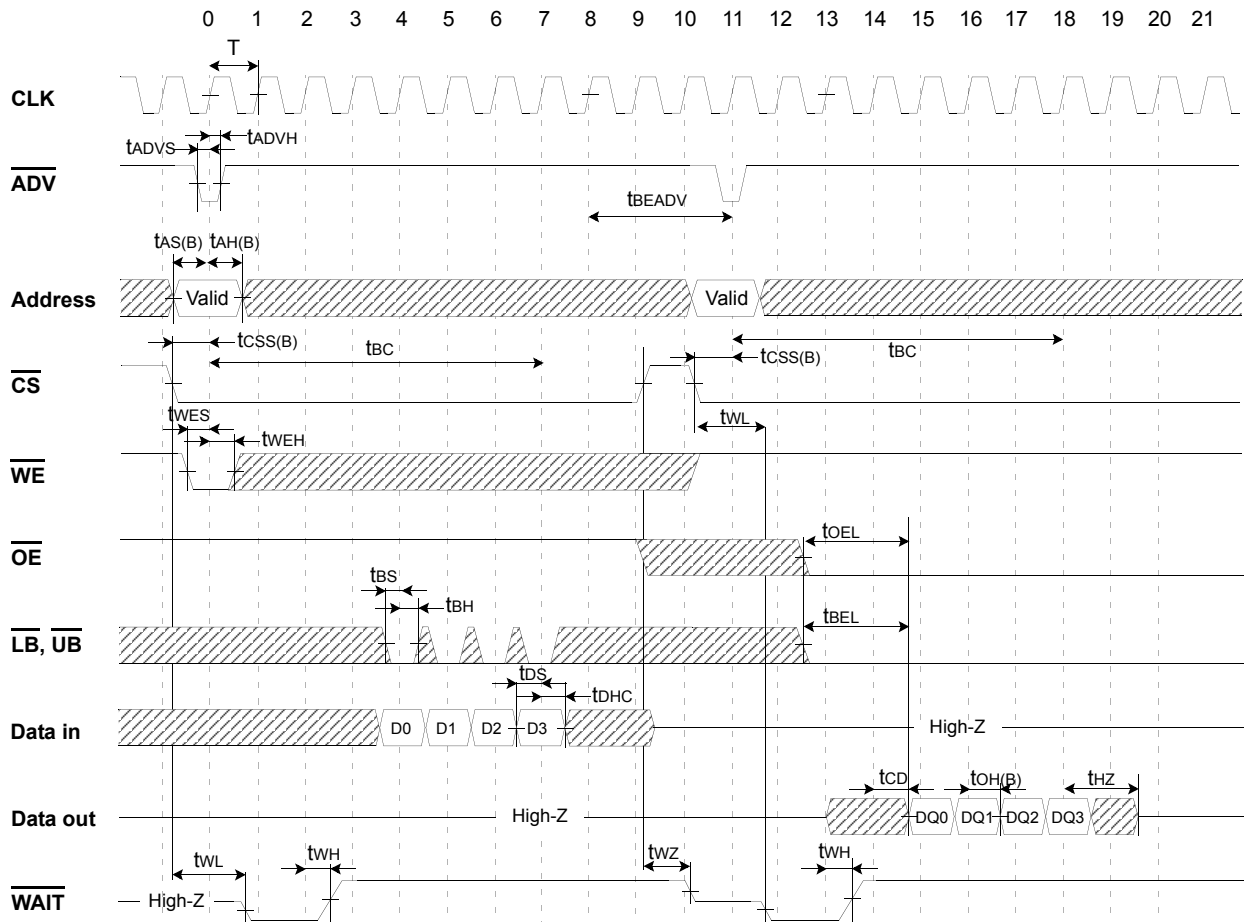


1. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
2. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
3. Burst operation should not be longer than tBC(2.5μs)

**K1B3216BDE**

**Burst WRITE followed by Burst READ**

(PS=VIH, Variable Latency=3, Burst Length=4, WP=Low Enable, WC=one clock prior to the data)



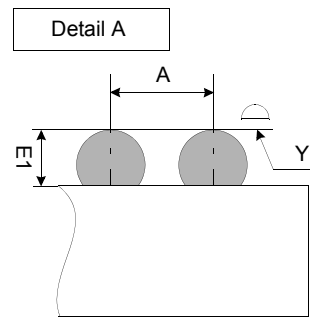
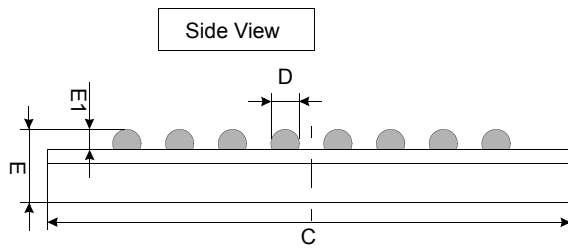
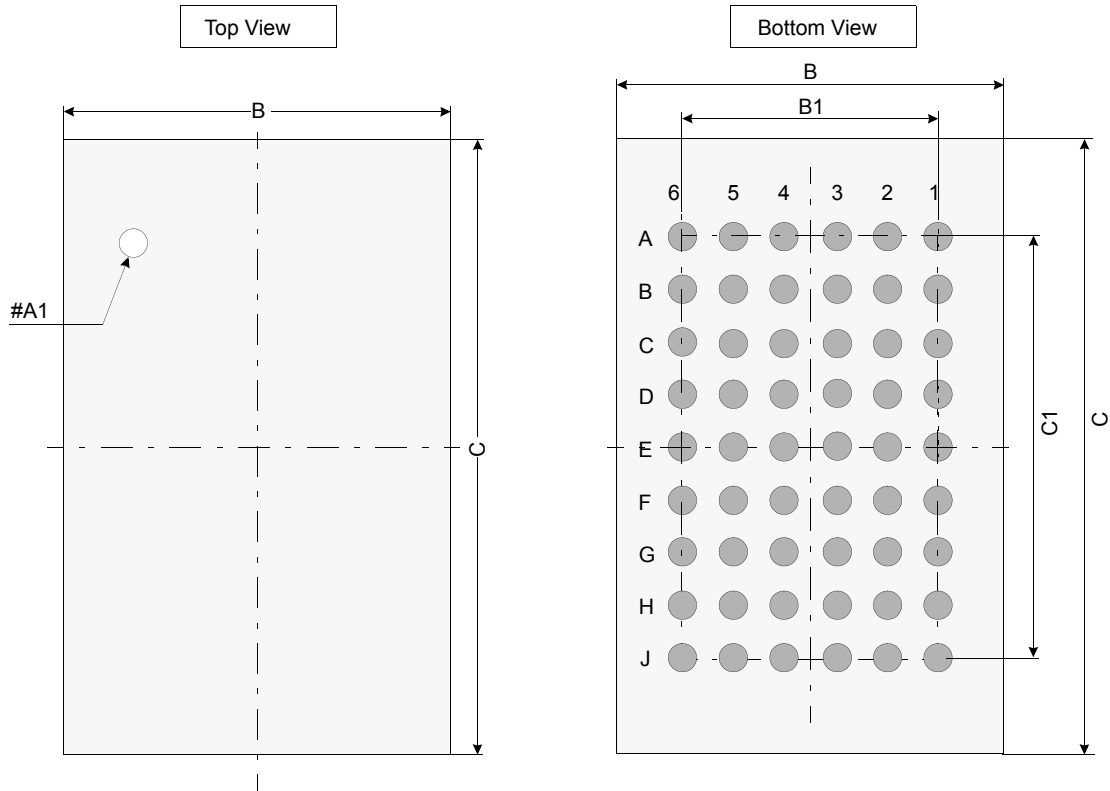
1. Refresh can not be implemented when tBEADV is in the range of 0ns ~ 13ns. It may cause Refresh fail to use the device under that condition over 2.5us without CS toggling. To avoid Refresh fail, 13ns for all frequency is needed for tBEADV.
2. /WAIT Low(tWL) : Data not available(driven by CS low going edge or ADV low going edge)  
 /WAIT High(tWH) : Data available(driven by Latency-1 clock)  
 /WAIT High-Z(tWZ) : Data don't care(driven by CS high going edge)
3. Multiple clock risings are allowed during low ADV period. The data starts after set Latency from the last clock rising.
4. Burst operation should not be longer than (tBC)2.5μs.

# K1B3216BDE

## PACKAGE DIMENSION

54 BALL FINE PITCH BGA(0.75mm ball pitch)

Unit: millimeters



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	6.00	-
D	0.40	0.45	0.50
E	-	-	1.00
E1	0.25	-	-
Y	-	-	0.10

**Notes.**

1. Ball counts: 54(9 row x 6 column)
2. Ball pitch: (x,y)=(0.75 x 0.75)(typ.)
3. All tolerance are  $\pm 0.050$  unless specified beside figure.
4. Typ: Typical
5. Y is coplanarity