Document Title

1Mx16 bit Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design target	May 30, 2002	Advance

1M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 1M x16 bit
- Power Supply Voltage: 1.7V~2.2V
- Three State Outputs
- Compatible with Low Power SRAM
- Deep Power Down: Memory cell data holds invalid
- Package Type: 48-TBGA

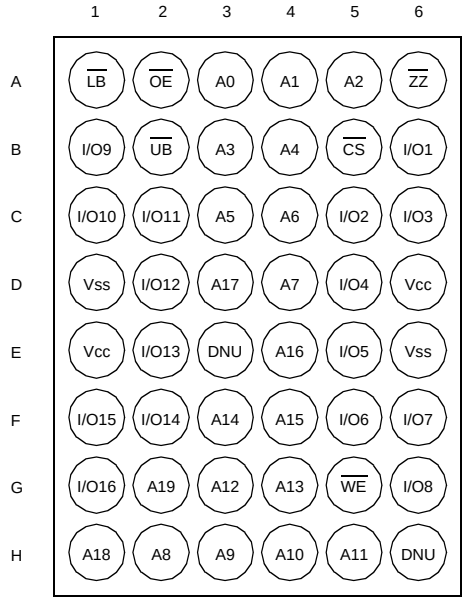
GENERAL DESCRIPTION

The K1S1616B5M is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports extended temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports deep power down mode for low standby current.

PRODUCT FAMILY

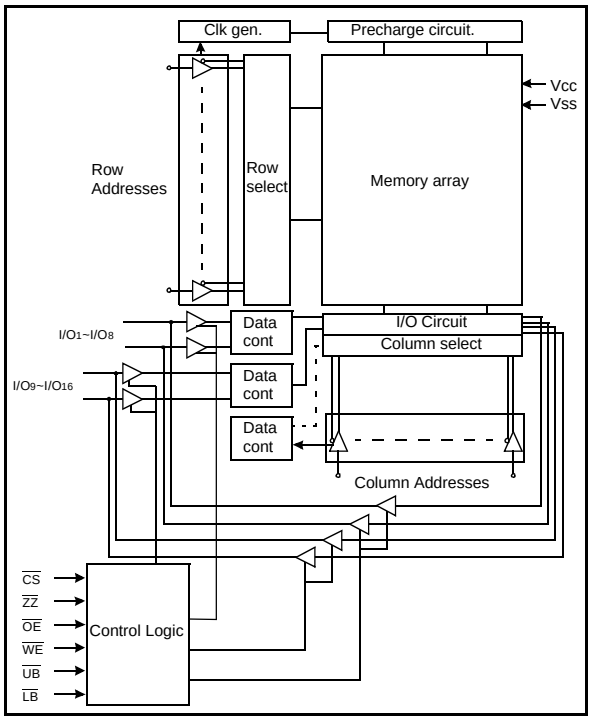
Product Family	Operating Temp.	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)	
K1S1616B5M-E	Extended(-25~85°C)	1.7V~2.2V	70/85ns	60µA	25mA	48-TBGA

PIN DESCRIPTION



48-TBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{ZZ}$	Deep Power Down	Vss	Ground
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{WE}$	Write Enable Input	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
A_0~A_{19}	Address Inputs	DNU	Do Not Use[1)]
I/O_1~I/O_{16}	Data Inputs/Outputs		

1) Reserved for future use.

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=1.7V) for a minimum 200μs with $\overline{CS}$=high.
3. Issue read operation at least twice.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	H	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

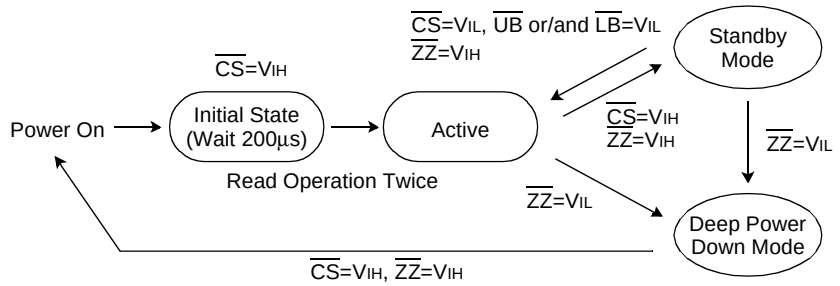
1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-25 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

Power Mode	Memory Cell Data	Standby Current(μA)	Wait Time(μs)
Standby	Valid	60	0
Deep Power Down	Invaild	10	200

PRODUCT LIST

Extended Temperature Products(-25~85°C)	
Part Name	**Function**
K1S1616B5M-EE70 K1S1616B5M-EE85	48-TBGA, 70ns 48-TBGA, 85ns

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	1.7V	1.8V	2.2V	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	1.4	-	V_{CC}+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

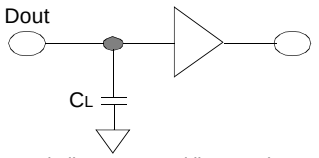
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	5	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}	-	-	25	mA
Output low voltage	V_{OL}	I_{OL} = 0.1mA	-	-	0.2	V
Output high voltage	V_{OH}	I_{OH} = -0.1mA	1.4	-	-	V
Standby Current(CMOS)	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, Other inputs=0~Vcc	-	-	60[1)]	µA

1. This value is valid over the entire operating temperature range.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2 to Vcc-0.2V
Input rising and falling time: 5ns
Input and output reference voltage: 0.5 x V_{CC}
Output load (See right): C_L=50pF



1. Including scope and jig capacitance

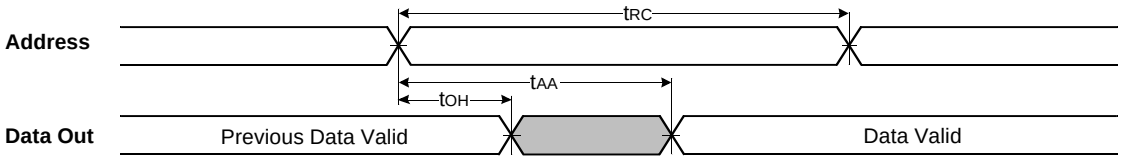
AC CHARACTERISTICS(V_{CC}=1.7~2.2V, T_A=-25 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			70ns[1)]		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	85	-	ns
	Address Access Time	t_{AA}	-	70	-	85	ns
	Chip Select to Output	t_{CO}	-	70	-	85	ns
	Output Enable to Valid Output	t_{OE}	-	35	-	40	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	-	85	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	70	-	85	-	ns
	Chip Select to End of Write	t_{CW}	60	-	70	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	70	-	ns
	Write Pulse Width	t_{WP}	50	-	60	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	20	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

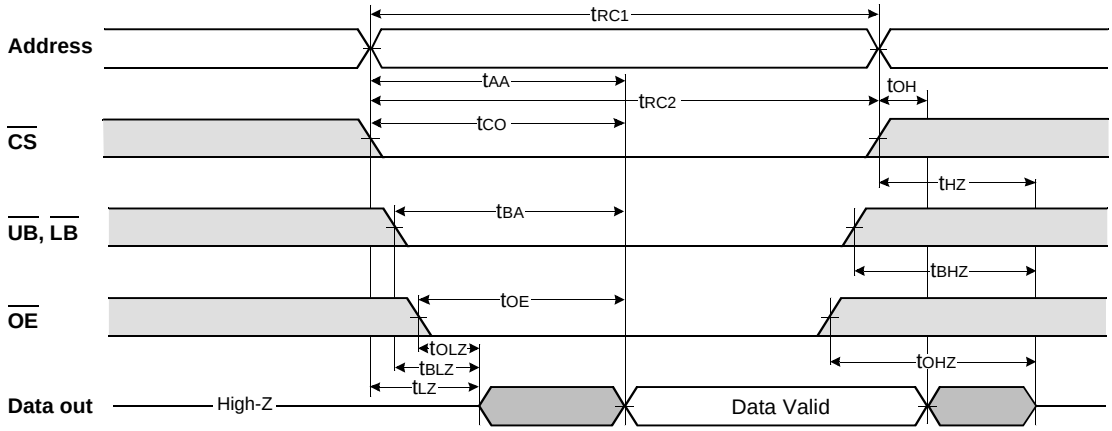
1. The limitation in continuous write operation is up to 50 times. If you want to write continuously over 50 times, please refer to the technical note.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



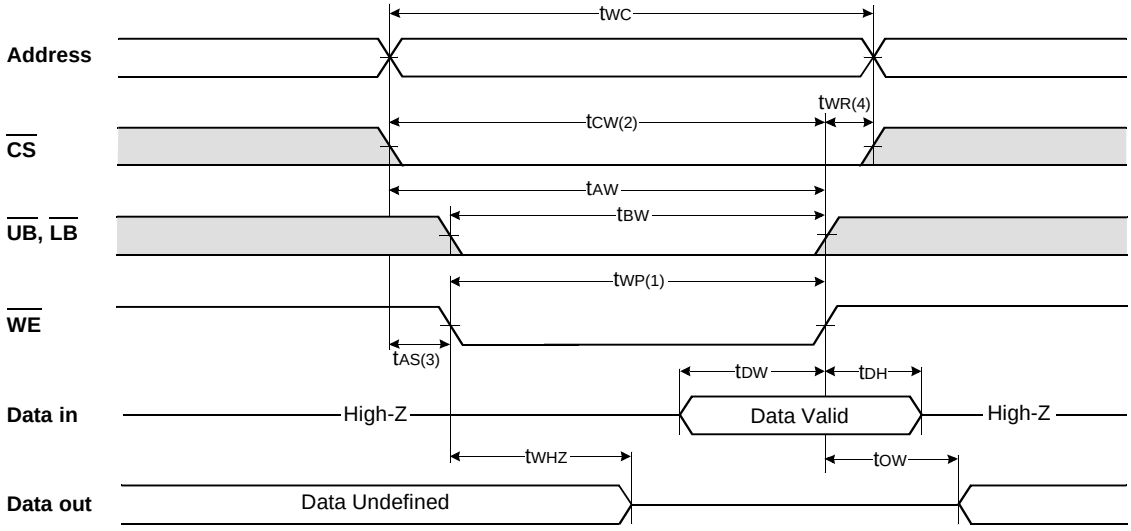
TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})



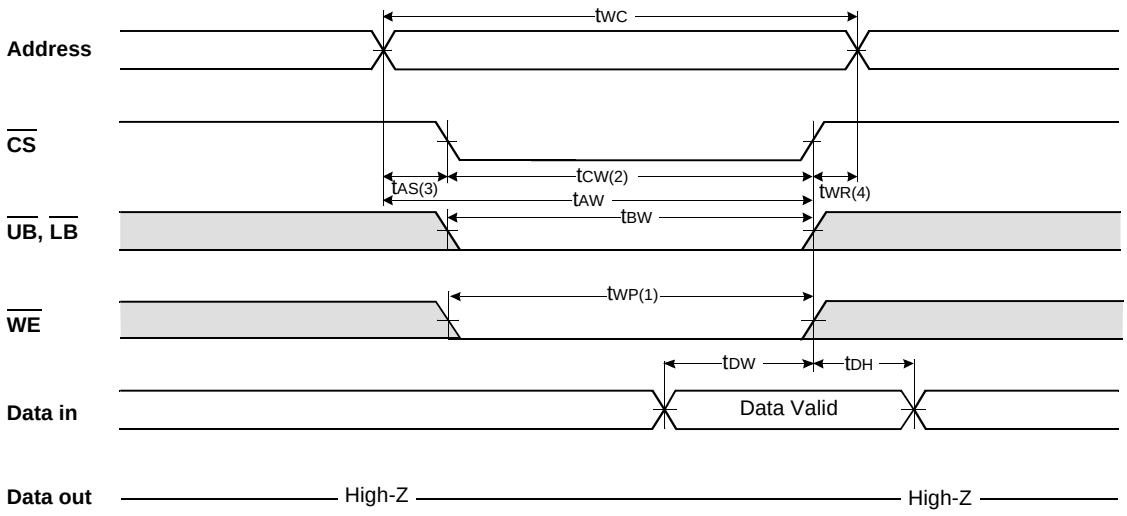
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. The minimum read cycle(t_{RC}) is determined by longer one of t_{RC1} and t_{RC2}.
4. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).

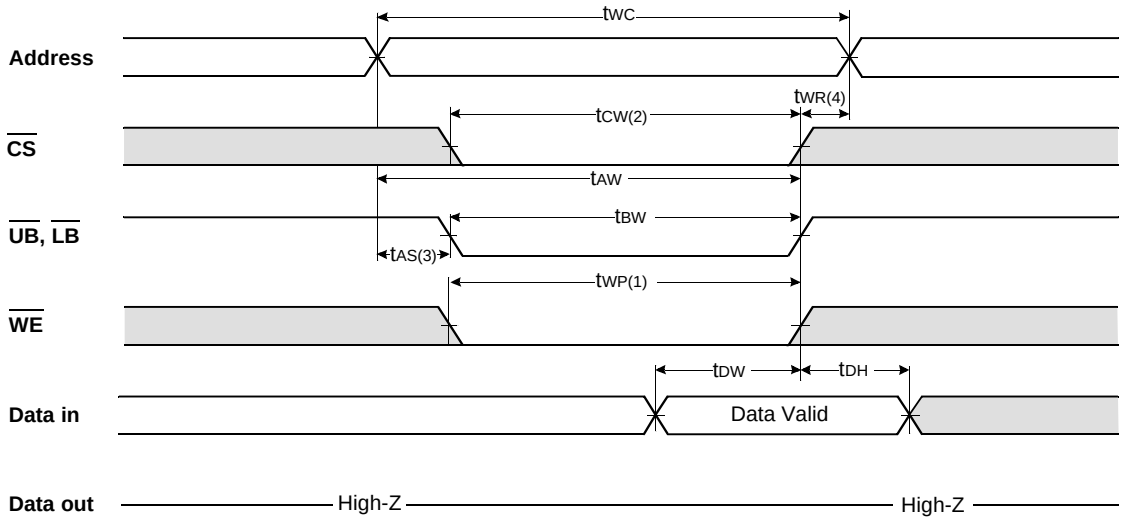
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{ZZ}$=V_{IH})



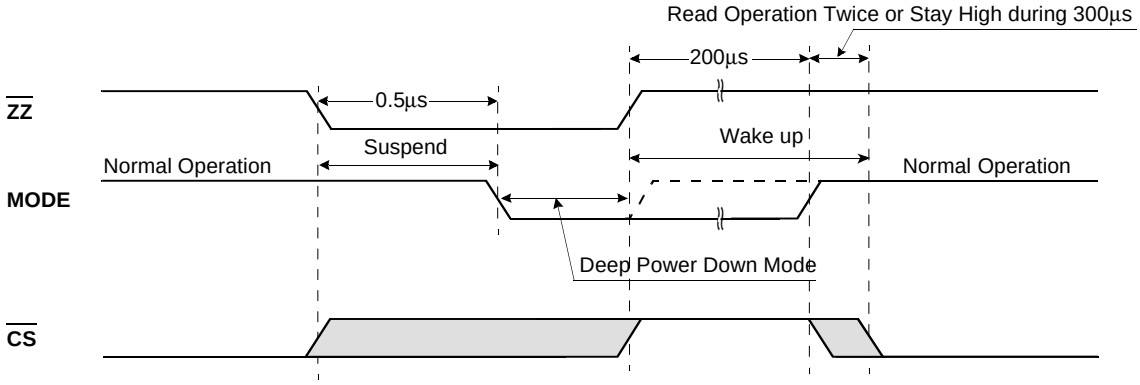
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

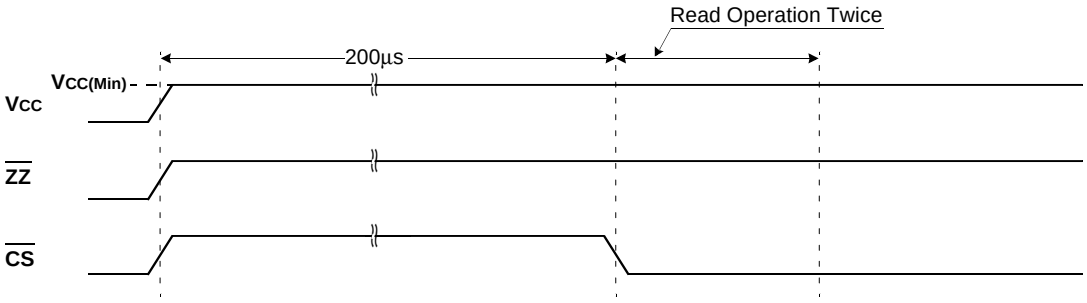
TIMING WAVEFORM OF DEEP POWER DOWN MODE



(DEEP POWER DOWN MODE)

1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence shown in next page.

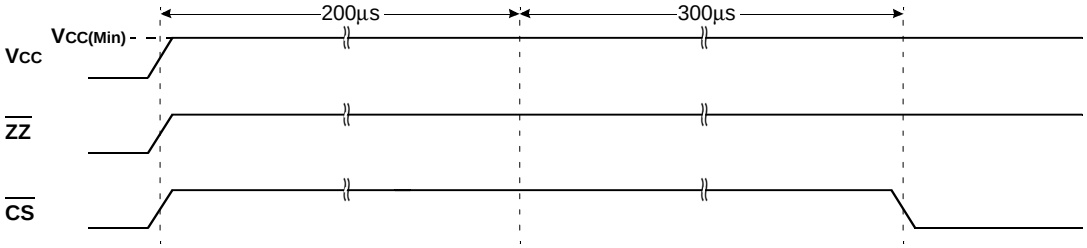
TIMING WAVEFORM OF POWER UP(1)



(POWER UP(1))

1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs with $\overline{CS}$ high and then toggle $\overline{CS}$ low and commit Read Operation at least twice. Then you get into the normal operation.
2. Read operation should be executed by toggling CS pin low.
3. The read operation must satisfy the specified t_{RC}.
4. $\overline{ZZ}$ pin should be kept high during whole power up sequence.

TIMING WAVEFORM OF POWER UP(2)(No Dummy Cycle)



(POWER UP(2))

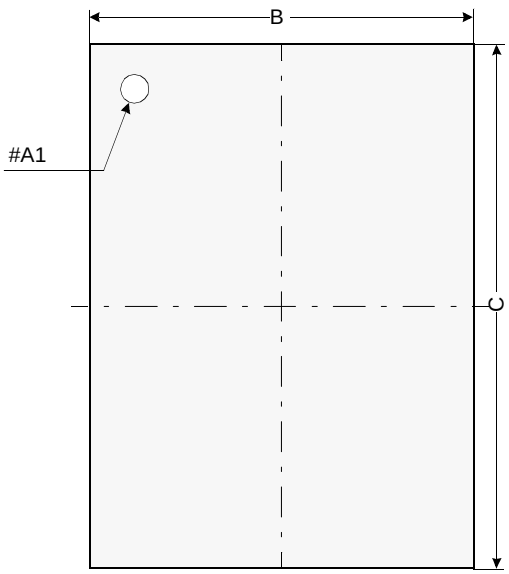
1. After V_{CC} reaches V_{CC}(Min.) following power application, wait 200µs and wait another 300µs with $\overline{CS}$ high if you don't want to commit dummy read cycle. After total 500µs wait, toggle CS low, then you get into the normal mode.
2. $\overline{ZZ}$ pin should be kept high during whole power up sequence.

PACKAGE DIMENSION

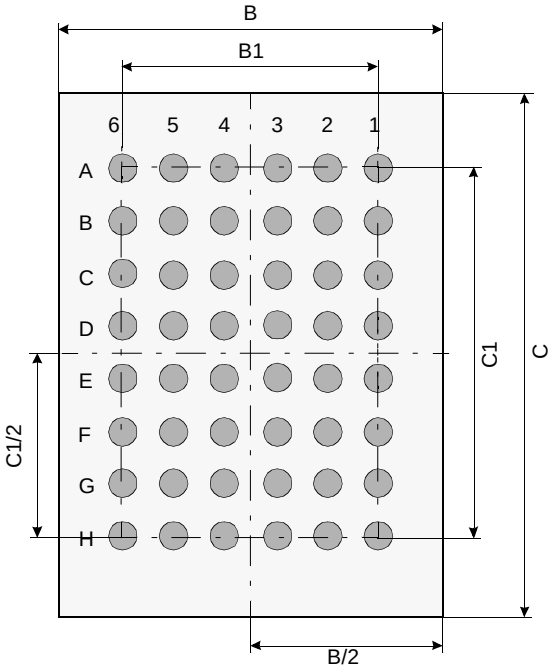
Unit: millimeters

48 TAPE BALL GRID ARRAY(0.75mm ball pitch)

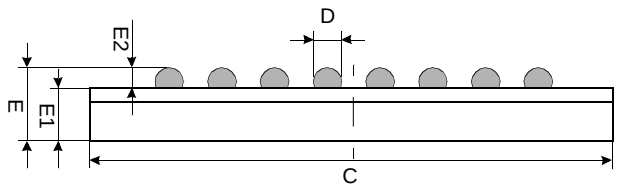
Top View



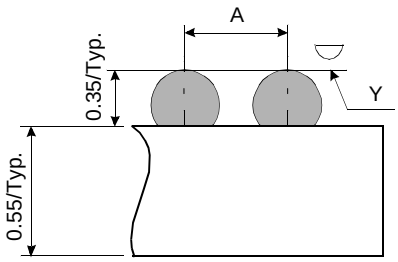
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B		TBD	
B1	-	3.75	-
C		TBD	
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)

TECHNICAL NOTE

UtRAM USAGE AND TIMING

INTRODUCTION

UtRAM is based on single-transistor DRAM cells. As with any other DRAM, the data in these cells must be periodically refreshed to prevent data loss. What makes the UtRAM unique is that it offers a true SRAM style interface that hides all refresh operations from the memory controller.

START WITH A DRAM TECHNOLOGY

The key point of UtRAM is its high speed and low power. This high speed comes from the use of many small blocks such as 32Kbits each to create UtRAM arrays. The small blocks have short word lines thus with little capacitance eliminating a major factor of operating current dissipation in conventional DRAM blocks.

Each independent macro-cell on a UtRAM device consists of a number of these blocks. Each chip has one or more macro.

The address decoding logic is also fast. UtRAM performs a complete read operation in every tRC, but UtRAM needs power up sequence like DRAM.

Power Up Sequence and Diagram
1. Apply power.
2. Maintain stable power for a minium 200µs with $\overline{CS}$=high.
3. Issue read operation at least 2 times.

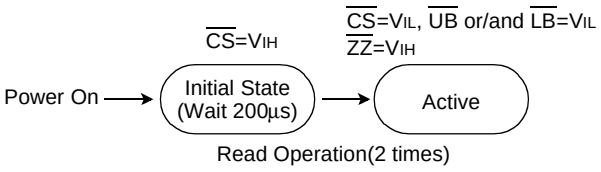


Figure 1.

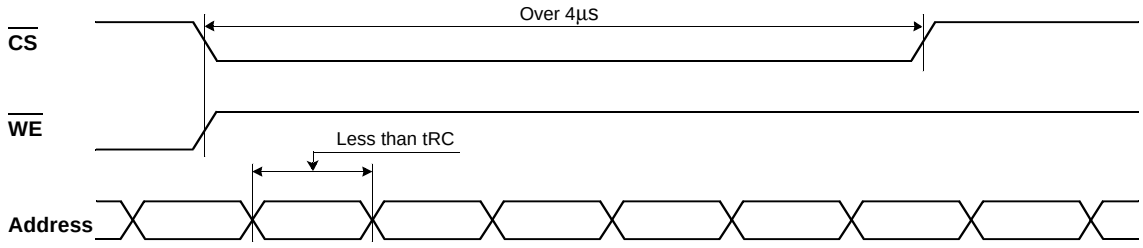
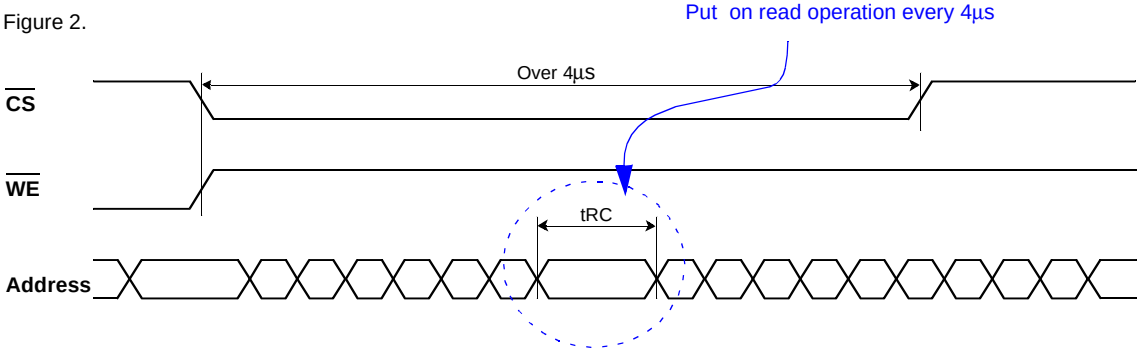


Figure 2.



DESIGN ACHIEVES SRAM SPECIFIC OPERATIONS

The UtRAM was designed to work just like an SRAM - without any waits or other overhead for precharging or refreshing its internal DRAM cells. SAMSUNG Electronics(SAMSUNG) hides these operations inside with advanced design technology - those are not to be seen from outside. Precharging takes place during every access, overlapped between the end of the cycle and the decoding portion of the next cycle.

Hiding refresh is more difficult. Every row in every block must be refreshed at least once during the refresh interval to prevent data loss. SAMSUNG provides an internal refresh controller for devices. When all accesses within refresh interval are directed to one macro-cell, as can happen in signal processing applications, a more sophisticated approach is required to hide refresh. The pseudo SRAM is sometimes used on these applications, which requires a memory controller that can hold off accesses when a refresh operation is needed. SAMSUNG's unique qualitative advantage over these parts(in addition to quantitative improvements in access speed and power consumption) is that the UtRAM never need to hold off accesses, and indeed it has no hold off signal. The circuitry that gives SAMSUNG this advantage is fairly simple but has not previously been disclosed.

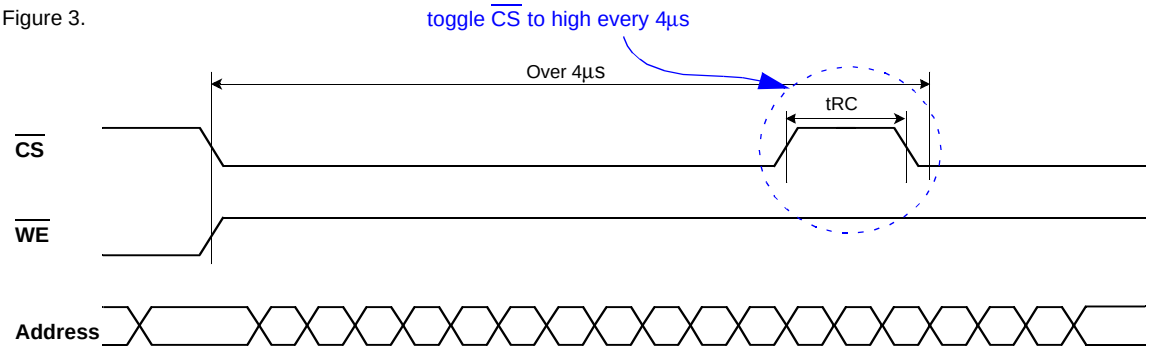
AVOID TIMING

Following figures show you an abnormal timing which is not supported on UtRAM and its solution.

If your system has a timing which sustains invalid states over 4µs at read mode like Figure 1, there are some guide lines for proper operation of UtRAM.

When your system has multiple invalid address signals shorter than tRC on the timing shown in Figure 1, UtRAM needs a normal read timing(tRC) during that cycle(Figure 2) or needs to toggle $\overline{CS}$ once to 'high' for about 'tRC'(Figure 3).

Figure 3.



Write operation has similar restriction to Read operation. If your system has a timing which sustains invalid states over 4µs at write mode and has continuous write signals with length of Min. tWC over 4µs like Figure 4, you must toggle WE once to high and make it stay high at least for tRC every 4µs or toggle CS once to high for about tRC.

Figure 4.

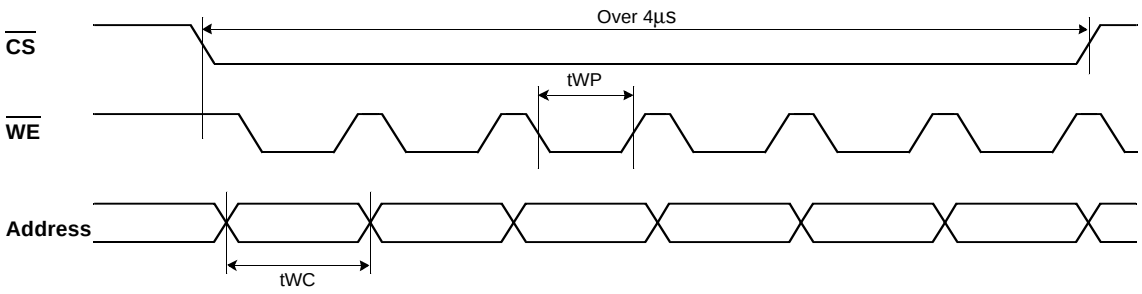


Figure 5.

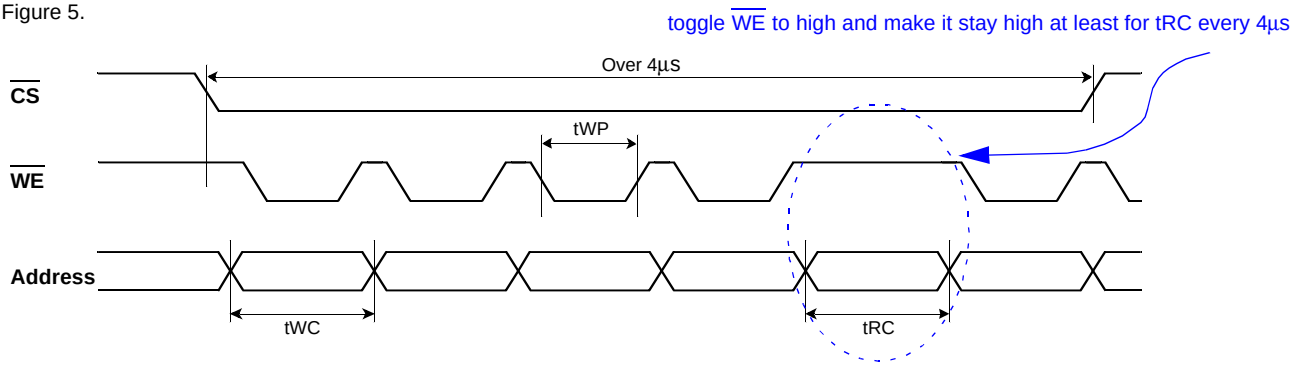


Figure 6.