128Mb (8M x 16 bit) UtRAM

Document Title

8Mx16 bit Page Mode Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial - Design target	April 13, 2006	Preliminary
1.0	Finalized - Corrected errata	July 19, 2006	Final
2.0	Revised - Corrected temperature -25℃ to -40℃ - Modified the test condition for DC parameter	October 10, 2006	Final

Table of Contents

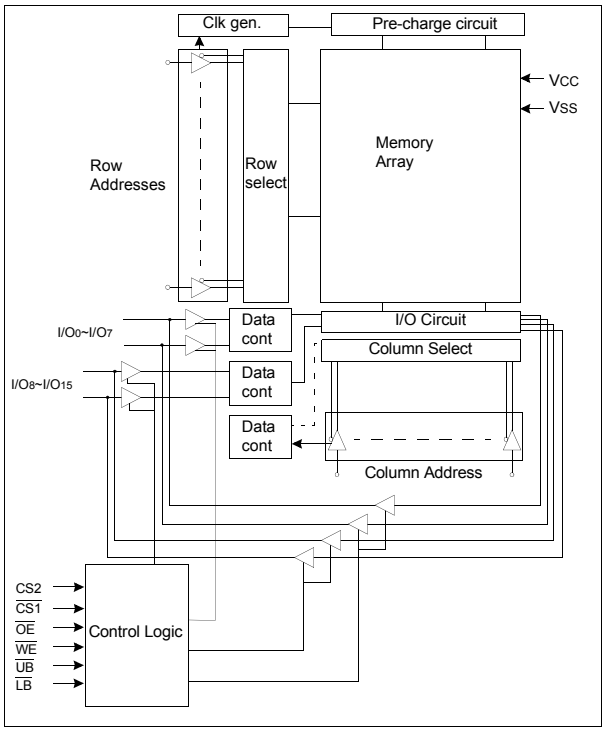
8M x 16 bit Page Mode Uni-Transistor Random Access Memory

GENERAL DESCRIPTION

The K1S28161CA is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device supports dual chip selection for user interface. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

FEATURES & FUNCTION BLOCK DIAGRAM

- Process technology: CMOS
- Organization: 8M x 16 bit
- Power supply voltage: 2.7V~3.1V
- Internal TCSR



PRODUCT FAMILY

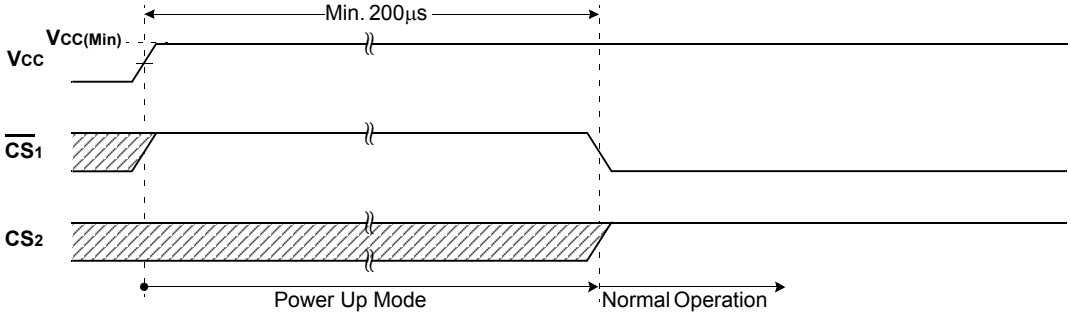
Product Family	Operating Temp.	Vcc Range	Speed (t_{RC})	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max.)	Operating (I_{CC2P}, Max.)	
K1S28161CA-I	Industrial(-40~85°C)	2.7~3.1V	70ns	280μA < 85°C 140μA < 40°C	40mA	TBD

POWER UP SEQUENCE

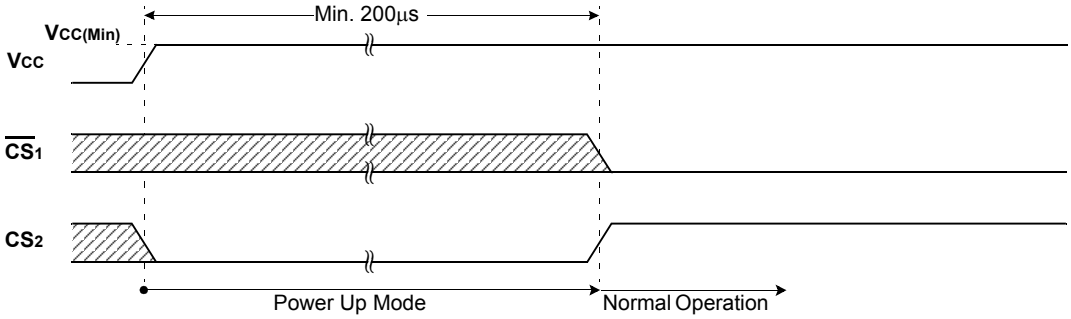
During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power(Vcc min.=2.7V) for a minimum 200μs with $\overline{CS}$1=high.or CS2=low.

TIMING WAVEFORM OF POWER UP(1) ($\overline{CS}_1$ controlled)



TIMING WAVEFORM OF POWER UP(2) (CS_2 controlled)



FUNCTIONAL DESCRIPTION

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	L	X[1]	X[1]	X[1]	X[1]	High-Z	High-Z	Deselected	Standby
X[1]	X[1]	X[1]	X[1]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1]	L	L	L	Din	Din	Word Write	Active

1. X means "Don't care". X should be low or high state.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Power supply voltage relative to Vss	V_{CC}, V_{CCQ}	-0.2 to 3.6V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V_{CC}	2.7	2.9	3.1	V
Power supply voltage(I/O)	V_{CCQ}	2.7	2.9	3.1	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	0.8 x V_{CCQ}	-	V_{CCQ}+0.2[2]	V
Input low voltage	V_{IL}	-0.2[3]	-	0.6	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CCQ} +1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CCQ}		-1	-	1	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{PS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to V_{CCQ}		-1	-	1	µA
Average Operating Current(Async)	I_{CC2}	Cycle time=70ns, I_{IO}=0mA[2], 100% duty, $\overline{CS}$=V_{IL}, CS2=V_{IH}, $\overline{UB}$ and $\overline{LB}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	40	mA
	I_{CC2P}	Cycle time=tRC+3tPC, I_{IO}=0mA[2], 100% duty, $\overline{CS}$=V_{IL}, CS2=V_{IH}, $\overline{UB}$ and $\overline{LB}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	25	mA
Output Low Voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-0.1mA		2.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1]	$\overline{CS}$≥V_{CCQ}-0.2V, $\overline{PS}$≥V_{CCQ}-0.2V, Other inputs=Vss or V_{CCQ}	< 40°C	-	-	140	µA
			< 85°C	-	-	280	µA

1. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize Refresh cycle below 40°C.
2. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

AC OPERATING CONDITIONS

TEST CONDITIONS

(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V

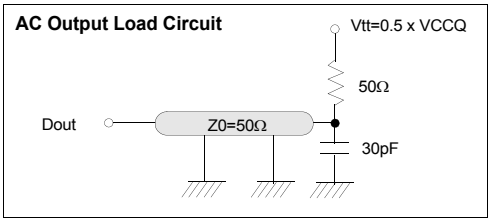
Input rising and falling time: 3ns

Input and output reference voltage: 0.5 x V_{CCQ}

Output load: C_L=30pF

V_{CC}:2.7V~3.1V

T_A: -40°C~85°C



AC CHARACTERISTICS

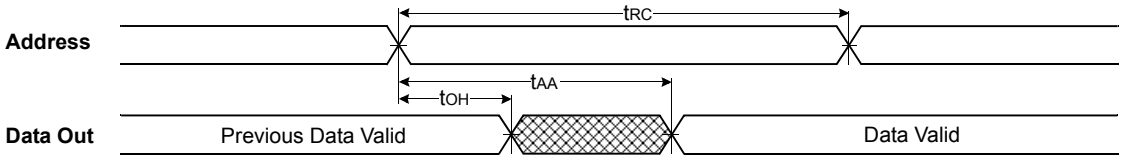
Parameter List		Symbol	Speed		Units
			Min	Max	
Common	$\overline{CS}$ High Pulse Width	$t_{CSHP(A)}$	10	-	ns
Asynch. Read	Read Cycle Time	t_{RC}	70	-	ns
	Page Read Cycle Time	t_{PC}	25	-	ns
	Address Access Time	t_{AA}	-	70	ns
	Page Access Time	t_{PA}	-	20	ns
	Chip Select to Output	t_{CO}	-	70	ns
	Output Enable to Valid Output	t_{OE}	-	35	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	ns
	Chip Select to Low-Z Output	t_{LZ}	5	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	5	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	ns
	Chip Disable to High-Z Output	t_{CHZ}	0	12	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	12	ns
	Output Disable to High-Z Output	t_{OHZ}	0	10	ns
	Output Hold	t_{OH}	5	-	ns
Asynch. Write	Write Cycle Time	t_{WC}	70	-	ns
	Chip Select to End of Write	t_{CW}	60	-	ns
	Address Set-up Time to Beginning of Write	t_{AS}	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	ns
	$\overline{WE}$ High Pulse Width	t_{WHP}	5	-	ns
	Write Recovery Time	t_{WR}	0	-	ns
	Data to Write Time Overlap	t_{DW}	30	-	ns
	Data Hold from Write Time	t_{DH}	0	-	ns

1. t_{WP}(min)=70ns for continuous write without $\overline{CS}$ toggling longer than 1.7us
2. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ} x 0.5
3. The Low-Z timings measure a 100mV transition away from the High-Z level toward either V_{OH} or V_{OL}.

TIMING WAVEFORMS

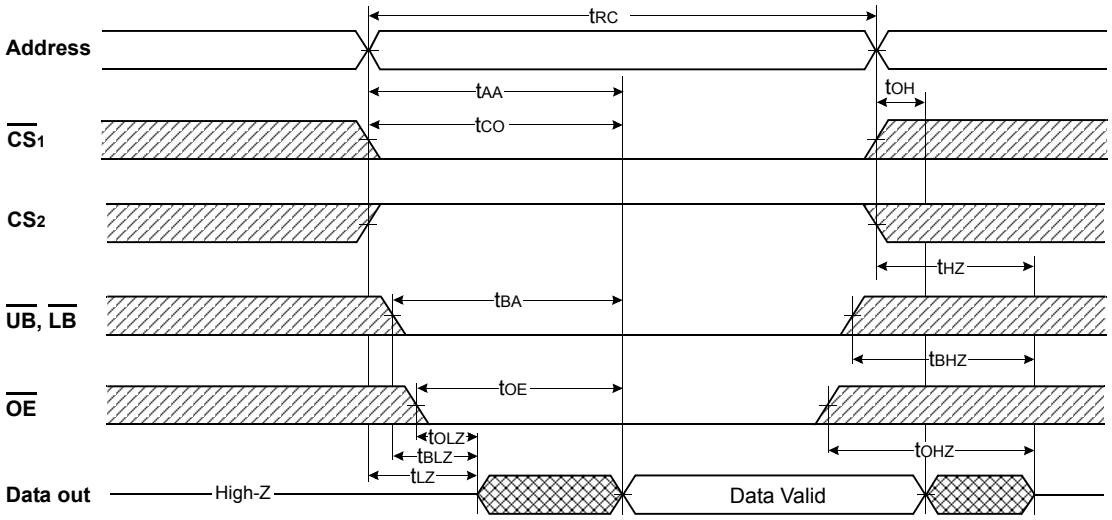
TIMING WAVEFORM OF READ CYCLE(1)

(Address Controlled, $\overline{CS1}$=$\overline{OE}$=V_{IL}, CS2=$\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})

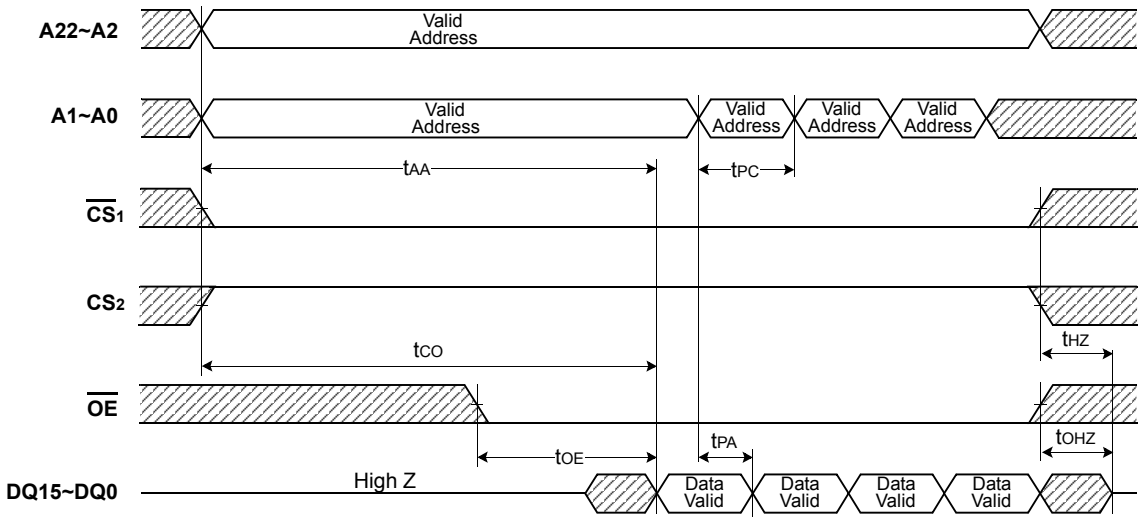


TIMING WAVEFORM OF READ CYCLE(2)

($\overline{WE}$=V_{IH})



TIMING WAVEFORM OF PAGE CYCLE (READ ONLY)

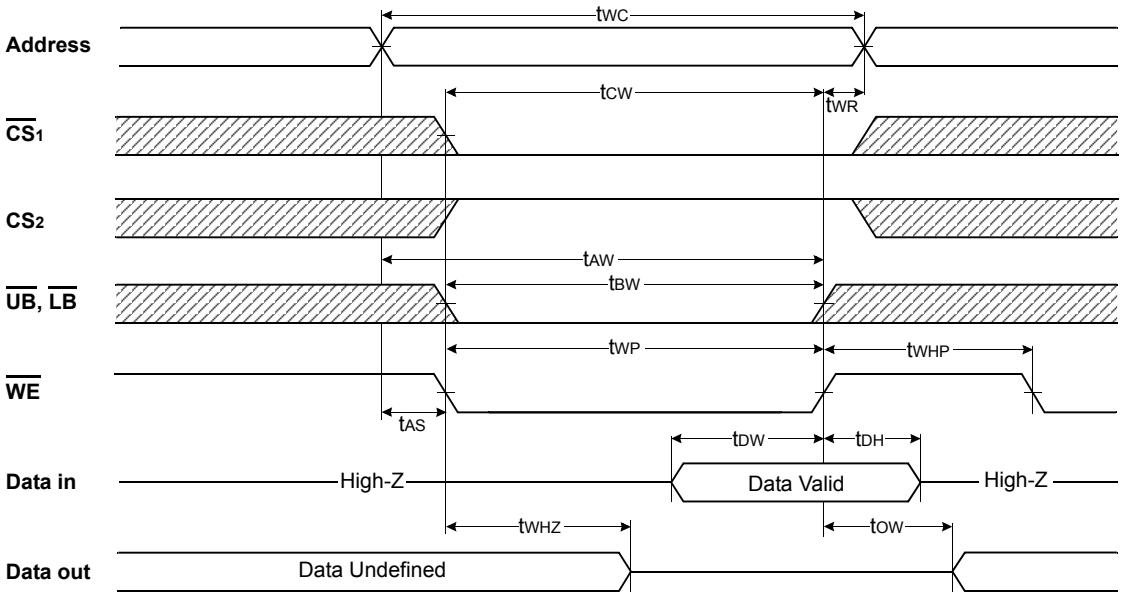


(READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.
3. tOE(max) is met only when $\overline{OE}$ becomes enabled after tAA(max).
4. If invalid address signals shorter than min. tRC are continuously repeated for over 1.7us, the device needs a normal read timing(tRC) or needs to sustain standby state for min. tRC at least once in every 1.7us.

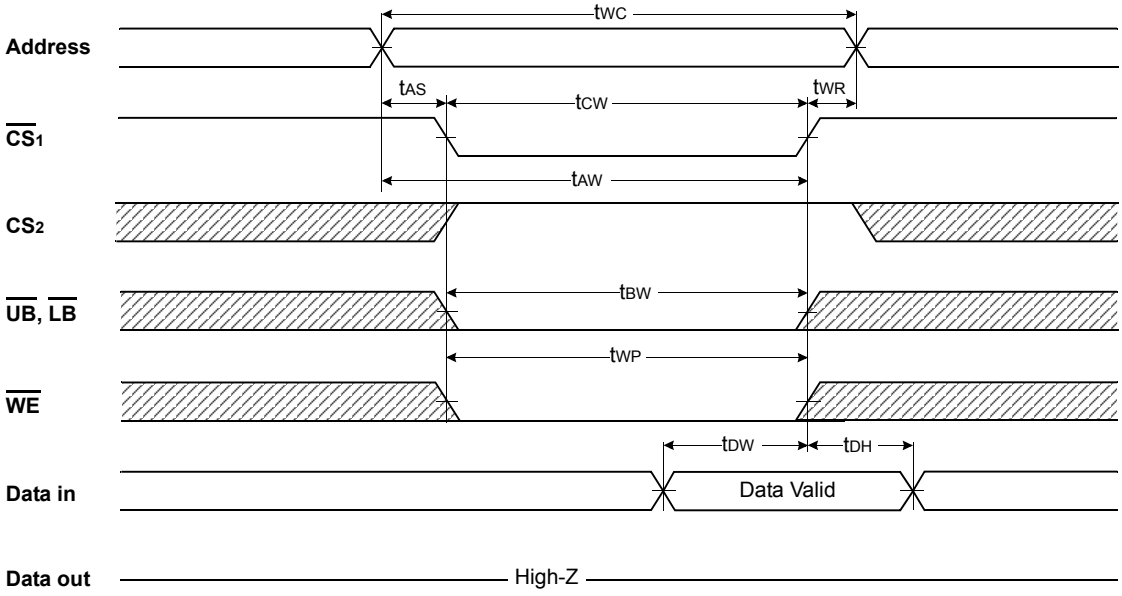
TIMING WAVEFORM OF WRITE CYCLE(1)

($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)

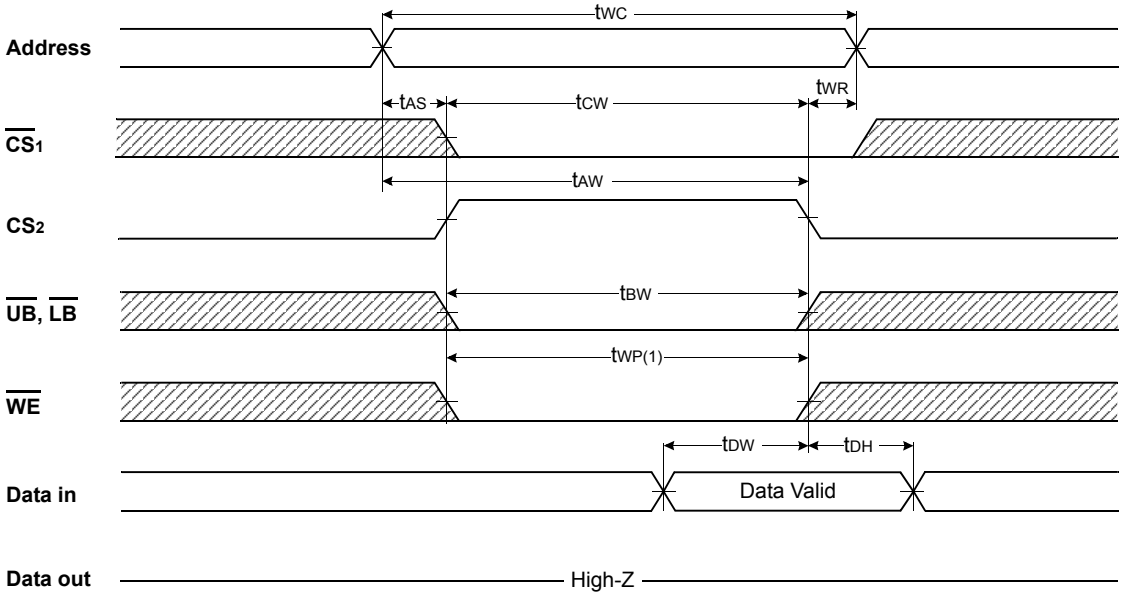
($\overline{CS_1}$ Controlled)



1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.
5. In asynchronous write cycle, Clock and $\overline{ADV}$ signals are ignored.
6. Condition for continuous write operation over 50 times : t_{WP}(min)=70ns

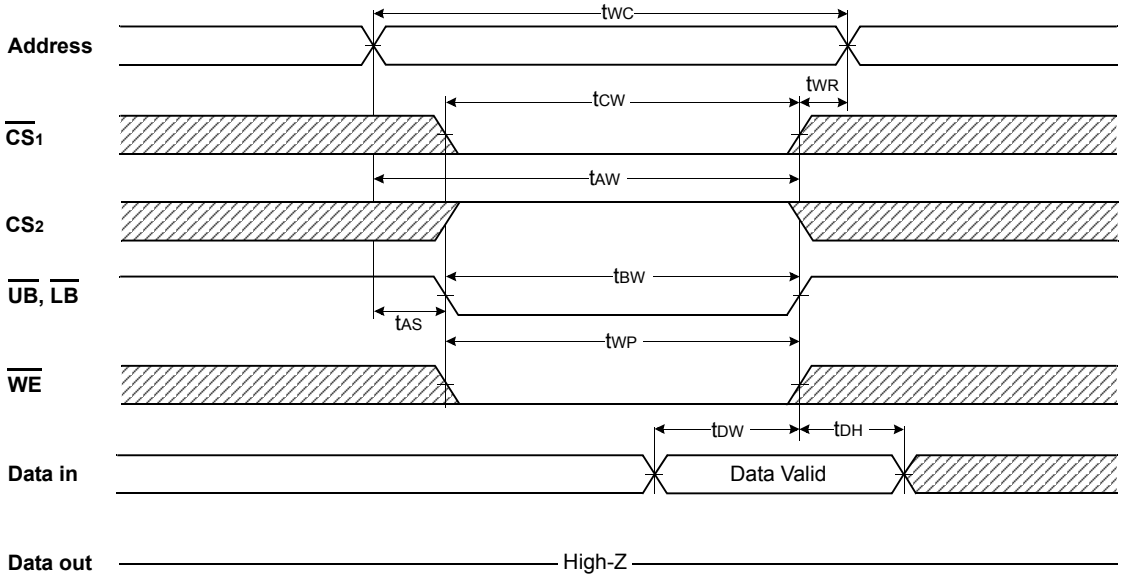
TIMING WAVEFORM OF WRITE CYCLE(3)

(CS2 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4)

(UB, LB Controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}_1$ and low $\overline{WE}$. A write begins when $\overline{CS}_1$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}_1$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}_1$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}_1$ or $\overline{WE}$ going high.