

256Mb (16M x 16 bit) UtRAM

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Document Title

16Mx16 bit Page Mode Uni-Transistor Random Access Memory

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial - Design Target	Jan. 24, 2008	Preliminary
1.0	finalized	Mar. 31, 2008	final

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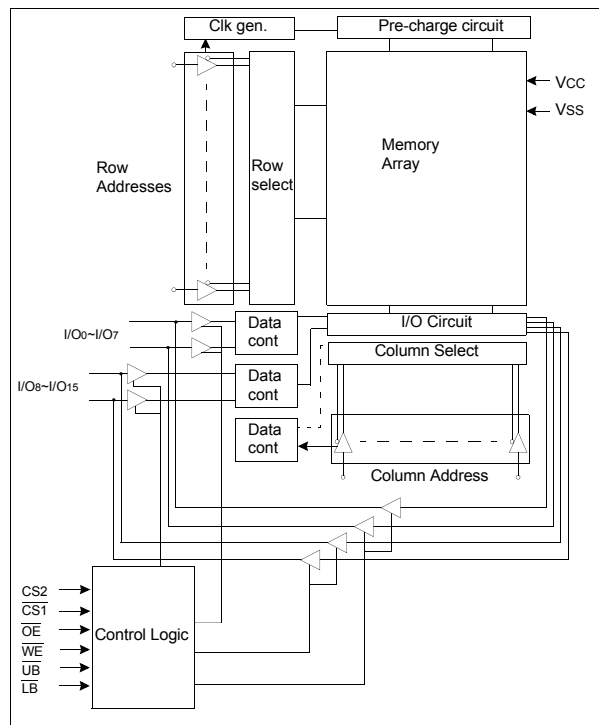
16M x 16 bit Page Mode Uni-Transistor CMOS RAM

1. GENERAL DESCRIPTION

The K1S5616BCA is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports 4 page read operation and Industrial temperature range. The device supports dual chip selection for user interface. The device also supports internal Temperature Compensated Self Refresh mode for the standby power saving at room temperature range.

2. FEATURES & FUNCTION BLOCK DIAGRAM

- Process technology: CMOS
- Organization: 16M x 16 bit
- Power supply voltage: 1.7V~1.95V
- Internal TCSR



3. PRODUCT FAMILY

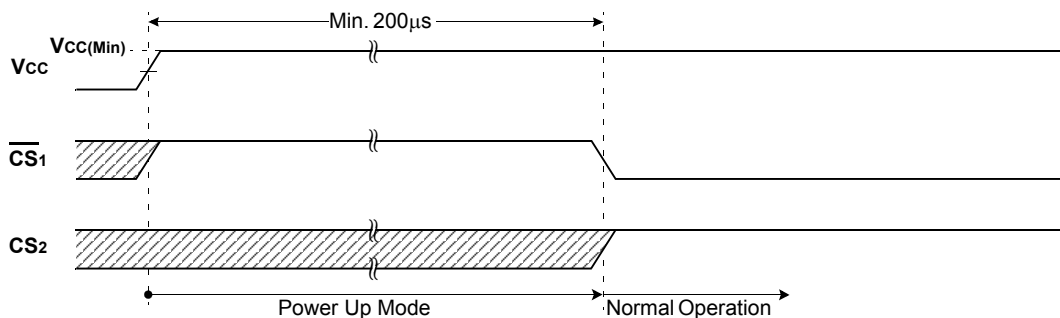
Product Family	Operating Temp.	Vcc Range	Speed (trc)	Power Dissipation	
				Standby (Isb1, Max.)	Operating (Icc2P, Max.)
K1S5616BCA-I	Industrial(-40~85°C)	1.7V~1.95V	70ns	350µA < 85°C 200µA < 40°C	25mA

4. POWER UP SEQUENCE

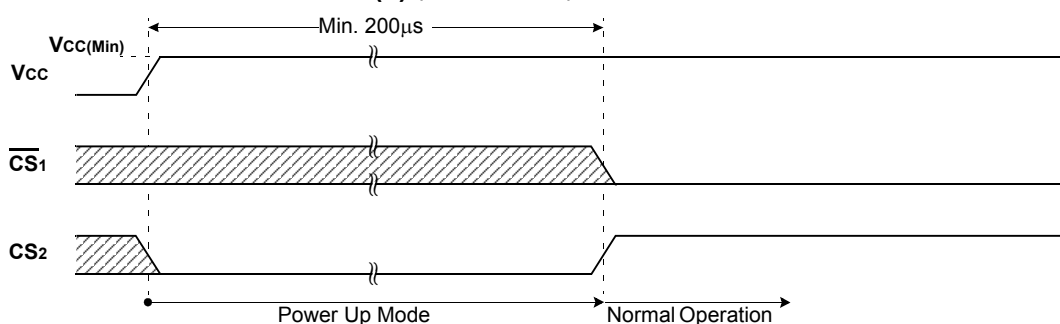
During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power ($V_{cc \text{ min.}}=1.7V$) for a minimum 200 μs with $\overline{CS1}$ =high.or $CS2$ =low.

TIMING WAVEFORM OF POWER UP(1) ($\overline{CS1}$ controlled)



TIMING WAVEFORM OF POWER UP(2) ($CS2$ controlled)



5. FUNCTIONAL DESCRIPTION

$\overline{CS1}$	$CS2$	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O ₁₋₈	I/O ₉₋₁₆	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	High-Z	Deselected	Standby
X ¹⁾	X ¹⁾	X ¹⁾	X ¹⁾	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X ¹⁾	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X ¹⁾	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X ¹⁾	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X ¹⁾	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X ¹⁾	L	L	L	Din	Din	Word Write	Active

NOTE:

1. X means "Don't care". X should be low or high state.

6. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.2 to V _{CCQ} +0.3V	V
Power supply voltage relative to Vss	V _{CC} , V _{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P _D	1.0	W
Storage temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _A	-25 to 85	°C

NOTE:

1. Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

7. RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core)	V _{CC}	1.7	1.8	1.95	V
Power supply voltage(I/O)	V _{CCQ}	1.7	1.8	1.95	V
Ground	V _{SS} , V _{SSQ}	0	0	0	V
Input high voltage	V _{IH}	0.8 x V _{CCQ}	-	V _{CCQ} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.4	V

NOTE:

1. T_A=-25 to 85°C, otherwise specified.
2. Overshoot: V_{CCQ}+1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

8. CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	8	pF

9. DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input Leakage Current	I _{LI}	V _{IN} =V _{SS} to V _{CCQ}	-1	-	1	μA	
Output Leakage Current	I _{LO}	$\overline{CS}=V_{IH}$, $\overline{PS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CCQ}	-1	-	1	μA	
Average Operating Current(Async)	I _{CC2}	Cycle time=70ns, I _{IO} =0mA ²⁾ , 100% duty, $\overline{CS}=V_{IL}$, $\overline{PS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	35	mA	
	I _{CC2P}	Cycle time=t _{RC} +3t _{PC} , I _{IO} =0mA ²⁾ , 100% duty, $\overline{CS}=V_{IL}$, $\overline{PS}=V_{IH}$, V _{IN} =V _{IL} or V _{IH}	-	-	25	mA	
Output Low Voltage	V _{OL}	I _{OL} =0.1mA	-	-	0.2	V	
Output High Voltage	V _{OH}	I _{OH} =-0.1mA	1.4	-	-	V	
Standby Current(CMOS)	I _{SB1} ¹⁾	$\overline{CS} \geq V_{CCQ}-0.2V$, $\overline{PS} \geq V_{CCQ}-0.2V$, Other inputs=V _{SS} or V _{CCQ}	< 40°C	-	-	200	μA
			< 85°C	-	-	350	μA

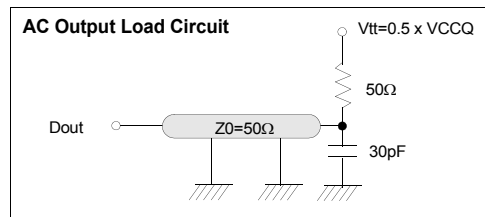
NOTE:

1. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize Refresh cycle below 40°C.
2. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

10. AC OPERATING CONDITIONS

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
 Input pulse level: 0.2V to Vcc-0.2V
 Input rising and falling time: 3ns
 Input and output reference voltage: 0.5 x Vccq
 Output load: CL=30pF
 Vcc:1.7V~1.95V
 TA: -25°C~85°C



11. AC CHARACTERISTICS

Parameter List		Symbol	Speed		Units
			Min	Max	
Common	\overline{CS} High Pulse Width	tCSHP(A)	10	-	ns
Asynch. Read	Read Cycle Time	tRC	70	-	ns
	Page Read Cycle Time	tPC	20	-	ns
	Address Access Time	tAA	-	70	ns
	Page Access Time	tPA	-	20	ns
	Chip Select to Output	tCO	-	70	ns
	Output Enable to Valid Output	tOE	-	20	ns
	\overline{UB} , \overline{LB} Access Time	tBA	-	70	ns
	Chip Select to Low-Z Output	tLZ	10	-	ns
	\overline{UB} , \overline{LB} Enable to Low-Z Output	tBLZ	5	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	ns
	Chip Disable to High-Z Output	tCHZ	0	10	ns
	\overline{UB} , \overline{LB} Disable to High-Z Output	tBHZ	0	10	ns
	Output Disable to High-Z Output	tOHZ	0	10	ns
	Output Hold	tOH	5	-	ns
Asynch. Write	Write Cycle Time	tWC	70	-	ns
	Chip Select to End of Write	tCW	60	-	ns
	Address Set-up Time to Beginning of Write	tAS	0	-	ns
	Address Valid to End of Write	tAW	60	-	ns
	\overline{UB} , \overline{LB} Valid to End of Write	tBW	60	-	ns
	Write Pulse Width	tWP	55 ¹⁾	-	ns
	\overline{WE} High Pulse Width	tWHP	5	-	ns
	Write Recovery Time	tWR	0	-	ns
	Data to Write Time Overlap	tDW	20	-	ns
	Data Hold from Write Time	tDH	0	-	ns

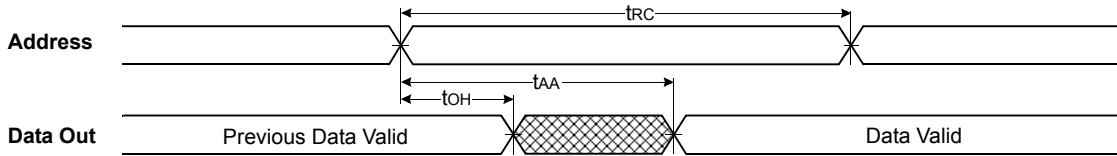
NOTE:

- tWP(min)=70ns for continuous write without \overline{CS} toggling longer than 1.7us
- The High-Z timings measure a 100mV transition from either VOH or VOL toward VCCQ x 0.5
- The Low-Z timings measure a 100mV transition away from the High-Z level toward either VOH or VOL.

12. TIMING WAVEFORMS

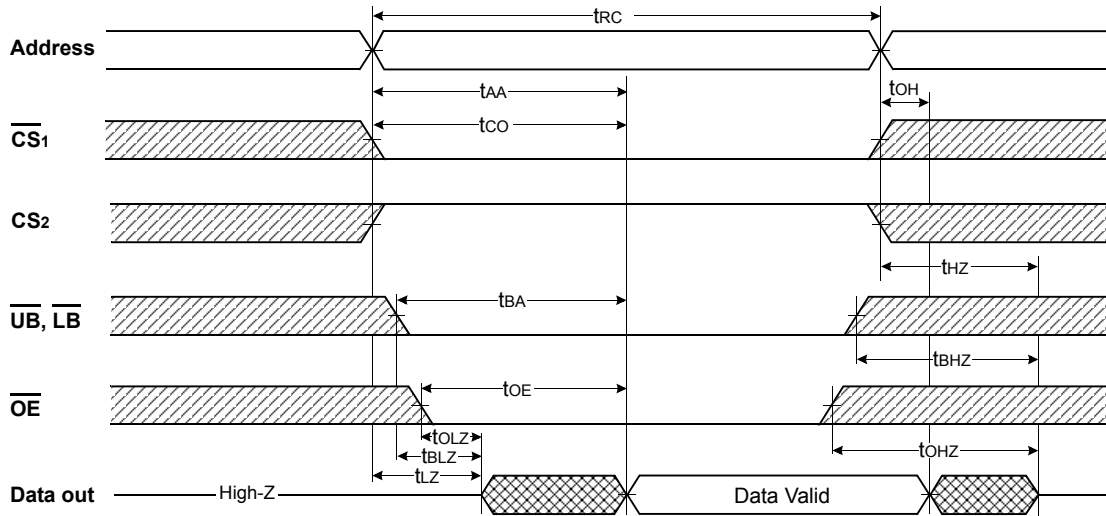
TIMING WAVEFORM OF READ CYCLE(1)

(Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$, \overline{UB} or/and $\overline{LB}=V_{IL}$)

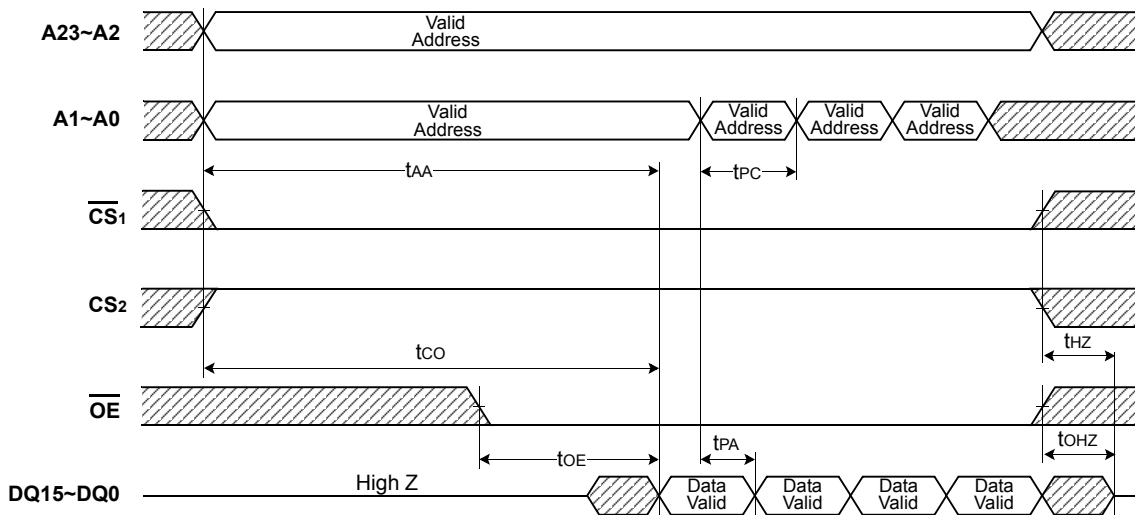


TIMING WAVEFORM OF READ CYCLE(2)

($\overline{WE}=V_{IH}$)



TIMING WAVEFORM OF PAGE CYCLE (READ ONLY)



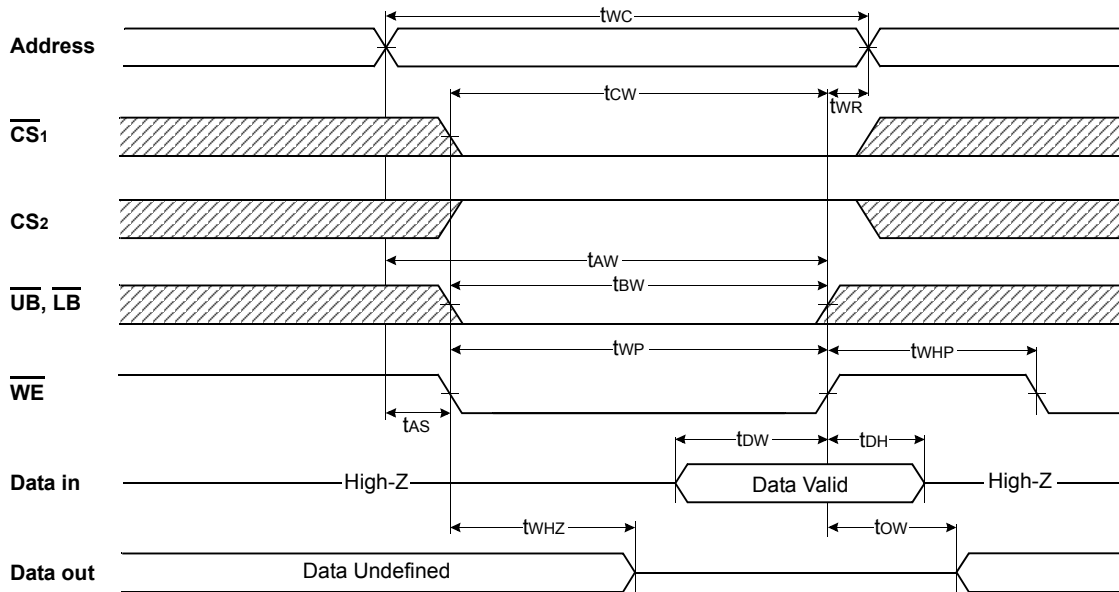
NOTE:

(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.
3. $t_{OE}(\text{max})$ is met only when \overline{OE} becomes enabled after $t_{AA}(\text{max})$.
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 1.7 μ s, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 1.7 μ s.

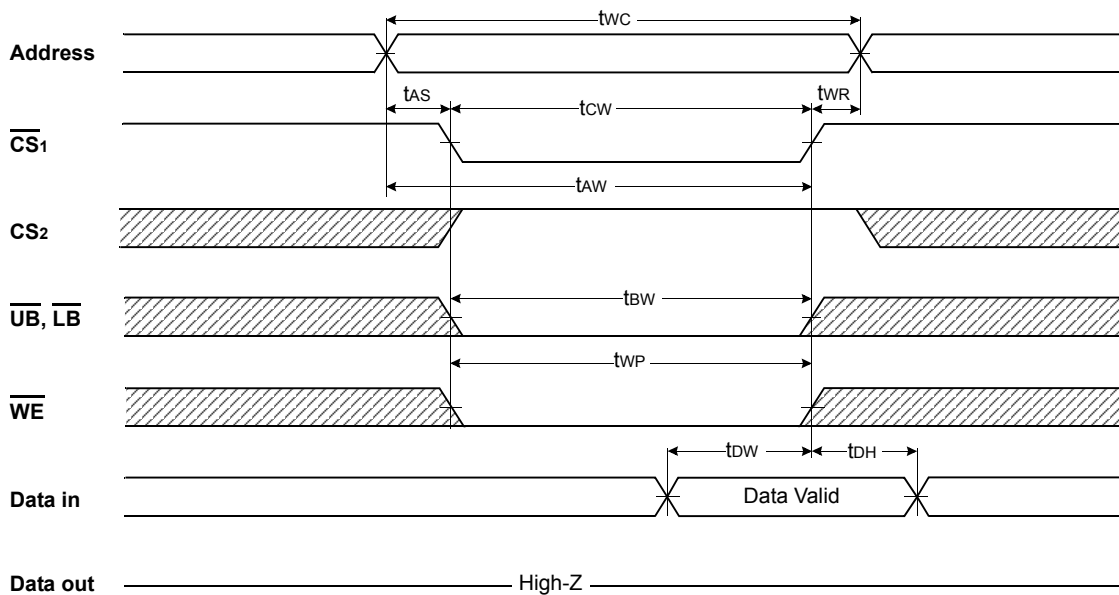
TIMING WAVEFORM OF WRITE CYCLE(1)

(\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)

($\overline{CS1}$ Controlled)

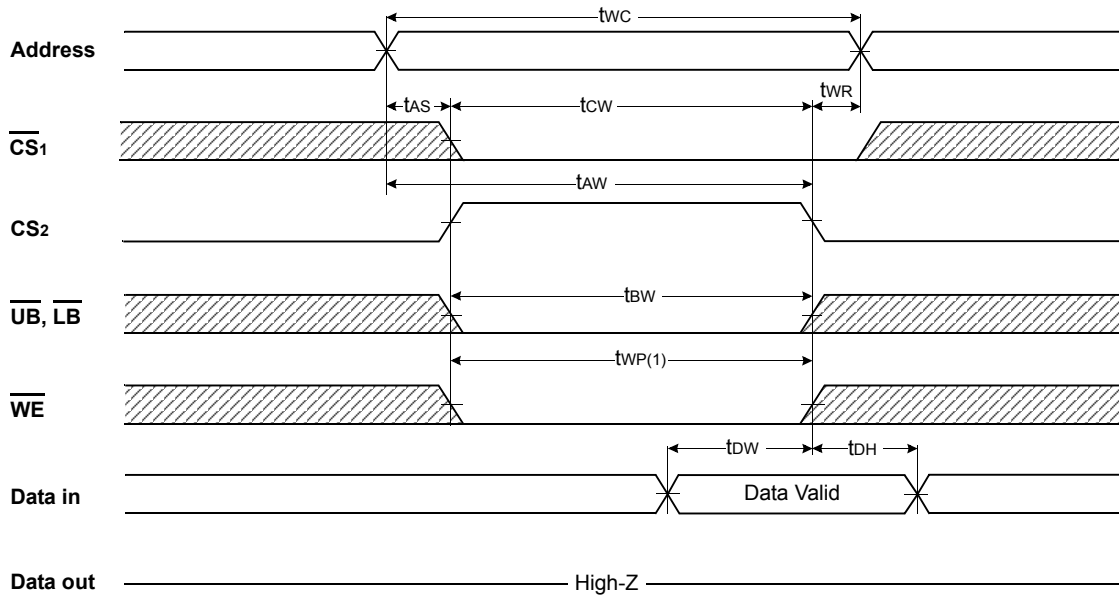


NOTE:

1. A write occurs during the overlap (t_{WP}) of low \overline{CS} and low \overline{WE} . A write begins when \overline{CS} goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when \overline{CS} goes high or \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS} going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with \overline{CS} or \overline{WE} going high.
5. In asynchronous write cycle, Clock and ADV signals are ignored.
6. Condition for continuous write operation over 50 times : $t_{WP}(\min)=70ns$

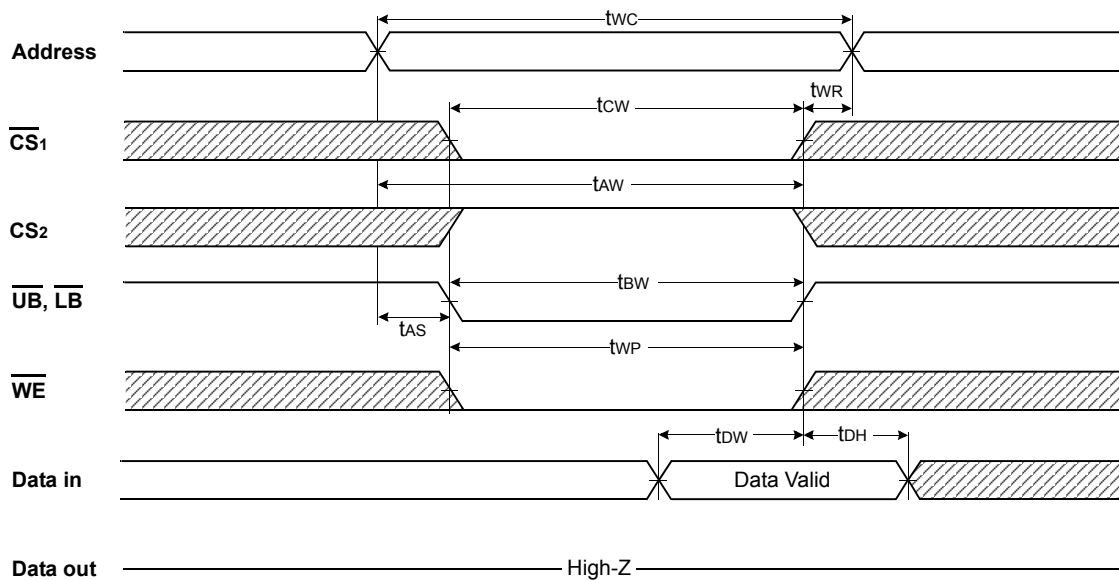
TIMING WAVEFORM OF WRITE CYCLE(3)

(CS2 Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4)

(UB, LB Controlled)



NOTE:

(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS1}$ and low \overline{WE} . A write begins when $\overline{CS1}$ goes low and \overline{WE} goes low with asserting \overline{UB} or \overline{LB} for single byte operation or simultaneously asserting \overline{UB} and \overline{LB} for double byte operation. A write ends at the earliest transition when $\overline{CS1}$ goes high and \overline{WE} goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{cw} is measured from the $\overline{CS1}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS1}$ or \overline{WE} going high.