

256Mbit GDDR SDRAM

**Revision 2.1
April 2005**

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K4D551638F-TC

256M GDDR SDRAM

Revision History

Revision 2.1(April 29, 2005)

- Modified CKE input functional description on page 5.
- Added K4D551638F-TC60 from the data sheet.

Revision 2.0(March 24, 2005)

- Removed K4D551638F-TC60 from the data sheet.
- Typo corrected.

Revision 1.9(February 24, 2005)

- Typo corrected.

Revision 1.8 (August 30, 2004)

- DC Spec defined for -TC33/36/40

Revision 1.7 (June 15, 2004)

- Changed VDD/VDDQ of K4D551638F-TC33 from $2.8V \pm 0.1V$ to $2.8V(\min)/2.95V(\max)$
- Spec for -TC33/36/40 still in target

Revision 1.6 (March 31, 2004)

- AC Changes : Refer to the AC characteristics of page 13 and 14.

Revision 1.5 (March 18, 2004)

- Added K4D551638F-TC33 in the data sheet.
- Target spec defined for -TC33

Revision 1.4 (February 27, 2004)

- Added K4D551638F-TC36/40 in the data sheet.
- Target spec defined for -TC36/40

Revision 1.3 (December 5, 2003)

- Changed VDD/VDDQ of K4D551638F-TC50 from $2.5V \pm 5\%$ to $2.6V \pm 0.1V$

Revision 1.2 (November 11, 2003)

- "Write-Interrupted by Read Function" is supported

Revision 1.1 (October 13, 2003)

- Defined ICC7 value

Revision 1.0 (October 10, 2003)

- Defined DC spec
- Changed part number of 16Mx16 GDDR F-die from K4D561638F-TC to K4D551638F-TC.

Revision 0.1 (October 2, 2003) - *Target Spec*

- Added Lead free package part number in the data sheet.
- Removed K4D561638F-TC40 from the data sheet.

K4D551638F-TC

256M GDDR SDRAM

4M x 16Bit x 4 Banks Graphic Double Data Rate Synchronous DRAM with Bi-directional Data Strobe and DLL

FEATURES

- 2.6V ± 0.1V power supply for device operation
- 2.6V ± 0.1V power supply for I/O interface
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
 - Read latency 3 (clock)
 - Burst length (2, 4 and 8)
 - Burst type (sequential & interleave)
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write-Interrupted by Read Function
- 2 DQS's (1DQS / Byte)
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 64ms refresh period (8K cycle)
- 66pin TSOP-II
- Maximum clock frequency up to 300MHz
- Maximum data rate up to 600Mbps/pin

ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	Interface	VDD & VDDQ	Package
K4D551638F-TC33	300MHz	600Mbps/pin	SSTL_2	2.8V ~ 2.95V	66pin TSOP-II
K4D551638F-TC36	275MHz	550Mbps/pin		2.8V±0.1V	
K4D551638F-TC40	250MHz	500Mbps/pin		2.6V±0.1V	
K4D551638F-TC50	200MHz	400Mbps/pin			
K4D551638F-TC60*	166MHz	333Mbps/pin		2.5V±0.125V	

1. K4D551638F-LC is the Lead Free package part number.
2. For the K4D551638F-TC60, VDD & VDDQ = 2.5V ± 5%
3. For the K4D551638F-TC36, VDD & VDDQ = 2.8V ± 0.1V
4. For the K4D551638F-TC33, VDD & VDDQ = 2.8V ~ 2.95V

GENERAL DESCRIPTION

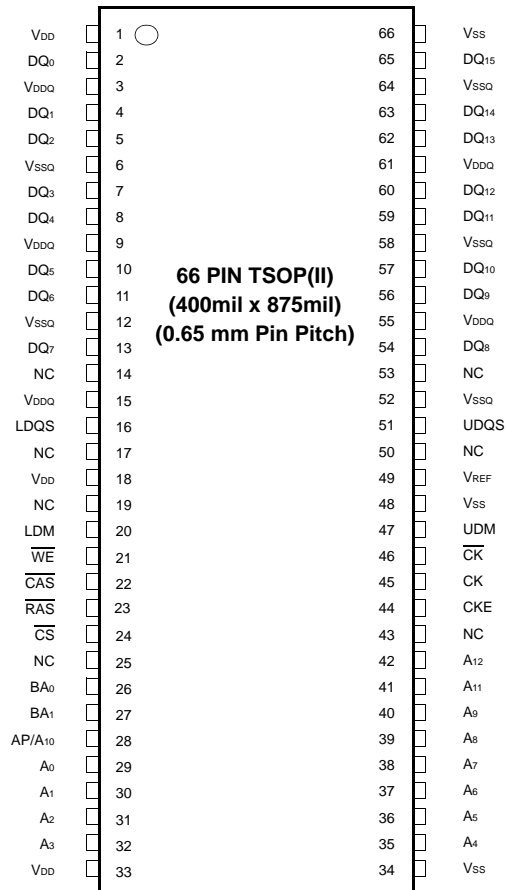
FOR 4M x 16Bit x 4 Bank GDDR SDRAM

The K4D551638F is 268,435,456 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 4,194,304 words by 16 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.1GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

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PIN CONFIGURATION (Top View)



PIN DESCRIPTION

CK, \overline{CK}	Differential Clock Input	BA0, BA1	Bank Select Address
CKE	Clock Enable	A0 ~A12	Address Input
\overline{CS}	Chip Select	DQ0 ~ DQ15	Data Input/Output
\overline{RAS}	Row Address Strobe	VDD	Power
\overline{CAS}	Column Address Strobe	VSS	Ground
WE	Write Enable	VDDQ	Power for DQ's
L(U)DQS	Data Strobe	VSSQ	Ground for DQ's
L(U)DM	Data Mask	NC	No Connection
RFU	Reserved for Future Use	VREF	Reference voltage

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INPUT/OUTPUT FUNCTIONAL DESCRIPTION

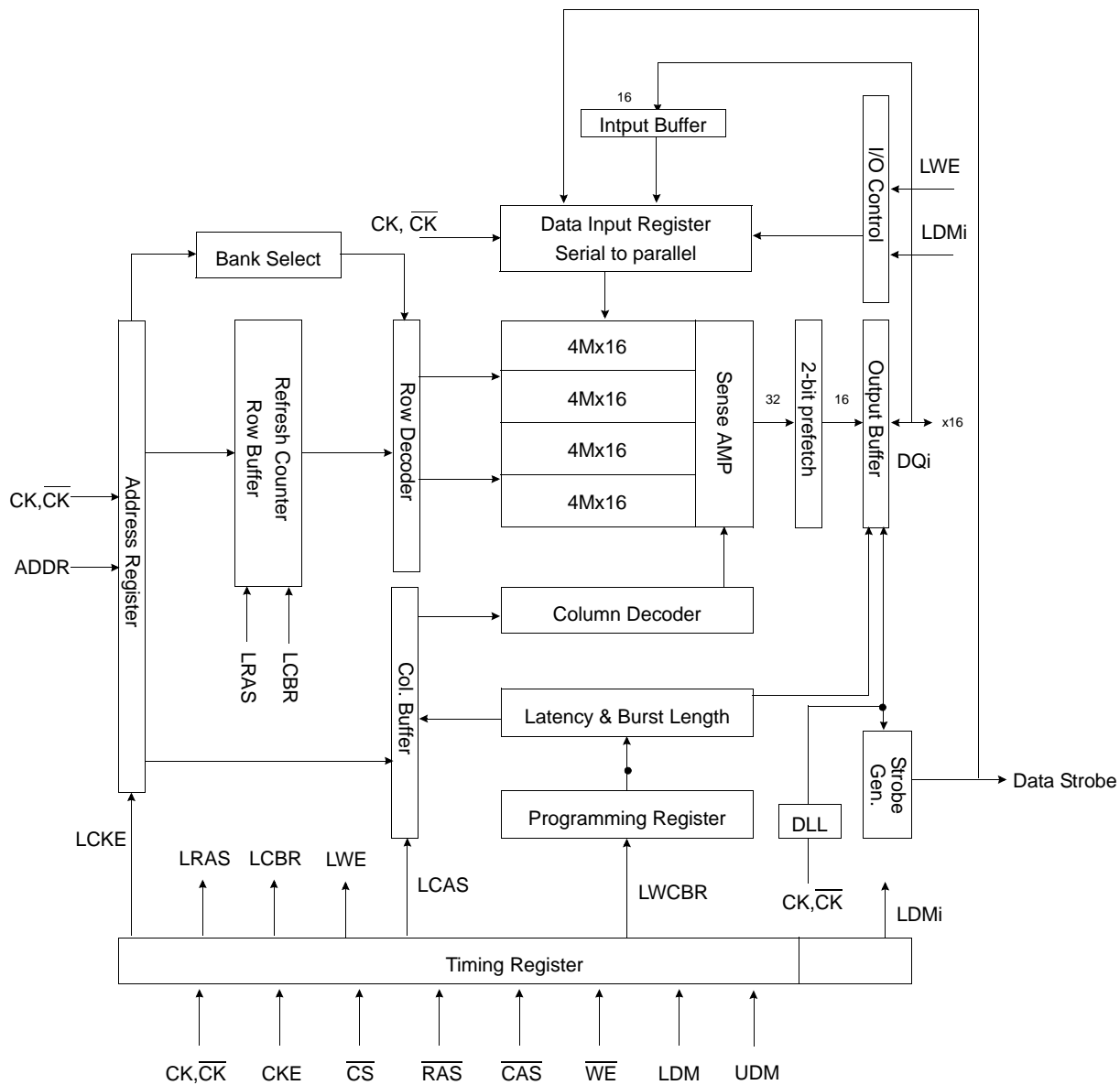
Sym-	Type	Function
CK, \overline{CK}^*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ's and DM's that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the \overline{CK} signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode. CKE is synchronous for Power down entry and exit, and for Self refresh entry. CKE is asynchronous for Self refresh exit, and for output disable. CKE must be maintained high through Read and Write accesses. Input buffers, excluding CK, \overline{CK} and CKE are disabled during Power down. Input buffers, excluding CKE are disabled during Self refresh. CKE is an SSTL_2 input, but will detect a LVCMOS low level after Vdd is applied upon 1st power up. After Vref has become stable during the power on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper Self refresh entry and exit, Vref must be maintained to this input.
\overline{CS}	Input	\overline{CS} enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
\overline{RAS}	Input	Latches row addresses on the positive going edge of the CK with \overline{RAS} low. Enables row access & precharge.
\overline{CAS}	Input	Latches column addresses on the positive going edge of the CK with \overline{CAS} low. Enables column access.
\overline{WE}	Input	Enables write operation and row precharge. Latches data in starting from \overline{CAS} , \overline{WE} active.
LDQS, UDQS	Input/Output	Data input and output are synchronized with both edge of DQS. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15.
LDM, UDM	Input	Data in Mask. Data In is masked by DM Latency=0 when DM is high in burst write. For the x16, LDM corresponds to the data on DQ0-DQ7 ; UDM corresponds to the data on DQ8-DQ15.
DQ0 ~ DQ15	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA0, BA1	Input	Selects which bank is to be active.
A0 ~ A12	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA0 ~ RA12, Column addresses : CA0 ~ CA8.
VDD/VSS	Power Supply	Power and ground for the input buffers and core logic.
VDDQ/VSSQ	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
VREF	Power Supply	Reference voltage for inputs, used for SSTL interface.
NC/RFU	No connection/ Reserved for future use	This pin is recommended to be left "No connection" on the device

*1 : The timing reference point for the differential clocking is the cross point of CK and \overline{CK} .
For any applications using the single ended clocking, apply VREF to \overline{CK} pin.

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BLOCK DIAGRAM (4Mbit x 16I/O x 4 Bank)



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FUNCTIONAL DESCRIPTION

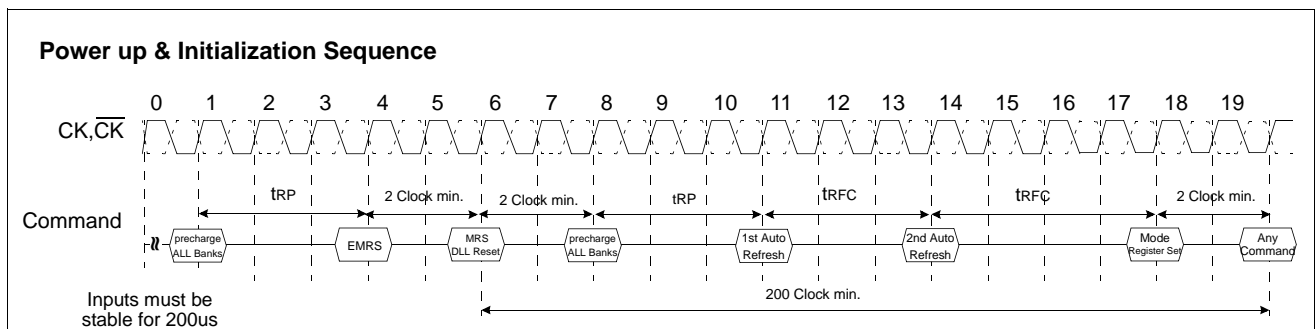
• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
 - Apply VDD before VDDQ .
 - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,CK⁻), apply NOP and take CKE to be high .
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL
- *1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.
- *1,2 7. Issue precharge command for all banks of the device.
8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

*2 Sequence of 6&7 is regardless of the order.



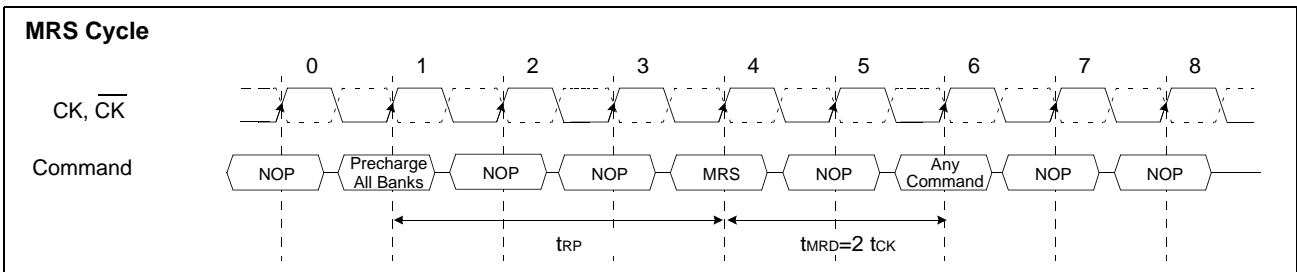
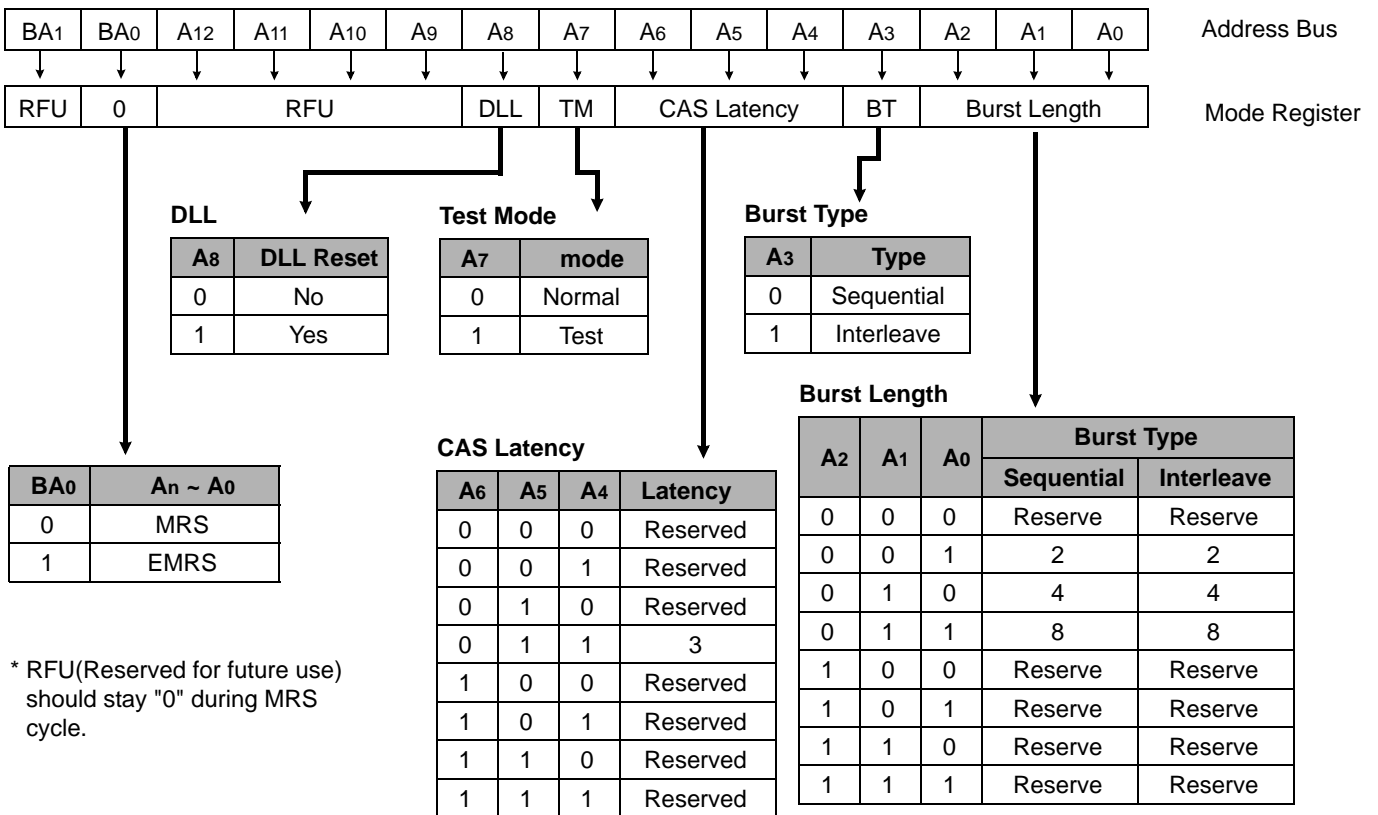
*** When the operating frequency is changed, DLL reset should be required again.
After DLL reset again, the minimum 200 cycles of clock input is needed to lock the DLL.**

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MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs CAS latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on CS, RAS, CAS and WE (The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A0 ~ A12 and BA0, BA1 in the same cycle as CS, RAS, CAS and WE going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, CAS latency(read latency from column address) uses A4 ~ A6. A7 is used for test mode. A8 is used for DLL reset. A7,A8, BA0 and BA1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and CAS latencies.



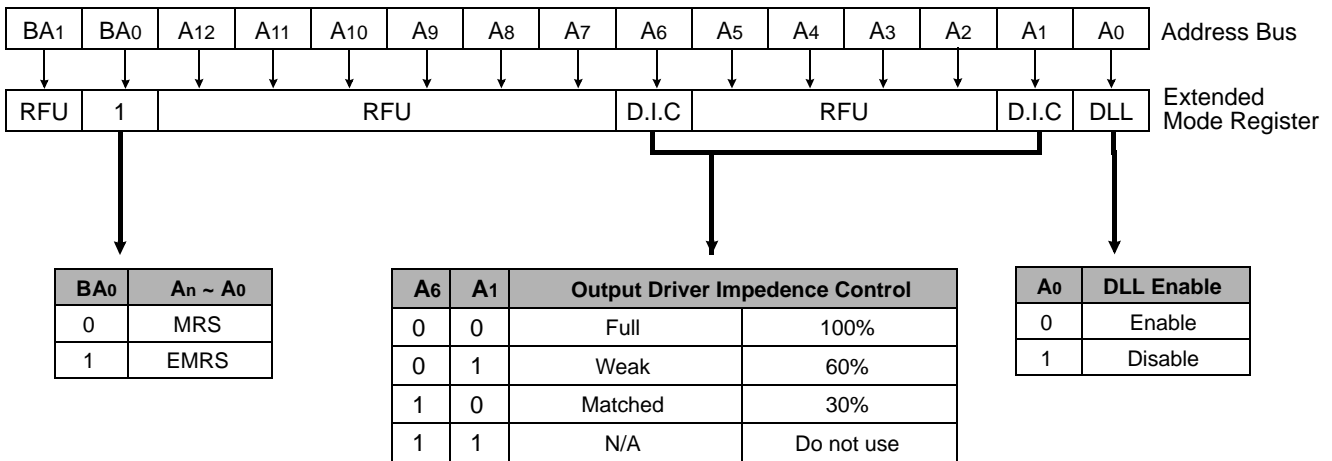
*1 : MRS can be issued only at all banks precharge state.
 *2 : Minimum t_{RP} is required to issue MRS command.

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EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A12 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



*1 : RFU(Reserved for future use) should stay "0" during EMRS cycle.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	V _{DD}	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	V _{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	2.0	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V _{DD}	2.5	2.6	2.7	V	1, 7
Output Supply voltage	V _{DDQ}	2.5	2.6	2.7	V	1
Reference voltage	V _{REF}	0.49*V _{DDQ}	-	0.51*V _{DDQ}	V	2
Termination voltage	V _{tt}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3
Input logic high voltage	V _{IH(DC)}	V _{REF} +0.15	-	V _{DDQ} +0.30	V	4
Input logic low voltage	V _{IL(DC)}	-0.30	-	V _{REF} -0.15	V	5
Output logic high voltage	V _{OH}	V _{tt} +0.76	-	-	V	I _{OH} =-15.2mA
Output logic low voltage	V _{OL}	-	-	V _{tt} -0.76	V	I _{OL} =+15.2mA
Input leakage current	I _{IL}	-5	-	5	uA	6
Output leakage current	I _{OL}	-5	-	5	uA	6

- Note :**
- Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
 - V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed + 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed + 25mV for DC error and an additional + 25mV for AC noise.
 - V_{tt} of the transmitting device must track V_{REF} of the receiving device.
 - V_{IH(max.)}= V_{DDQ} +1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
 - V_{IL(min.)}= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
 - For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V.
 - For the K4D551638F-TC60 , VDD & VDDQ =2.5V ± 5%,
For the K4D551638F-TC36 , VDD & VDDQ =2.8V ± 0.1V
and For the K4D551638F-TC33 , VDD & VDDQ = 2.8V ~ 2.95V**

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DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, TA=0 to 65°C)

Parameter	Symbol	Test Condition	Version					Unit	Note
			-33	-36	-40	-50	-60		
Operating Current (One Bank Active)	I _{CC1}	Burst Lenth=2 trc ≥ trc(min) IoL=0mA, tcc= tcc(min)	210	205	165	150	125	mA	1
Precharge Standby Current in Power-down mode	I _{CC2P}	CKE ≤ V _{IL} (max), tcc= tcc(min)	6	6	5	4	3	mA	
Precharge Standby Current in Non Power-down mode	I _{CC2N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc= tcc(min)	50	45	37	25	20	mA	
Active Standby Current power-down mode	I _{CC3P}	CKE ≤ V _{IL} (max), tcc= tcc(min)	70	65	60	55	35	mA	
Active Standby Current in in Non Power-down mode	I _{CC3N}	CKE ≥ V _{IH} (min), CS ≥ V _{IH} (min), tcc= tcc(min)	100	95	80	75	56	mA	
Operating Current (Burst Mode)	I _{CC4}	trc ≥ trFC(min)trc ≥ trFC(min) Page Burst, All Banks activated.	405	400	320	250	200	mA	
Refresh Current	I _{CC5}	trc ≥ trFC(min)	275	270	220	200	180	mA	2
Self Refresh Current	I _{CC6}	CKE ≤ 0.2V	4	4	4	3	3	mA	
Operating Current (4Bank Interleaving)	I _{CC7}	Burst Length=4, trc ≥ trFC(min) IoL=0mA, tcc = tcc(min)	520	515	410	380	350	mA	

- Note** : 1. Measured with outputs open.
2. Refresh period is 64ms

AC INPUT OPERATING CONDITIONS

Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}=2.6V±0.1V, V_{DDQ}=2.6V±0.1V ,TA=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V _{IH}	V _{REF} +0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V _{IL}	-	-	V _{REF} -0.35	V	
Clock Input Differential Voltage; CK and \overline{CK}	V _{ID}	0.7	-	V _{DDQ} +0.6	V	1
Clock Input Crossing Point Voltage; CK and \overline{CK}	V _{IX}	0.5*V _{DDQ} -0.2	-	0.5*V _{DDQ} +0.2	V	2

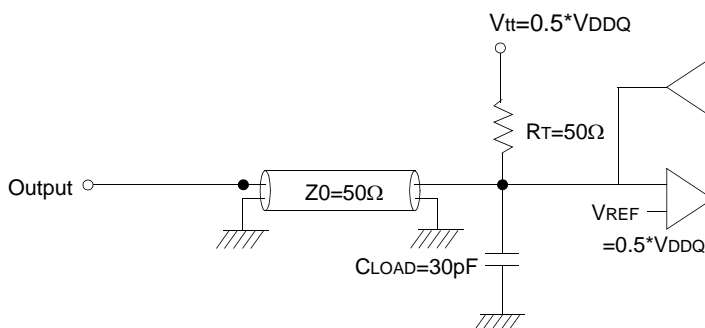
- Note** : 1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on \overline{CK}
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same

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AC OPERATING TEST CONDITIONS ($V_{DD}=2.6V \pm 0.1V$, $T_A= 0$ to $65^{\circ}C$)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	$0.50 \cdot V_{DDQ}$	V	
CK and \overline{CK} signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	$V_{REF}+0.35/V_{REF}-0.35$	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE ($V_{DD}=2.6V$, $T_A= 25^{\circ}C$, $f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, \overline{CK})	C_{IN1}	1.0	5.0	pF
Input capacitance(A_0 ~ A_{12} , BA_0 ~ BA_1)	C_{IN2}	1.0	4.0	pF
Input capacitance (CKE, CS, RAS, CAS, WE)	C_{IN3}	1.0	4.0	pF
Data & DQS input/output capacitance(DQ_0 ~ DQ_{15})	C_{OUT}	1.0	6.5	pF
Input capacitance(DM_0 ~ DM_3)	C_{IN4}	1.0	6.5	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	$0.1 + 0.01$	μF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	$0.1 + 0.01$	μF

- Note :**
- V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
 - V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

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AC CHARACTERISTICS

Parameter	Symbol	-33		-36		-40		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK cycle time	CL=3 tCK	3.3	10	3.6	10	4.0	10	5.0	10	6.0	12	ns	
CK high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK	tDQSCK	-0.6	0.6	-0.6	0.6	-0.6	0.6	-0.55	0.55	-0.6	0.6	ns	
Output access time from CK	tAC	-0.6	0.6	-0.6	0.6	-0.6	0.6	-0.65	0.65	-0.7	0.7	ns	
Data strobe edge to Dout edge	tDQSQ	-	0.35	-	0.4	-	0.4	-	0.4	-	0.45	ns	1
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.85	1.15	0.85	1.15	0.85	1.15	0.72	1.28	0.75	1.25	tCK	
DQS-In setup time	tWPRES	0	-	0	-	0	-	0	-	0	-	ns	
DQS-in hold time	tWPREH	0.35	-	0.35	-	0.35	-	0.25	-	0.25	-	tCK	
DQS write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.35	-	0.35	-	tCK	
DQS-In low level width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.35	-	0.35	-	tCK	
Address and Control input setup	tIS	0.9	-	0.9	-	0.9	-	0.6	-	0.8	-	ns	
Address and Control input hold	tIH	0.9	-	0.9	-	0.9	-	0.6	-	0.8	-	ns	
DQ and DM setup time to DQS	tDS	0.35	-	0.4	-	0.4	-	0.4	-	0.45	-	ns	
DQ and DM hold time to DQS	tDH	0.35	-	0.4	-	0.4	-	0.4	-	0.45	-	ns	
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Data output hold time from DQS	tQH	tHP- 0.35	-	tHP-0.4	-	tHP-0.4	-	tHP-0.5	-	tHP- 0.55	-	ns	1

Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
 - . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
 - . X=A frequency dependent timing allowance account for tDQSQmax

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AC CHARACTERISTICS (I)

Parameter	Symbol	-33		-36		-40		-50		-60		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time	tRC	15	-	15	-	13	-	12	-	10	-	tCK	
Refresh row cycle time	tRFC	17	-	17	-	15	-	14	-	12	-	tCK	
Row active time	tRAS	10	100K	10	100K	9	100K	8	100K	7	100K	tCK	
RAS to CAS delay for Read	tRCDRD	5	-	5	-	4	-	4	-	3	-	tCK	
RAS to CAS delay for Write	tRCDWR	3	-	3	-	2	-	2	-	2	-	tCK	
Row precharge time	tRP	5	-	5	-	4	-	4	-	3	-	tCK	
Row active to Row active	tRRD	3	-	3	-	3	-	2	-	2	-	tCK	
Last data in to Row precharge @Normal Precharge	tWR	3	-	3	-	3	-	3	-	3	-	tCK	1
Last data in to Row precharge @Auto Precharge	tWR_A	3	-	3	-	3	-	3	-	3	-	tCK	1
Last data in to Read command	tCDLR	3	-	2	-	2	-	2	-	1	-	tCK	1
Col. address to Col. address	tCCD	1	-	1	-	1	-	1	-	1	-	tCK	
Mode register set cycle time	tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	tDAL	8	-	8	-	7	-	7	-	6	-	tCK	
Exit self refresh to read command	tXSR	200	-	200	-	200	-	200	-	200	-	tCK	
Power down exit time	tPDEX	3tCK + tIS	-	3tCK + tIS	-	3tCK + tIS	-	1tCK + tIS	-	1tCK + tIS	-	ns	
Refresh interval time	tREF	7.8	-	7.8	-	7.8	-	7.8	-	7.8	-	us	

Note : 1. For normal write operation, even numbers of Din are to be written inside DRAM

AC CHARACTERISTICS (II)

(Unit : Number of Clock)

K4D551638F-TC33

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
300MHz (3.3ns)	3	15	17	10	5	3	5	3	8	tCK

K4D551638F-TC36

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
275MHz (3.6ns)	3	15	17	10	5	3	5	3	8	tCK

K4D551638F-TC40

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
250MHz (4.0ns)	3	13	15	9	4	2	4	3	7	tCK
200MHz (5.0ns)	3	12	14	8	4	2	4	3	7	tCK

K4D551638F-TC50

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
200MHz (5.0ns)	3	12	14	8	4	2	4	3	7	tCK

K4D551638F-TC60

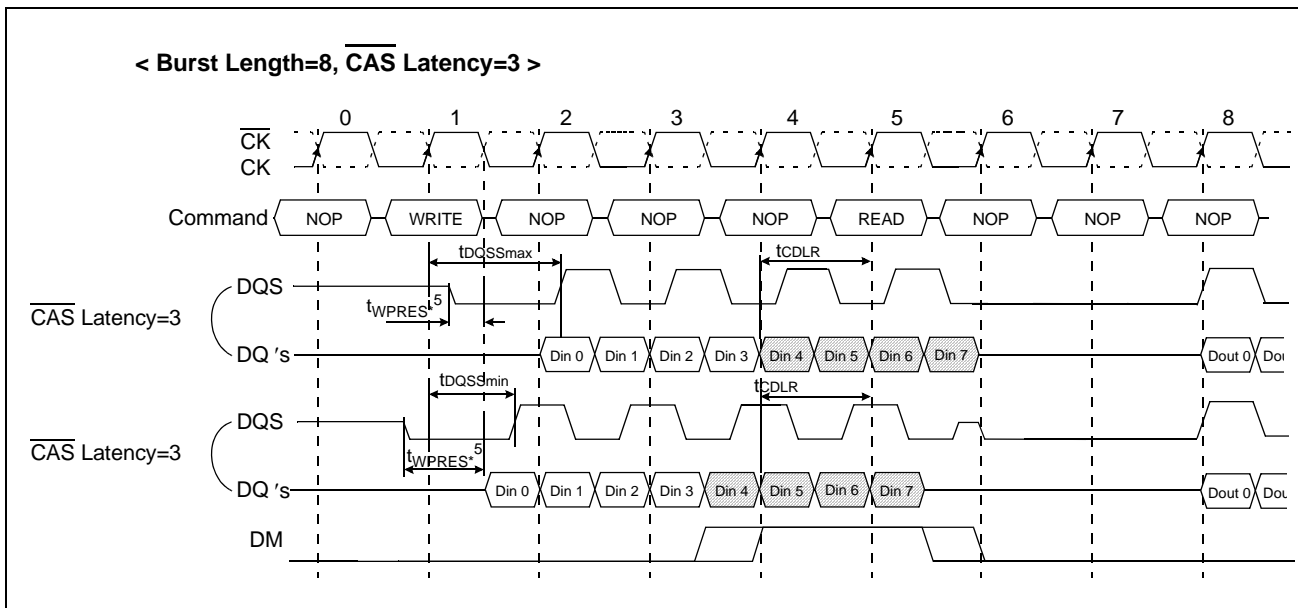
Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	tDAL	Unit
166MHz (6.0ns)	3	10	12	7	3	2	3	2	6	tCK

K4D551638F-TC

256M GDDR SDRAM

Write Interrupted by a Read & DM

A burst write can be interrupted by a read command of any bank. The DQ's must be in the high impedance state at least one clock cycle before the interrupting read data appear on the outputs to avoid data contention. When the read command is registered, any residual data from the burst write cycle must be masked by DM. The delay from the last data to read command (t_{CDLR}) is required to avoid the data contention DRAM inside. Data that are presented on the DQ pins before the read command is initiated will actually be written to the memory. Read command interrupting write can not be issued at the next clock edge of that of write command.



The following function established how a Read command may interrupt a Write burst and which input data is not written into the memory.

1. For Read commands interrupting a Write burst, the minimum Write to Read command delay is 2 clock cycles. The case where the Write to Read delay is 1 clock cycle is disallowed
2. For Read commands interrupting a Write burst, the DM pin must be used to mask the input data words which immediately precede the interrupting Read operation and the input data word which immediately follows the interrupting Read operation
3. For all cases of a Read interrupting a Write, the DQ and DQS buses must be released by the driving chip (i.e., the memory controller) in time to allow the buses to turn around before the GDDR drives them during a read operation.
4. If input Write data is masked by the Read command, the DQS input is ignored by the GDDR.

*** This function is only supported in 200/166MHz.**

