

# 18Mb B-die Sync. SRAM Specification

**100TQFP with Pb & Pb-Free**  
**(RoHS compliant)**

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**Document Title**

**512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM**

**Revision History**

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial draft	Mar. 23. 2004	Advance
0.1	1. Update the DC current spec(Icc, Isb)	May. 21, 2004	Preliminary
0.2	1. Change the ISB,ISB1,ISB2 - ISB ; from 120mA to 170mA - ISB1 ; from 80mA to 150mA - ISB2 ; from 80mA to 130mA	Sep. 21. 2004	Preliminary
0.3	1. Remove the 1.8V Vdd voltage level	Oct. 18.2004	Preliminary
0.4	1. Remove the -16 speed bin	Jan. 04. 2005	Preliminary
1.0	1. Finalize the datasheet	July 18. 2005	Final
2.0	1. Add the overshoot timing	Feb. 16. 2006	Final
3.0	1. Change ordering information	Apr. 03. 2006	Final

**18Mb SPB (2E2D) Synchronous SRAM Ordering Information**

Org.	VDD (V)	Speed (ns)	Access Time (ns)	Part Number	RoHS Avail.
1Mx18	3.3/2.5	5.0	3.1	K7A161831B-P(Q) <sup>1</sup> C(I) <sup>2</sup> 20	√
512Kx36	3.3/2.5	5.0	3.1	K7A163631B-P(Q) <sup>1</sup> C(I) <sup>2</sup> 20	√

Note 1. P(Q) [Package type] : P-Pb Free, Q-Pb  
2. C(I) [Operating Temperature] : C-Commercial, I-Industrial

**512Kx36 & 1Mx18-Bit Synchronous Pipelined Burst SRAM**

**FEATURES**

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- $V_{DD}$  = 2.5 or 3.3V +/- 5% Power Supply.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- $\overline{LBO}$  Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 2cycle Disable.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$ ,  $\overline{ADSC}$ ,  $\overline{ADV}$  Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package (Lead and Lead free package)
- Operating in commercial and industrial temperature range.

**GENERAL DESCRIPTION**

The K7A163631B and K7A161831B are 18,874,368-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 512K(1M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications;  $\overline{GW}$ ,  $\overline{BW}$ ,  $\overline{LBO}$ , ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by  $\overline{GW}$ , and each byte write is performed by the combination of  $\overline{WEx}$  and  $\overline{BW}$  when  $\overline{GW}$  is high. And with  $\overline{CS}_1$  high,  $\overline{ADSP}$  is blocked to control signals.

Burst cycle can be initiated with either the address status processor( $\overline{ADSP}$ ) or address status cache controller( $\overline{ADSC}$ ) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance( $\overline{ADV}$ ) input.

$\overline{LBO}$  pin is DC operated and determines burst sequence(linear or interleaved).

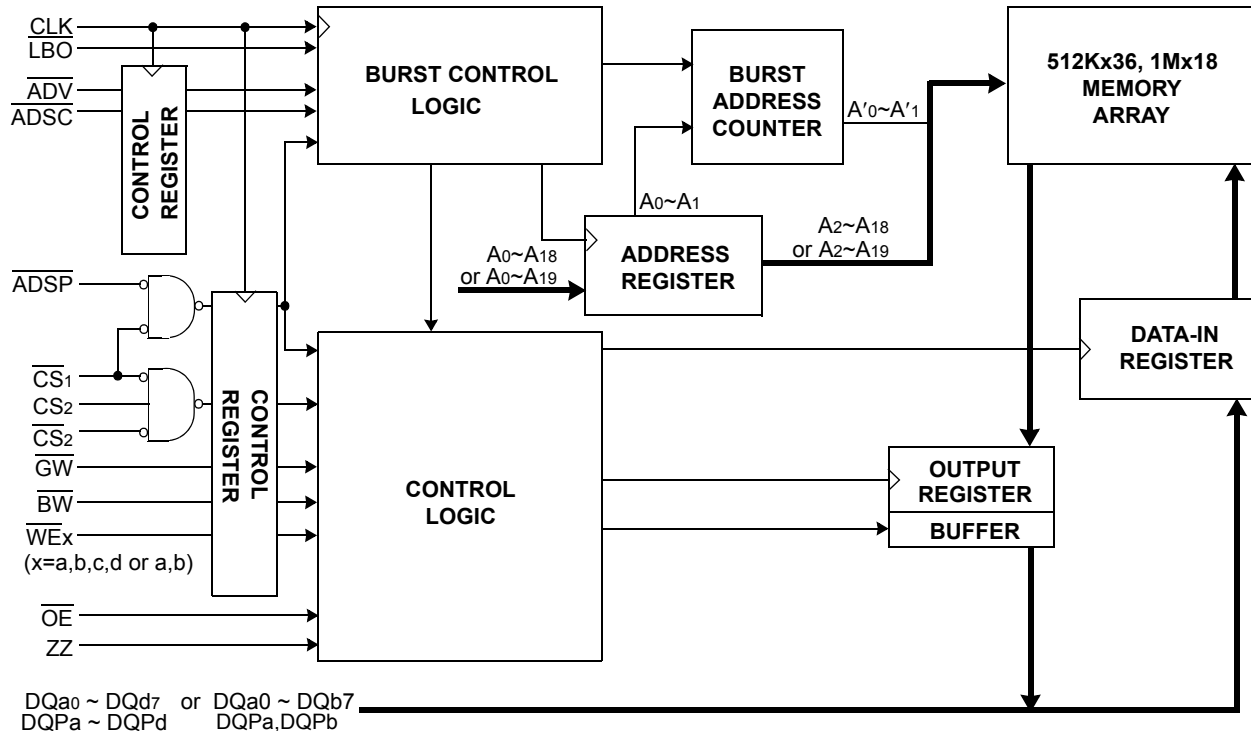
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7A163631B and K7A161831B are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

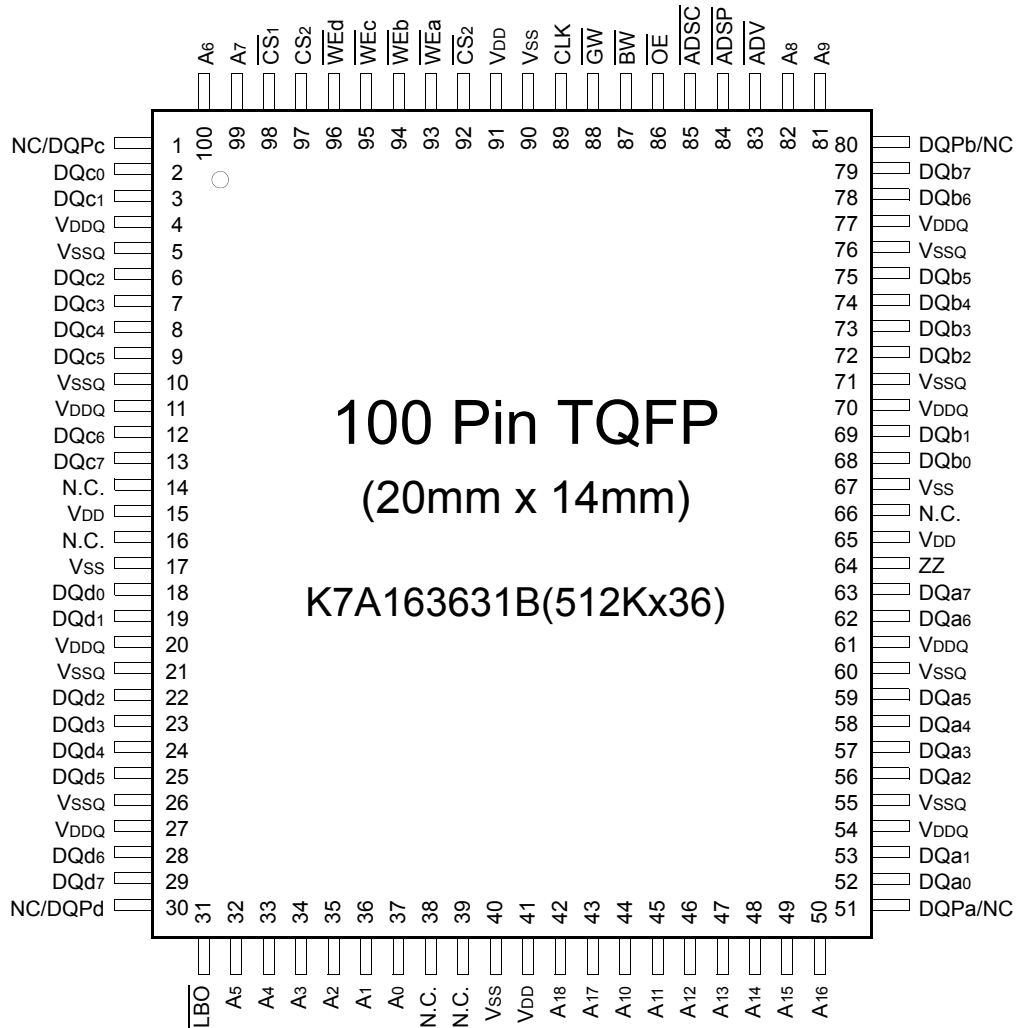
**FAST ACCESS TIMES**

PARAMETER	Symbol	-20	Unit
Cycle Time	tCYC	5.0	ns
Clock Access Time	tCD	3.1	ns
Output Enable Access Time	tOE	3.1	ns

**LOGIC BLOCK DIAGRAM**



**PIN CONFIGURATION(TOP VIEW)**

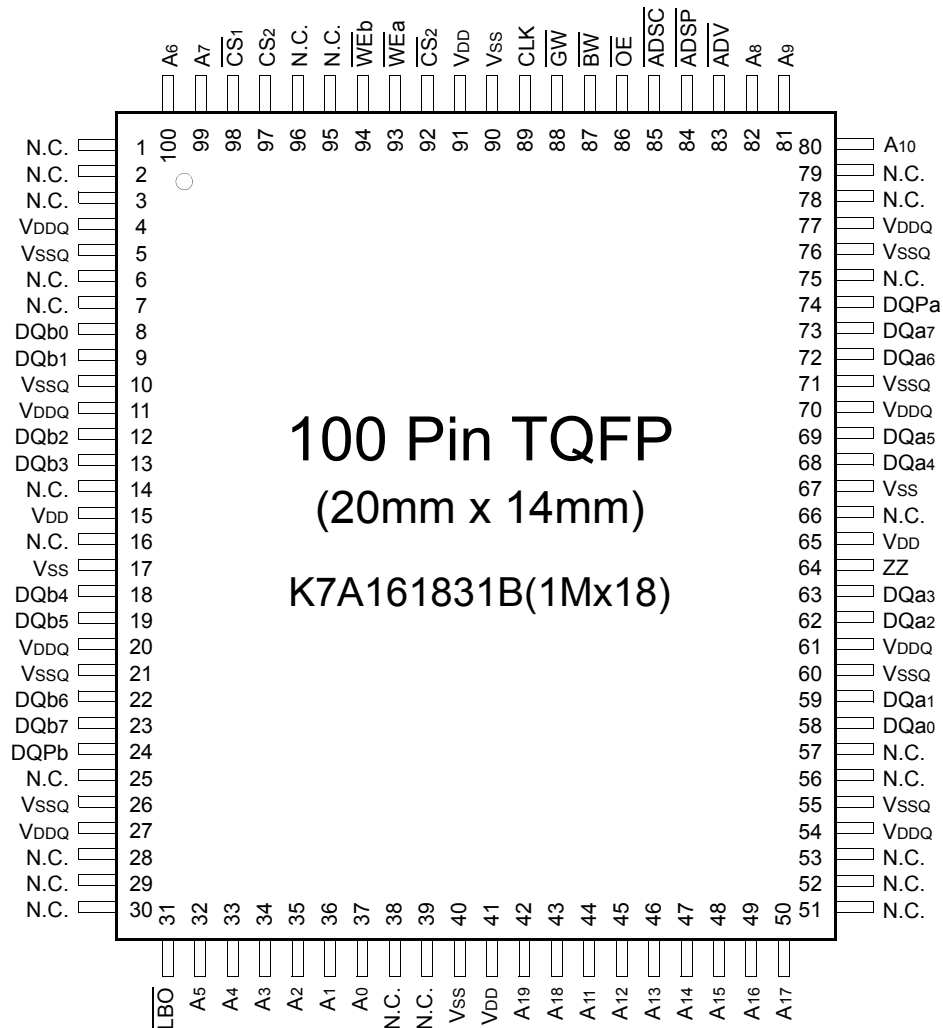


**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,42,43,44,45,46,47,48,49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
ADV	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,66
ADSP	Address Status Processor	84	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
CS2	Chip Select	92	or N.C.		
WEx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
OE	Output Enable	86	VSSQ	Output Ground	5,10,21,26,55,60,71,76
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

**Note** : 1. A<sub>0</sub> and A<sub>1</sub> are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**PIN CONFIGURATION(TOP VIEW)**



**PIN NAME**

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,42 43,44,45,46,47,48,49 50,80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	1,2,3,6,7,14,16,25,28,29 30,38,39,51,52,53,56,57 66,75,78,79,95,96
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89			
CS1	Chip Select	98	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
CS2	Chip Select	97	DQb0 ~ b7		8,9,12,13,18,19,22,23
$\overline{CS2}$	Chip Select	92	DQP a, P b		74,24
$\overline{WEx}(x=a,b)$	Byte Write Inputs	93,94			
OE	Output Enable	86	VDDQ	Output Power Supply (3.3V or 2.5V)	4,11,20,27,54,61,70,77
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

**Note :** 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

**K7A163631B  
K7A161831B**

**512Kx36 & 1Mx18 Synchronous SRAM**

**FUNCTION DESCRIPTION**

The K7A163631B and K7A161831B are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of  $\overline{OE}$ ,  $\overline{LBO}$  and  $\overline{ZZ}$ ) are sampled on rising clock edges. The start and duration of the burst access is controlled by  $\overline{ADSC}$ ,  $\overline{ADSP}$  and  $\overline{ADV}$  and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with  $\overline{ADV}$ .

When  $\overline{ZZ}$  is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When  $\overline{ZZ}$  returns to low, the SRAM normally operates after 2cycles of wake up time.  $\overline{ZZ}$  pin is pulled down internally.

Read cycles are initiated with  $\overline{ADSP}$ (regardless of  $\overline{WEX}$  and  $\overline{ADSC}$ )using the new external address clocked into the on-chip address register whenever  $\overline{ADSP}$  is sampled low, the chip selects are sampled active, and the output buffer is enabled with  $\overline{OE}$ . In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of  $\overline{CLK}$ , are carried to the Data-out buffer by the next positive edge of  $\overline{CLK}$ . The data, registered in the Data-out buffer, are projected to the output pins.  $\overline{ADV}$  is ignored on the clock edge that samples  $\overline{ADSP}$  asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when  $\overline{WEX}$  are sampled High and  $\overline{ADV}$  is sampled low. And  $\overline{ADSP}$  is blocked to control signals by disabling  $\overline{CS1}$ .

All byte write is done by  $\overline{GW}$ (regardless of  $\overline{BW}$  and  $\overline{WEX}$ ), and each byte write is performed by the combination of  $\overline{BW}$  and  $\overline{WEX}$  when  $\overline{GW}$  is high.

Write cycles are performed by disabling the output buffers with  $\overline{OE}$  and asserting  $\overline{WEX}$ .  $\overline{WEX}$  are ignored on the clock edge that samples  $\overline{ADSP}$  low, but are sampled on the subsequent clock edges. The output buffers are disabled when  $\overline{WEX}$  are sampled Low(regardless of  $\overline{OE}$ ). Data is clocked into the data input register when  $\overline{WEX}$  sampled Low. The address increases internally to the next address of burst, if both  $\overline{WEX}$  and  $\overline{ADV}$  are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals( $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$  or  $\overline{WEd}$ ) sampled low. The  $\overline{WEa}$  control  $\overline{DQa0} \sim \overline{DQa7}$  and  $\overline{DQP a}$ ,  $\overline{WEb}$  controls  $\overline{DQb0} \sim \overline{DQb7}$  and  $\overline{DQP b}$ ,  $\overline{WEc}$  controls  $\overline{DQc0} \sim \overline{DQc7}$  and  $\overline{DQP c}$ , and  $\overline{WEd}$  control  $\overline{DQd0} \sim \overline{DQd7}$  and  $\overline{DQP d}$ . Read or write cycle may also be initiated with  $\overline{ADSC}$ , instead of  $\overline{ADSP}$ . The differences between cycles initiated with  $\overline{ADSC}$  and  $\overline{ADSP}$  as are follows;

$\overline{ADSP}$  must be sampled high when  $\overline{ADSC}$  is sampled low to initiate a cycle with  $\overline{ADSC}$ .

$\overline{WEX}$  are sampled on the same clock edge that sampled  $\overline{ADSC}$  low(and  $\overline{ADSP}$  high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the  $\overline{LBO}$  pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

**BURST SEQUENCE TABLE**

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1.  $\overline{LBO}$  pin must be tied to High or Low, and Floating State must not be allowed.

**ASYNCHRONOUS TRUTH TABLE**

OPERATION	$\overline{ZZ}$	$\overline{OE}$	I/O Status
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

**Notes**

1. X means "Don't Care".
2.  $\overline{ZZ}$  pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with  $\overline{OE}$ , otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

**TRUTH TABLES**

**SYNCHRONOUS TRUTH TABLE**

$\overline{CS}_1$	$CS_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	Operation
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care".  
 2. The rising edge of clock is symbolized by ↑.  
 3.  $\overline{WRITE} = L$  means Write operation in WRITE TRUTH TABLE.  
 $\overline{WRITE} = H$  means Read operation in WRITE TRUTH TABLE.  
 4. Operation finally depends on status of asynchronous input pins(ZZ and  $\overline{OE}$ ).

**WRITE TRUTH TABLE(x36)**

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

**WRITE TRUTH TABLE(x18)**

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".  
 2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).



**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT	
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V	
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V	
Voltage on Input Pin Relative to VSS	VIN	-0.3 to VDD+0.3	V	
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.3	V	
Power Dissipation	Pd	1.6	W	
Storage Temperature	TSTG	-65 to 150	°C	
Operating Temperature	Commercial	TOPR	0 to 70	°C
	Industrial	TOPR	-40 to 85	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C	

\*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C)**

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD1	2.375	2.5	2.625	V
	VDDQ1	2.375	2.5	2.625	V
	VDD2	3.135	3.3	3.465	V
	VDDQ2	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

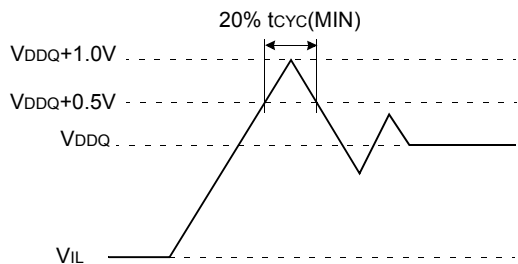
Notes: 1. The above parameters are also guaranteed at industrial temperature range.  
2. It should be VDDQ ≤ VDD

**CAPACITANCE\* (TA=25°C, f=1MHz)**

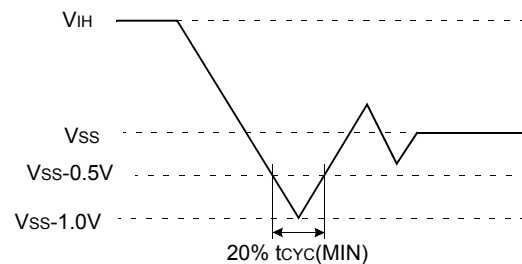
PARAMETER	SYMBOL	TEST CONDITION	Min	Max	Unit
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOUT=0V	-	6	pF

\*Note : Sampled not 100% tested.

**Overshoot Timing**



**Undershoot Timing**



**DC ELECTRICAL CHARACTERISTICS**

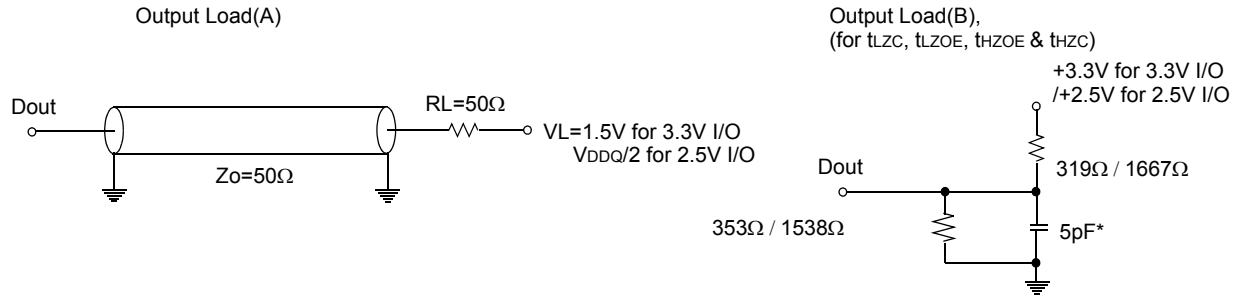
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES
Input Leakage Current(except ZZ)	IIL	VDD = Max ; VIN=VSS to VDD	-2	+2	μA	
Output Leakage Current	IOL	Output Disabled, VOUT=VSS to VDDQ	-2	+2	μA	
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ≤VIL, Cycle Time ≥ tCYC Min	-20	-	340	mA 1,2
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-20	-	170	mA
	ISB1	Device deselected, IOUT=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (VDD-0.2V or 0.2V)	-	-	150	mA
	ISB2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH	-	-	130	mA
Output Low Voltage(3.3V I/O)	VOL	IOL=8.0mA	-	0.4	V	
Output High Voltage(3.3V I/O)	VOH	IOH=-4.0mA	2.4	-	V	
Output Low Voltage(2.5V I/O)	VOL	IOL=1.0mA	-	0.4	V	
Output High Voltage(2.5V I/O)	VOH	IOH=-1.0mA	2.0	-	V	
Input Low Voltage(3.3V I/O)	VIL		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	VIH		2.0	VDD+0.3**	V	3
Input Low Voltage(2.5V I/O)	VIL		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	VIH		1.7	VDD+0.3**	V	3

- Notes :** 1. The above parameters are also guaranteed at industrial temperature range.  
 2. Reference AC Operating Conditions and Characteristics for input and timing.  
 3. Data states are all zero.  
 4. In Case of I/O Pins, the Max. VIH=VDDQ+0.3V.

**TEST CONDITIONS**

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3/2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

\* The above parameters are also guaranteed at industrial temperature range.



\* Including Scope and Jig Capacitance

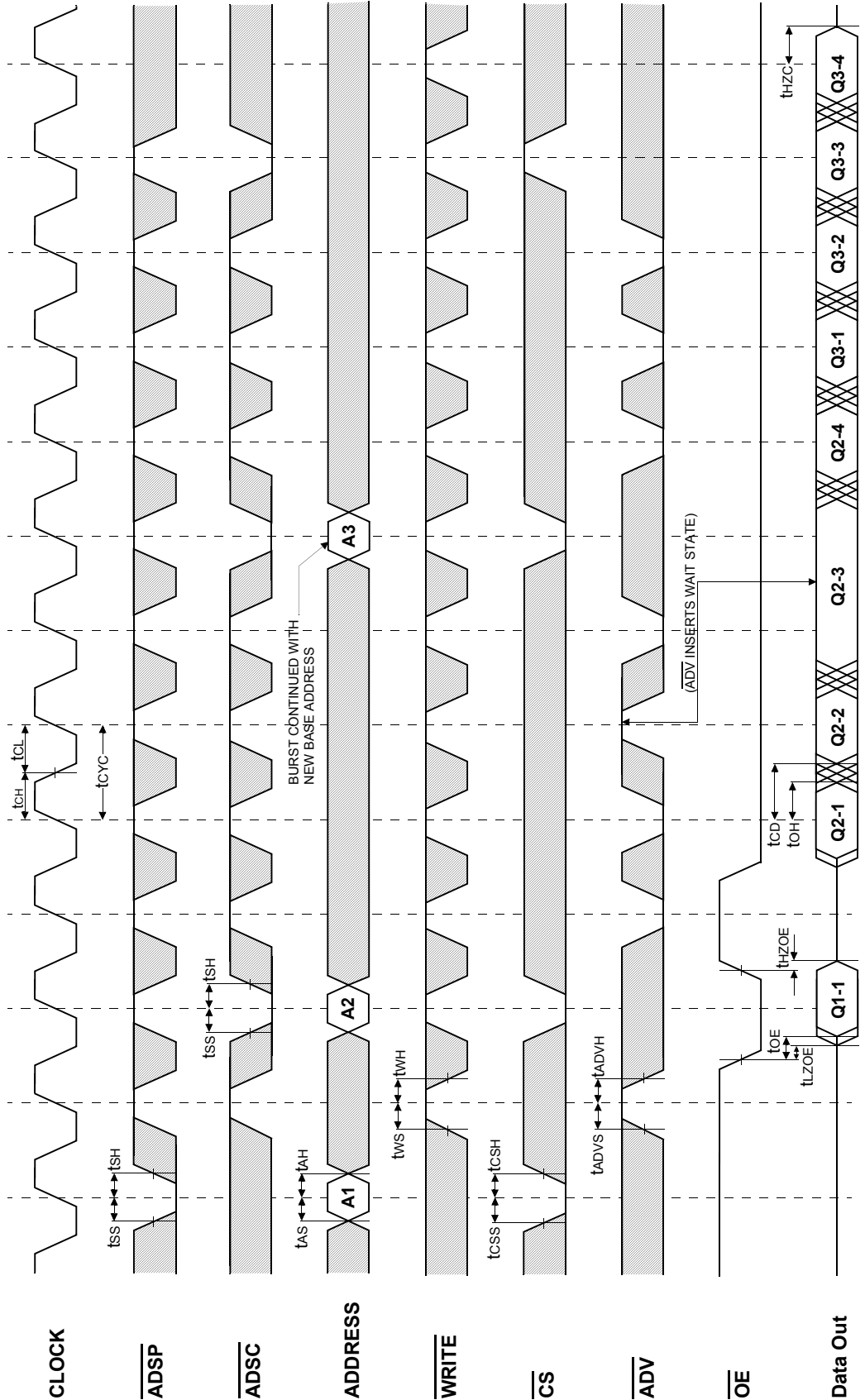
Fig. 1

**AC TIMING CHARACTERISTICS**

Parameter	Symbol	-20		Unit
		MIN	MAX	
Cycle Time	tCYC	5.0	-	ns
Clock Access Time	tCD	-	3.1	ns
Output Enable to Data Valid	tOE	-	3.1	ns
Clock High to Output Low-Z	tLZC	0	-	ns
Output Hold from Clock High	tOH	1.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.0	ns
Clock High to Output High-Z	tHZC	1.5	3.0	ns
Clock High Pulse Width	tCH	2.0	-	ns
Clock Low Pulse Width	tCL	2.0	-	ns
Address Setup to Clock High	tAS	1.4	-	ns
Address Status Setup to Clock High	tSS	1.4	-	ns
Data Setup to Clock High	tDS	1.4	-	ns
Write Setup to Clock High ( $\overline{GW}$ , $\overline{BW}$ , $\overline{WE}_x$ )	tWS	1.4	-	ns
Address Advance Setup to Clock High	tADVS	1.4	-	ns
Chip Select Setup to Clock High	tCSS	1.4	-	ns
Address Hold from Clock High	tAH	0.4	-	ns
Address Status Hold from Clock High	tSH	0.4	-	ns
Data Hold from Clock High	tDH	0.4	-	ns
Write Hold from Clock High ( $\overline{GW}$ , $\overline{BW}$ , $\overline{WE}_x$ )	tWH	0.4	-	ns
Address Advance Hold from Clock High	tADVH	0.4	-	ns
Chip Select Hold from Clock High	tCSH	0.4	-	ns
ZZ High to Power Down	tPDS	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	cycle

- Notes :**
1. The above parameters are also guaranteed at industrial temperature range.
  2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever  $\overline{ADSC}$  and/or  $\overline{ADSP}$  is sampled low and  $\overline{CS}$  is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
  3. Both chip selects must be active whenever  $\overline{ADSC}$  or  $\overline{ADSP}$  is sampled low in order for the this device to remain enabled.
  4.  $\overline{ADSC}$  or  $\overline{ADSP}$  must not be asserted for at least 2 Clock after leaving ZZ state.

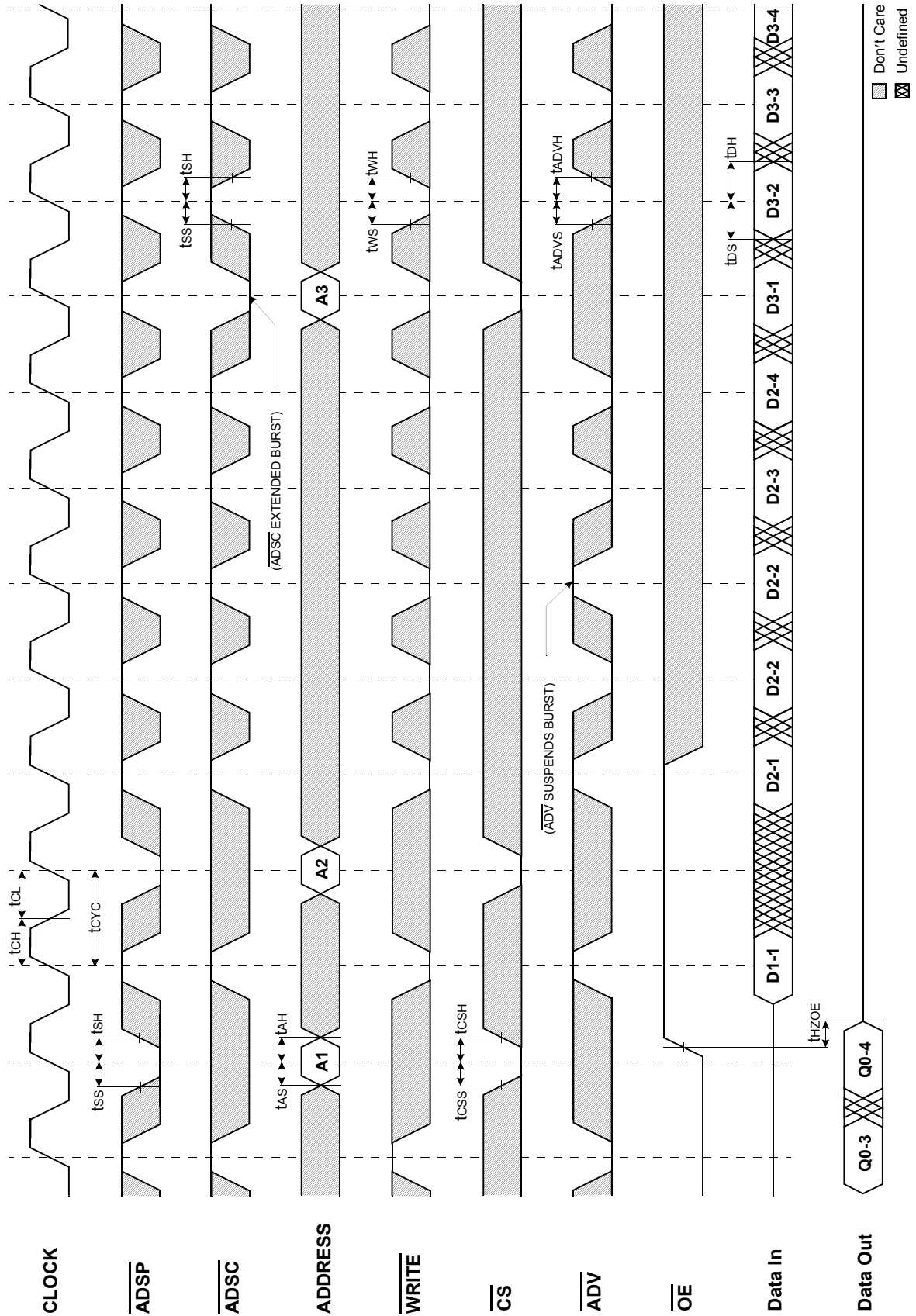
TIMING WAVEFORM OF READ CYCLE



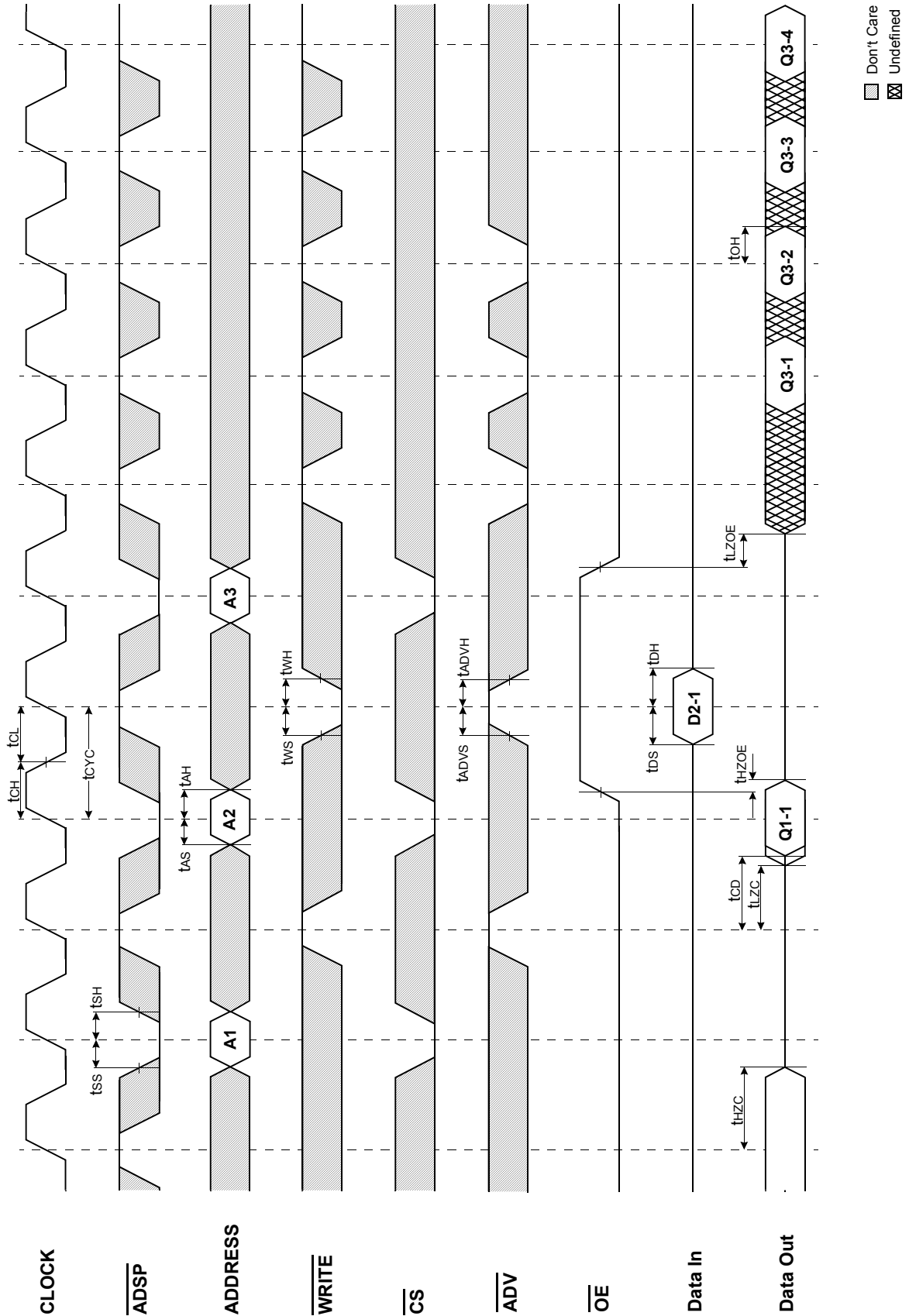
□ Don't Care  
⊗ Undefined

NOTES :  $\overline{WRITE} = L$  means  $\overline{GW} = L$ , or  $\overline{GW} = H$ ,  $\overline{BW} = L$ ,  $\overline{WEX} = L$   
 $\overline{CS} = L$  means  $\overline{CS}_1 = L$ ,  $\overline{CS}_2 = H$  and  $\overline{CS}_2 = L$   
 $\overline{CS} = H$  means  $\overline{CS}_1 = H$ , or  $\overline{CS}_1 = L$  and  $\overline{CS}_2 = H$ , or  $\overline{CS}_1 = L$ , and  $\overline{CS}_2 = L$

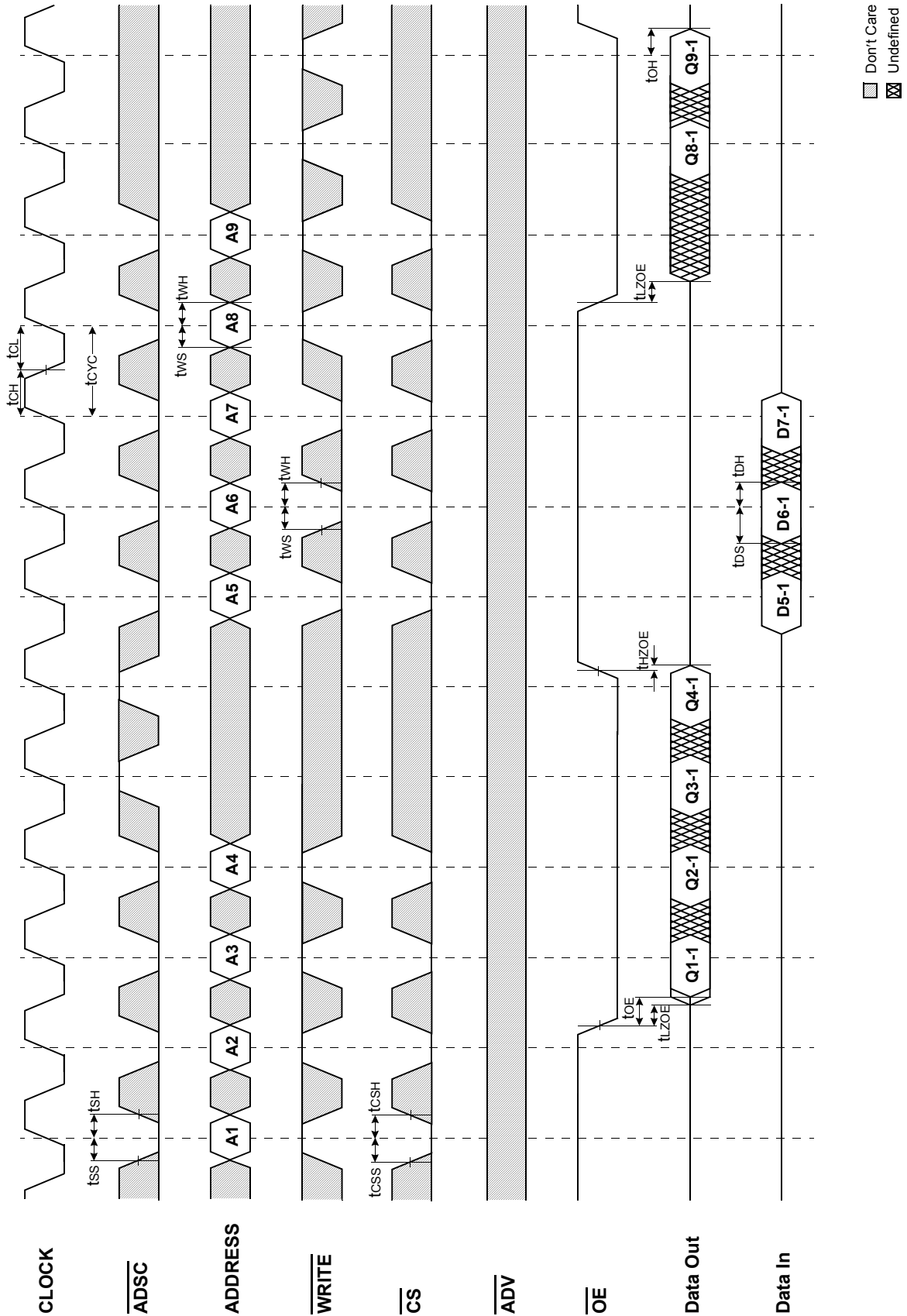
TIMING WAVEFORM OF WRTE CYCLE



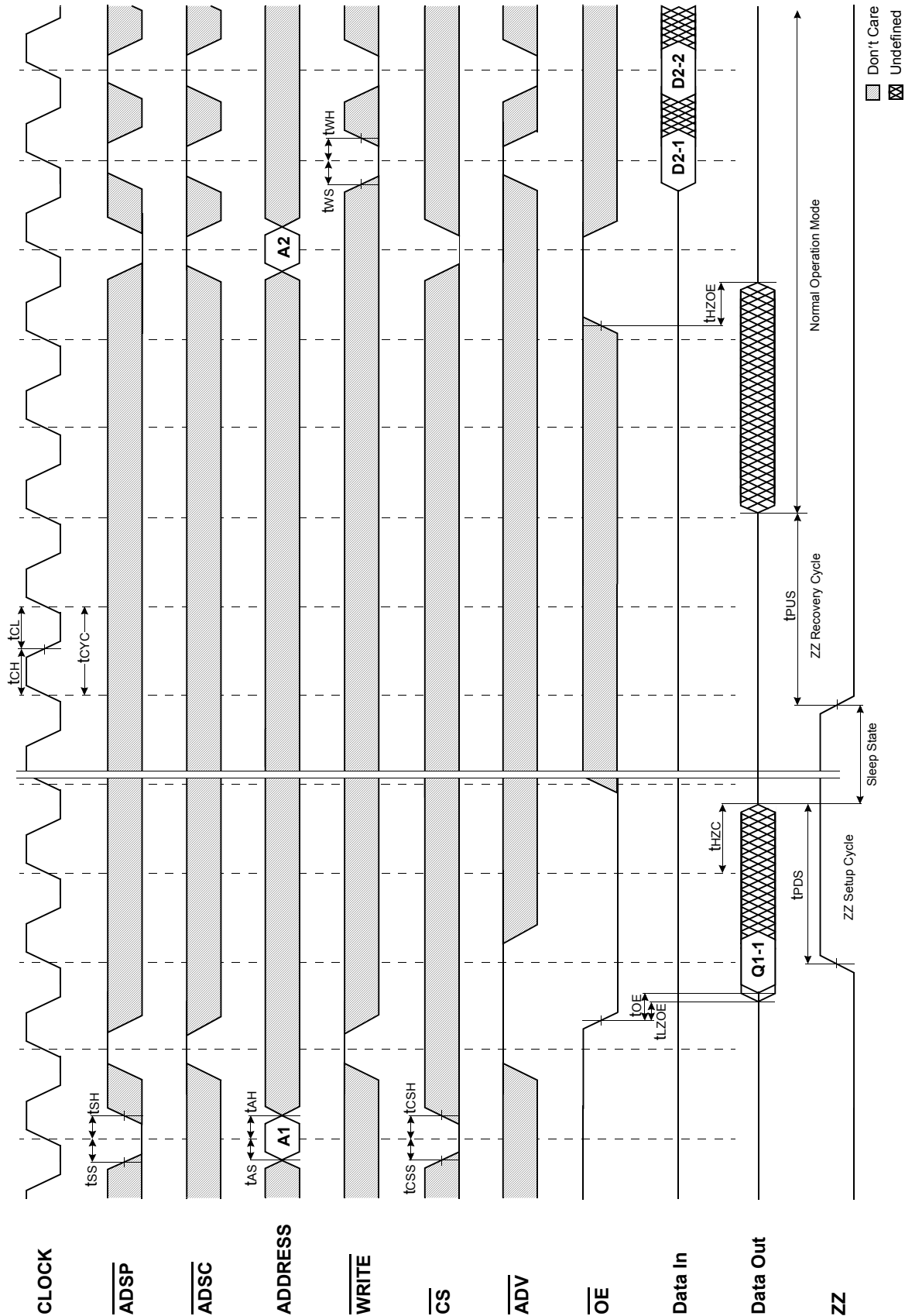
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED,  $\overline{\text{ADSC}}=\text{HIGH}$ )



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED,  $\overline{\text{ADSP}}=\text{HIGH}$ )



TIMING WAVEFORM OF POWER DOWN CYCLE

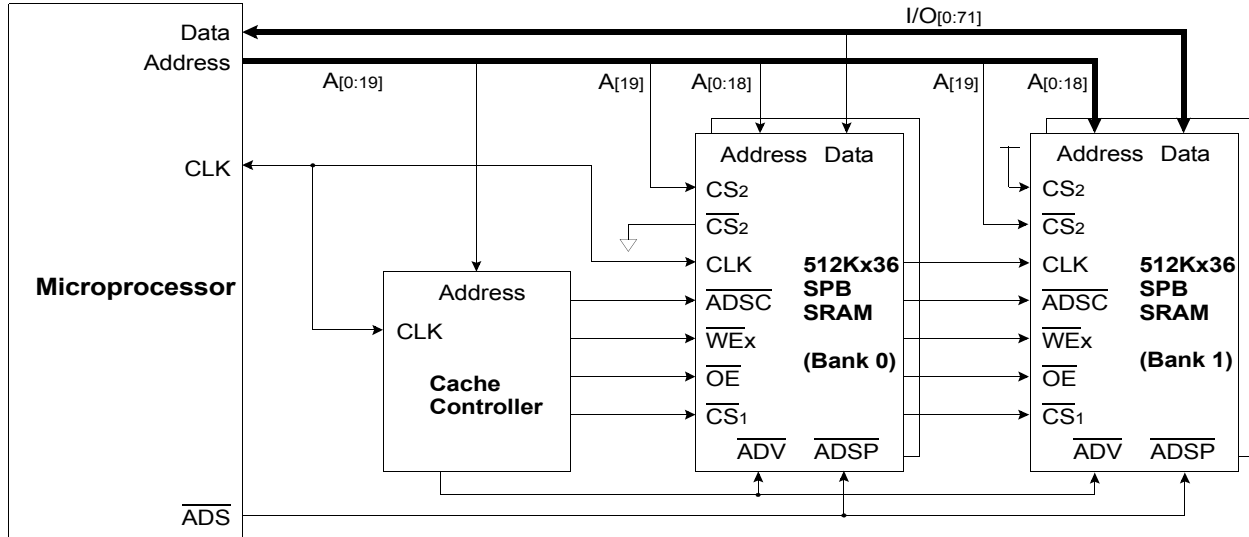




**APPLICATION INFORMATION**

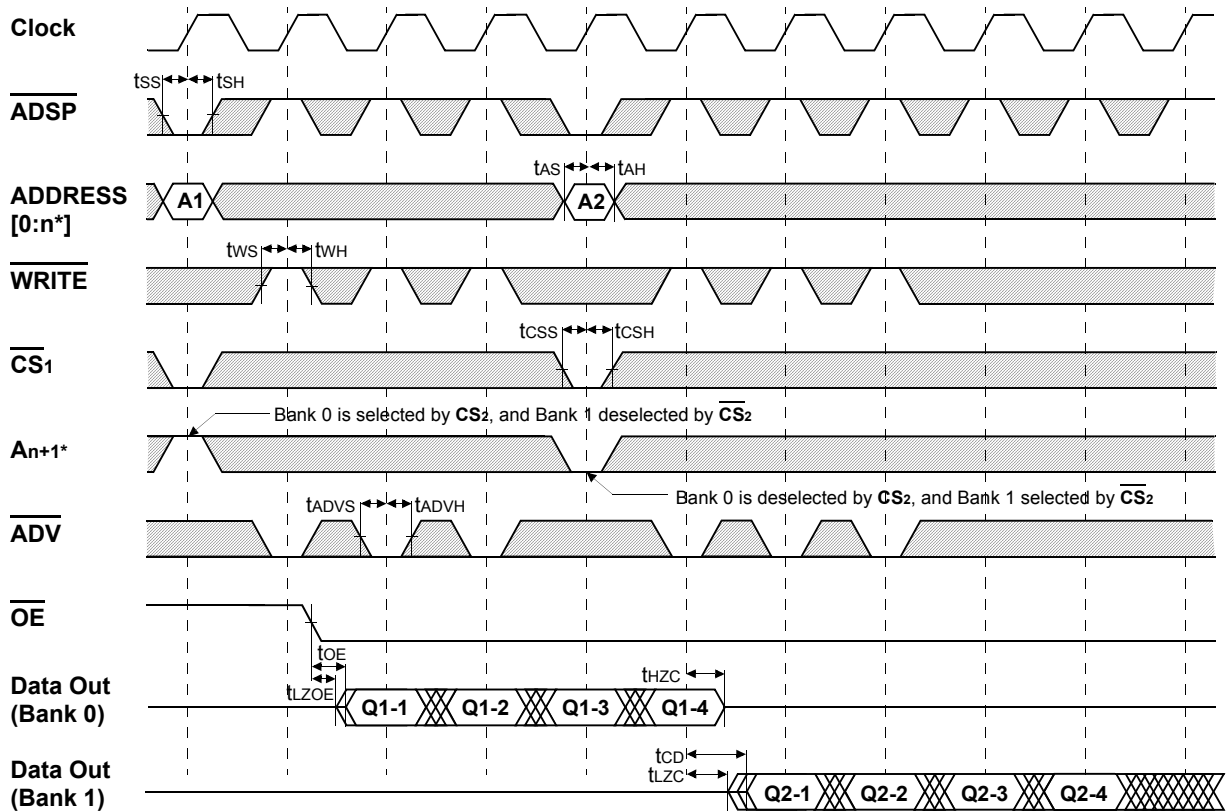
**DEPTH EXPANSION**

The Samsung 512Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 512K depth to 1M depth without extra logic.



**INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)**

**(ADSP CONTROLLED , ADSC=HIGH)**



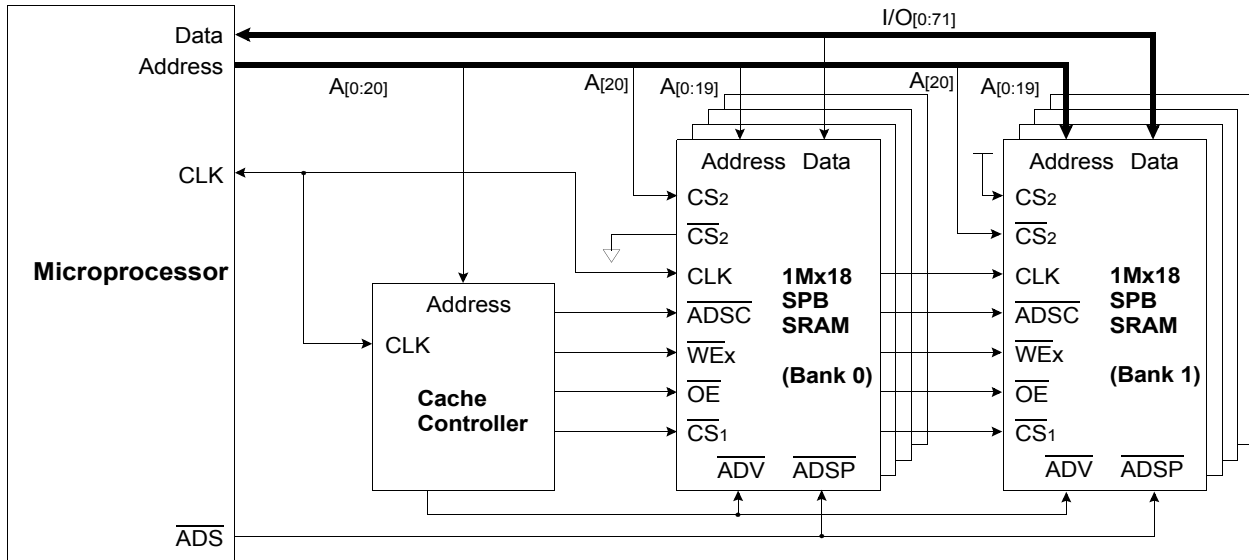
\*Notes : n = 14 32K depth , 15 64K depth  
16 128K depth , 17 256K depth  
18 512K depth , 19 1M depth

□ Don't Care    ⊗ Undefined

**APPLICATION INFORMATION**

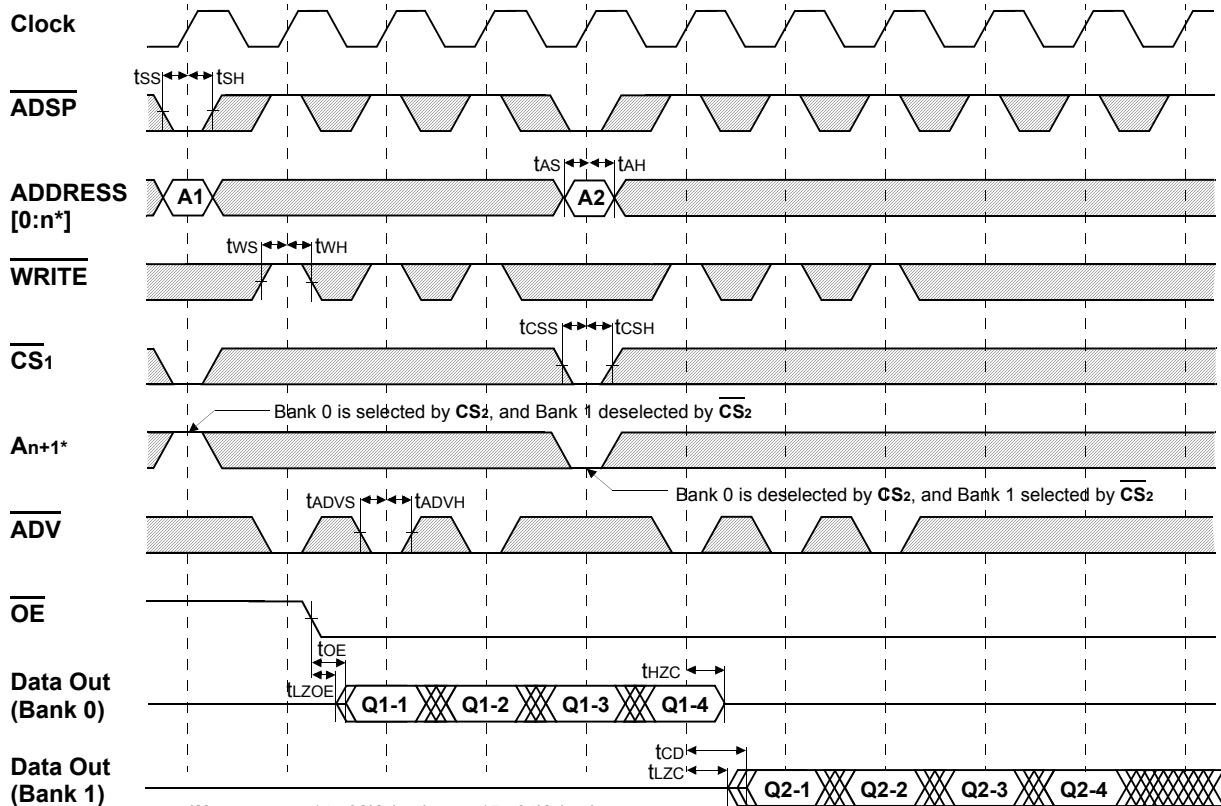
**DEPTH EXPANSION**

The Samsung 1Mx18 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



**INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)**

**( $\overline{ADSP}$  CONTROLLED ,  $\overline{ADSC}$ =HIGH)**



\*Notes : n = 14 32K depth , 15 64K depth  
 16 128K depth , 17 256K depth  
 18 512K depth , 19 1M depth  
 20 2M depth

□ Don't Care    ⊗ Undefined

PACKAGE DIMENSIONS

