36Mb Late Write SRAM Specification

119BGA with Pb & Pb-Free

(RoHS compliant)

Document Title

1Mx36 & 2Mx18 Synchronous Pipelined SRAM

Revision History

Rev. No.	History	Draft Date	Remark
Rev. 0.0	1. Initial Document	Dec. 2005	Advance
Rev. 0.1	1. Change V_{DD} range : from 1.8~2.5V to 1.8 or 2.5V	Jan. 2006	Preliminary
Rev. 0.2	1. Put the data in the table of DC Characteristics, Pin Capacitance and Thermal Resistance.	Apr. 2006	Preliminary
Rev. 0.3	1. Change Samsung JEDEC Code in ID REGISTER DEFINITION	Jun. 2006	Preliminary
Rev. 1.0	1. Correct typo	Aug. 2006	Final
Rev. 1.1	1. Change Max. V_{REF} and V_{CM}-CLK from 0.9V to 0.95V in recommended DC operating conditions.	Dec. 2006	Final
Rev. 1.2	1. Change V_{OH} in JTAG DC OPERATING CONDITION	Feb. 2007	Final

1Mx36 & 2Mx18 Synchronous Pipelined SRAM

FEATURES

- 1Mx36 or 2Mx18 Organizations.
- 1.8 or 2.5V V_{DD}/1.5V ~1.8V_{DDQ}.
- HSTL Input and Output Levels.
- Differential, HSTL Clock Inputs K, $\overline{K}$.
- Synchronous Read and Write Operation
- Registered Input and Registered Output
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- Programmable Impedance Output Drivers.
- JTAG 1149.1 Compatible Test Access port.
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm).

GENERAL DESCRIPTION

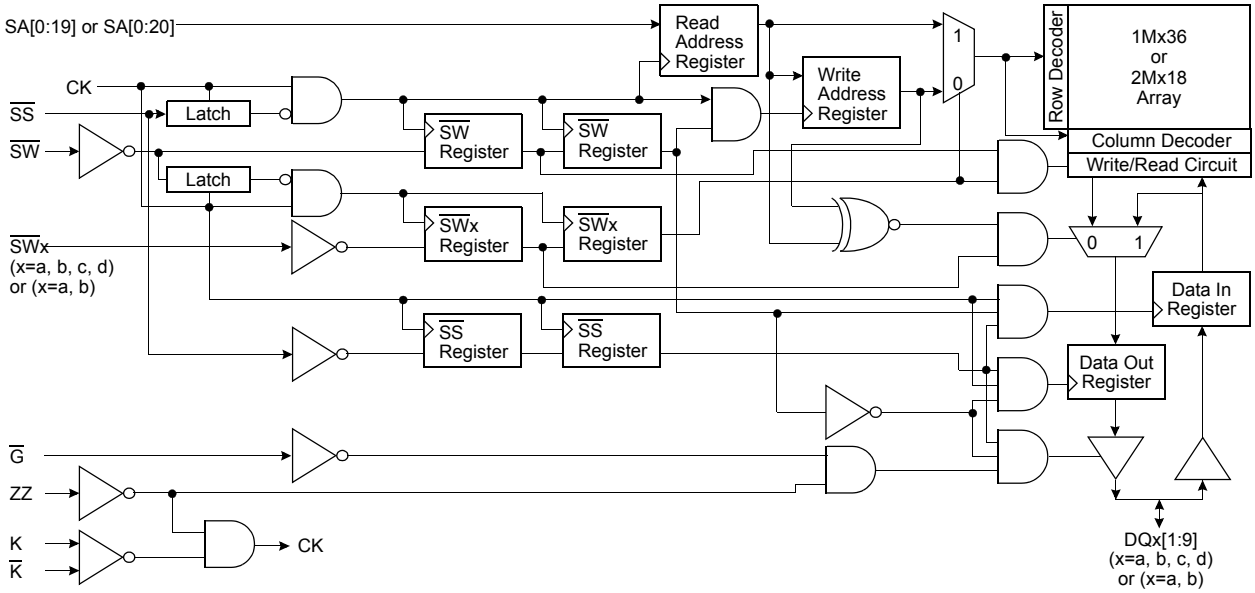
The K7P323674C and K7P321874C are 37,748,736 bit Synchronous Pipeline Mode SRAM. It is organized as 1,048,576 words of 36 bits(or 2,097,152 words of 18 bits)and is implemented in SAMSUNG′s advanced CMOS technology.
Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, All addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers edge of the next rising edge of the K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

ORDERING INFORMATION

Org.	Maximum Frequency	Access Time	VDD	Part Number
1Mx36	300MHz	1.6	2.5V	K7P323674C-H(G)[1]C30
	250MHz	2.0	1.8 / 2.5V	K7P323674C-H(G)[1]C25
2Mx18	300MHz	1.6	2.5V	K7P321874C-H(G)[1]C30
	250MHz	2.0	1.8 / 2.5V	K7P321874C-H(G)[1]C25

Note 1 : H(G) [Package type] : G-Pb Free, H-Pb
2 : 300MHz is supported only at 2.5V V_{DD}. 250MHz is the maximum speed at 1.8V V_{DD}

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	V_{REF}	HSTL Input Reference Voltage
SAn	Synchronous Address Input	M_1, M_2	Read Protocol Mode Pins (M_1=V_{SS}, M_2=V_{DDQ})
DQn	Bi-directional Data Bus	$\overline{G}$	Asynchronous Output Enable
$\overline{SW}$	Synchronous Global Write Enable	$\overline{SS}$	Synchronous Select
$\overline{SW}$a	Synchronous Byte a Write Enable	TCK	JTAG Test Clock
$\overline{SW}$b	Synchronous Byte b Write Enable	TMS	JTAG Test Mode Select
$\overline{SW}$c	Synchronous Byte c Write Enable	TDI	JTAG Test Data Input
$\overline{SW}$d	Synchronous Byte d Write Enable	TDO	JTAG Test Data Output
ZZ	Asynchronous Power Down	ZQ	Output Driver Impedance Control
V_{DD}	Core Power Supply	V_{SS}	GND
V_{DDQ}	Output Power Supply	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P323674C(1Mx36)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	SA	SA	SA	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	V_{SS}	ZQ	V_{SS}	DQb	DQb
E	DQc	DQc	V_{SS}	$\overline{SS}$	V_{SS}	DQb	DQb
F	V_{DDQ}	DQc	V_{SS}	$\overline{G}$	V_{SS}	DQb	V_{DDQ}
G	DQc	DQc	$\overline{SW}$c	NC	$\overline{SW}$b	DQb	DQb
H	DQc	DQc	V_{SS}	NC	V_{SS}	DQb	DQb
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	DQd	DQd	V_{SS}	K	V_{SS}	DQa	DQa
L	DQd	DQd	$\overline{SW}$d	$\overline{K}$	$\overline{SW}$a	DQa	DQa
M	V_{DDQ}	DQd	V_{SS}	$\overline{SW}$	V_{SS}	DQa	V_{DDQ}
N	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
P	DQd	DQd	V_{SS}	SA	V_{SS}	DQa	DQa
R	NC	SA	M_1	V_{DD}	M_2	SA_2	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

K7P321874C(2Mx18)

	1	2	3	4	5	6	7
A	V_{DDQ}	SA	SA	NC	SA	SA	V_{DDQ}
B	NC	SA	SA	SA	SA	SA	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	NC	V_{SS}	ZQ	V_{SS}	DQa	NC
E	NC	DQb	V_{SS}	$\overline{SS}$	V_{SS}	NC	DQa
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQa	V_{DDQ}
G	NC	DQb	$\overline{SW}$b	NC	NC	NC	DQa
H	DQb	NC	V_{SS}	NC	V_{SS}	DQa	NC
J	V_{DDQ}	V_{DD}	V_{REF}	V_{DD}	V_{REF}	V_{DD}	V_{DDQ}
K	NC	DQb	V_{SS}	K	V_{SS}	NC	DQa
L	DQb	NC	NC	$\overline{K}$	$\overline{SW}$a	DQa	NC
M	V_{DDQ}	DQb	V_{SS}	$\overline{SW}$	V_{SS}	NC	V_{DDQ}
N	DQb	NC	V_{SS}	SA	V_{SS}	DQa	NC
P	NC	DQb	V_{SS}	SA	V_{SS}	NC	DQa
R	NC	SA	M_1	V_{DD}	M_2	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}

Read Operation

During reads, the address is registered during the frist clock edge, the internal array is read between this first edge and the second edge, and data is captured in the output register and driven to the CPU during the second clock edge. $\overline{SS}$ is driven low during this cycle, signaling that the SRAM should drive out the data.
During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and $\overline{SW}$ are sampled on the clock rising edge. $\overline{SW}$ is low on the rising clock. Write data is sampled on the rising clock, one cycle after write address and $\overline{SW}$ have been sampled by the SRAM. $\overline{SS}$ will be driven low during the same cycle that the Address, $\overline{SW}$ and $\overline{SW}$[a:d] are valid to signal that a valid operation is on the Address and Control Input.
Pipelined write are supported. This is done by using write data buffers on the SRAM that capture the write addresses on one write cycle, and write the array on the next write cycle. The "next write cycle" can actually be many cycles away, broken by a series of read cycles. Byte writes are supported. The byte write signals $\overline{SW}$[a:d] signal which 9-bit bytes will be writen. Timing of $\overline{SW}$[a:d] is the same as the $\overline{SW}$ signal.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address Latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array. The bypassing of the SRAM array occurs on a byte by byte basis. If one byte is written and the other bytes are not, read data from the last written will have new byte data from the write data buffer and the other bytes from the SRAM array.

Programmable Impedance Output Buffer Operation

This HSTL Late Write SRAM has been designed with programmable impedance output buffers. The SRAMs output buffer impedance can be adjusted to match the system data bus impedance, by connecting a external resistor (RQ) between the ZQ pin of the SRAM and V_{SS}. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. For example, a 250Ω resistor will give an output buffer impedance of 50Ω. The allowable range of RQ is from 175Ω to 350Ω. Internal circuits evaluate and periodically adjust the output buffer impedance, as the impedance is affected by drifts in supply voltage and temperature. One evaluation occurs every 32 clock cycles, with each evaluation moving the output buffer impedance level only one step at a time toward the optimum level. Impedance updates occur when the SRAM is in High-Z state, and thus are triggered by write and deselect operations. Updates will also be triggered with G HIGH initiated High-Z state, providing the specified G setup and hold times are met. Impedance match is not instantaneous upon power-up. In order to guarantee optimum output driver impedance, the SRAM requires a minimum number of non-read cycles (1,024) after power-up. The output buffers can also be programmed in a minimum impedance configuration by connecting ZQ to V_{SS} or V_{DDQ}.

Mode Control

There are two mode control select pins (M_1 and M_2) used to set the proper read protocol. This SRAM supports single clock pipelined operating mode. For proper specified device operation, M_1 must be connected to V_{SS} and M_2 must be connected to V_{DDQ}. These mode pins must be set at power-up and must not change during device operation.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

Sleep Mode

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin high. During sleep mode, all other inputs are ignored and outputs are brought to a High-Impedance state. Sleep mode current and output High-Z are guaranteed after the specified sleep mode enable time. During sleep mode the memory array data content is preserved. Sleep mode must not be initiated until after all pending operations have completed, as any pending operation is not guaranteed to properly complete after sleep mode is initiated. Normal operations can be resumed by bringing the ZZ pin low, but only after the specified sleep mode recovery time.

TRUTH TABLE

K	ZZ	$\overline{G}$	$\overline{SS}$	$\overline{SW}$	$\overline{SWa}$	$\overline{SWb}$	$\overline{SWc}$	$\overline{SWd}$	DQa	DQb	DQc	DQd	Operation
X	H	X	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Power Down Mode. No Operation
X	L	H	X	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled.
↑	L	L	H	X	X	X	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Output Disabled. No Operation
↑	L	L	L	H	X	X	X	X	DOUT	DOUT	DOUT	DOUT	Read Cycle
↑	L	X	L	L	H	H	H	H	Hi-Z	Hi-Z	Hi-Z	Hi-Z	No Bytes Written
↑	L	X	L	L	L	H	H	H	DIN	Hi-Z	Hi-Z	Hi-Z	Write first byte
↑	L	X	L	L	H	L	H	H	Hi-Z	DIN	Hi-Z	Hi-Z	Write second byte
↑	L	X	L	L	H	H	L	H	Hi-Z	Hi-Z	DIN	Hi-Z	Write third byte
↑	L	X	L	L	H	H	H	L	Hi-Z	Hi-Z	Hi-Z	DIN	Write fourth byte
↑	L	X	L	L	L	L	L	L	DIN	DIN	DIN	DIN	Write all bytes

NOTE : K & $\overline{K}$ are complementary

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to VSS	VDD	-0.5 to 3.13	V
Output Supply Voltage Relative to VSS	VDDQ	-0.5 to 2.4	V
Voltage on any I/O pin Relative to VSS	VIN	-0.5 to VDDQ+0.5 (2.4V MAX)	V
Output Short-Circuit Current	IOUT	25	mA
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature	TSTG	-55 to 125	°C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD1	2.37	2.5	2.63	V	7
	VDD2	1.7	1.8	1.9	V	7
Output Power Supply Voltage	VDDQ	1.4	1.5	1.9	V	
Input High Level	VIH	VREF+0.1	-	VDDQ+0.3	V	1, 2
Input Low Level	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.6	VDDQ/2	0.95	V	
Clock Input Signal Voltage	VIN-CLK	-0.3	-	VDDQ+0.3	V	1, 4
Clock Input Differential Voltage	VDIF-CLK	0.1	-	VDDQ+0.6	V	1, 5
Clock Input Common Mode Voltage	VCM-CLK	0.6	0.75	0.95	V	1, 6

NOTE : 1. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.
2. VIH (Max)DC=VDDQ+0.3, VIH (Max)AC=VDDQ+0.85V(pulse width ≤ 3ns).
3. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.5V(pulse width ≤ 3ns).
4. VIN-CLK specifies the maximum allowable DC level for the differential clock. i.e VIL-CLK and VIH-CLK.
5. VDIF-CLK specifies the minimum Clock differential voltage required for switching. i.e DC voltage difference between VIL-CLK and VIH-CLK.
6. VCM-CLK specifies the Clock crossing point for the differential clock or the allowable common clock level for a single ended clock
7. This device support both 250MHz and 300MHz frequency at VDD1. and support only 250MHz frequency at VDD2.

PIN CAPACITANCE

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	4	pF
Data Output Capacitance	C_{OUT}	V_{OUT}=0V	-	5	pF
Clock Capacitance	C_{CLK}	V_{CLK}=0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=1MHz)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current-x36 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD30} I_{DD25}	-	620 550	mA	1, 2
Average Power Supply Operating Current-x18 (V_{IN}=V_{IH} or V_{IL}, ZZ & $\overline{SS}$=V_{IL})	I_{DD30} I_{DD25}	-	570 500	mA	1, 2
Power Supply Standby Current (V_{IN}=V_{IH} or V_{IL}, ZZ=V_{IH})	I_{SBZZ}	-	70	mA	1
Active Standby Power Supply Current (V_{IN}=V_{IH} or V_{IL}, $\overline{SS}$=V_{IH}, ZZ=V_{IL})	I_{SBSS}	-	200	mA	1
Input Leakage Current (V_{IN}=V_{SS} or V_{DDQ})	I_{LI}	-1	1	μA	
Output Leakage Current (V_{OUT}=V_{SS} or V_{DDQ}, DQ in High-Z)	I_{LO}	-1	1	μA	
Output High Voltage(Programmable Impedance Mode)	V_{OH1}	V_{DDQ}/2	V_{DDQ}	V	3,5
Output Low Voltage(Programmable Impedance Mode)	V_{OL1}	V_{SS}	V_{DDQ}/2	V	4,5
Output High Voltage(I_{OH}=-0.1mA)	V_{OH2}	V_{DDQ}-0.2	V_{DDQ}	V	6
Output Low Voltage(I_{OL}=0.1MA)	V_{OL2}	V_{SS}	0.2	V	6
Output High Voltage(I_{OH}=-6mA)	V_{OH3}	V_{DDQ}-0.4	V_{DDQ}	V	6
Output Low Voltage(I_{OL}=6mA)	V_{OL3}	V_{SS}	0.4	V	6

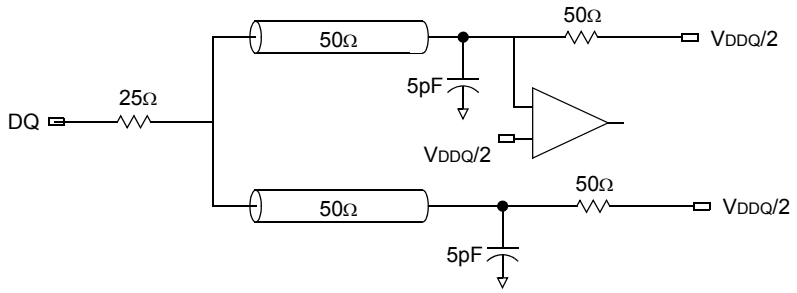
NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.
3. $|I_{OH}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ @V_{OH}=V_{DDQ}/2 for $175\Omega \le RQ \le 350\Omega$.
4. $|I_{OL}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ @V_{OL}=V_{DDQ}/2 for $175\Omega \le RQ \le 350\Omega$.
5. Programmable Impedance Output Buffer Mode. The ZQ pin is connected to V_{SS} through RQ.
6. Minimum Impedance Output Buffer Mode. The ZQ pin is connected to V_{SS} or V_{DD}.

AC TEST CONDITIONS (T_A=0 ~ 70°C, V_{DD}=1.7 ~ 1.9V and 2.37 ~ 2.63V, V_{DDQ}=1.4~1.9V)

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	V_{DD}	1.7~1.9 and 2.37~2.63	V
Output Power Supply Voltage	V_{DDQ}	1.4~1.9	V
Input High/Low Level	V_{IH}/V_{IL}	$V_{DDQ}/2 \pm 0.5$	V
Input Reference Level	V_{REF}	$V_{DDQ}/2$	V
Input Rise/Fall Time	T_R/T_F	0.5/0.5	ns
Input and Out Timing Reference Level		$V_{DDQ}/2$	V
Clock Input Timing Reference Level		Cross Point	V

NOTE : Parameters are tested with RQ=250Ω and V_{DDQ}=1.5V.

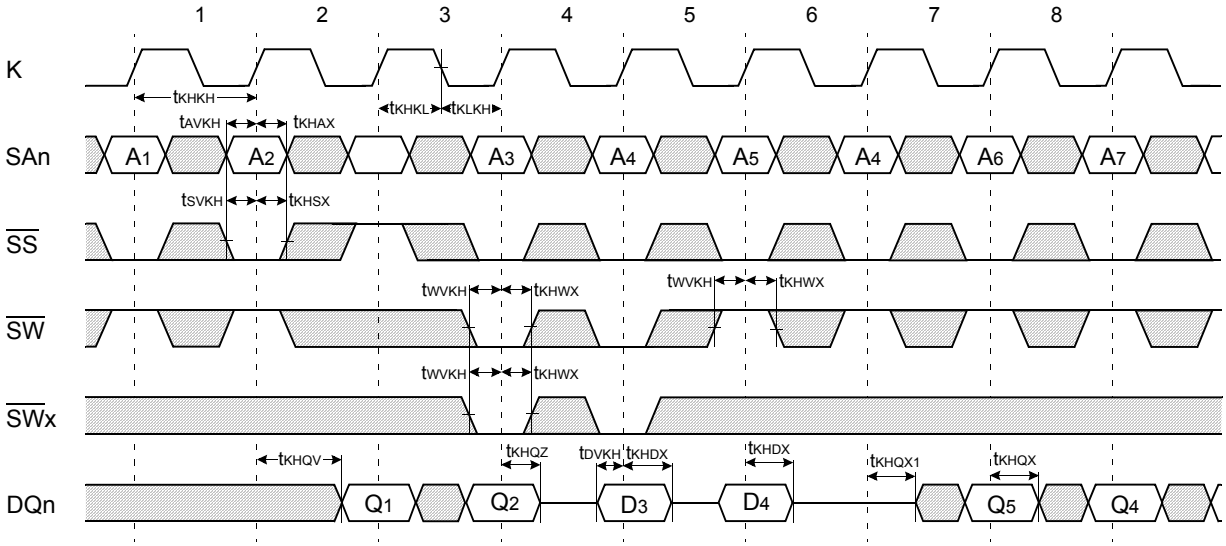
AC TEST OUTPUT LOAD



AC CHARACTERISTICS

Parameter	Symbol	-30		-25		Unit	Note
		2.5V V_{DD} Only		1.8V / 2.5V V_{DD}			
		Min	Max	Min	Max		
Clock Cycle Time	t_{KHKH}	3.3	-	4.0	-	ns	
Clock High Pulse Width	t_{KHKL}	1.3	-	1.6	-	ns	
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.6	-	ns	
Clock High to Output Valid	t_{KHQV}	-	1.6	-	2.0	ns	
Clock High to Output Hold	t_{KHQX}	0.5	-	0.5	-	ns	
Address Setup Time	t_{AVKH}	0.3	-	0.3	-	ns	
Address Hold Time	t_{KHAX}	0.5	-	0.5	-	ns	
Write Data Setup Time	t_{DVKH}	0.3	-	0.3	-	ns	
Write Data Hold Time	t_{KHDX}	0.5	-	0.5	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Setup Time	t_{WVKH}	0.3	-	0.3	-	ns	
$\overline{SW}$, $\overline{SW}$[a:d] Hold Time	t_{KHWX}	0.5	-	0.5	-	ns	
$\overline{SS}$ Setup Time	t_{SVKH}	0.3	-	0.3	-	ns	
$\overline{SS}$ Hold Time	t_{KHSX}	0.5	-	0.5	-	ns	
Clock High to Output Hi-Z	t_{KHQZ}	-	1.6	-	2.0	ns	
Clock High to Output Low-Z	t_{KHQX1}	0.5	-	0.5	-	ns	
$\overline{G}$ High to Output High-Z	t_{GHQZ}	-	1.6	-	2.0	ns	
$\overline{G}$ Low to Output Low-Z	t_{GLQX}	0.5	-	0.5	-	ns	
$\overline{G}$ Low to Output Valid	t_{GLQV}	-	1.6	-	2.0	ns	
ZZ High to Power Down(Sleep Time)	t_{ZZE}	-	15	-	15	ns	
ZZ Low to Recovery(Wake-up Time)	t_{ZZR}	-	20	-	20	ns	

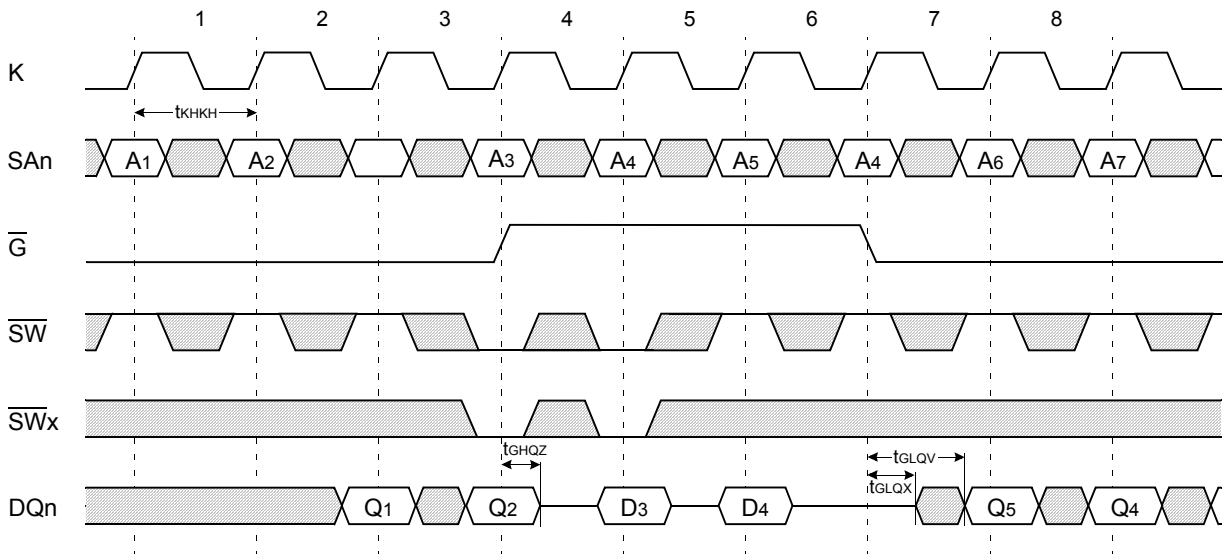
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ($\overline{SS}$ Controlled, $\overline{G}$=Low)



NOTE

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A_4 being a match from the last write cycle address.

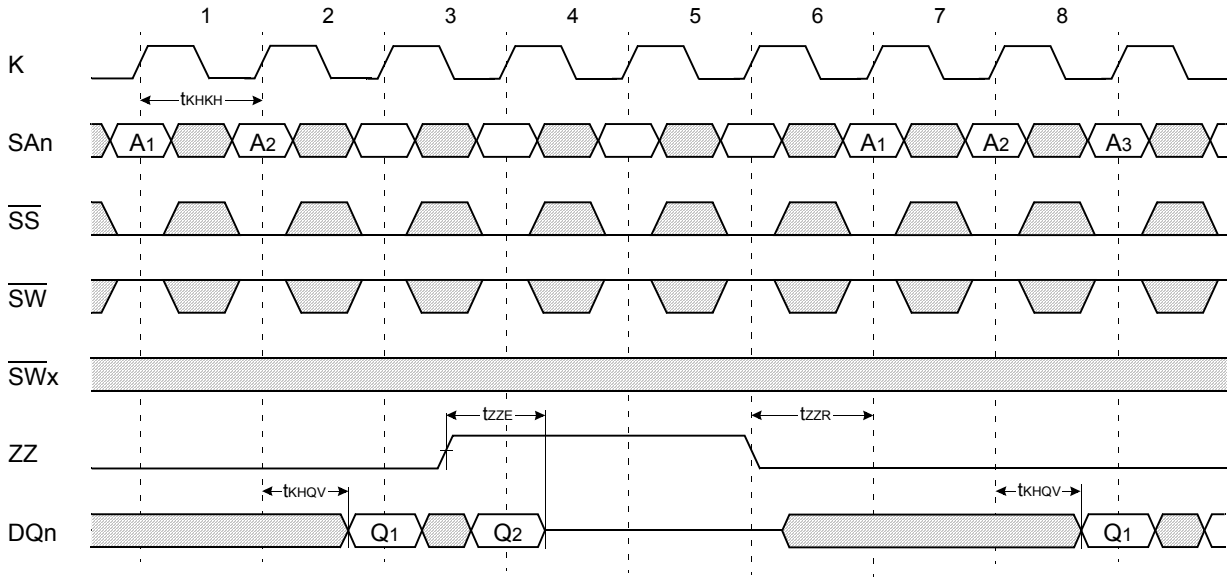
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES ($\overline{G}$ Controlled, $\overline{SS}$=Low)



NOTE

1. D_3 is the input data written in memory location A_3.
2. Q_4 is the output data read from the write data buffer(not from the cell array), as a result of address A4 being a match from the last write cycle address.

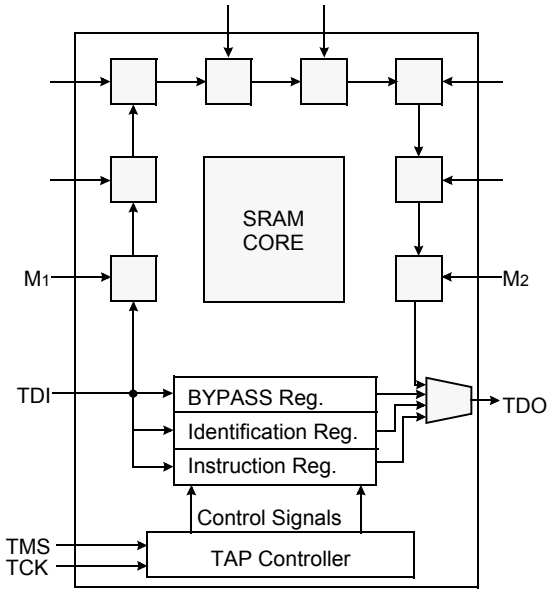
TIMING WAVEFORMS OF STANDBY CYCLES



IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Teat Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



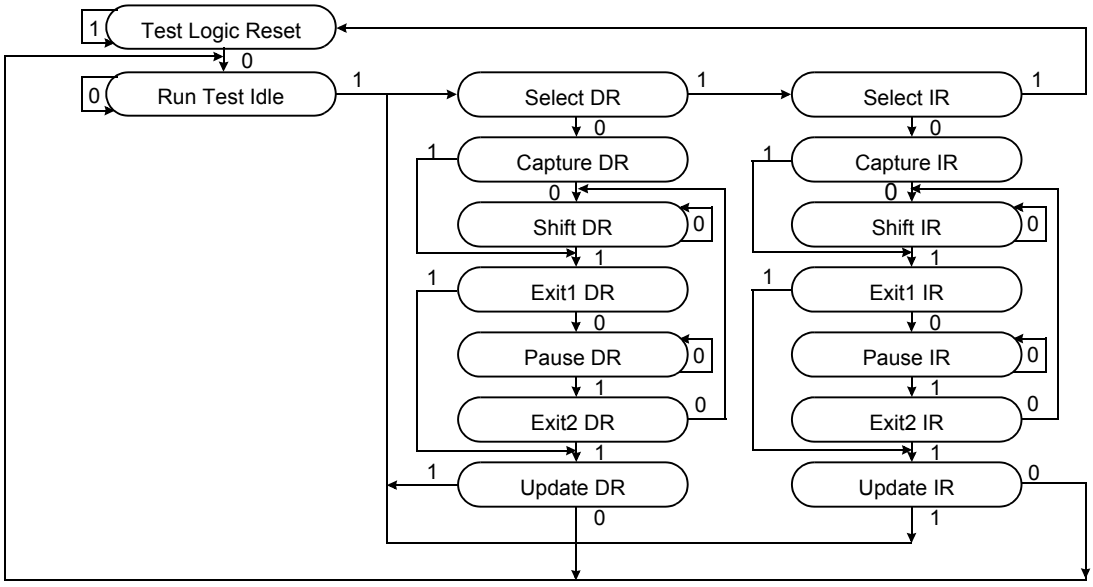
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	PRIVATE		5
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction dose not places DQs in Hi-Z.
5. PRIVATE is reserved for the exclusive use of SAMSUNG. This instruction should not be used.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1Mx36	3 bits	1 bits	32 bits	70 bits
2Mx18	3 bits	1 bits	32 bits	51 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
1Mx36	0000	01000 00100	XXXXXX	00011001110	1
2Mx18	0000	01001 00011	XXXXXX	00011001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	3B	SA		SA	5B	35
37	2B	SA		SA	6B	34
38	3A	SA		SA	5A	33
39	3C	SA		SA	5C	32
40	2C	SA		SA	6C	31
41	2A	SA		SA	6A	30
42	2D	DQc_9		DQb_9	6D	29
43	1D	DQc_8		DQb_8	7D	28
44	2E	DQc_7		DQb_7	6E	27
45	1E	DQc_6		DQb_6	7E	26
46	2F	DQc_5		DQb_5	6F	25
47	2G	DQc_4		DQb_4	6G	24
48	1G	DQc_3		DQb_3	7G	23
49	2H	DQc_2		DQb_2	6H	22
50	1H	DQc_1		DQb_1	7H	21
51	3G	$\overline{SW}c$		$\overline{SW}b$	5G	20
52	4D	ZQ		$\overline{G}$	4F	19
53	4E	$\overline{SS}$		K	4K	18
54	4B	SA		$\overline{K}$	4L	17
55	4H	NC*1		$\overline{SW}a$	5L	16
56	4M	$\overline{SW}$		DQa_1	7K	15
57	3L	$\overline{SW}d$		DQa_2	6K	14
58	1K	DQd_1		DQa_3	7L	13
59	2K	DQd_2		DQa_4	6L	12
60	1L	DQd_3		DQa_5	6M	11
61	2L	DQd_4		DQa_6	7N	10
62	2M	DQd_5		DQa_7	6N	9
63	1N	DQd_6		DQa_8	7P	8
64	2N	DQd_7		DQa_9	6P	7
65	1P	DQd_8		ZZ	7T	6
66	2P	DQd_9		SA	5T	5
67	3T	SA		SA	6R	4
68	2R	SA		SA	4T	3
69	4N	SA		SA	4P	2
70	3R	M_1		M_2	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	3B	SA		SA	5B	25
27	2B	SA		SA	6B	24
28	3A	SA		SA	5A	23
29	3C	SA		SA	5C	22
30	2C	SA		SA	6C	21
31	2A	SA		SA	6A	20
				DQa_9	6D	19
32	1D	DQb_1				
33	2E	DQb_2				
				DQa_8	7E	18
				DQa_7	6F	17
34	2G	DQb_3				
				DQa_6	7G	16
				DQa_5	6H	15
35	1H	DQb_4				
36	3G	$\overline{SW}b$				
37	4D	ZQ		$\overline{G}$	4F	14
38	4E	$\overline{SS}$		K	4K	13
39	4B	SA		$\overline{K}$	4L	12
40	4H	NC*1		$\overline{SW}a$	5L	11
41	4M	$\overline{SW}$		DQa_4	7K	10
42	2K	DQb_5		DQa_3	6L	9
43	1L	DQb_6				
44	2M	DQb_7		DQa_2	6N	8
45	1N	DQb_8		DQa_1	7P	7
				ZZ	7T	6
46	2P	DQb_9		SA	5T	5
47	3T	SA		SA	6R	4
48	2R	SA				
49	4N	SA		SA	4P	3
50	2T	SA		SA	6T	2
51	3R	M_1		M_2	5R	1

NOTE :1. Pin 4H is no connection pin to internal chip and the scanned data is "0".

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	2.5	2.63	V	
Input High Level	V_{IH}	0.7*V_{DD}	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.3*V_{DD}	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	0.75*V_{DD}	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

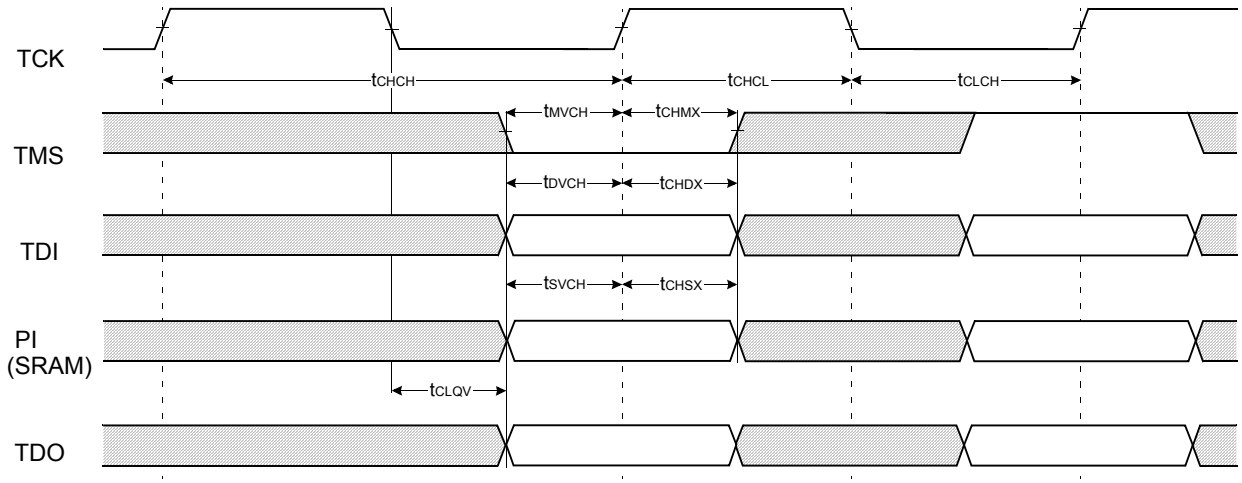
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	V_{DD}/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		V_{DD}/2	V	1

NOTE : 1. See SRAM AC test output load on page 7.

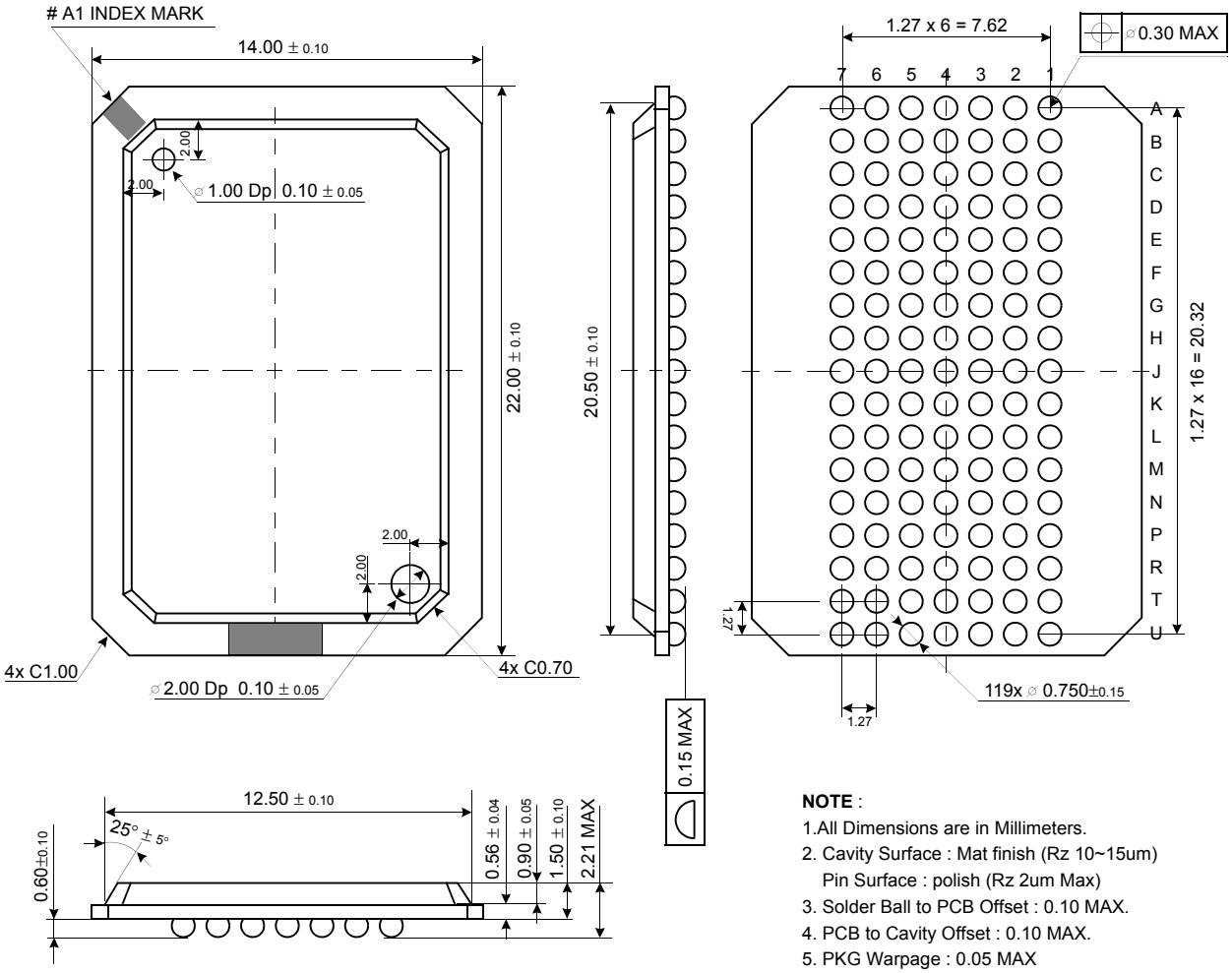
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



119 BGA PACKAGE DIMENSIONS



NOTE :
1.All Dimensions are in Millimeters.
2. Cavity Surface : Mat finish (Rz 10~15um)
Pin Surface : polish (Rz 2um Max)
3. Solder Ball to PCB Offset : 0.10 MAX.
4. PCB to Cavity Offset : 0.10 MAX.
5. PKG Warpage : 0.05 MAX

119 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient (at still air)	Theta_JA	20.0	°C/W	1.5W Heating
Junction to Case	Theta_JC	4.3	°C/W	
Junction to Board	Theta_JB	5.4	°C/W	1.5W Heating

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D$ x Theta_JA.