

**M312L6423DT0**

**184pin 1U Registered DDR SDRAM MODULE**

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# 512MB DDR SDRAM MODULE

(64Mx72(32Mx72\*2 bank) based on 32Mx8 DDR SDRAM)

Registered 184pin DIMM  
72-bit ECC/Parity

Revision 0.0

January. 2002

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**Revision History**

**Revision 0 (Jan. 2002)**

1. First release for internal usage

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## M312L6423DT0 DDR SDRAM 184pin DIMM

64Mx72 DDR SDRAM 184pin DIMM based on 32Mx8

### GENERAL DESCRIPTION

The Samsung M312L6423DT0 is 64M bit x 72 Double Data Rate SDRAM high density memory modules. The Samsung M312L6423DT0 consists of eighteen CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages, mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M312L6423DT0 is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### FEATURE

- Performance range

Part No.	Max Freq.	Interface
M312L6423DT0-C(L)A2	133MHz(7.5ns@CL=2)	SSTL_2
M312L6423DT0-C(L)B0	133MHz(7.5ns@CL=2.5)	
M312L6423DT0-C(L)A0	100MHz(10ns@CL=2)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : **Height 1200 mil**, double sided component

### PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS		
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45		
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ		
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0		
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1		
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5		
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS		
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46		
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47		
10	/RESET	41	A2	71	*CS2	102	NC	133	DQ31	163	*CS3		
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ		
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52		
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53		
14	DQS1	45	CB1	75	*CK2	106	DQ13	137	CK0	167	*A13		
15	VDDQ	46	VDD	76	*CK2	107	DM1	138	/CK0	168	VDD		
16	*CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6		
17	*CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54		
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55		
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ		
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC		
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60		
22	VDDQ		KEY	83	DQ56	114	DQ20		KEY	175	DQ61		
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS		
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7		
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62		
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63		
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ		
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0		
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1		
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2		
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD		

### PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit(Data-in/data-out)
DQS0 ~ DQS8	Data Strobe input/output
CK0, $\overline{CK0}$	Clock input
CKE0, CKE1	Clock enable input
CS0, CS1	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DM0 ~ DM8	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply ( 2.3V to 3.6V )
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
$\overline{RESET}$	Reset enable
NC	No connection

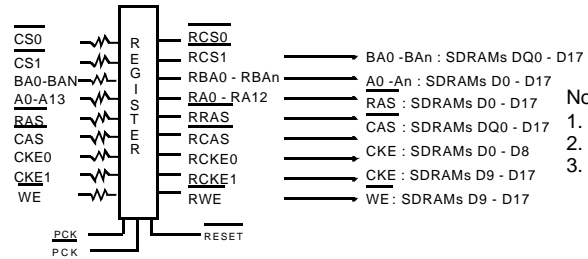
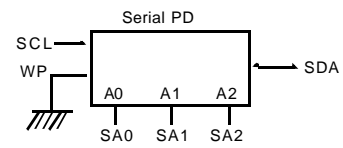
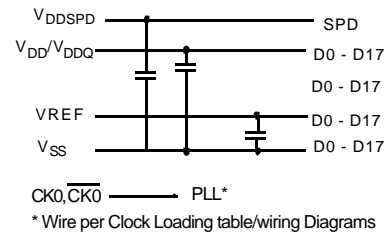
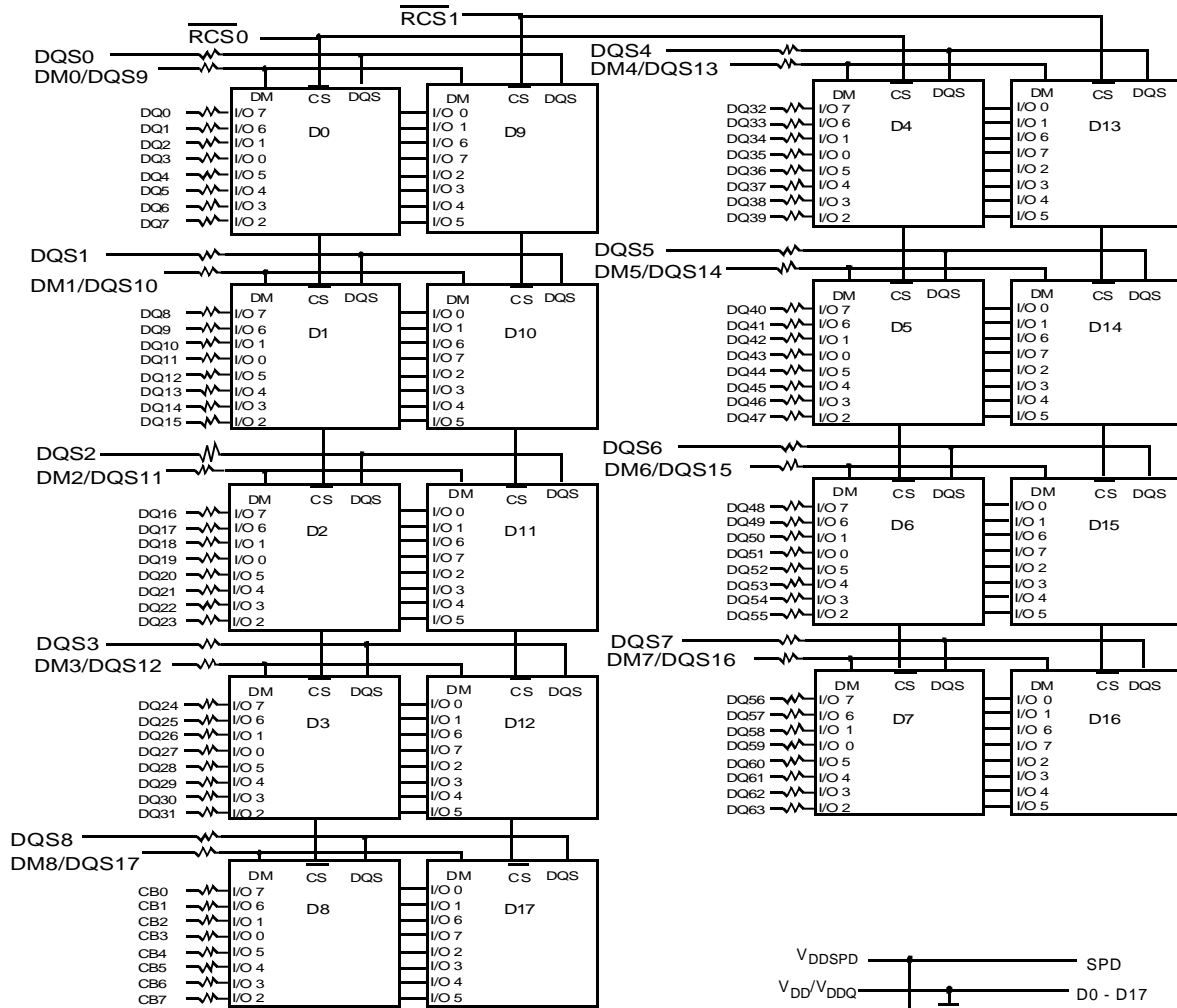
\* These pins are not used in this module.

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## Functional Block Diagram



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
  2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
  3. DQ, DQS, DM/DQS resistors: 22 Ohms.

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### Absolute Maximum Rate

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 ~ 3.6	V
Voltage on $V_{DD}$ & $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DD}, V_{DDQ}$	-1.0 ~ 3.6	V
Storage temperature	$T_{STG}$	-55 ~ +150	°C
Power dissipation	$P_D$	27	W
Short circuit current	$I_{OS}$	50	mA

**Note** : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### POWER & DC OPERATING CONDITIONS (SSTL\_2 In/Out)

Recommended operating conditions(Voltage referenced to  $V_{SS}=0V$ ,  $T_A=0$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal $V_{DD}$ of 2.5V)	$V_{DD}$	2.3	2.7		
I/O Supply voltage	$V_{DDQ}$	2.3	2.7	V	
I/O Reference voltage	$V_{REF}$	$V_{DDQ}/2-50mV$	$V_{DDQ}/2+50mV$	V	1
I/O Termination voltage(system)	$V_{TT}$	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	4
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(DC)$	0.3	$V_{DDQ}+0.6$	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	$V_{IX}(DC)$	1.15	1.35	V	5
Input leakage current	$I_I$	-2	2	$\mu A$	
Output leakage current	$I_{OZ}$	-5	5	$\mu A$	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	$I_{OH}$	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	$I_{OL}$	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	$I_{OH}$	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	$I_{OL}$	9		mA	

- Notes**
- Includes  $\pm 25mV$  margin for DC offset on  $V_{REF}$ , and a combined total of  $\pm 50mV$  margin for all AC noise and DC offset on  $V_{REF}$ , bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on  $V_{REF}$  and internal DRAM noise coupled TO  $V_{REF}$ , both of which may result in  $V_{REF}$  noise.  $V_{REF}$  should be de-coupled with an inductance of  $\leq 3nH$ .
  - $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$ , and must track variations in the DC level of  $V_{REF}$
  - $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
  - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a  $V_{REF}$  envelop that has been bandwidth limited to 200MHZ.
  - The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the dc level of the same.
  - These characteristics obey the SSTL-2 class II standards.

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**DDR SDRAM IDD spec table**

Symbol	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2)	Unit	Note
IDD0	2310	2310	2170	mA	
IDD1	2550	2550	2420	mA	
IDD2P	1140	1140	1140	mA	
IDD2F	1380	1380	1340	mA	
IDD2Q	1540	1540	1460	mA	
IDD3P	1620	1620	1560	mA	
IDD3N	1940	1940	1820	mA	
IDD4R	2790	2790	2560	mA	
IDD4W	2680	2680	2340	mA	
IDD5	2970	2970	2770	mA	
IDD6	1160	1160	1160	mA	
IDD6	Low Power	1130	1130	mA	Optional
IDD7A	4200	4200	3600	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

For the IDD spec of a DDR SDRAM Module with 2 rows, SAMSUNG defines the test condition of each row as below:

Test (condition)	
1 row (Active)	2 row (Stand by)
IDD0	IDD3N
IDD1	IDD3N
IDD2P	IDD2P
IDD2F	IDD2F
IDD2Q	IDD2Q
IDD3P	IDD3P
IDD3N	IDD3N
IDD4R	IDD3N
IDD4W	IDD3N
IDD5	IDD3N
IDD6	IDD6
IDD7	IDD3N

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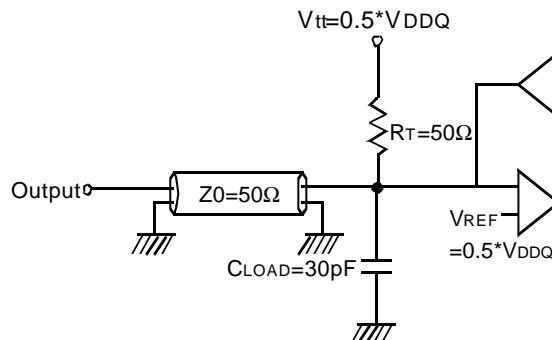
## AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	V <sub>IL</sub> (AC)		V <sub>REF</sub> - 0.31	V	3
Input Differential Voltage, CK and CK inputs	V <sub>ID</sub> (AC)	0.7	V <sub>DDQ</sub> +0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	V <sub>IX</sub> (AC)	0.5*V <sub>DDQ</sub> -0.2	0.5*V <sub>DDQ</sub> +0.2	V	2

- Note
1. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .
  2. The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.
  3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relative to a V<sub>ref</sub> envelope that has been bandwidth limited 20MHz.

## AC OPERATING TEST CONDITIONS (V<sub>DD</sub>=2.5V, V<sub>DDQ</sub>=2.5V, T<sub>A</sub>= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * V <sub>DDQ</sub>	V	
Input signal maximum peak swing	1.5	V	
Input Levels(V <sub>IH</sub> /V <sub>IL</sub> )	V <sub>REF</sub> +0.31/V <sub>REF</sub> -0.31	V	
Input timing measurement reference level	V <sub>REF</sub>	V	
Output timing measurement reference level	V <sub>tt</sub>	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL\_2)

## Input/Output CAPACITANCE (V<sub>DD</sub>=2.5, V<sub>DDQ</sub>=2.5V, T<sub>A</sub>= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A <sub>0</sub> ~ A <sub>12</sub> , BA <sub>0</sub> ~ BA <sub>1</sub> , RAS, CAS, WE )	C <sub>IN1</sub>	-	12	pF
Input capacitance(CKE <sub>0</sub> ,CKE <sub>1</sub> )	C <sub>IN2</sub>	-	12	pF
Input capacitance( $\overline{CS_0}$ , $\overline{CS_1}$ )	C <sub>IN3</sub>	-	11	pF
Input capacitance( CLK <sub>0</sub> , /CLK <sub>0</sub> )	C <sub>IN4</sub>	-	12	pF
Input capacitance(DM <sub>0</sub> ~DM <sub>8</sub> )	C <sub>IN5</sub>	-	16	pF
Data & DQS input/output capacitance(DQ <sub>0</sub> ~DQ <sub>63</sub> )	C <sub>OUT1</sub>	-	16	pF
Data input/output capacitance(CB <sub>0</sub> ~CB <sub>7</sub> )	C <sub>OUT2</sub>	-	16	pF

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**AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)**

Parameter	Symbol	-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	65		65		70		ns		
Refresh row cycle time	tRFC	75		75		80		ns		
Row active time	tRAS	45	120K	45	120K	48	120K	ns		
RAS to CAS delay	tRCD	20		20		20		ns		
Row precharge time	tRP	20		20		20		ns		
Row active to Row active delay	tRRD	15		15		15		ns		
Write recovery time	tWR	15		15		15		ns		
Last data in to Read command	tWTR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	CL=2.0	tCK	7.5	12	10	12	10	12	ns	5
	CL=2.5		7.5	12	7.5	12			ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/CK	tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to output data edge	tDQSQ	-	0.5	-	0.5	-	0.6	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	2	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time(fast)	tIS	0.9		0.9		1.1		ns	6	
Address and Control Input hold time(fast)	tIH	0.9		0.9		1.1		ns	6	
Address and Control Input setup time(slow)	tIS	1.0		1.0		1.1		ns	6	
Address and Control Input hold time(slow)	tIH	1.0		1.0		1.1		ns	6	
Data-out high impedance time from CK/CK	tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data-out low impedance time from CK/CK	tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			



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Parameter	Symbol	-TCA2 (DDR266A)		-TCB0 (DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns	7,8,9
Control & Address input pulse width	tIPW	2.2		2.2		2.5		ns	
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns	
Power down exit time	tPDEX	7.5		7.5		10		ns	
Exit self refresh to non-Read command	tXSNR	75		75		80		ns	4
Exit self refresh to read command	tXSRD	200		200		200		tCK	
Refresh interval time	tREFI	7.8		7.8		7.8		us	1
Output DQS valid window	tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Active to Read with Auto precharge command	tRAP	20		20		20			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

- Maximum burst refresh cycle : 8
- The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with tRCD satisfied after this command.
- For registered DIMMs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t<sub>IS</sub>/t<sub>IH</sub> in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t<sub>DS</sub>/t<sub>DH</sub> in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

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8. I/O Setup/Hold Plateau Derating

I/O Input Level	$\Delta t_{DS}$	$\Delta t_{DH}$
(mV)	(ps)	(ps)
$\pm 280$	+50	+50

This derating table is used to increase  $t_{DS}/t_{DH}$  in the case where the input level is flat below  $V_{REF} \pm 310mV$  for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	$\Delta t_{DS}$	$\Delta t_{DH}$
(ns/V)	(ps)	(ps)
0	0	0
$\pm 0.25$	+50	+50
$\pm 0.5$	+100	+100

This derating table is used to increase  $t_{DS}/t_{DH}$  in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as  $1/SlewRate1-1/SlewRate2$ . For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

**<Reference>**

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	$\Delta t_{IH}/t_{IS}$ (ps)	$\Delta t_{DSS}/t_{DSH}$ (ps)	$\Delta t_{AC}/t_{DQSCK}$ (ps)	$\Delta t_{LZ}(\min)$ (ps)	$\Delta t_{HZ}(\max)$ (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

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**Command Truth Table**

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh	H	H	L	L	L	H	X			3	
	Entry		L								3	
	Self Refresh	L	H	L	H	H	H	X			3	
				Exit	H	X	X			X		3
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable	H	X	L	H	L	H	V	L	Column Address (A0~A9)		4
	Auto Precharge Enable								H			4
Write & Column Address	Auto Precharge Disable	H	X	L	H	L	L	V	L	Column Address (A0~A9)		4
	Auto Precharge Enable								H			4, 6
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection	H	X	L	L	H	L	V	L	X		
	All Banks							X	H			5
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X					
				L	V	V	V					
DM		H	X					X			8	
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9	
				L	H	H	H				9	

Note : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

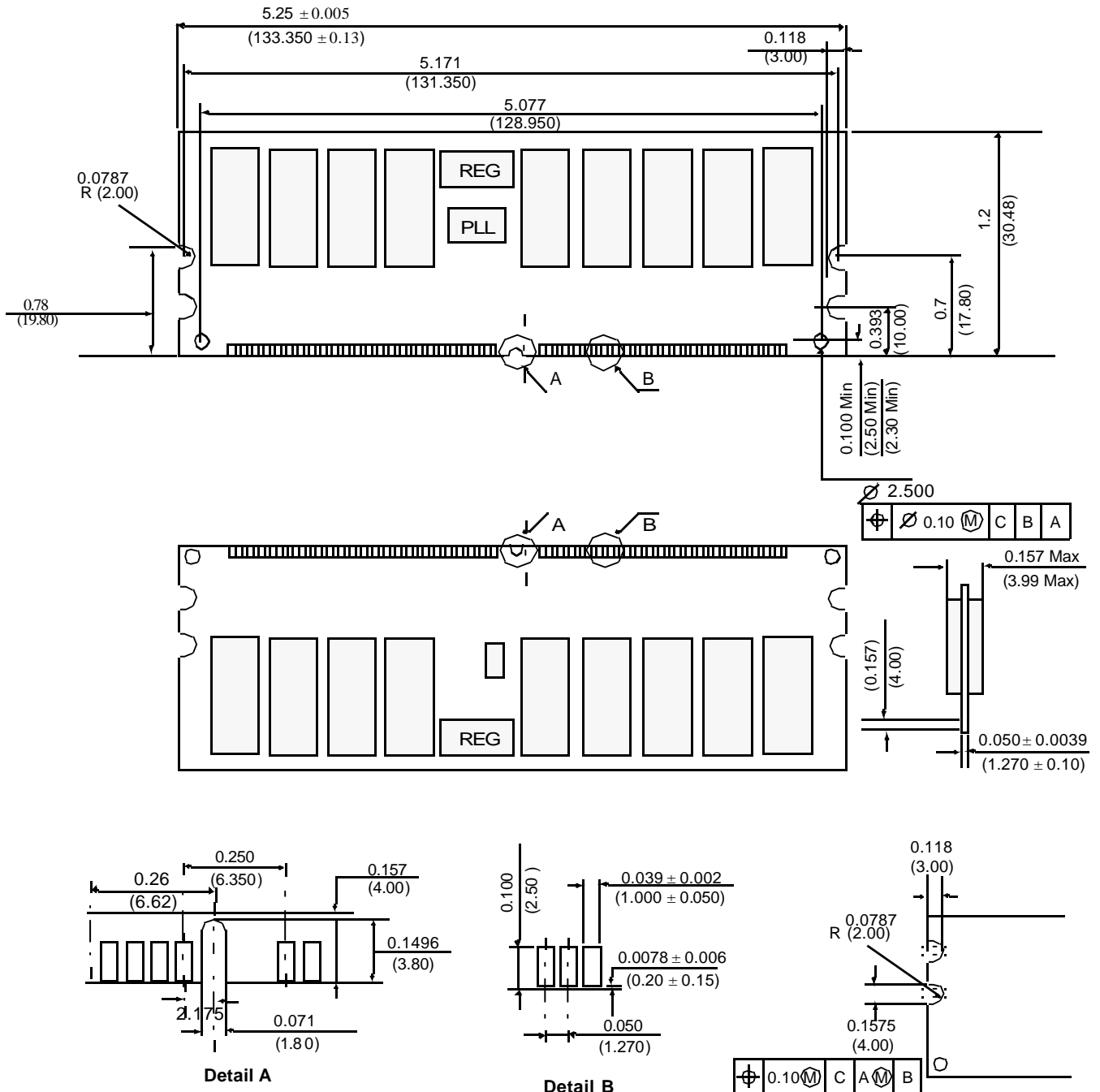
- EMRS/ MRS can be issued only at all banks precharge state.  
A new command can be issued 2 clock cycles after EMRS or MRS.
- Auto refresh functions are same as the CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.  
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
- If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
- During burst write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
- This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

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**PACKAGE DIMENSIONS**

Units : Inches (Millimeters)

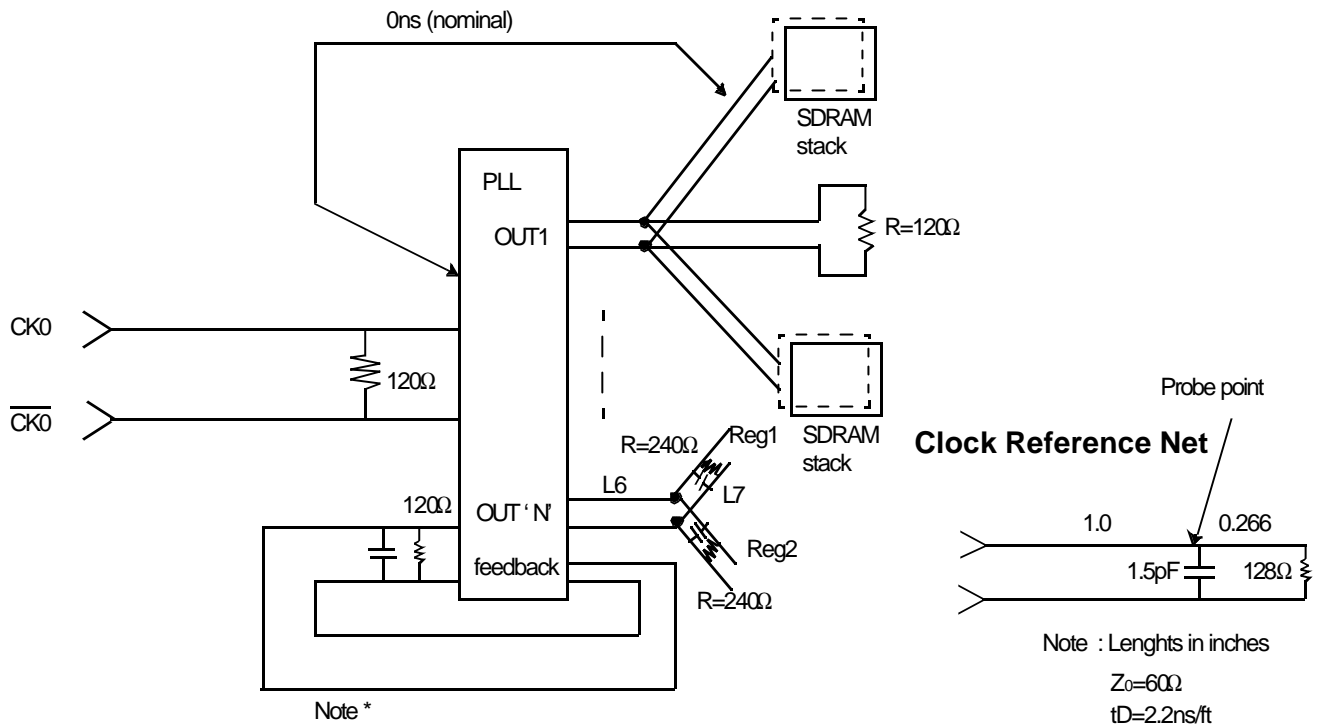


Tolerances :  $\pm 0.005(.13)$  unless otherwise specified  
 The used device is 32Mx8 SDRAM, TSOP  
 SDRAM Part NO : K4H560838D

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**184pin 1U Registered DDR SDRAM MODULE**

**184 Pin DDR Registered DIMM Clock Topolgy**



Notes\* :

1. The Clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns(nominal).
2. Input,output, and feedback clock lines are terminated from line to leine as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar maner.
4. termination resistors for the PLL feedback path clocks are loacted after the pins of the PLL.