256MB DDR SDRAM MODULE

(32Mx72 based on 32Mx8 DDR SDRAM)

Registered 184pin DIMM
72-bit ECC/Parity

Revision 1.1

May. 2002

Revision History

Revision 0 (Aug 1998)

1. First release for internal usage

Revision 0.1 (Aug. 1999)

1. Modified binning policy

From	To
-Z (133Mhz)	-Z (133Mhz/266Mbps@CL=2)
-8 (125Mhz)	-Y (133Mhz/266Mbps@CL=2.5)
-0 (100Mhz)	-0 (100Mhz/200Mbps@CL=2)

2.Modified the following AC spec values

	From.		To.		
	-Z	-0	-Z	-Y	-0
tAC	+/- 0.75ns	+/- 1ns	+/- 0.75ns	+/- 0.75ns	+/- 0.8ns
tDQSCK	+/- 0.75ns	+/- 1ns	+/- 0.75ns	+/- 0.75ns	+/- 0.8ns
tDQSQ	+/- 0.5ns	+/- 0.75ns	+/- 0.5ns	+/- 0.5ns	+/- 0.6ns
tDS/tDH	0.5 ns	0.75 ns	0.5 ns	0.5 ns	0.6 ns
tCDLR*1	2.5tCK-tDQSS	2.5tCK-tDQSS	1tCK	1tCK	1tCK
tPRE*1	1tCK +/- 0.75ns	1tCK +/- 1ns	0.9/1.1 tCK	0.9/1.1 tCK	0.9/1.1 tCK
tRPST*1	tCK/2 +/- 0.75ns	tCK/2 +/- 1ns	0.4/0.6 tCK	0.4/0.6 tCK	0.4/0.6 tCK
tHZQ*1	tCK/2 +/- 0.75ns	tCK/2 +/- 1ns	+/- 0.75ns	+/- 0.75ns	+/-0.8ns

*1 : Changed description method for the same functionality. This means no difference from the previous version.

3.Changed the following AC parameter symbol From tDQCK To tAC
Output data access time from CK/$\overline{CK}$.

Revision 0.2 (Sept. 1999)

1. Changed the odering information.

1-1. Exclude KM mark.

From	To
KMM383...	M383.....

1-2. PCB Revison

From	To
- Blank: 1st generation	- 0: 1st gernation
- A : 2nd generation	- 1: 2nd generation
- B : 2nd generation	- 2: 3nd generation
Example:KMM383L3223AT	M383L3223AT0

1-3. Modified binning policy

From	To
- 0 (100Mhz/200Mbps@CL=2)	- A0 (100Mhz/200Mbps@CL=2)
- Z (133Mhz/266Mbps@CL=2)	- A2 (133Mhz/266Mbps@CL=2)
- Y (133Mhz/266Mbps@CL=2.5)	- B0 (133Mhz/266Mbps@CL=2.5)

Revision 0.3 (December. 1999)

1. Changed from 3.3V to 2.5V in VDDSPD power.

Revision 0.4 (April. 2000)

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1. Changed pin 90 from WP to NC in pin configuration table.
2. Removed WP in pin description.

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3. Changed bypassing to reflect common Vdd/Vddq plane.
4. Added A12, BA1.
5. Removed WP from serial PD.

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6. Changed Power & DC operating condition.

Parameter	Symbol	From		To	
		Min	Max	Min	Max
I/O Reference voltage	V_{REF}	1.15	1.35	0.49*VDDQ	0.51*VDDQ
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.18	V_{DDQ}+0.3	V_{REF}+0.15	V_{DDQ}+0.3
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.18	-0.3	V_{REF}-0.15
Input leakage current	I_I	-5	5	-2	2
Output High Current (V_{OUT} = 1.95V)	I_{OH}	-15.2		-16.8	
Output Low Current (V_{OUT} = 0.35V)	I_{OL}	15.2		16.8	

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7. Added Overshoot/Undershoot spec
   . Vih(max) = 4.2V, the overshoot voltage duration is ≤ 3ns at VDD.
   . Vil(min) =- 1.5V, the overshoot voltage duration is ≤ 3ns at VSS.

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8. Changed AC operating conditions as follows.

Parameter/Condition	Symbol	From		To	
		Min	Max	Min	Max
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.35		VREF + 0.31	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.35		VREF - 0.31
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	0.62	VDDQ+0.6

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9. Changed AC parameters as follows.

Parameter	from	to	Comments
tDQSQ	+/- 0.5(PC266), +/- 0.6(PC200)	+0.5(PC266), +0.6(PC200)	
tDV	+/- 0.35tCK	-	Removed

10. Added AC parameters as follows

Parameter	Symbol	-A2(PC266@CL=2)		-B0(PC266@CL=2.5)		-A0(PC200@CL=2)	
		Min	Max	Min	Max	Min	Max
Output DQS valid window	tQH	tHPmin -0.75ns	-	tHPmin -0.75ns	-	tHPmin -1.0ns	-
Clock half period	tHP	tCLmin or tCH-	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-
QFC setup to first DQS edge on reads	tQCS	0.9	1.1	0.9	1.1	0.9	1.1
QFC hold after last DQS edge on reads	tDQCH	0.4	0.6	0.4	0.6	0.4	0.6
Write command to QFC delay on write	tQCSW		4.0		4.0		4.0
Write burst end to QFC delay on write	tQCHW	1.25ns	0.5tCK	1.25ns	0.5tCK	1.25ns	0.5tCK
Write burst end to QFC delay on write interrupted by Precharge	tQCHWI	1.25ns	1.5tCK	1.25ns	1.5tCK	1.25ns	1.5tCK

Revision 0.5 (April. 2000)

1. Changed from A-die to B-die.

Revision 0.6 (June. 2000)

1. Changed PCB version from T0 to T1.

Revision 0.7 (October. 2000)

1.Added DC target spec values.

2.Deleted tDAL in AC parameter X.

Revision 0.8 (November. 2000)

1.Changed component placement on module PCB in package dimesions.

Revision 0.9 (June. 2001)

1. Changed module current speificaton
2. Changed typo size on module PCB in package dimesions. (from 2.6mm to 3mm).
3. Changed AC parameter table.

Revision 1.0 (Dec. 2001)

- Add derating values for the specifications if the single-ended clock skew rate is less than 1.0V/ns in page 47.
- Revised "Absolute maximum rating" table in page 38.
  . Changed "Voltage on VDDQ supply relative to VSS" value from -0.5~3.6V to -1~3.6V
  . Changed "power dissipation" value from 1.0W to 1.5W.
- Revised AC parameter table

	From						To					
	DDR266A		DDR266B		DDR200		DDR266A		DDR266B		DDR200	
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
tHZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tLZ	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	tACmin -400ps	tACmax -400ps	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8
tWPST (tCK)	0.25		0.25		0.25		0.4	0.6	0.4	0.6	0.4	0.6
tPDEX	10ns		10ns		10ns		7.5ns		7.5ns		10ns	

- Deleted typical current in IDD spec. table
- Included address and control input setup/hold time(tIS/tIH) at slow slew rate in DDR200/266 AC specification
- Deleted Exit self refresh to write command(tXSW) in DDR200/266 AC specification
- Rename tXSA(exit self refresh to bank active command) to tXSNR(exit self refresh to non read command) at DDR200/266
- Rename tXSR(exit self refresh to read command) to tXSRD at DDR200/266
- Rename tWPREH(DQS in hold time) to tWPRE at DDR200/266
- Rename tREF(Refresh interval time) to tREFI at DDR200/266
- Changed tWR value from 2tCK to 15ns.
--Rename tCDLR(Write data out to Read command) t0 tWTR
- Added tDAL(tWR+tRP)

Revision 1.1 (May. 2002)

1. Change pin location of A13 from pin 103 to pin 167

M383L3223BT1 DDR SDRAM 184pin DIMM

32Mx72 DDR SDRAM 184pin DIMM based on 32Mx8

GENERAL DESCRIPTION

The Samsung M383L3223BT1 is 32M bit x 72 Double Data Rate SDRAM high density memory modules based on first generation of 256Mb DDR SDRAM respectively. The Samsung M383L3223BT1 consists of nine CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages, mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M383L3223BT1 is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

• Performance range

Part No.	Max Freq.	Interface
M383L3223BT1-C(L)A2	133MHz(7.5ns@CL=2)	SSTL_2
M383L3223BT1-C(L)B0	133MHz(7.5ns@CL=2.5)	
M383L3223BT1-C(L)A0	100MHz(10ns@CL=2)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : **Height 1700 (mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

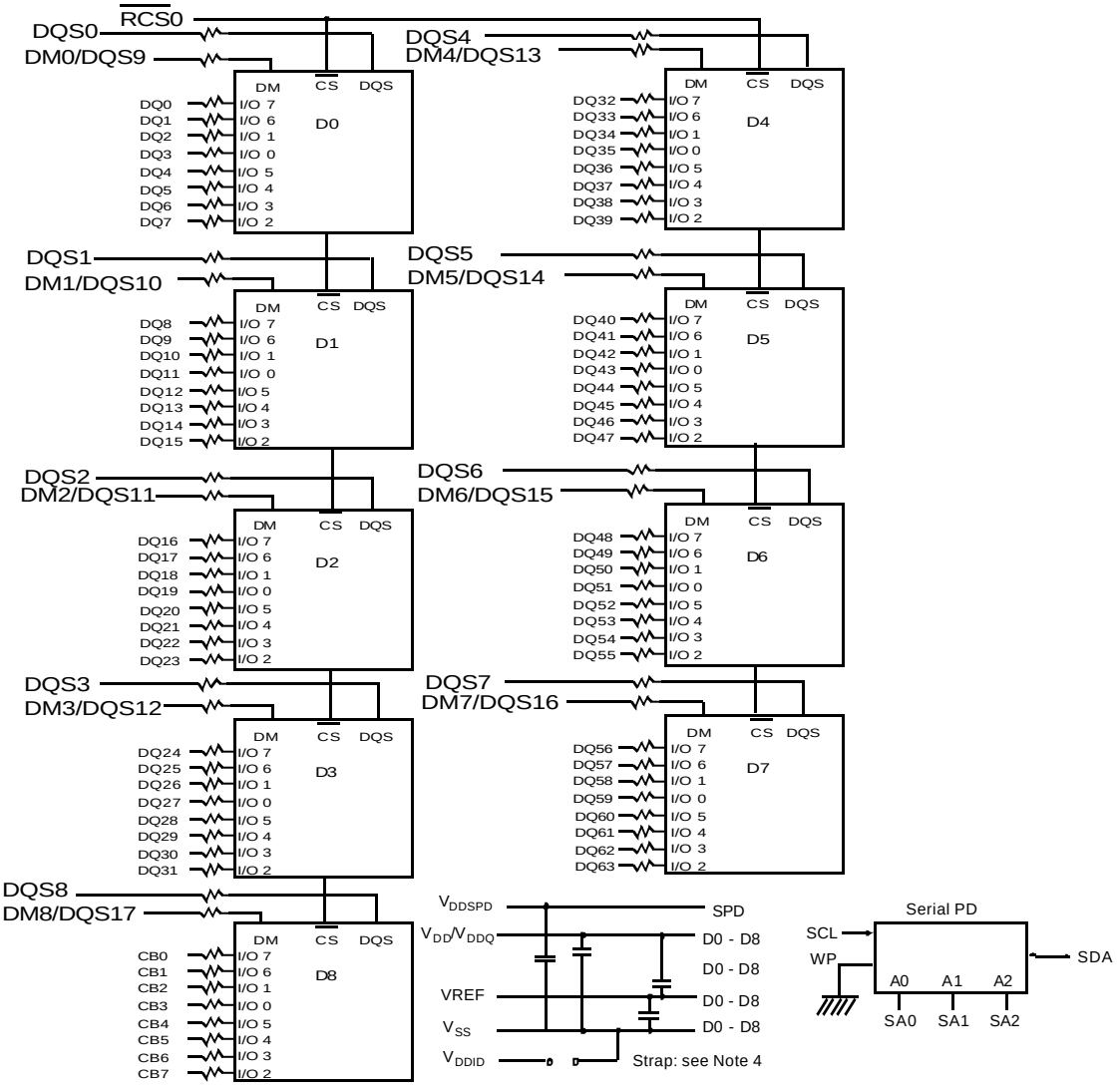
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	*/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	/RESET	41	A2	71	*/CS2	102	NC	133	DQ31	163	*/CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	*/CK2	106	DQ13	137	CK0	167	*A13
15	VDDQ	46	VDD	76	*CK2	107	DM1	138	/CK0	168	VDD
16	*CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	*/CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	*CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit(Data-in/data-out)
DQS0 ~ DQS8	Data Strobe input/output
CK0,$\overline{CK0}$	Clock input
CKE0	Clock enable input
$\overline{CS0}$	Chip select input
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
DM0 ~ DM8	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
$\overline{RESET}$	Reset enable
NC	No connection

* These pins are not used in this module.

Functional Block Diagram



Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/CS relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms.
4. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD = VDDQ
STRAP IN (VSS): VDD ≠ VDDQ.

Absolute Maximum Rate

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} & V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	13.5	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V_{DD} of 2.5V)	V_{DD}	2.3	2.7		
I/O Supply voltage	V_{DDQ}	2.3	2.7	V	
I/O Reference voltage	V_{REF}	VDDQ/2-50mV	VDDQ/2+50mV	V	1
I/O Termination voltage(system)	V_{TT}	V_{REF}-0.04	V_{REF}+0.04	V	2
Input logic high voltage	V_{IH}(DC)	V_{REF}+0.15	V_{DDQ}+0.3	V	4
Input logic low voltage	V_{IL}(DC)	-0.3	V_{REF}-0.15	V	4
Input Voltage Level, CK and $\overline{CK}$ inputs	V_{IN}(DC)	-0.3	V_{DDQ}+0.3	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	V_{ID}(DC)	0.3	V_{DDQ}+0.6	V	3
Input crossing point voltage, CK and $\overline{CK}$ inputs	V_{IX}(DC)	1.15	1.35	V	5
Input leakage current	I_I	-2	2	uA	
Output leakage current	I_{OZ}	-5	5	uA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} + 0.84V	I_{OH}	-16.8		mA	
Output High Current(Normal strengh driver) ;V_{OUT} = V_{TT} - 0.84V	I_{OL}	16.8		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} + 0.45V	I_{OH}	-9		mA	
Output High Current(Half strengh driver) ;V_{OUT} = V_{TT} - 0.45V	I_{OL}	9		mA	

Notes 1. Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.

2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}

3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.

4. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.

5. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the dc level of the same.

6. These charactericteristics obey the SSTL-2 class II standards.

DDR SDRAM SPEC Items and Test Conditions

Conditions	Symbol
Operating current - One bank Active-Precharge; tRC=tRCmin; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	**IDD0**
Operating current - One bank operation ; One bank open, BL=4, Reads - Refer to the following page for detailed test condition	**IDD1**
Percharge power-down standby current; All banks idle; power - down mode; CKE = <VIL(max); Vin = Vref for DQ,DQS and DM	**IDD2P**
Precharge Floating standby current; CS# > =VIH(min);All banks idle; CKE > = VIH(min); Address and other control inputs changing once per clock cycle; Vin = Vref for DQ,DQS and DM	**IDD2F**
Precharge Quiet standby current; CS# > = VIH(min); All banks idle; CKE > = VIH(min); Address and other control inputs stable with keeping >= VIH(min) or =<VIL(max); Vin = Vref for DQ ,DQS and DM	**IDD2Q**
Active power - down standby current ; one bank active; power-down mode; CKE=< VIL (max); Vin = Vref for DQ,DQS and DM	**IDD3P**
Active standby current; CS# >= VIH(min); CKE>=VIH(min); one bank active; active - precharge; tRC=tRASmax; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	**IDD3N**
Operating current - burst read; Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; 50% of data changing at every burst; Iout = 0 m A	**IDD4R**
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	**IDD4W**
Auto refresh current; tRC = tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz ; distributed refresh	**IDD5**
Self refresh current; CKE =< 0.2V; External clock should be on; tCK = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B	**IDD6**
Orerating current - Four bank operation ; Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	**IDD7A**

DDR SDRAM I_{DD} spec table

Symbol	A2(DDR266@CL=2)	B0(DDR266@CL=2.5)	A0(DDR200@CL=2)	Unit	Notes
IDD0	2120	2120	2010	mA	
IDD1	2430	2430	2290	mA	
IDD2P	1330	1330	1300	mA	
IDD2F	1420	1420	1380	mA	
IDD2Q	1520	1520	1460	mA	
IDD3P	1460	1460	1400	mA	
IDD3N	1640	1640	1550	mA	
IDD4R	3040	3040	2700	mA	
IDD4W	3680	3680	3140	mA	
IDD5	3020	3020	2850	mA	
IDD6	1120	1120	1120	mA	
IDD7A	4560	4560	4120	mA	

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

< Detailed test conditions for DDR SDRAM IDD1 & IDD7 >

IDD1 : Operating current: One bank operation

1. Only one bank is accessed with tRC(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. Iout = 0mA4. Timing patterns
   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRCD = 2*tCK, tRAS = 5*tCK
     Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst
   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst
   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRCD = 3*tCK, tRC = 9*tCK, tRAS = 5*tCK
     Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
     *50% of data changing at every burst

IDD7A : Operating current: Four bank operation

1. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
2. Timing patterns
   - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2*tCK, tRCD= 3*tCK, Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst

   - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2*tCK, tRCD = 3*tCK
     Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst

   - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL2=2, BL=4, tRRD = 2*tCK, tRCD = 3*tCK,Read with autoprecharge
     Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing
     *100% of data changing at every burst

   Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

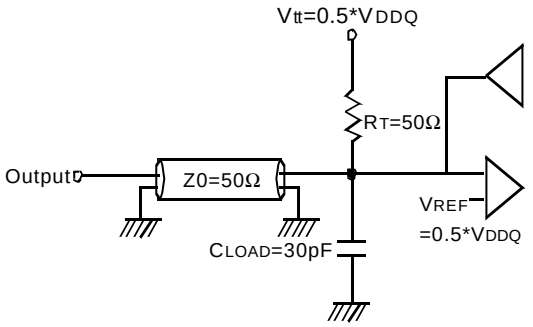
AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note 1. VID is the magnitude of the difference between the input level on CK and the input on $\overline{CK}$.
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pim on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specificatims are refation to a Vref envelope that has been bandwidth limited 20MHz.

AC OPERATING TEST CONDITIONS (VDD=2.5V, VDDQ=2.5V, TA= 0 to 70°C)

Parameter	Value	Unit	Note
Input reference voltage for Clock	0.5 * VDDQ	V	
Input signal maximum peak swing	1.5	V	
Input Levels(VIH/VIL)	VREF+0.31/VREF-0.31	V	
Input timing measurement reference level	VREF	V	
Output timing measurement reference level	Vtt	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE (VDD=2.5, VDDQ=2.5V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(A0 ~ A12, BA0 ~ BA1,$\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	CIN1	-	12	pF
Input capacitance(CKE0)	CIN2	-	12	pF
Input capacitance($\overline{CS}$0,)	CIN3	-	11	pF
Input capacitance(CLK0, /CLK0)	CIN4	-	12	pF
Input capacitance(DM0~DM8)	CIN5	-	11	pF
Data & DQS input/output capacitance(DQ0~DQ63)	COUT1	-	11	pF
Data input/output capacitance(CB0~CB7)	COUT2	-	11	pF

AC Timming Parameters & Specifications (These AC charicteristics were tested on the Component)

Parameter		Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Row cycle time		tRC	65		65		70		ns	
Refresh row cycle time		tRFC	75		75		80		ns	
Row active time		tRAS	45	120K	45	120K	48	120K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	20		20		20		ns	
Row precharge time		tRP	20		20		20		ns	
Row active to Row active delay		tRRD	15		15		15		ns	
Write recovery time		tWR	15		15		15		ns	
Last data in to Read command		tWTR	1		1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		1		tCK	
Clock cycle time	CL=2.0	tCK	7.5	12	10	12	10	12	ns	5
	CL=2.5		7.5	12	7.5	12			ns	5
Clock high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/$\overline{CK}$		tDQSCK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Output data access time from CK/$\overline{CK}$		tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data strobe edge to ouput data edge		tDQSQ	-	0.5	-	0.5	-	0.6	ns	5
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		0		ns	2
DQS-in hold time		tWPRE	0.25		0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising-hold time		tDSH	0.2		0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		0.35		tCK	
DQS-in cycle time		tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time(fast)		tIS	0.9		0.9		1.1		ns	6
Address and Control Input hold time(fast)		tIH	0.9		0.9		1.1		ns	6
Address and Control Input setup time(slow)		tIS	1.0		1.0		1.1		ns	6
Address and Control Input hold time(slow)		tIH	1.0		1.0		1.1		ns	6
Data-out high impedence time from CK/$\overline{CK}$		tHZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Data-out low impedence time from CK/$\overline{CK}$		tLZ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	
Input Slew Rate(for input only pins)		tSL(I)	0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)		tSL(IO)	0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)		tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10
Output Slew Rate(x16)		$tSL_{(O)}$	0.7	5	0.7	5	0.7	5	V/ns	10
Output Slew Rate Matching Ratio(rise to fall)		t_{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		

Parameter		Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Mode register set cycle time		tMRD	15		15		16		ns	
DQ & DM setup time to DQS		tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS		tDH	0.5		0.5		0.6		ns	7,8,9
DQ & DM input pulse width		tDIPW	1.75		1.75		2		ns	
Power down exit time		tPDEX	7.5		7.5		10		ns	
Exit self refresh to non-Read command		tXSNR	75		75		80		ns	4
Exit self refresh to read command		tXSRD	200		200		200		tCK	
Refresh interval time	64Mb, 128Mb	tREFI	15.6		15.6		15.6		us	1
	256Mb		7.8		7.8		7.8		us	1
Output DQS valid window		tQH	tHP -tQHS	-	tHP -tQHS	-	tHP -tQHS	-	ns	5
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor		tQHS		0.75		0.75		0.8	ns	
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	3
Autoprecharge write recovery + Precharge time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	11

1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter ($t_{JIT(HP)}$) of the PLL and the half period jitter due to crosstalk ($t_{JIT(crosstalk)}$) on the DIMM.

6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtDS	ΔtDH
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

8. I/O Setup/Hold Plateau Derating

I/O Input Level	ΔtDS	ΔtDH
(mV)	(ps)	(ps)
± 280	+50	+50

This derating table is used to increase tDS/tDH in the case where the input level is flat below VREF ± 310mV for a duration of up to 2ns.

9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	ΔtDS	ΔtDH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 5V/ns and slew rate 2 =.4V/ns then the Delta Rise/Fall Rate =-0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

10. This parameter is fir system simulation purpose. It is guranteed by design.

11. For each of the terms, if not already an integer, round to the next highest integer. tCK is actual to the system clock cycle time.

<Note>

The following table specifies derating values for the specifications listed if the single-ended clock skew rate is less than 1.0V/ns.

CK slew rate (Single ended)	ΔtIH/tIS (ps)	ΔtDSS/tDSH (ps)	ΔtAC/tDQSCK (ps)	ΔtLZ(min) (ps)	ΔtHZ(max) (ps)
1.0V/ns	0	0	0	0	0
0.75V/ns	+50	+50	+50	-50	+50
0.5V/ns	+100	+100	+100	-100	+100

Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

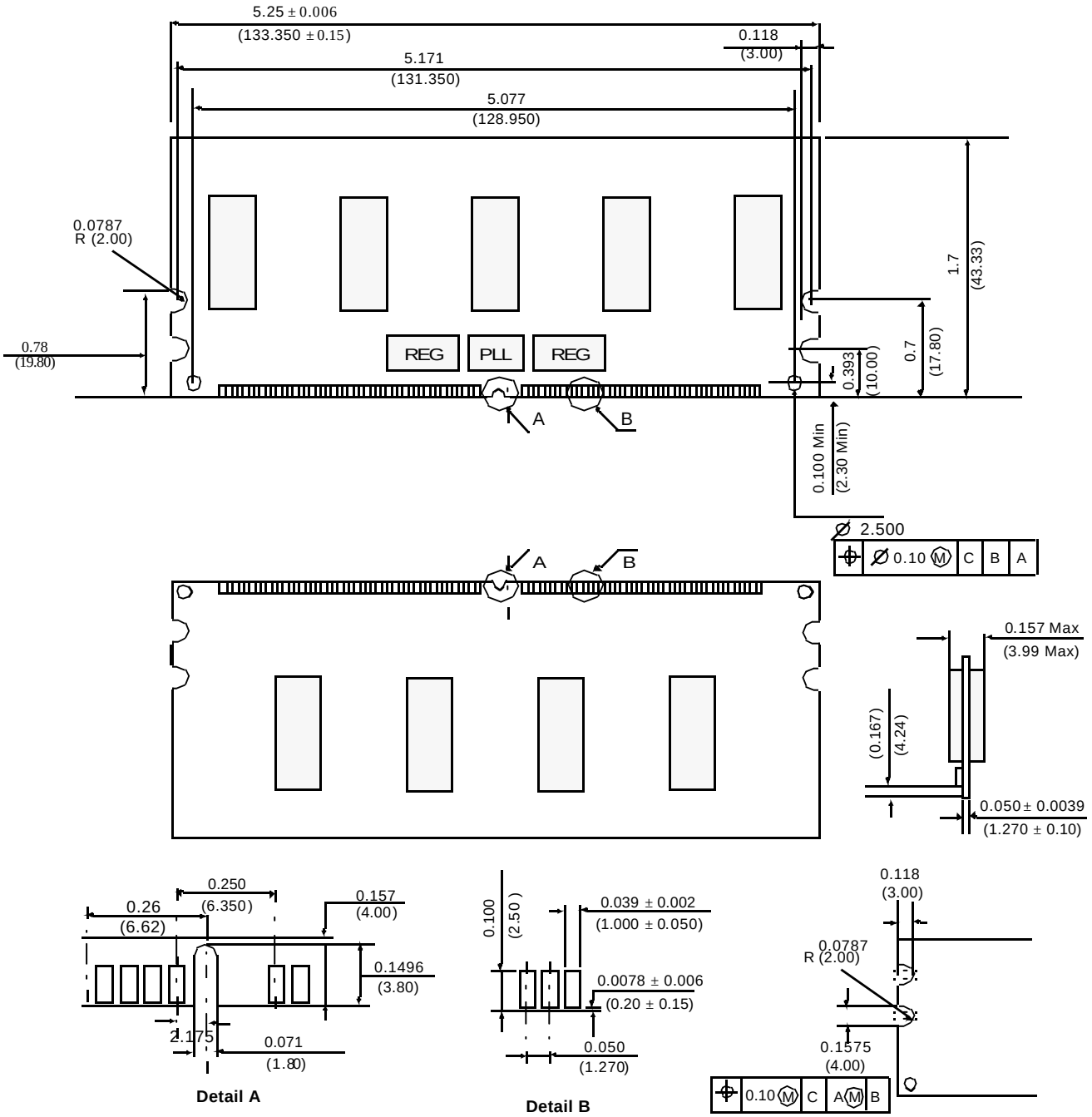
COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note
Register	Extended MRS		H	X	L	L	L	L	OP CODE			1, 2
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address A0~A9	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address A0~A9	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
		Exit	L	H	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM			H	X					X			8
No operation (NOP) : Not defined			H	X	H	X	X	X	X			9
					L	H	H	H				9

Note : 1. OP Code : Operand Code. A_0 ~ A_{12} & BA_0 ~ BA_1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3. Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1 : Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
5. If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

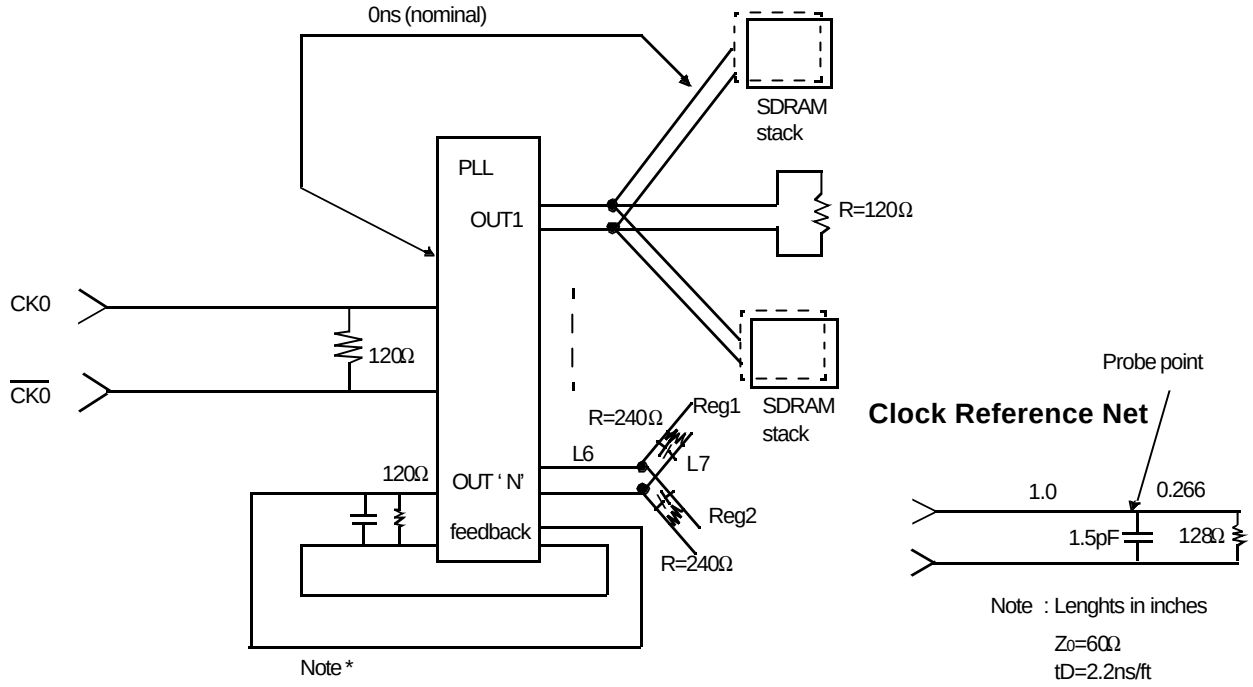
PACKAGE DIMENSIONS

Units : Inches (Millimeters)



Tolerances : ± 0.005(.13) unless otherwise specified
The used device is 32Mx8 SDRAM, TSOP
SDRAM Part NO : K4H560838B-TC

184 Pin DDR Registered DIMM Clock Topolgy



Notes* :

1. The Clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns(nominal).
2. Input,output, and feedback clock lines are terminated from line to leine as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any addtional PLL outputs will be wired in a similar maner.
4. termination resistors for the PLL feedback path clocks are loacted after the pins of the PLL.