

M383L6423AT0

184pin Registered DDR SDRAM MODULE

512MB DDR SDRAM MODULE

(64Mx72(32Mx72*2 bank) based on 32Mx8 DDR SDRAM)

Registered 184pin DIMM
72-bit ECC/Parity

Revision 0.4

April. 2000

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Revision History

Revision 0 (Aug 1998)

1. First release for internal usage

Revision 0.1 (Aug. 1999)

1. Modified binning policy

From	To
-Z (133Mhz)	-Z (133Mhz/266Mbps@CL=2)
-8 (125Mhz)	-Y (133Mhz/266Mbps@CL=2.5)
-0 (100Mhz)	-0 (100Mhz/200Mbps@CL=2)

2. Modified the following AC spec values

	From.		To.		
	-Z	-0	-Z	-Y	-0
tAC	+/- 0.75ns	+/- 1ns	+/- 0.75ns	+/- 0.75ns	+/- 0.8ns
tDQSCK	+/- 0.75ns	+/- 1ns	+/- 0.75ns	+/- 0.75ns	+/- 0.8ns
tDQSQ	+/- 0.5ns	+/- 0.75ns	+/- 0.5ns	+/- 0.5ns	+/- 0.6ns
tDS/tDH	0.5 ns	0.75 ns	0.5 ns	0.5 ns	0.6 ns
tCDLR ^{*1}	2.5tCK-tDQSS	2.5tCK-tDQSS	1tCK	1tCK	1tCK
tPRE ^{*1}	1tCK +/- 0.75ns	1tCK +/- 1ns	0.9/1.1 tCK	0.9/1.1 tCK	0.9/1.1 tCK
tRPST ^{*1}	tCK/2 +/- 0.75ns	tCK/2 +/- 1ns	0.4/0.6 tCK	0.4/0.6 tCK	0.4/0.6 tCK
tHZQ ^{*1}	tCK/2 +/- 0.75ns	tCK/2 +/- 1ns	+/- 0.75ns	+/- 0.75ns	+/-0.8ns

^{*1} : Changed description method for the same functionality. This means no difference from the previous version.

3. Changed the following AC parameter symbol From tDQCK To tAC
Output data access time from CK/CK .

Revision 0.2 (Sept. 1999)

1. Changed the ordering information.

- 1-1. Exclude KM mark.

From	To
KMM381...	M381.....

- 1-2. PCB Revision

From	To
- Blank: 1st generation	- 0: 1st generation
- A : 2nd generation	- 1: 2nd generation
- B : 2nd generation	- 2: 3rd generation
Example:KMM383L6423AT	M383L6423AT0

- 1-3. Modified binning policy

From	To
- 0 (100Mhz/200Mbps@CL=2)	- A0 (100Mhz/200Mbps@CL=2)
- Z (133Mhz/266Mbps@CL=2)	- A2 (133Mhz/266Mbps@CL=2)
- Y (133Mhz/266Mbps@CL=2.5)	- B0 (133Mhz/266Mbps@CL=2.5)

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Revision 0.3 (December. 1999)

1. Changed from 3.3V to 2.5V in VDDSPD power.

Revision 0.4 (April. 2000)

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1. Changed pin 90 from WP to NC in pin configuration table.
2. Removed WP in pin description.

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3. Changed bypassing to reflect common Vdd/Vddq plane.
4. Added A12, BA1.
5. Removed WP from serial PD.

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6. Changed Power & DC operating condition.

Parameter	Symbol	From		To	
		Min	Max	Min	Max
I/O Reference voltage	VREF	1.15	1.35	0.49*VDDQ	0.51*VDDQ
Input logic high voltage	VIH(DC)	VREF+0.18	VDDQ+0.3	VREF+0.15	VDDQ+0.3
Input logic low voltage	VIL(DC)	-0.3	VREF-0.18	-0.3	VREF-0.15
Input leakage current	II	-5	5	-2	2
Output High Current (V _{OUT} = 1.95V)	IOH	-15.2		-16.8	
Output Low Current (V _{OUT} = 0.35V)	IoL	15.2		16.8	

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7. Added Overshoot/Undershoot spec
 - . Vih(max) = 4.2V, the overshoot voltage duration is ≤ 3ns at VDD.
 - . Vil(min) = -1.5V, the overshoot voltage duration is ≤ 3ns at VSS.

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8. Changed AC operating conditions as follows.

Parameter/Condition	Symbol	From		To	
		Min	Max	Min	Max
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.35		VREF + 0.31	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.35		VREF - 0.31
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	0.62	VDDQ+0.6

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9. Changed AC parameters as follows.

Parameter	from	to	Comments
tDQSQ	+/- 0.5(PC266), +/- 0.6(PC200)	+0.5(PC266), +0.6(PC200)	
tDV	+/- 0.35tCK	-	Removed

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10. Added AC parameters as follows

Parameter	Symbol	-A2(PC266@CL=2)		-B0(PC266@CL=2.5)		-A0(PC200@CL=2)	
		Min	Max	Min	Max	Min	Max
Output DQS valid window	tQH	tHPmin -0.75ns	-	tHPmin -0.75ns	-	tHPmin -1.0ns	-
Clock half period	tHP	tCLmin or tCH-	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-
QFC setup to first DQS edge on reads	tQCS	0.9	1.1	0.9	1.1	0.9	1.1
QFC hold after last DQS edge on reads	tDQCH	0.4	0.6	0.4	0.6	0.4	0.6
Write command to QFC delay on write	tQCSW		4.0		4.0		4.0
Write burst end to QFC delay on write	tQCHW	1.25ns	0.5tCK	1.25ns	0.5tCK	1.25ns	0.5tCK
Write burst end to QFC delay on write interrupted by Precharge	tQCHWI	1.25ns	1.5tCK	1.25ns	1.5tCK	1.25ns	1.5tCK

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M383L6423AT0 DDR SDRAM 184pin DIMM

64Mx72 DDR SDRAM 184pin DIMM based on 32Mx8

GENERAL DESCRIPTION

The Samsung M383L6423AT0 is 64M bit x 72 Double Data Rate SDRAM high density memory modules based on first generation of 256Mb DDR SDRAM respectively. The Samsung M383L6423AT0 consists of eighteen CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages, mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M383L6423AT0 is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURE

- Performance range

Part No..	Max Freq. (Speed)	Interface
M383L6423AT0-C(L)A2	133MHz(7.5ns@CL=2)	SSTL_2
M383L6423AT0-C(L)B0	133MHz(7.5ns@CL=2.5)	
M383L6423AT0-C(L)A0	100MHz(10ns@CL=2)	

- Power supply
Vdd: 2.5V ± 0.2V
Power: C - normal, L - Low power
- MRS cycle with address key programs
CAS Latency (Access from column address):2,2.5
Burst length ;2, 4, 8
Data scramble ;Sequential & Interleave
- Serial presence detect with EEPROM
- PCB : **Height 1700 (mil)**, double sided component

PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	/RESET	41	A2	71	NU	102	NC	133	DQ31	163	NU
11	VSS	42	VSS	72	DQ48	103	*A13	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	NU	106	DQ13	137	CK0	167	NC,FETEN
15	VDDQ	46	VDD	76	NU	107	DM1	138	/CK0	168	VDD
16	NU	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	NU	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
CB0 ~ CB7	Check bit(Data-in/data-out)
DQS0 ~ DQS8	Data Strobe input/output
CK0,CK0	Clock input
CKE0,CKE1	Clock enable input
CS0, CS1	Chip select input
RAS	Row address strobe
CAS	Column address strobe
WE	Write enable
DM0 ~ DM8	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQs(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.5V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
RESET	Reset enable
FETEN	FET Enable
NC	No connection

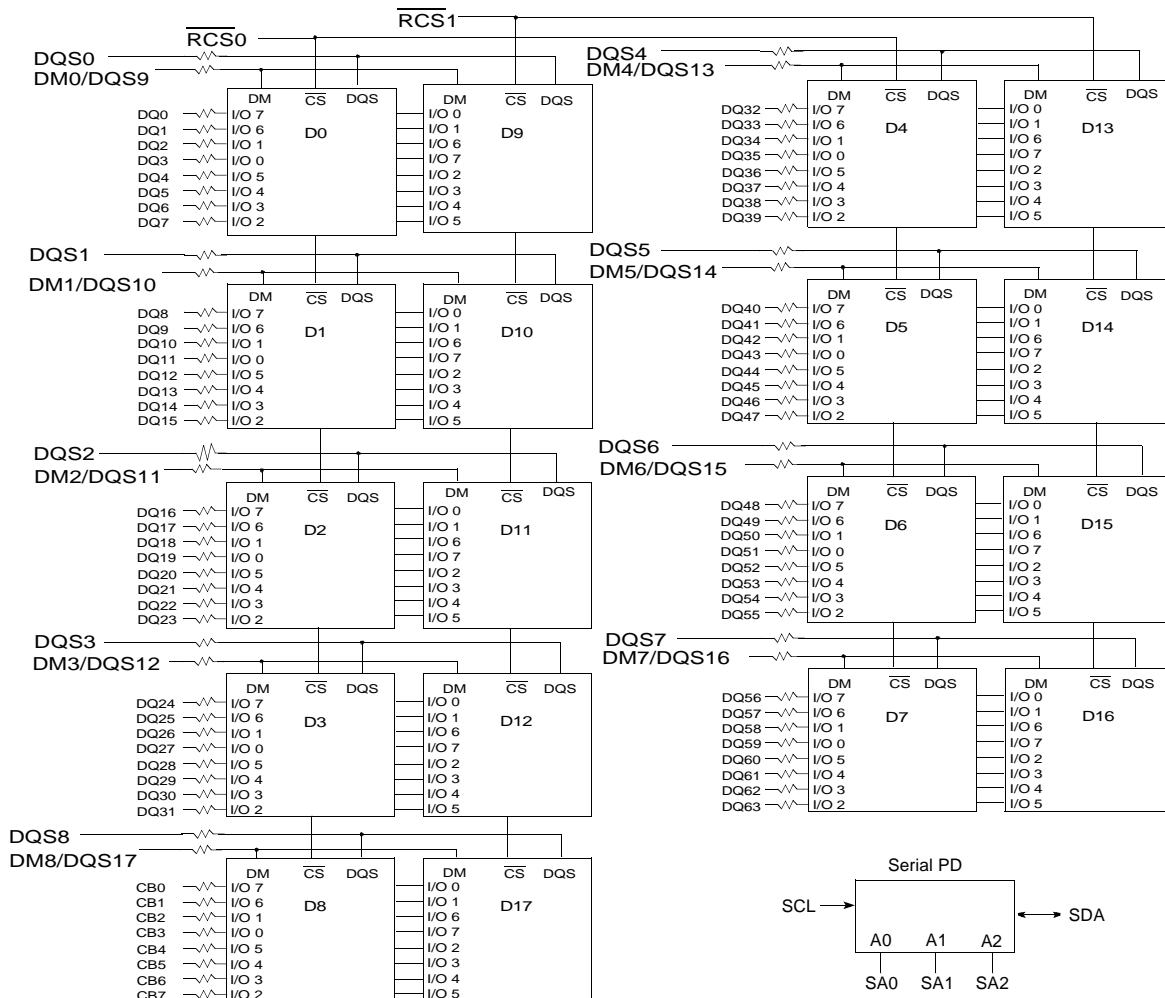
* These pins are not used in this module.

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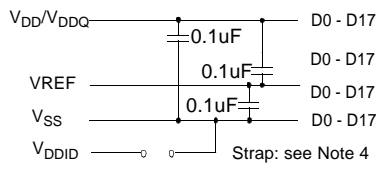
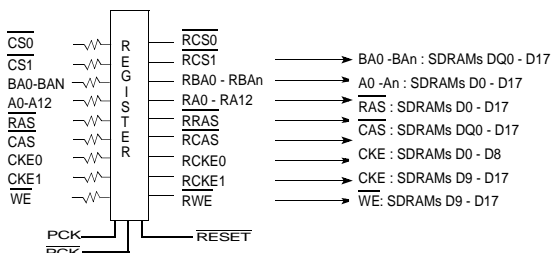
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Functional Block Diagram



CK0, CK0 → PLL*
 * Wire per Clock Loading table/wiring Diagrams



- Notes:
1. DQ-to-I/O wiring is shown as recommended but may be changed.
 2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
 3. DQ, DQS, DM resistors: 22 Ohms.
 4. VDDID strap connections (for memory device VDD, VDDQ):
 STRAP OUT (OPEN): VDD = VDDQ
 STRAP IN (VSS): VDD≠VDDQ.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on V _{DD} supply relative to Vss	V _{DD}	-1.0 ~ 4.6	V
Voltage on V _{DDQ} supply relative to Vss	V _{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	18	W
Short circuit current	I _{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS (SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V _{DD} of 2.5V)	V _{DD}	2.3	2.7		
I/O Supply voltage	V _{DDQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	0.49*V _{DDQ}	0.51*V _{DDQ}	V	1
I/O Termination voltage(system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{DDQ} +0.3	V	
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	V _{IN} (DC)	-0.3	V _{DDQ} +0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	V _{ID} (DC)	0.3	V _{DDQ} +0.6	V	3
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current (V _{OUT} = 1.95V)	I _{OH}	-16.8		mA	
Output Low Current (V _{OUT} = 0.35V)	I _{OL}	16.8		mA	

Notes 1. V_{REF} is expected to be equal to 0.5*V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value
 2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}
 3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{\text{CK}}$.

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DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, TA=0 to 70°C

Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-A2	-B0	-A0		
Operating Current (One Bank Active)	IDD1	Burst=2 tRC=tRC(min), CL=2.5 I _{OUT} =0mA, Active-Read-Precharge		T.B.D	T.B.D	T.B.D	mA	1
Precharge Power-down Standby Current	IDD2P	CKE≤VIL(max), tCK=tCK(min), All banks idle		T.B.D			mA	
Precharge Standby Current in Non Power-down mode	IDD2N	CKE≥VIH(min), \overline{CS} ≥VIH(min), tCK=tCK(min)		T.B.D			mA	
Active Standby Current in Power-down mode	IDD3P	All banks idle, CKE≤VIL(max), tCK=tCK(min)		T.B.D			mA	
Active Standby Current in Non Power-down mode	IDD3N	One bank; Active-Precharge, tRC=tRAS(max), tCK=tCK(min)		T.B.D			mA	
Operating Current(Read)	IDD4R	Burst=2, tCK=tCK(min), I _{OUT} =0mA	2.5	T.B.D	T.B.D	T.B.D	mA	1
			2	T.B.D	T.B.D	T.B.D		
Operating Current(Write)	IDD4W	Burst=2, tCK=tCK(min)	2.5	T.B.D	T.B.D	T.B.D	mA	1
			2	T.B.D	T.B.D	T.B.D		
Auto Refresh Current	IDD5	tRC≥tRFC(min)		T.B.D			mA	2
Self Refresh Current	IDD6	CKE≤0.2V		T.B.D			mA	

- Note :** 1. Measured with outputs open.
2. Refresh period is 64ms

AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	1
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	2
Input Differential Voltage, CK and CK inputs	VID(AC)	0.62	VDDQ+0.6	V	3
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	4

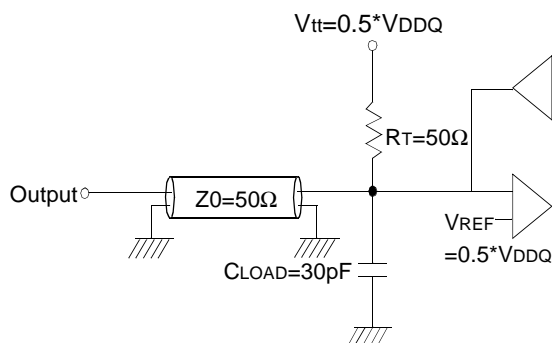
- Note 1. Vih(max) = 4.2V. The overshoot voltage duration is ≤ 3ns at VDD.
2. Vil(min) = -1.5V. The undershoot voltage duration is ≤ 3ns at VSS.
3. VID is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
4. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

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AC OPERATING TEST CONDITIONS ($V_{DD}=2.5V$, $V_{DDQ}=2.5V$, $T_A= 0$ to $70^{\circ}C$)

Parameter	Value	Unit	Note
Input reference voltage for Clock	$0.5 * V_{DDQ}$	V	
Input signal maximum peak swing	1.5	V	
Input signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	$V_{REF}+0.31/V_{REF}-0.31$	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Load Circuit		



(Fig. 1) Output Load Circuit (SSTL_2)

Input/Output CAPACITANCE ($V_{DD}=2.5$, $V_{DDQ}=2.5V$, $T_A= 25^{\circ}C$, $f=1MHz$)

Parameter	Symbol	Min	Max	Unit
Input capacitance($A_0 \sim A_{12}$, $BA_0 \sim BA_1$, \overline{RAS} , \overline{CAS} , \overline{WE})	CIN1	-	12	pF
Input capacitance($\overline{CKE}_0, \overline{CKE}_1$)	CIN2	-	12	pF
Input capacitance($\overline{CS}_0, \overline{CS}_1$)	CIN3	-	11	pF
Input capacitance($\overline{CLK}_0, /\overline{CLK}_0$)	CIN4	-	12	pF
Input capacitance($DM_0 \sim DM_8$)	CIN5	-	16	pF
Data & DQS input/output capacitance($DQ_0 \sim DQ_{63}$)	COUT1	-	16	pF
Data input/output capacitance($CB_0 \sim CB_7$)	COUT2	-	16	pF

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AC CHARACTERISTICS. (These AC characteristics were tested on the Component)

Parameter	Symbol	- A2(PC266@CL=2)		- B0(PC266@CL=2.5)		- A0(PC200@CL=2)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	65		65		70		ns		
Refresh row cycle time	tRFC	75		75		80		ns		
Row active time	tRAS	45	12K	48	12K	48	12K	ns		
RAS to CAS delay	tRCD	20		20		20		ns		
Row precharge time	tRP	20		20		20		ns		
Row active to Row active delay	tRRD	15		15		15		ns		
Write recovery time	tWR	2		2		2		tCK		
Last data in to Read command	tCDLR	1		1		1		tCK		
Last data in to Write command	tCDLW	0		0		0		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	CL=2.0	tCK	7.5	15	10	15	10	15	ns	
	CL=2.5		7	15	7.5	15	8	15	ns	
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/CK	tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to output data edge	tDQSQ	-	+0.5	-	+0.5	-	+0.6	ns		
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
Data out high impedance time from CK/	tHZQ	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns	2	
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRE	0		0		0		ns	3	
DQS-in hold time	tWPRE	0.25		0.25		0.25		tCK		
DQS-in high level width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
DQS-in low level width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time	tIS	0.9		0.9		1.1		ns		
Address and Control Input hold time	tIH	0.9		0.9		1.1		ns		
Mode register set cycle time	tMRD	15		15		16		ns		
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns		
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns		
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns		
Power down exit time	tPDEX	10		10		10		ns		
Exit self refresh to write command	tXSW	95				116		ns		

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Parameter		Symbol	-A2(PC266@CL=2)		-B0(PC266@CL=2.5)		-A0(PC200@CL=2)		Unit	Note
			Min	Max	Min	Max	Min	Max		
Exit self refresh to bank active command		tXSA	75		75		80		ns	7
Exit self refresh to read command		tXSR	200		200		200		Cycle	
Refresh interval time	256Mb	tREF	7.8		7.8		7.8		us	1
Output DQS valid window		tQH	tHPmin -0.75ns	-	tHPmin -0.75ns	-	tHPmin -1.0ns	-	ns	
Clock half period		tHP	tCLmin or tCH-	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
DQS write postamble time		tWPST	0.25		0.25		0.25		tCK	4
Auto precharge write recovery + Precharge time		tDAL	35		35		35		ns	
QFC setup to first DQS edge on reads		tQCS	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
QFC hold after last DQS edge on reads		tDQCH	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write command to QFC delay on write		tQCSW		4.0		4.0		4.0	ns	
Write burst end to QFC delay on write		tQCHW	1.25ns	0.5tCK	1.25ns	0.5tCK	1.25ns	0.5tCK		5
Write burst end to QFC delay on write interrupted by Precharge		tQCHWI	1.25ns	1.5tCK	1.25ns	1.5tCK	1.25ns	1.5tCK		6

Note : 1. Maximum burst refresh of 8

2. tHZQ transitions occurs in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving.
3. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
4. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
5. The value of tQCSW min. is 1.25ns from the last low going data strobe edge to \overline{QFC} high. And the value of tQCSW max. is 0.5tck from the first high going clock edge after the last low going data strobe edge to QFC high.
6. the value of tQCSWI max. is 1.5tck from the first high going clock edge after the last low going data strobe edge to QFC high.
7. A write command can be applied with tRCD satisfied after this command.

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SIMPLIFIED TRUTH TABLE

COMMAND		CKEn-1	CKEn	\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0,1	A10/AP	A11,A12 A9 ~ A0	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L							3	
		Exit	L	H	L	H	H	H	X		3	
			H	X							X	X
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	5
	All Banks								X	H		
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
	Exit	L	H	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	V	V	V					
DM		H	X					X		8		
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9	
				L	H	H	H				9	

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note : 1. OP Code : Operand Code. A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

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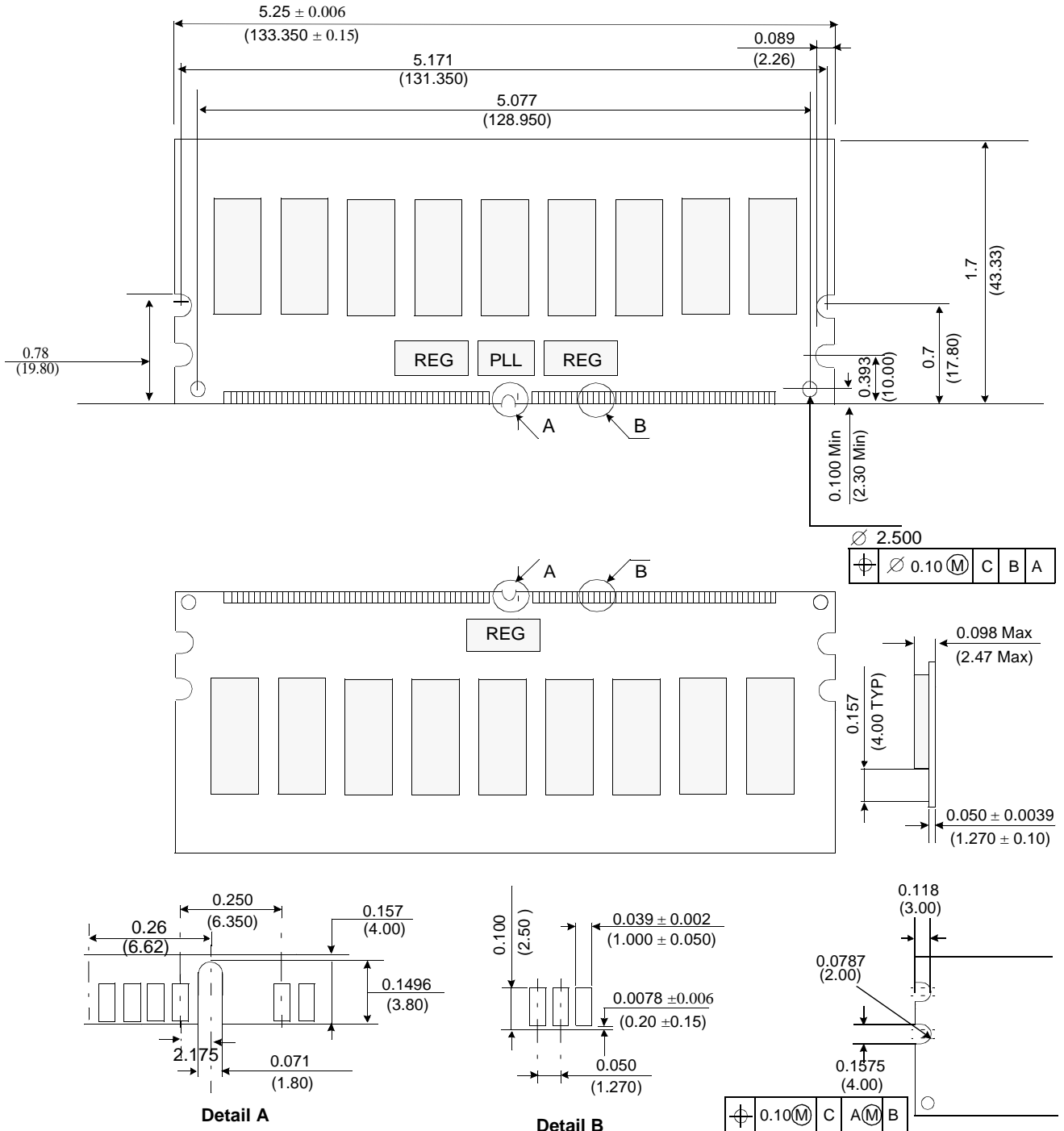
6. During burst write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

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PACKAGE DIMENSIONS

Units : Inches (Millimeters)

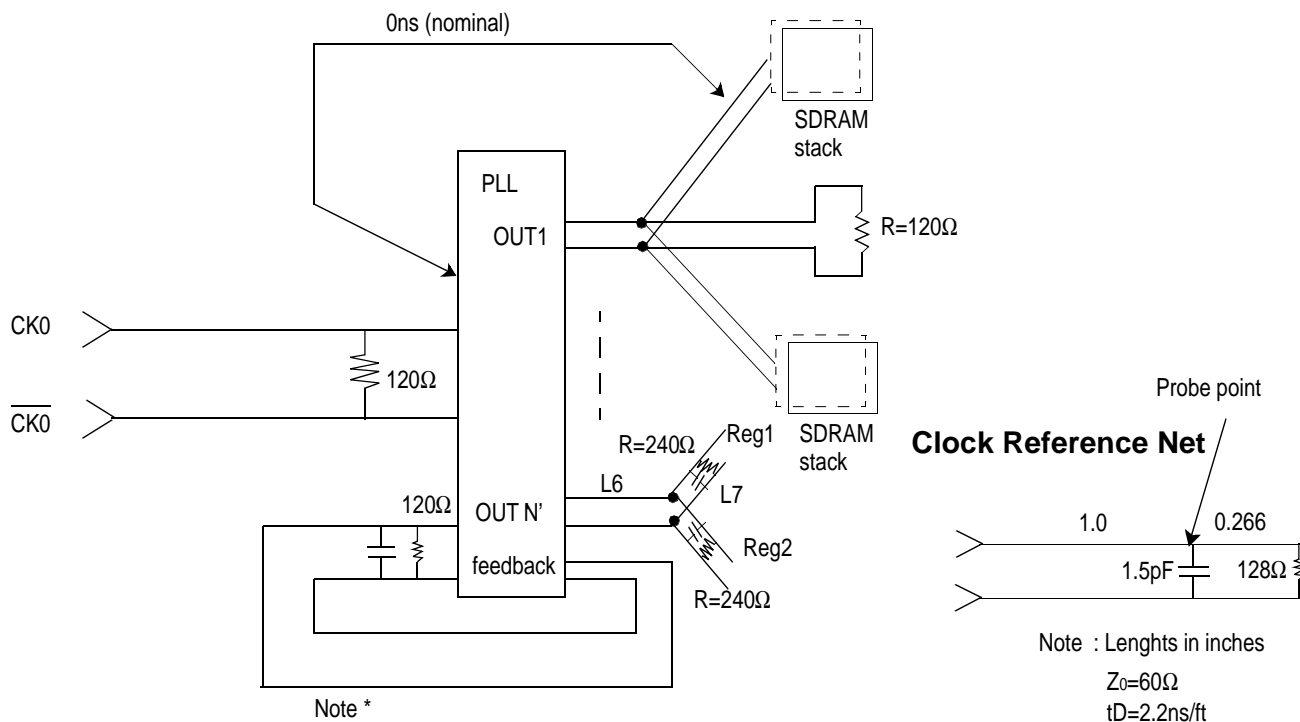


Tolerances : ± 0.005 (.13) unless otherwise specified
 The used device is 32Mx8 SDRAM, TSOP
 SDRAM Part NO : K4H560838A-TC

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184 Pin DDR Registered DIMM Clock Topolgy



Notes* :

1. The Clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns(nominal).
2. Input,output, and feedback clock lines are terminated from line to leine as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar maner.
4. termination resistors for the PLL feedback path clocks are loacted after the pins of the PLL.