Revision History

Version 1.0 (May 2003)
- First Copy *- Based on the 1.0 ver. (July 2002) 288Mbit D-die SO-RIMM^{TM} Module Datasheet.*

Version 1.1 (Aug. 2003)
- Add PGA type 144MB NexMod Module. *- Add the discription of index pin marking.* *- Correct the physical dimension of PGA NexMod Module.*

Version 1.2 (Dec . 2003)
- Add interposer ball diameter

MN18R1624(8)DF0
MP18R1624(8)DF0

(16Mx18)*4(8)pcs NexMod™ Module based on 288Mb D-die, 32s banks,16K/32ms Refresh, 2.5V

Overview

The NexMod™ module is a general purpose for high-performance memory subsystem suitable for a broad range of applications including networking, digital consumer, mobile "Thin and light" PCs, and other applications systems where high bandwidth and low latency are required.

The NexMod product family addresses the needs of customers designing space-constrained systems. The Single-Channel RDRAM® NexMod memory module is a cost effective, small volumetric form factor solution that provides virtually all the components needed for a complete Rambus® Channel. The NexMod module simplifies system layout and speeds time-to-market by placing the end-of-channel termination, VRM(Voltage Regulator Module) and DRCG(Direct Rambus™ Clock Generator) all on the module.

The NexMod module is consisted of 288Mb RDRAM devices. These are extremely high speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level(RSL) technology permits up to 1066MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers up to at 0.94ns per two bytes (7.5ns per 16 bytes)

The RDRAM Architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The seperate control and data buses with independent row and column control yield high bus efficiency. The RDRAM device's thirty-two bank architecture supports up to four simultaneous transactions per device.

Features

- ♦ High speed up to 1066MHz RDRAM storage
- ♦ 200 bottom connector pads with 1.27mm pad spacing
- ♦ Module footprint : 1.1 inches x 2.0 inches
- ♦ Module PCB size : 50.80mm x 27.94mm x 1.0mm
- ♦ Interposer type-1 PCB size: 7.62mm x 26.67mm x 1.1mm
- ♦ Interposer type-2 PCB size: 7.62mm x 26.67mm x 2.1mm
- ♦ Each RDRAM device has 32 banks, for a total of 128/256 banks on 144MB/288MB module respectively
- ♦ Serial Presence Detect(SPD) support
- ♦ Operates from a 2.5 volt supply (± 5%)
- ♦ Low power and powerdown self refresh modes
- ♦ Sperate Row and Column buses for heigher efficiency
- ♦ WBGA package (92 balls)
- ♦ Simplifies system layout and speeds time-to-market
  - Terminations/DRCG/VRM(generates Vterm) on module
  - RDRAM VREF generated on module
- ♦ Stacked PCB design improves signal integrity and margin
  - Shortened channel length by stacking PCB and placing termination on module
  - Optional BGA or PGA connectors to mainboard enable mounting flexibility
  - BGA interposers within module

Key Timing Parameters/Part Numbers

The following table lists the frequency and latency bins available for NexMod modules.

Table 1: Part Number by Freq. & Latency

Organization	Speed			Part Number
	Bin	I/O Freq. (MHz)	t_{rac} (Row Access Time) ns	
64M x 18	-CT9	1066	32P	MN[a](P[b])18R1624DF0-CT9
	-CM8	800	40	MN(P)18R1624DF0-CM8
128M x 18	-CT9	1066	32P	MN(P)18R1628DF0-CT9
	-CM8	800	40	MN(P)18R1628DF0-CM8

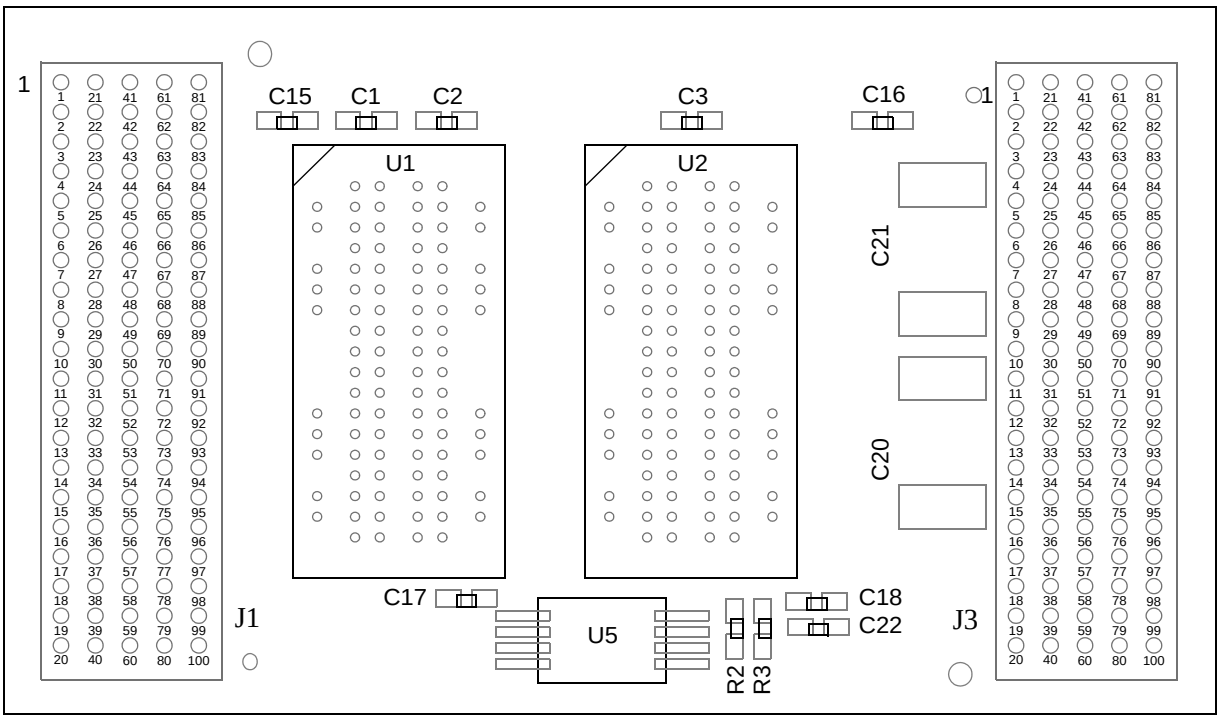
a. BGA type connector
b. PGA type connector

Form Factor

The NexMod modules are offered in 200-ball(or pin) 1.27mm bottom connector ball(or pin) pitch form factor suitable for 200 contact NexMod connectors. Figure 1 below, shows a eight device NexMod module.

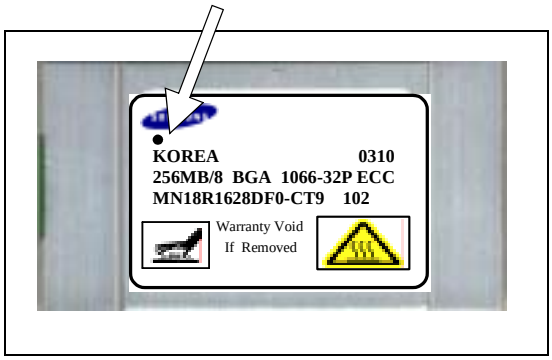
Figure 1 : NexMode Module shown with heat spreader removed

Figure 2 : NexMode Module Pin Location



J1 connector **J3 connector**

The marker"● " is directing the pin #1 of J1 connector.



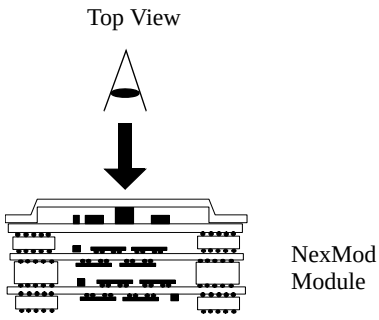


Table 2: Module Ball (or Pin) Numbers and Signal Names

Table 2a : J1 Connector

Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
A1	Vdd	A21	Vdd	A41	Vcmos	A61	Vcmos	A81	Vcmos
A2	Vdd	A22	SCK	A42	Gnd	A62	DQA8	A82	Gnd
A3	Vdd	A23	DQA6	A43	Gnd	A63	CMD	A83	Vterm*
A4	Vdd	A24	DQA4	A44	Gnd	A64	DQA7	A84	Vterm*
A5	Vdd	A25	DQA2	A45	Gnd	A65	DQA5	A85	Vterm*
A6	Vdd	A26	DQA0	A46	Gnd	A66	DQA3	A86	Gnd
A7	Gnd	A27	CFM	A47	Gnd	A67	DQA1	A87	Gnd
A8	Gnd	A28	CFMN	A48	Gnd	A68	CTMN	A88	CTMN-DRCG*
A9	Gnd	A29	ROW1	A49	Gnd	A69	CTM	A89	CTM-DRCG*
A10	Gnd	A30	COL4	A50	Gnd	A70	ROW2	A90	Gnd
A11	Gnd	A31	COL2	A51	Gnd	A71	ROW0	A91	Vref
A12	Gnd	A32	COL0	A52	Gnd	A72	COL3	A92	Vref
A13	Gnd	A33	DQB0	A53	Gnd	A73	COL1	A93	Gnd
A14	Vdd	A34	DQB2	A54	Gnd	A74	DQB1	A94	SIN
A15	Vdd	A35	DQB4	A55	Gnd	A75	DQB3	A95	Gnd
A16	Vdd	A36	DQB6	A56	Gnd	A76	DQB5	A96	Gnd
A17	SA0	A37	Gnd	A57	Gnd	A77	DQB7	A97	Gnd
A18	SA1	A38	REFCLK	A58	Gnd	A78	DQB8	A98	Vdd3.3
A19	SA2	A39	SDA	A59	SWP	A79	Gnd	A99	Vdd3.3
A20	PCLK/M	A40	Gnd	A60	SYNCLK/N	A80	SVdd	A100	SCL

* Note : Vterm, CTMN-DRCG and CTM-DRCG pins are only used if internal VRM and DRCG options are not used on the NexMod Module.

Table 2b : J3 Connector

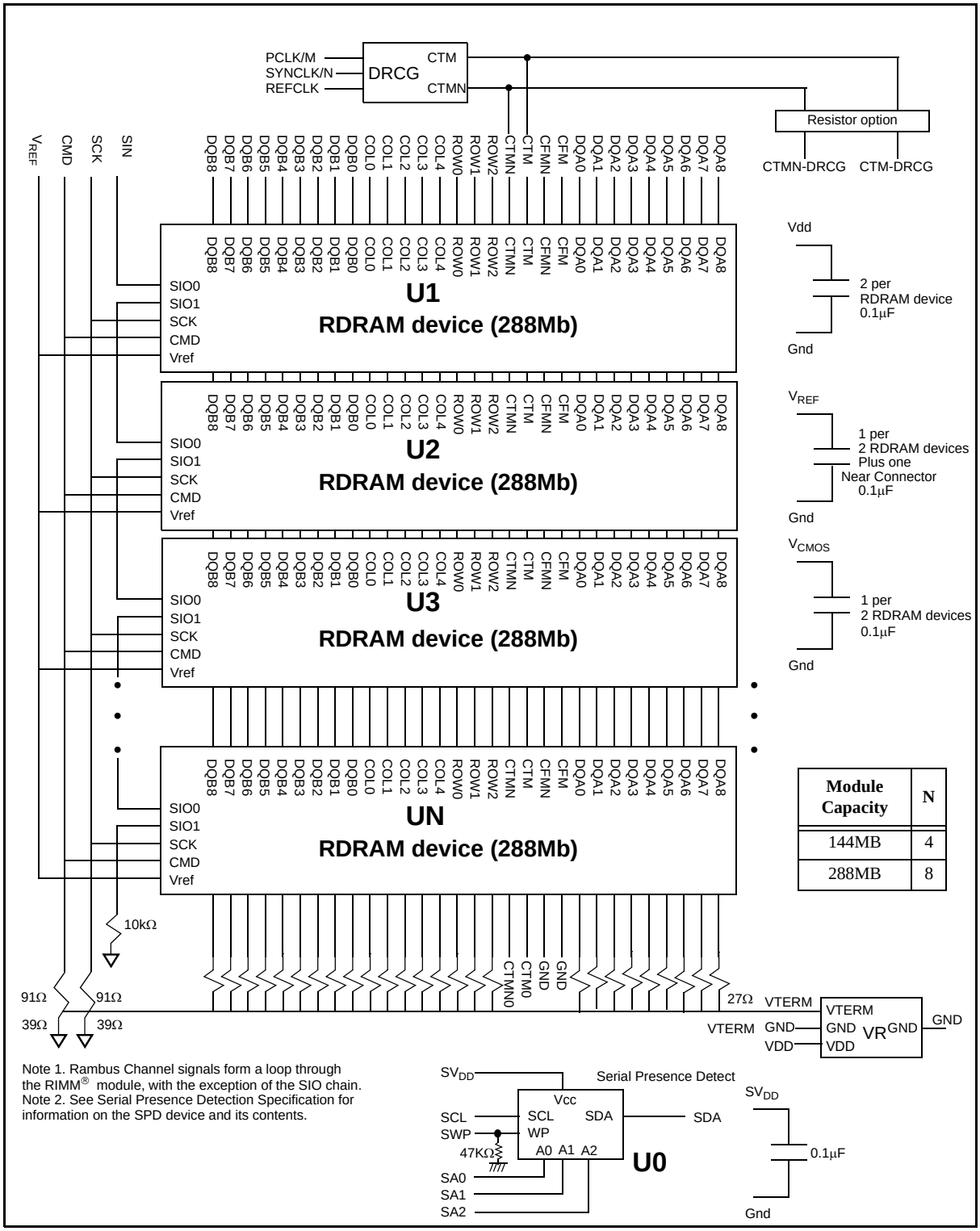
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
B1	Vcmos	B21	Vcmos	B41	Vcmos	B61	Vdd	B81	Vdd
B2	Gnd	B22	RESERVED*	B42	Gnd	B62	RESERVED*	B82	Vdd
B3	Vterm	B23	RESERVED*	B43	Gnd	B63	RESERVED*	B83	Vdd
B4	Vterm	B24	RESERVED*	B44	Gnd	B64	RESERVED*	B84	Vdd
B5	Vterm	B25	RESERVED*	B45	Gnd	B65	RESERVED*	B85	Vdd
B6	Gnd	B26	RESERVED*	B46	Gnd	B66	RESERVED*	B86	Vdd
B7	Gnd	B27	RESERVED*	B47	Gnd	B67	RESERVED*	B87	Gnd
B8	Gnd	B28	RESERVED*	B48	Gnd	B68	RESERVED*	B88	Gnd
B9	Gnd	B29	RESERVED*	B49	Gnd	B69	RESERVED*	B89	Gnd
B10	Gnd	B30	RESERVED*	B50	Gnd	B70	RESERVED*	B90	Gnd
B11	Vref	B31	RESERVED*	B51	Gnd	B71	RESERVED*	B91	Gnd
B12	Vref	B32	RESERVED*	B52	Gnd	B72	RESERVED*	B92	Gnd
B13	Gnd	B33	RESERVED*	B53	Gnd	B73	RESERVED*	B93	Gnd
B14	RESERVED*	B34	RESERVED*	B54	Gnd	B74	RESERVED*	B94	Gnd
B15	Gnd	B35	RESERVED*	B55	Gnd	B75	RESERVED*	B95	Vdd
B16	Gnd	B36	RESERVED*	B56	Gnd	B76	RESERVED*	B96	Vdd
B17	Gnd	B37	RESERVED*	B57	Gnd	B77	Gnd	B97	Vdd
B18	Gnd	B38	RESERVED*	B58	Gnd	B78	Vdd	B98	Vdd
B19	Gnd	B39	Gnd	B59	Gnd	B79	Vdd	B99	Vdd
B20	Gnd	B40	Gnd	B60	Gnd	B80	Gnd	B100	Gnd

* Note : Reserved pins are used during module assembly at the factory. Do not connect in system layout.

Table 3 : Module Connector Pad Description

Signal	Pins	I/O	Type	Description
Gnd	A7, A8, A9, A10, A11, A12, A13, A37, A40, A42, A43, A44, A45, A46, A47, A48, A49, A50, A51, A52, A53, A54, A55, A56, A57, A58, A79, A82, A86, A87, A90, A93, A95, A96, A97, B2, B6, B7, B8, B9, B10, B13, B15, B16, B17, B18, B19, B20, B39, B40, B42, B43, B44, B45, B46, B47, B48, B49, B50, B51, B52, B53, B54, B55, B56, B57, B58, B59, B60, B77, B80, B87, B88, B89, B90, B91, B92, B93, B94, B100			Ground reference for connenctor pads, RDRAM core, and interface. 79 pads.
CFM	A27	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
CFMN	A28	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
CMD	A63	**I**	**V_{CMOS}**	Serial command input used to read from and write to the control registers. Also used for power management.
COL4.. COL0	A30, A72, B31, A73, A32	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.
CTM	A69	**O**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
CTMN	A68	**O**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
DQA8.. DQA0	A62, B64, A23, B65, A24, B66, A25, B67, A26	**I/O**	**RSL**	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. DQA8 is non-functional on modules with x16 RDRAM devices
DQB8.. DQB0	A78, A77, A36, A76, A35, A75, A34, A74, A33	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. DQB8 is non-functional on modules with x16 RDRAM devices.
ROW2.. ROW0	A70, A29, A71	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses.
SCK	A22	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	B14, B22, A23, B24, B25, B26, B27, B28, B29, B30, B31, B32, B33, B34, B35, B36, B37, B38, B62, B63, B64, B65, B66, B67, B68, B69, B70, B71, B72, B73, B74, B75, B76			These pads are not connected. These 33 connector pads are reserved for future use.
SA0	A17	**I**	**SVdd**	Serial Presence Detect Address 0.
SA1	A18	**I**	**SVdd**	Serial Presence Detect Address 1.
SA2	A19	**I**	**SVdd**	Serial Presence Detect Address 2.
SCL	A100	**I**	**SVdd**	Serial Presence Detect Clock

Signal	Pins	I/O	Type	Description
SDA	A39	**I/O**	**SVdd**	Serial Presence Detect Data(Open Collector I/O)
SIN	A94	**I/O**	**V_{CMOS}**	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM device on the module
SVdd	A80			SPD Voltage. Used for signals SCL, SDA, SWP, SA0, SA1 and SA2
SWP	A59	**I**	**SVdd**	Serial Presence Detect Write Protection(active high). When low, the SPD can be written as well as read
PCLK/M	A20		**Vdd3.3**	Phase detector input(DRCG)
SYN-CLK/N	A60		**Vdd3.3**	Phase detector input(DRCG)
REFCLK	A38		**Vdd3.3**	Reference clock(DRCG)
CTM-DRCG	A89	**I**	**RSL**	Clock to master routed to last device in channel. Positive polarity
CTMN-DRCG	A88	**I**	**RSL**	Clock to master routed to last device in channel. Negative polarity
Vdd3.3	A98, A99			Supply voltage for DRCG
Vcmos	A41, A61, A81, B1, B21, B41			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT
Vdd	A1, A2, A3, A4, A5, A6, A14, A15, A16, A21, B61, B78, B79, B81, B82, B83, B84, B85, B86, B95, B96, B97, B98, B99			Supply voltage for the RDRAM core and interface logic
Vref	A91, A92, B11, B12			Logic threshold reference voltage for RSL signals.



Module Capacity	N
144MB	4
288MB	8

Note 1. Rambus Channel signals form a loop through the RIMM® module, with the exception of the SIO chain.
Note 2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Figure 3: NexMod Module Functional Diagram

Absolute Maximum Ratings

Table 4 : Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C

DC Recommended Electrical Conditions

Table 5 : DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers CMOS I/O power supply at pad for 1.8V controllers	V_{DD} 1.8 - 0.1	V_{DD} 1.8 + 0.2	V V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{TERM}	Termination Voltage	1.8 - 0.2	1.8 + 0.2	V
V_{SPD}	Serial Presence Detector- Positive power supply	2.2	3.6	V

Table 6 : NexMod Module Capacity and Number of RDRAM device

NexMod Module Capacity	144MB	288MB
Number of 288Mb RDRAM devices	4	8

NexMod Module Current Profile

Table 7 : NexMod Module Current Profile

I_{DD}	NexMod Module Capacity:		144MB	288MB	Unit
	Number of 288Mb RDRAM devices		4	8	
	NexMod module power conditions [a b c]	Freq.	Max	Max	
I_{DD1}	One RDRAM device in Read[d], balance in NAP mode	-1066	712	728	mA
		-800	572	588	
I_{DD2}	One RDRAM device in Read[d], balance in Standby mode	-1066	1000	1400	mA
		-800	800	1120	
I_{DD3}	One RDRAM device in Read[d], balance in Active mode	-1066	1150	1750	mA
		-800	920	1400	
I_{DD4}	One RDRAM device in Write, balance in NAP mode	-1066	802	818	mA
		-800	632	648	
I_{DD5}	One RDRAM device in Write, balance in Standby mode	-1066	1090	1490	mA
		-800	860	1180	
I_{DD6}	One RDRAM device in Write, balance in Active mode	-1066	1240	1840	mA
		-800	980	1460	

a. Actual power will depend on memory controller and usage patterns. Power does not include Refresh Current.
b. Memory current only, Total power of module should include all active elements' power on termination module.
c. DRCG on NexMod module always consume power regardless internal DRCG option. (example: VDD = 3.0± 0.15V, IDD= Max. 150mA)
d. I/O current is a function of the % of 1's, to add I/O power for 50% 1's, X18 ECC module needs to add 290mA for the following: V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.

AC Electrical Specifications

Table 8 : AC Electrical Specifications

Symbol	Parameter and Conditions	Min	Typ	Max	Unit
Z_L	Module Impedance of RSL Signals	25.2	28	30.8	Ω
$Z_{UL\text{-}CMOS}$	Module Impedance of SCK and CMOS signals	23.8	28	32.2	Ω
T_{PD}	Propagation Delay variation of RSL signals. Average clock delay from pad to pad of all RSL clock nets (CTM, CTMN, CFM and CFMN)			See Table10[a,b]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} [b,c] for 4 and 8 device modules	-21		21	ps
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay	-250		250	ps
$\Delta T_{PD\text{-}SCK,CMD}$	Propagation delay variation of CMD signals with respect to SCK signal	-200		200	ps

a. Table 10 lists parameters and specifications for different storage capacity NexMod Modules that use 288Mb RDRAM devices.
b. T_{PD} or Average clock delay is defined as the delay from finger to finger of RSL signal.
c. If the NexMod module meets the following specification, then it is compliant to the specification. If the NexMod module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table 9 below.

Adjusted ΔT_{PD} Specification

Table 9 : Adjusted ΔT_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min / Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 4 and 8 device modules	+/-[17+(18*N*ΔZ0)][a]	-30	30	ps

a. Where: N = Number of RDRAM devices installed on the NexMod module
ΔZ0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

AC Electrical Specifications for NexMod Modules

Table 10: AC Electrical Specifications for NexMod Modules

Symbol	NexMod Module Capacity		144MB	288MB	Unit
	Number of 288Mb RDRAM devices		4	8	
	Parameter and Condition for NexMod modules	Freq.	Max	Max	
T_{PD}	Propagation Delay, all RSL signals	-1066	1.28	1.32	ns
		-800	1.28	1.32	
V_{α}/V_{IN}	Attenuation Limit	-1066	16.0	16.0	%
		-800	12.0	16.0	
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)	-1066	4.0	4.0	%
		-800	2.0	4.0	
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)	-1066	2.0	2.0	%
		-800	1.5	2.0	
R_{DC}	DC Resistance Limit	-1066	0.9	1.4	Ω
		-800	0.9	1.4	

Physical Dimension -1 (Top View layout dimension)

The following defines the NexMod module dimensions. All units are in millimeters.

The dimension without tolerance specification use the default tolerance of ±0.1[±0.004].

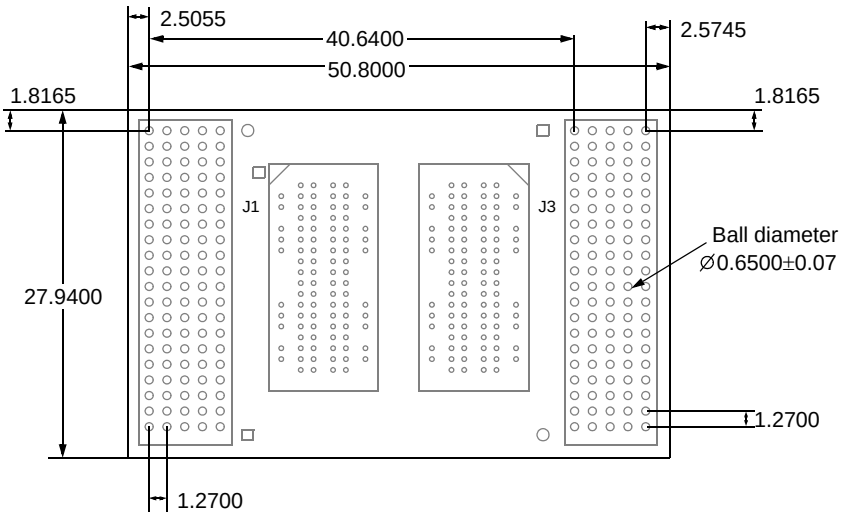


Figure 4a : Module physical dimension

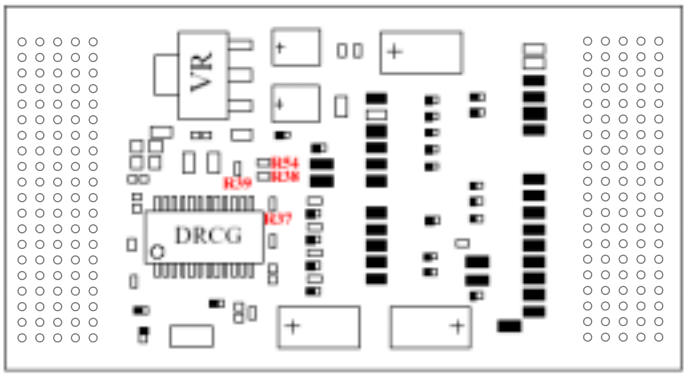


Figure 4b : termination module layout

Location of Resistors

Type	Populated Resitor	DRCG multiply factor
1	R39/R54	4
2	R39/R38	5.333
3	R37/R54	6
4*	R37/R38	8

* Only Type 4 module is available.

Figure 4: NexMode Module Top view layout Dimension

Physical Dimension -2 (Vertical dimension)

The following defines the NexMod module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate. The dimension without tolerance specification use the default tolerance of ±0.4[±0.015].

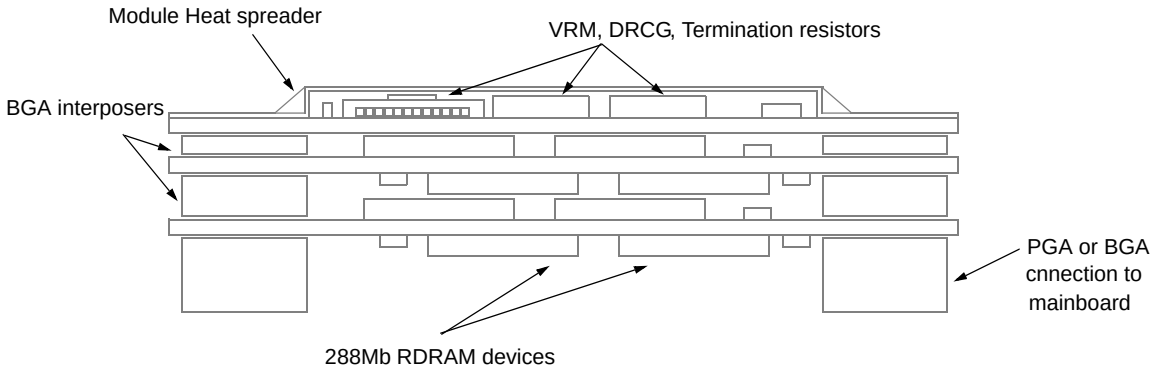


Figure 5a : NexMod Module vertical structure

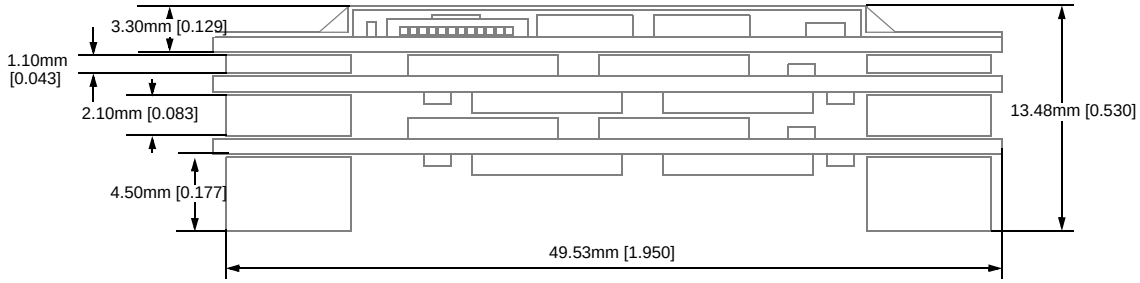


Figure 5b : 288MB NexMod Module with PGA connector vertical dimensions

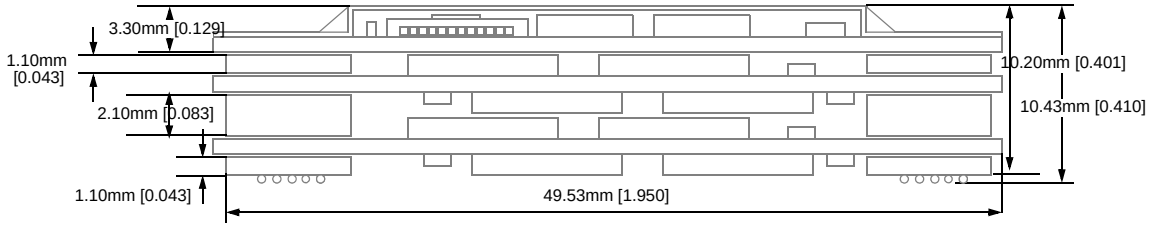


Figure 5c : 288MB NexMod Module with BGA connector vertical dimensions

Figure 5: NexMod Module Vertical Dimension

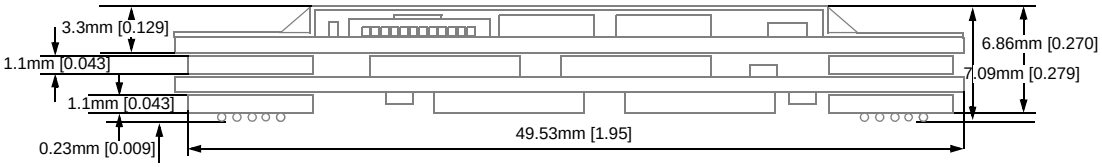


Figure 5d : 144MB NexMod Module with BGA connector vertical dimensions

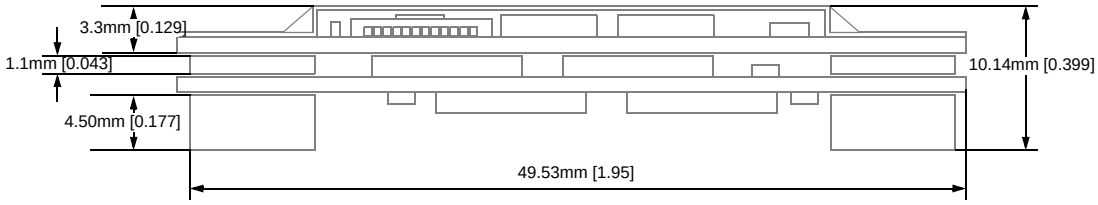


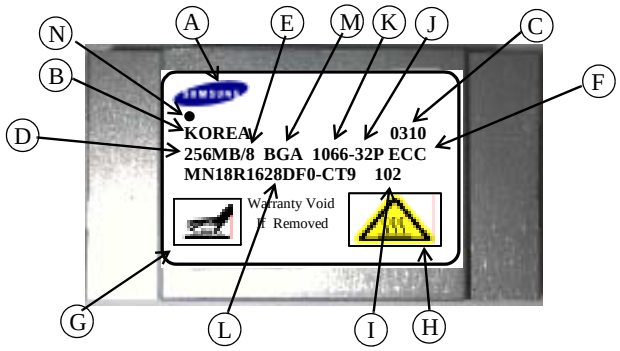
Figure 5e : 144MB NexMod Module with PGA connector vertical dimensions

Figure 5: NexMod Module Vertical Dimension

NexMod Module Marking

The NexMod modules available from Samsung are marked like Figure 5 below. This marking also assists users to specify and verify if the correct NexMod modules are installed in their systems. In the diagram, a label is shown attached to the NexMod module's heat spreader.

Information contained on the label is specific to the NexMod module and provides RDRAM device information without requiring removal of the NexMod module's heat spreader.



	Label Field	Description	Marked Text	Unit
A	Vendor Logo	NexMod Module Vendor SAMSUNG Logo Area	SAMSUNG	-
B	Country	Country of origin	KOREA	-
C	Year & Week code	Manufactured Year & Week code	yyww	-
D	Module Memory Capacity	Number of 9-bit MBytes of RDRAM storage in NexMod Module	128/256MB	MBytes
E	Number of RDRAM devices	Number of RDRAM devices contained in the NexMod Module	4/8	RDRAM devices
F	ECC Support	Indicates whether the NexMod module supports 9 (ECC) bit Bytes	ECC = 9 bit Bytes	-
G	Notice!	Hot surface caution notice.	-	-
H	Caution Logo	ISO Standard	-	-
I	Gerber & SPD Version	PCB Gerber file & SPD code version used on NexMod Module	Gerber : SPD : 2 = 1.3 ver.	-
J	tRAC	Row Access Time	-32P, -40	ns
K	Memory Speed	Data transfer speed for RDRAM device	1066, 800	MHz
L	Part No.	SAMSUNG NexMod Module part No.	See Table 1	-
M	Connector type	Module connector to main board	BGA/PGA	-
N	Index pin marking	the direction of J1 connector's pin #1	●	-

Figure 5: NexMod Module Marking Example

Table Of Contents

Document Version 1.2

Samsung Electronics Co. Ltd.
San #16 Banwol-ri, Taean-Eup Hwasung-City,
Gyeonggi-Do, KOREA

Telephone: 82-31-208-6369
Fax: 82-31-208-6799
http://www.intl.samsungsemi.com