Revision History

Version 0.1 (February 2004) - *Preliminary*
- First Copy *- Based on the 1.0 ver. (July 2002) 288Mbit D-die SO-RIMM™ Module Datasheet.*

Version 1.0 (May 2004)
- Eliminate "Preliminary"

MS18R1622(4/8)EH0

(16Mx18)*2(4/8)pcs SO-RIMM™ based on 288Mb E-die, 32s banks,16K/32ms Refresh, 2.5V

Overview

The SO-RIMM™ module is a general purpose high-performance memory subsystem suitable for a broad range of applications including networking systemsnetworking systems, digital con sumer systems, mobile "Thin and light" PCs, and other applications where high bandwidth and low latency are required.

The SO-RIMM module consists of 288Mb RDRAM® devices.These are extremely high speed CMOS DRAMs organized as 16M words by 18 bits. The use of Rambus Signaling Level(RSL) technology permits up to 1066MHz transfer rates while using conventional system and board design technologies. RDRAM devices are capable of sustained data transfers up to at 0.94ns per two bytes (7.5ns per 16 bytes)

The RDRAM Architecture enables the highest sustained bandwidth for multiple, simultaneous, randomly addressed, memory transactions. The seperate control and data buses with independent row and column control yield high bus efficiency. The RDRAM device's thirty-two bank architecture supports up to four simultaneous transactions per device.

Features

- High speed of 1066MHz and 800MHz per pin
- 160 edge connector pads with 0.65mm pad spacing
- Maximum module PCB size : 67.6mm x 31.25mm x 1.00mm (2.66" x 1.23" x 0.039")
- Each RDRAM device has 32 banks, for a total of 256,128,64 banks on each 288MB,144MB,72MB module respectively
- Gold plated edge connector pad contacts
- Serial Presence Detect(SPD) support
- Operates from a 2.5 volt supply (± 5%)
- Low power and powerdown self refresh modes
- Sperate Row and Column buses for heigher efficiency
- WBGA lead free package SO-RIMM Module(92 balls)

Key Timing Parameters/Part Numbers

The following table lists the frequency and latency bins available for SO-RIMM modules.

Table 1: Part Number by Freq. & Latency

Organization	Speed			Part Number
	Bin	I/O Freq. (MHz)	t_{rac} (Row Access Time) ns	
32M x 18	-CT9	1066	32P	MS18R1622EH0-CT9
	-CM8	800	40	MS18R1622EH0-CM8
	-CK8	800	45	MS18R1622EH0-CK8
64M x 18	-CT9	1066	32P	MS18R1624EH0-CT9
	-CM8	800	40	MS18R1624EH0-CM8
	-CK8	800	45	MS18R1624EH0-CK8
128M x 18	-CT9	1066	32P	MS18R1628EH0-CT9
	-CM8	800	40	MS18R1628EH0-CM8
	-CK8	800	45	MS18R1628EH0-CK8

Form Factor

The SO-RIMM modules are offered in 160-pad 0.65mm edge connector pad pitch form factor suitable for 160 contact SO-RIMM connectors. Figure 1 below, shows a eight device SO-RIMM module.

Note: On double sided modules, RDRAM devices are also installed on bottom side of PCB.

Figure 1: SO-RIMM Module shown with heat spreader removed

Table 2: Module Pad Numbers and Signal Names

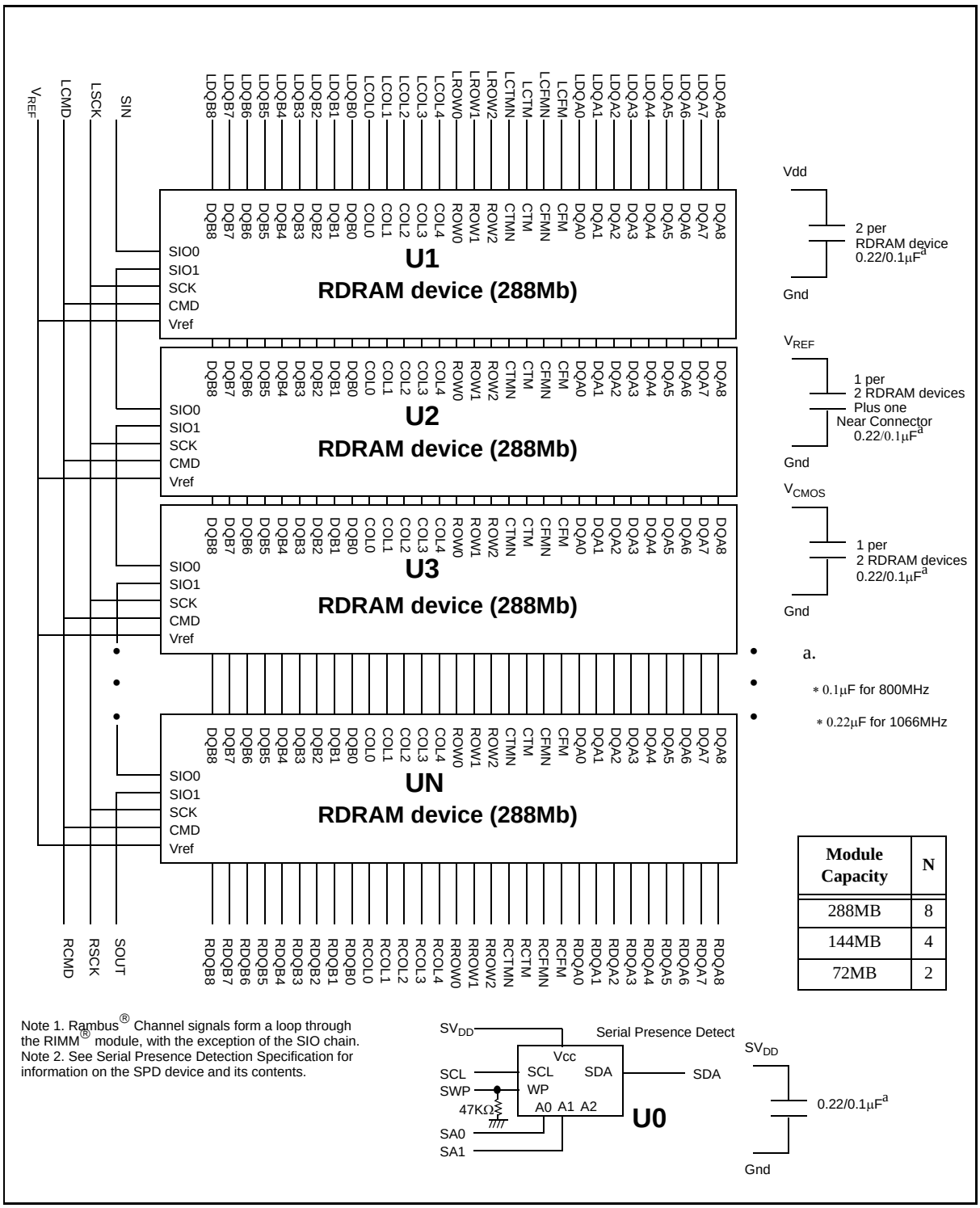
Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTM	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTMN	B14	LROW2
A15	Gnd	B15	Gnd
A16	LROW1	B16	LROW0
A17	Gnd	B17	Gnd
A18	LCOL4	B18	LCOL3
A19	Gnd	B19	Gnd
A20	LCOL2	B20	LCOL1
A21	Gnd	B21	Gnd
A22	LCOL0	B22	LDQB1
A23	Gnd	B23	Gnd
A24	LDQB0	B24	LDQB3
A25	Gnd	B25	Gnd
A26	LDQB2	B26	LDQB5
A27	Gnd	B27	Gnd
A28	LDQB4	B28	LDQB7
A29	Gnd	B29	Gnd
A30	LDQB6	B30	LDQB8
A31	Gnd	B31	Gnd
A32	LSCK	B32	LCMD
A33	Gnd	B33	Gnd
A34	SOUT	B34	SIN
A35	Vdd	B35	Vdd
A36	NC	B36	NC
A37	Gnd	B37	Gnd
A38	NC	B38	NC
A39	Vcmos	B39	Vcmos
A40	NC	B40	NC

Pin	Pin Name	Pin	Pin Name
A41	NC	B41	NC
A42	Vref	B42	Vref
A43	SCL	B43	SA0
A44	Vdd	B44	Vdd
A45	SDA	B45	SA1
A46	Vdd	B46	Vdd
A47	SVdd	B47	SWP
A48	Gnd	B48	Gnd
A49	RSCK	B49	RCMD
A50	Gnd	B50	Gnd
A51	RDQB8	B51	RDQB6
A52	Gnd	B52	Gnd
A53	RDQB7	B53	RDQB4
A54	Gnd	B54	Gnd
A55	RDQB5	B55	RDQB2
A56	Gnd	B56	Gnd
A57	RDQB3	B57	RDQB0
A58	Gnd	B58	Gnd
A59	RDQB1	B59	RCOL0
A60	Gnd	B60	Gnd
A61	RCOL1	B61	RCOL2
A62	Gnd	B62	Gnd
A63	RCOL3	B63	RCOL4
A64	Gnd	B64	Gnd
A65	RROW0	B65	RROW1
A66	Gnd	B66	Gnd
A67	RROW2	B67	RCTMN
A68	Gnd	B68	Gnd
A69	RCFMN	B69	RCTM
A70	Gnd	B70	Gnd
A71	RCFM	B71	RDQA0
A72	Gnd	B72	Gnd
A73	RDQA1	B73	RDQA2
A74	Gnd	B74	Gnd
A75	RDQA3	B75	RDQA4
A76	Gnd	B76	Gnd
A77	RDQA5	B77	RDQA6
A78	Gnd	B78	Gnd
A79	RDQA7	B79	RDQA8
A80	Gnd	B80	Gnd

Table 3 : Module Connector Pad Description

Signal	Pins	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A37, A48, A50, A52, A54, A56, A58, A60, A62, A64, A66, A68, A70, A72, A74, A76, A78, A80, B1, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B23, B25, B27, B29, B31, B33, B37, B48, B50, B52, B54, B56, B58, B60, B62, B64, B66, B68, B70, B72, B74, B76, B78, B80			Ground reference for RDRAM core and interface. 72 pins.
LCFM	B10	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B32	**I**	**V_{CMOS}**	Serial Command Pin. Pin used to read from and write to the control registers. Also used for power management.
LCOL4.. LCOL0	A18, B18, A20, B20, A22	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A12	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A14	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8.. LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	**I/O**	**RSL**	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. LDQA8 is non-functional on modules with x16 RDRAM devices
LDQB8.. LDQB0	B30, B28, A30, B26, A28, B24, A26, B22, A24	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2.. LROW0	B14, A16, B16	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A32	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A36, B36, A38, B38, A40, B40, A41, B41			These pads are not connected. These 24 connector pads are reserved for future use.
RCFM	A71	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	A69	**I**	**RSL**	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
RCMD	B49	**I**	**V_{CMOS}**	Serial Command Input. Pin used to read from and write to the control registers. Also used for power management.
RCOL4.. RCOL0	B63, A63, B61, A61, B59	**I**	**RSL**	Column bus. 5-bit bus containing control and address information for column accesses.

Signal	Pins	I/O	Type	Description
RCTM	B69	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	B67	**I**	**RSL**	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	B79, A79, B77, A77, B75, A75, B73, A73, B71	**I/O**	**RSL**	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. RDQA8 is non-functional on modules x16 RDRAM devices.
RDQB8.. RDQB0	A51, A53, B51, A55, B53, A57, B55, A59, B57	**I/O**	**RSL**	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. RDQB8 is non-functional on modules x16 RDRAM devices.
RROW2.. RROW0	A67, B65, A65	**I**	**RSL**	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A49	**I**	**V_{CMOS}**	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B43	**I**	**SV_{DD}**	Serial Presence Detect Address 0.
SA1	B45	**I**	**SV_{DD}**	Serial Presence Detect Address 1.
SCL	A43	**I**	**SV_{DD}**	Serial Presence Detect Clock.
SDA	A45	**I/O**	**SV_{DD}**	Serial Presence Detect Data (Open Collector I/O).
SIN	B34	**I/O**	**V_{CMOS}**	Serial I/O. Pin for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM device on the module.
SOUT	A34	**I/O**	**V_{CMOS}**	Serial I/O. Pin for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM device on the module.
SV_{DD}	A47			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	B47	**I**	**SV_{DD}**	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A39, B39			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A35, B35, A44, B44, A46, B46			Supply voltage for the RDRAM core and interface logic.
Vref	A42, B42			Logic threshold reference voltage for RSL signals.



Module Capacity	N
288MB	8
144MB	4
72MB	2

Note 1. Rambus® Channel signals form a loop through the RIMM® module, with the exception of the SIO chain.
Note 2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Figure 2: SO-RIMM Module Functional Diagram

Absolute Maximum Ratings

Table 4 : Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd	- 0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd	- 0.5	V_{DD} + 1.0	V
T_{STORE}	Storage temperature	- 50	100	°C
T_{PLATE}	Plate temperature	-	92	°C

DC Recommended Electrical Conditions

Table 5 : DC Recommended Electrical Conditions

Symbol	Parameter and Conditions	Min	Max	Unit
V_{DD}	Supply voltage	2.50 - 0.13	2.50 + 0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers CMOS I/O power supply at pad for 1.8V controllers	V_{DD} 1.8 - 0.1	V_{DD} 1.8 + 0.2	V V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{SPD}	Serial Presence Detector- Positive power supply	2.2	3.6	V

Table 6 : SO-RIMM Module Capacity and Number of RDRAM device

SO-RIMM Module Capacity	288MB	144MB	72MB
Number of 288Mb RDRAM devices	8	4	2

SO-RIMM Module Current Profile

Table 7 : SO-RIMM Module Current Profile

I_{DD}	SO-RIMM Module Capacity		288MB	144MB	72MB	Unit
	Number of 288Mb RDRAM devices		8	4	2	
	SO-RIMM module power conditions [a]	Freq.	Max	Max	Max	
I_{DD1}	One RDRAM device in Read[b], balance in NAP mode	-1066	778	762	754	mA
		-800	628	612	604	
I_{DD2}	One RDRAM device in Read[b], balance in Standby mode	-1066	1485	1065	855	mA
		-800	1265	885	695	
I_{DD3}	One RDRAM device in Read[b], balance in Active mode	-1066	1870	1230	910	mA
		-800	1545	1005	735	
I_{DD4}	One RDRAM device in Write, balance in NAP mode	-1066	768	752	744	mA
		-800	608	592	584	
I_{DD5}	One RDRAM device in Write, balance in Standby mode	-1066	1475	1055	845	mA
		-800	1245	865	675	
I_{DD6}	One RDRAM device in Write, balance in Active mode	-1066	1860	1220	900	mA
		-800	1525	985	715	

a. Actual power will depend on memory controller and usage patterns. Power does not include Refresh Current.
b. I/O current is a function of the % of 1's, to add I/O power for 50% 1's for X18 ECC module for the following: V_{DD} = 2.5V, V_{TERM} = 1.8V, V_{REF} = 1.4V and V_{DIL} = V_{REF} - 0.5V.

AC Electrical Specifications

Table 8 : AC Electrical Specifications

Symbol	Parameter and Conditions	Min	Typ	Max	Unit
Z_L	Module Impedance of RSL Signals	25.2	28	30.8	Ω
$Z_{UL-CMOS}$	Module Impedance of SCK and CMOS signals	23.8	28	32.2	Ω
T_{PD}	Propagation Delay variation of RSL signals. Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN)	-		See Table10[a,b]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} [b,c] for 2, 4 and 8 device modules	-21		21	ps
$\Delta T_{PD-CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay	-250		250	ps
$\Delta T_{PD-SCK,CMD}$	Propagation delay variation of CMD signals with respect to SCK signal	-200		200	ps

a. Table 10 lists parameters and specifications for different storage capacity SO-RIMM Modules that use 288Mb RDRAM devices.
b. T_{PD} or Average clock delay is defined as the delay from finger to finger of RSL signal.
c. If the SO-RIMM module meets the following specification, then it is compliant to the specification. If the SO-RIMM module does not meet these specifications, then the specification can be adjusted by the "Adjusted ΔT_{PD} Specification" table 9 below.

Adjusted ΔT_{PD} Specification

Table 9 : Adjusted ΔT_{PD} Specification

Symbol	Parameter and Conditions	Adjusted Min/Max	Absolute Min / Max		Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} for 2, 4 and 8 device modules	+/-[17+(18*N*ΔZ0)][a]	-30	30	ps

a. Where: N = Number of RDRAM devices installed on the SO-RIMM module
ΔZ0 = delta Z0% = (max Z0 - min Z0)/(min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

AC Electrical Specifications for SO-RIMM Modules

Table 10: AC Electrical Specifications for SO-RIMM Modules

Symbol	SO-RIMM Module Capacity		288MB	144MB	72MB	Unit
	Number of 288Mb RDRAM devices		8	4	2	
	Parameter and Condition for SO-RIMM modules	Freq.	Max	Max	Max	
T_{PD}	Propagation Delay, all RSL signals	-1066	1.32	1.06	1.06	ns
		-800	1.32	1.06	1.06	
V_{α}/V_{IN}	Attenuation Limit	-1066	17.0	17.0	17.0	%
		-800	16.0	16.0	16.0	
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @ 20%-80%)	-1066	4.0	4.0	4.0	%
		-800	4.0	4.0	4.0	
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @ 20%-80%)	-1066	2.0	2.0	2.0	%
		-800	2.0	2.0	2.0	
R_{DC}	DC Resistance Limit	-1066	1.4	0.9	0.9	Ω
		-800	1.4	0.9	0.9	

Physical Dimensions -1 *(For PCB)*

The following defines the SO-RIMM module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate. The dimensions without tolerance specification use the default tolerance of ±0.127[±0.005]. The maximum height of the module is 31.25mm [1.23inches].

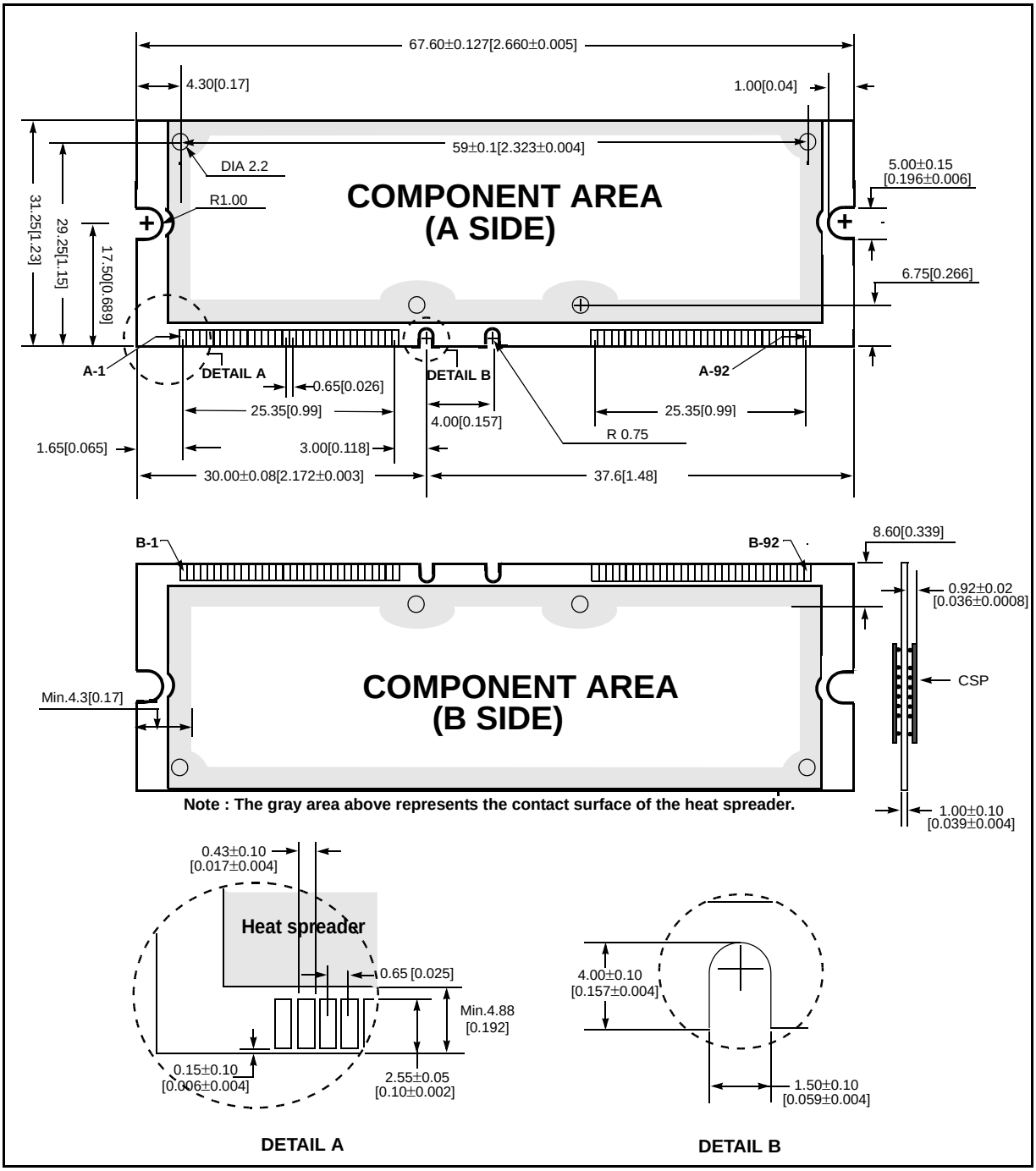


Figure 3: SO-RIMM Module PCB Physical Dimensions

Physical Dimensions -2 *(For Heat Spreader)*

The following defines the SO-RIMM module dimensions. All units are in millimeters with inches in brackets[ ], where appropriate. The dimensions without tolerance specification use the default tolerance of ±0.12[±0.005].

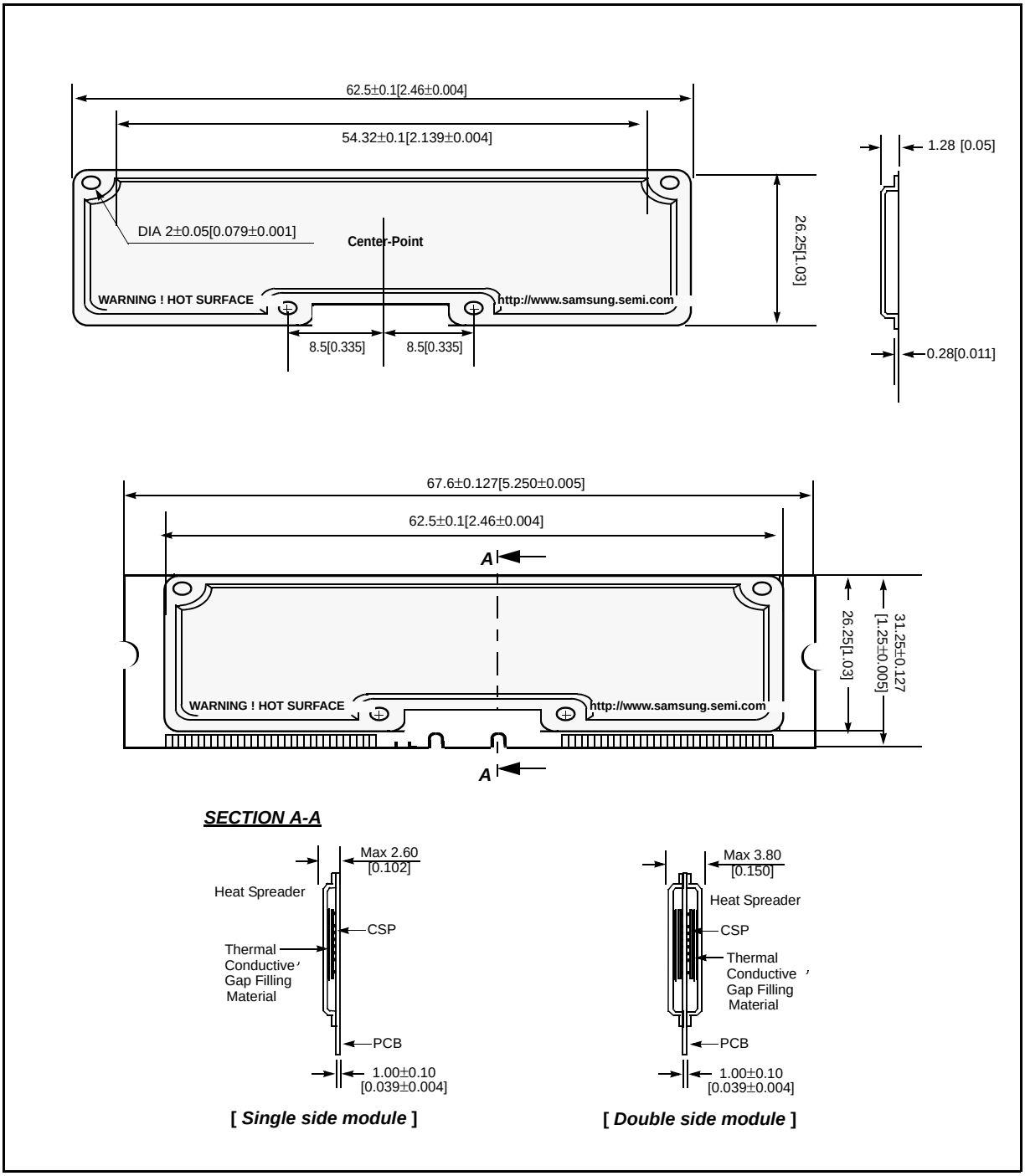
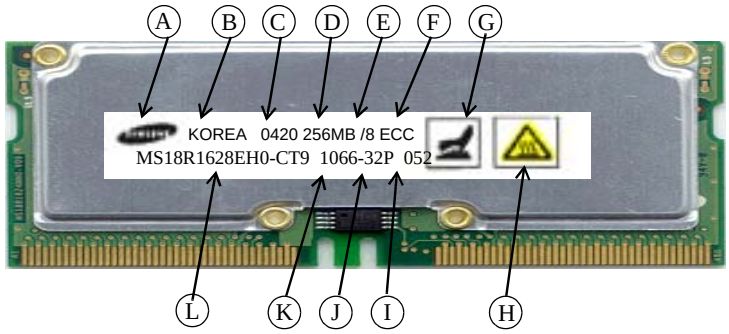


Figure 4: Heat Spreader Physical Dimensions

Standard SO-RIMM Module Marking

The SO-RIMM modules available from Samsung are marked like Figure 5 below. This marking also assists users to specify and verify if the correct SO-RIMM modules are installed in their systems. In the diagram, a label is shown attached to the SO-RIMM module's heat spreader.

Information contained on the label is specific to the SO-RIMM module and provides RDRAM device information without requiring removal of the SO-RIMM module's heat spreader.



	Label Field	Description	Marked Text	Unit
A	Vendor Logo	SO-RIMM Module Vendor SAMSUNG Logo Area	SAMSUNG	-
B	Country	Country of origin	KOREA	-
C	Year & Week code	Manufactured Year & Week code	yyww	-
D	Module Memory Capacity	Number of 8-bit or 9-bit MBytes of RDRAM storage in SO-RIMM module	64MB, 128MB, 256MB	MBytes
E	Number of RDRAM devices	Number of RDRAM devices contained in the SO-RIMM module	2/4/8	RDRAM devices
F	ECC Support	Indicates whether the SO-RIMM module supports 9 (ECC) bit Bytes	ECC = 9 bit Bytes	-
G	Notice!	Hot surface caution notice.	-	-
H	Caution Logo	ISO Standard	-	-
I	Gerber & SPD Version	PCB Gerber file & SPD code version used on SO-RIMM Module	Gerber : 05 = 0.5 ver 09 = 0.9 ver SPD : 2 = 1.3 ver.	-
J	tRAC	Row Access Time	-32P, -40, -45	ns
K	Memory Speed	Data transfer speed for RDRAM device	1066, 800	MHz
L	Part No.	SAMSUNG SO-RIMM Module part No.	See Table 1	-

Figure 5: SO-RIMM Module Marking Example

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