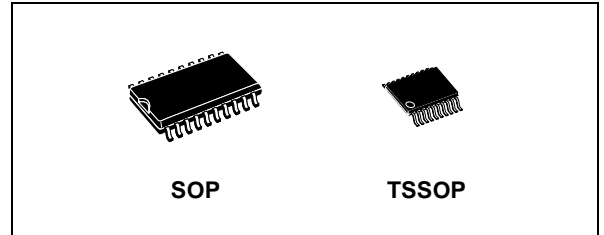


## OCTAL D-TYPE FLIP FLOP NON-INVERTING (3-STATE) WITH 5V TOLERANT INPUTS AND OUTPUTS

- 5V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED:  
 $f_{MAX} = 150 \text{ MHz (MIN.) at } V_{CC} = 3\text{V}$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 24\text{mA (MIN.) at } V_{CC} = 3\text{V}$
- PCI BUS LEVELS GUARANTEED AT 24 mA
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 2.0\text{V to } 3.6\text{V (1.5V Data Retention)}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)
- ESD PERFORMANCE:  
HBM > 2000V (MIL STD 883 method 3015);  
MM > 200V

### DESCRIPTION

The 74LCX574 is a low voltage CMOS OCTAL D-TYPE FLIP FLOP with 3 STATE OUTPUT NON-INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology. It is ideal for low power and high speed 3.3V applications; it can be interfaced to 5V signal environment for both inputs and outputs. These 8 bit D-Type flip-flops are controlled by a clock input (CK) and an output enable input ( $\overline{OE}$ ). On the positive transition of the clock, the Q



**Table 1: Order Codes**

PACKAGE	T & R
SOP	74LCX574MTR
TSSOP	74LCX574TTR

outputs will be set to the logic state that were setup at the  $\overline{D}$  inputs.

While the ( $\overline{OE}$ ) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The Output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

It has same speed performance at 3.3V than 5V AC/ACT family, combined with a lower power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

**Figure 1: Pin Connection And IEC Logic Symbols**

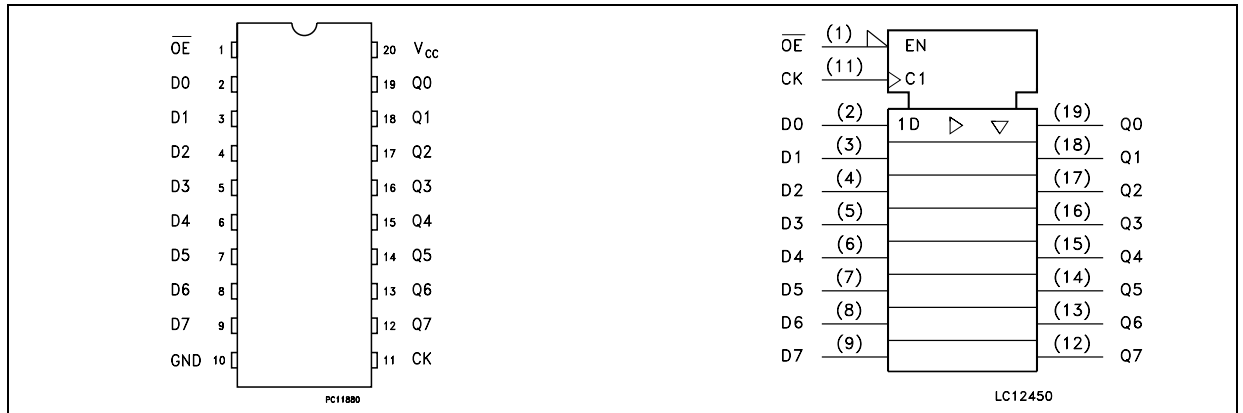


Figure 2: Input And Output Equivalent Circuit

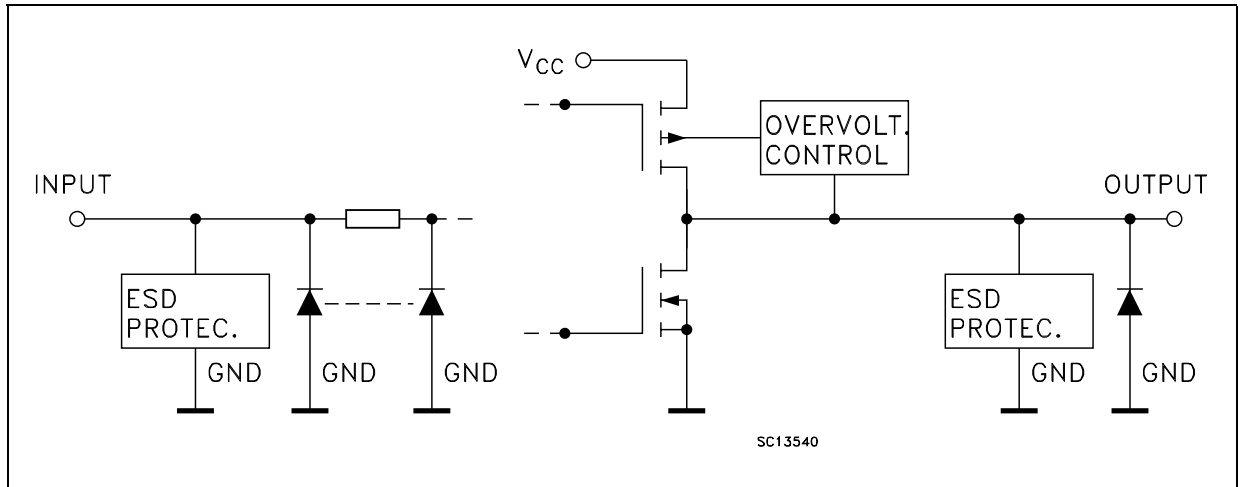


Table 2: Pin Description

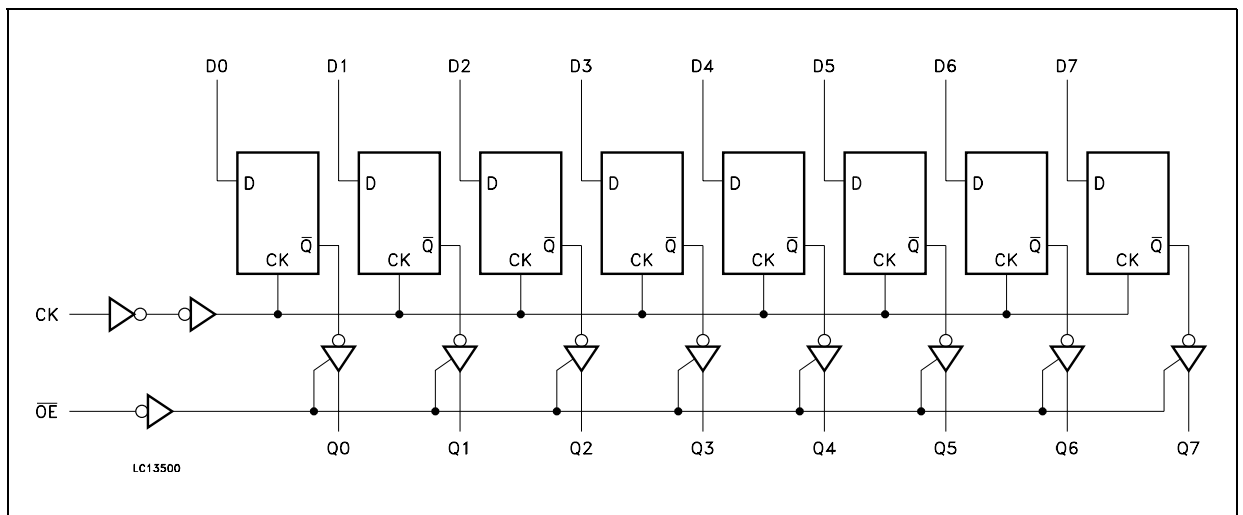
PIN N°	SYMBOL	NAME AND FUNCTION
1	OE	3-State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Outputs
11	CK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive Supply Voltage

Table 3: Truth Table

INPUT			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance

Figure 3: Logic Diagram



This logic diagram has not been used to estimate propagation delays

**Table 4: Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage (OFF State)	-0.5 to +7.0	V
$V_O$	DC Output Voltage (High or Low State) (note 1)	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 50	mA
$I_{OK}$	DC Output Diode Current (note 2)	- 50	mA
$I_O$	DC Output Current	$\pm 50$	mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$	mA
$I_{GND}$	DC Ground Current per Supply Pin	$\pm 100$	mA
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

- 1)  $I_O$  absolute maximum rating must be observed  
 2)  $V_O < GND$

**Table 5: Recommended Operating Conditions**

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage (note 1)	2.0 to 3.6	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage (OFF State)	0 to 5.5	V
$V_O$	Output Voltage (High or Low State)	0 to $V_{CC}$	V
$I_{OH}, I_{OL}$	High or Low Level Output Current ( $V_{CC} = 3.0$ to $3.6V$ )	$\pm 24$	mA
$I_{OH}, I_{OL}$	High or Low Level Output Current ( $V_{CC} = 2.7V$ )	$\pm 12$	mA
$T_{op}$	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2)	0 to 10	ns/V

- 1) Truth Table guaranteed: 1.5V to 3.6V  
 2)  $V_{IN}$  from 0.8V to 2V at  $V_{CC} = 3.0V$

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value				Unit
		V <sub>CC</sub> (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage	2.7 to 3.6		2.0		2.0		V
V <sub>IL</sub>	Low Level Input Voltage					0.8		0.8
V <sub>OH</sub>	High Level Output Voltage	2.7 to 3.6	I <sub>O</sub> =-100 μA	V <sub>CC</sub> -0.2		V <sub>CC</sub> -0.2		V
		2.7	I <sub>O</sub> =-12 mA	2.2		2.2		
		3.0	I <sub>O</sub> =-18 mA	2.4		2.4		
			I <sub>O</sub> =-24 mA	2.2		2.2		
V <sub>OL</sub>	Low Level Output Voltage	2.7 to 3.6	I <sub>O</sub> =100 μA		0.2		0.2	V
		2.7	I <sub>O</sub> =12 mA		0.4		0.4	
		3.0	I <sub>O</sub> =16 mA		0.4		0.4	
			I <sub>O</sub> =24 mA		0.55		0.55	
I <sub>I</sub>	Input Leakage Current	2.7 to 3.6	V <sub>I</sub> = 0 to 5.5V		± 5		± 5	μA
I <sub>off</sub>	Power Off Leakage Current	0	V <sub>I</sub> or V <sub>O</sub> = 5.5V		10		10	μA
I <sub>OZ</sub>	High Impedance Output Leakage Current	2.7 to 3.6	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = 0 to V <sub>CC</sub>		± 5		± 5	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 to 3.6	V <sub>I</sub> = V <sub>CC</sub> or GND		10		10	μA
			V <sub>I</sub> or V <sub>O</sub> = 3.6 to 5.5V		± 10		± 10	
ΔI <sub>CC</sub>	I <sub>CC</sub> incr. per Input	2.7 to 3.6	V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500		500	μA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min.	Typ.	Max.	
V <sub>OLP</sub>	Dynamic Low Level Quiet Output (note 1)	3.3	C <sub>L</sub> = 50pF V <sub>IL</sub> = 0V, V <sub>IH</sub> = 3.3V		0.8		V
V <sub>OLV</sub>					-0.8		

1) Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH to LOW or LOW to HIGH. The remaining output is measured in the LOW state.

Table 8: AC Electrical Characteristics

Symbol	Parameter	Test Condition				Value				Unit
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)	R <sub>L</sub> (Ω)	t <sub>s</sub> = t <sub>r</sub> (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time	2.7	50	500	2.5	1.5	9.5	1.5	9.5	ns
		3.0 to 3.6				1.5	8.5	1.5	8.5	
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time to HIGH and LOW level	2.7	50	500	2.5	1.5	9.5	1.5	9.5	ns
		3.0 to 3.6				1.5	8.5	1.5	8.5	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time from HIGH to LOW level	2.7	50	500	2.5	1.5	8.5	1.5	8.5	ns
		3.0 to 3.6				1.5	7.5	1.5	7.5	
t <sub>S</sub>	Set-Up Time, HIGH or LOW level (Dn to CK)	2.7	50	500	2.5	2.5		2.5		ns
		3.0 to 3.6				2.5		2.5		
t <sub>H</sub>	Hold Time, HIGH or LOW level (Dn to CK)	2.7	50	500	2.5	1.5		1.5		ns
		3.0 to 3.6				1.5		1.5		
t <sub>W</sub>	CK Pulse Width, HIGH or LOW	2.7	50	500	2.5	3.3		3.3		ns
		3.0 to 3.6				3.3		3.3		
f <sub>MAX</sub>	Clock Pulse Frequency	3.0 to 3.6	50	500	2.5	165		150		MHz
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output To Output Skew Time (note1, 2)	3.0 to 3.6	50	500	2.5		1.0		1.0	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ )

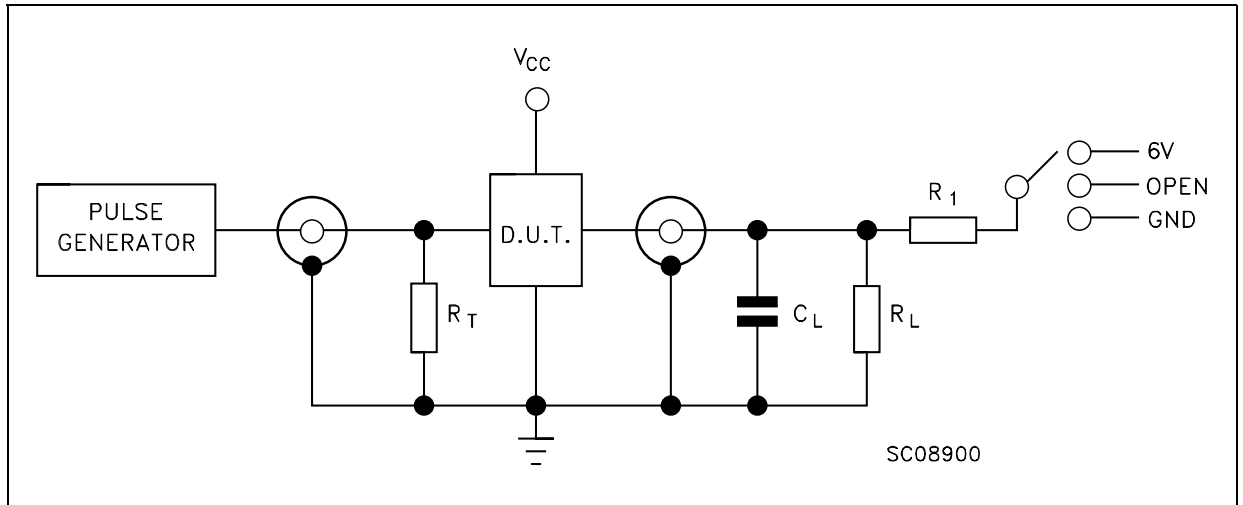
2) Parameter guaranteed by design

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C			
				Min.	Typ.	Max.	
C <sub>IN</sub>	Input Capacitance	3.3	V <sub>IN</sub> = 0 to V <sub>CC</sub>		6		pF
C <sub>OUT</sub>	Output Capacitance	3.3	V <sub>IN</sub> = 0 to V <sub>CC</sub>		12		pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	3.3	f <sub>IN</sub> = 10MHz V <sub>IN</sub> = 0 or V <sub>CC</sub>		25		pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$  (per flip-flop)

Figure 4: Test Circuit



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L$  = 50 pF or equivalent (includes jig and probe capacitance)  
 $R_L$  =  $R_1$  = 500Ω or equivalent  
 $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays, Setup And Hold Times, Maximum CK Frequency (f=1MHz; 50% duty cycle)

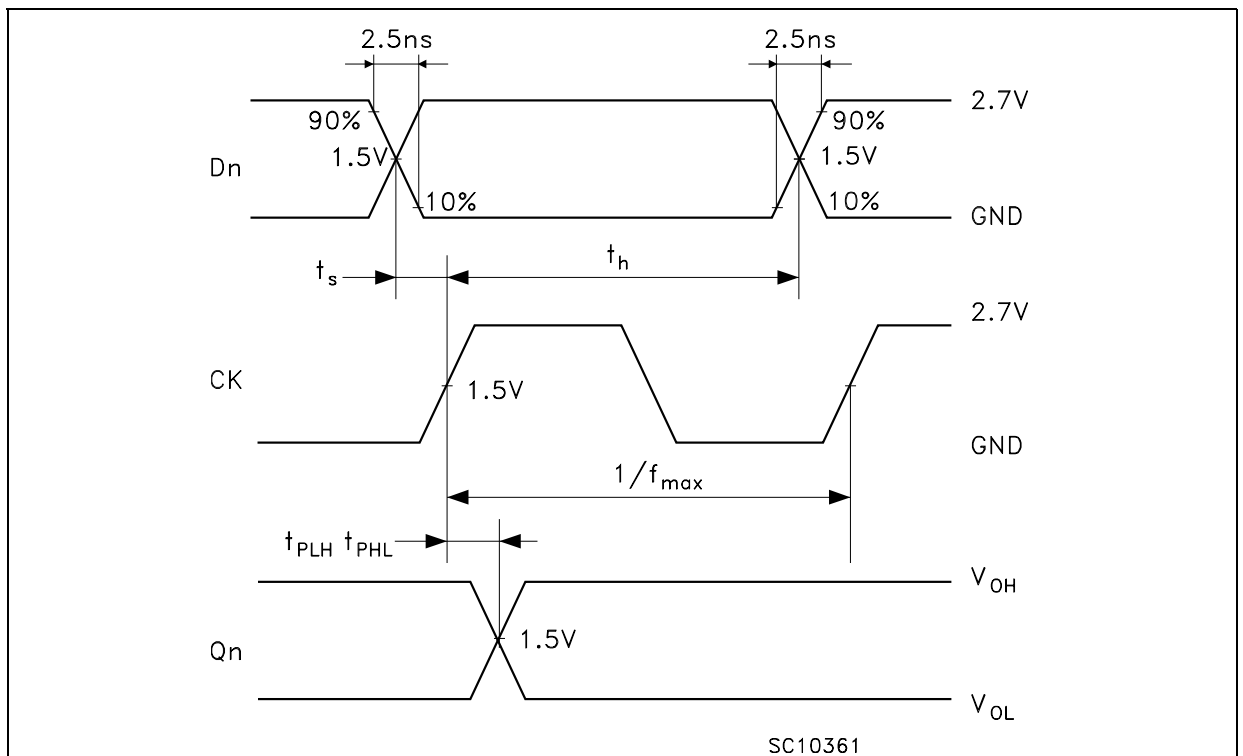
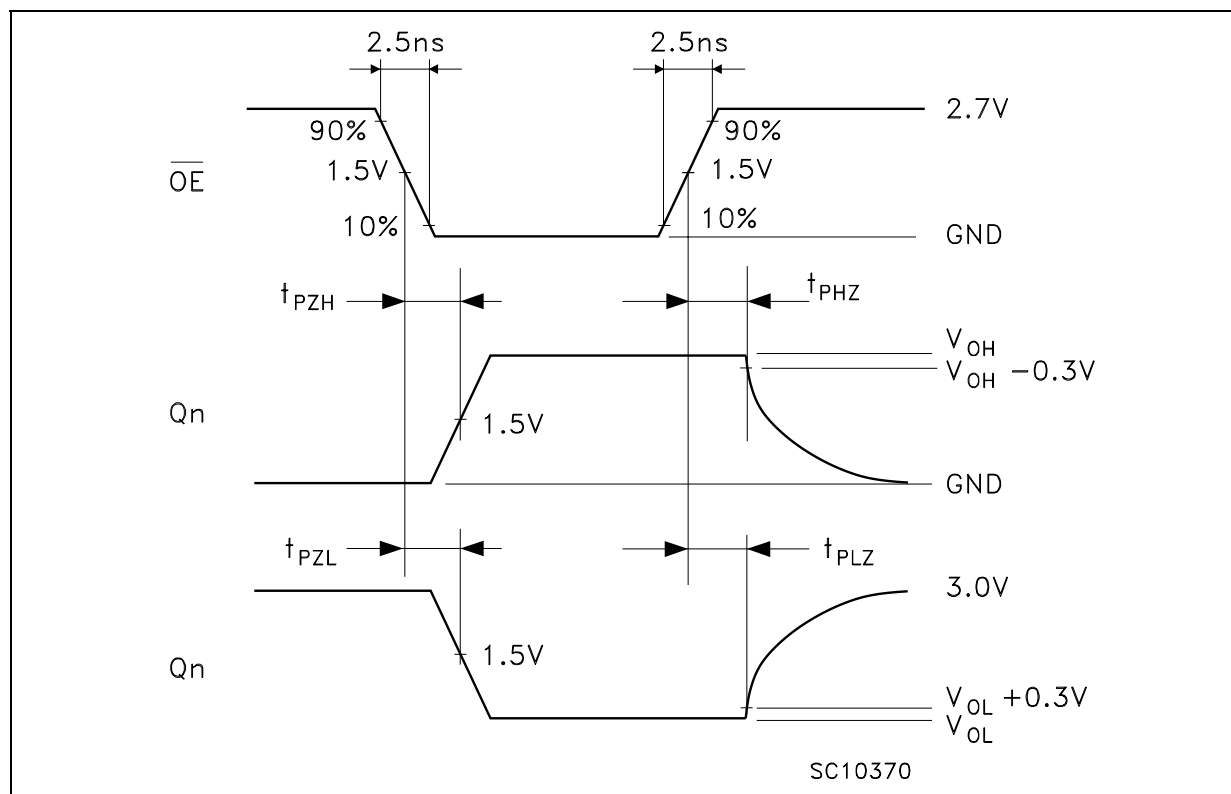
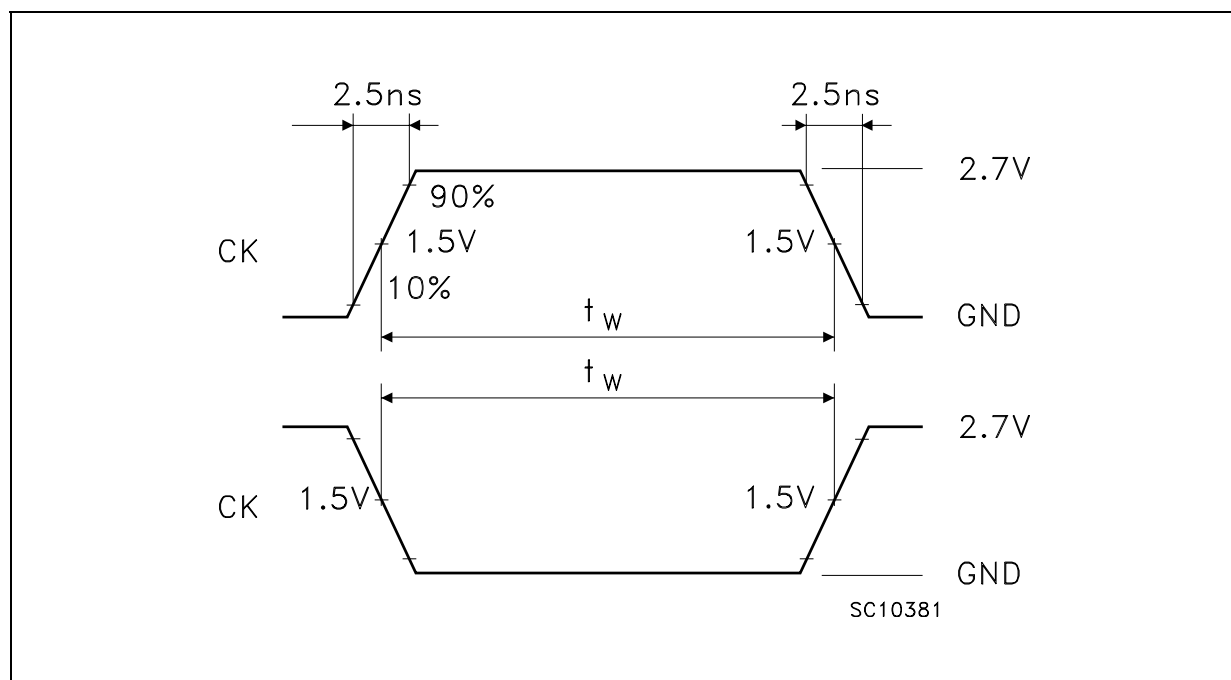
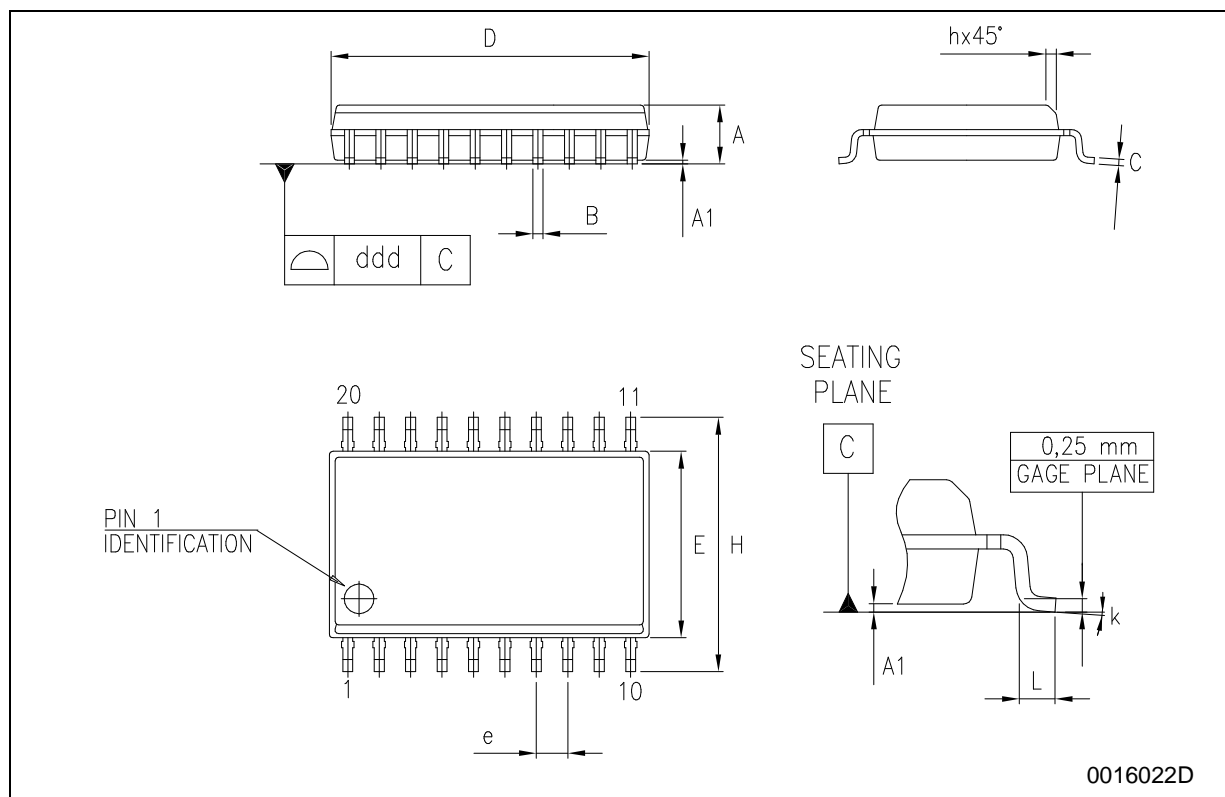


Figure 6: Waveform - Output Enable And Disable Times ( $f=1\text{MHz}$ ; 50% duty cycle)Figure 7: Waveform - Pulse Width ( $f=1\text{MHz}$ ; 50% duty cycle)

## SO-20 MECHANICAL DATA

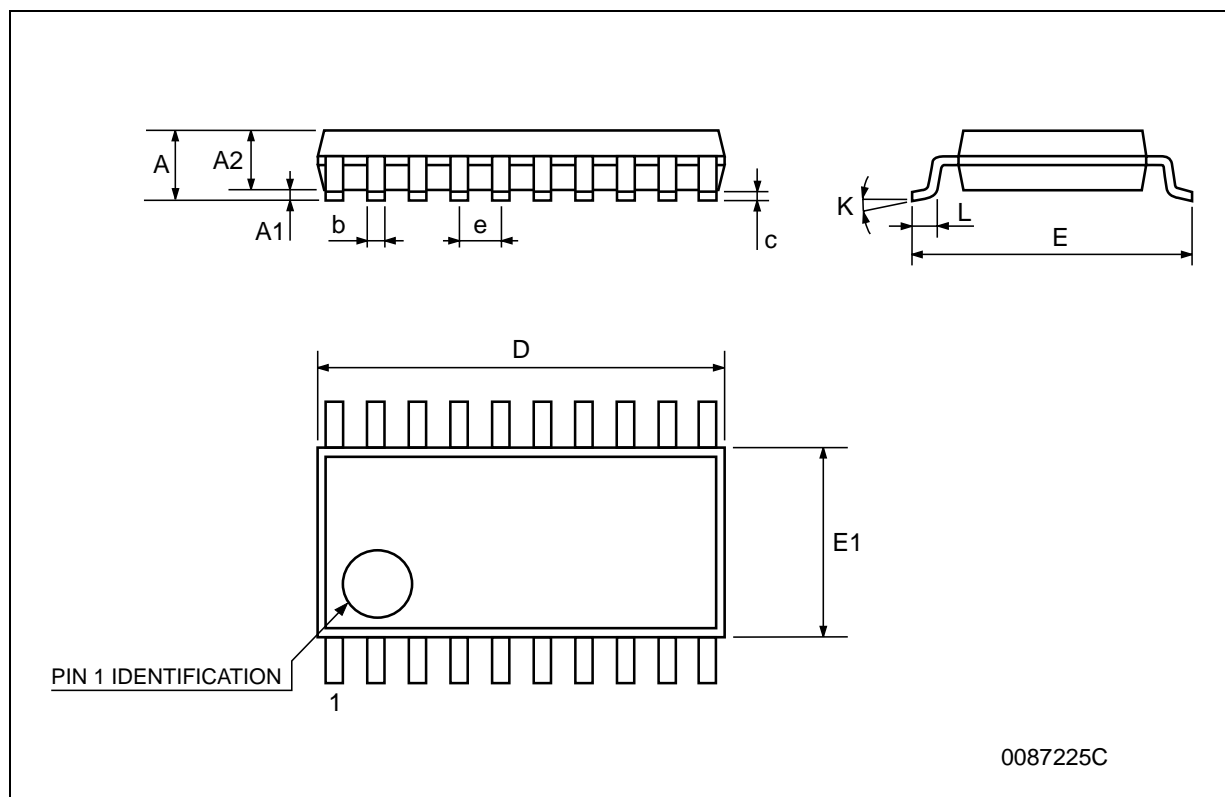
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004





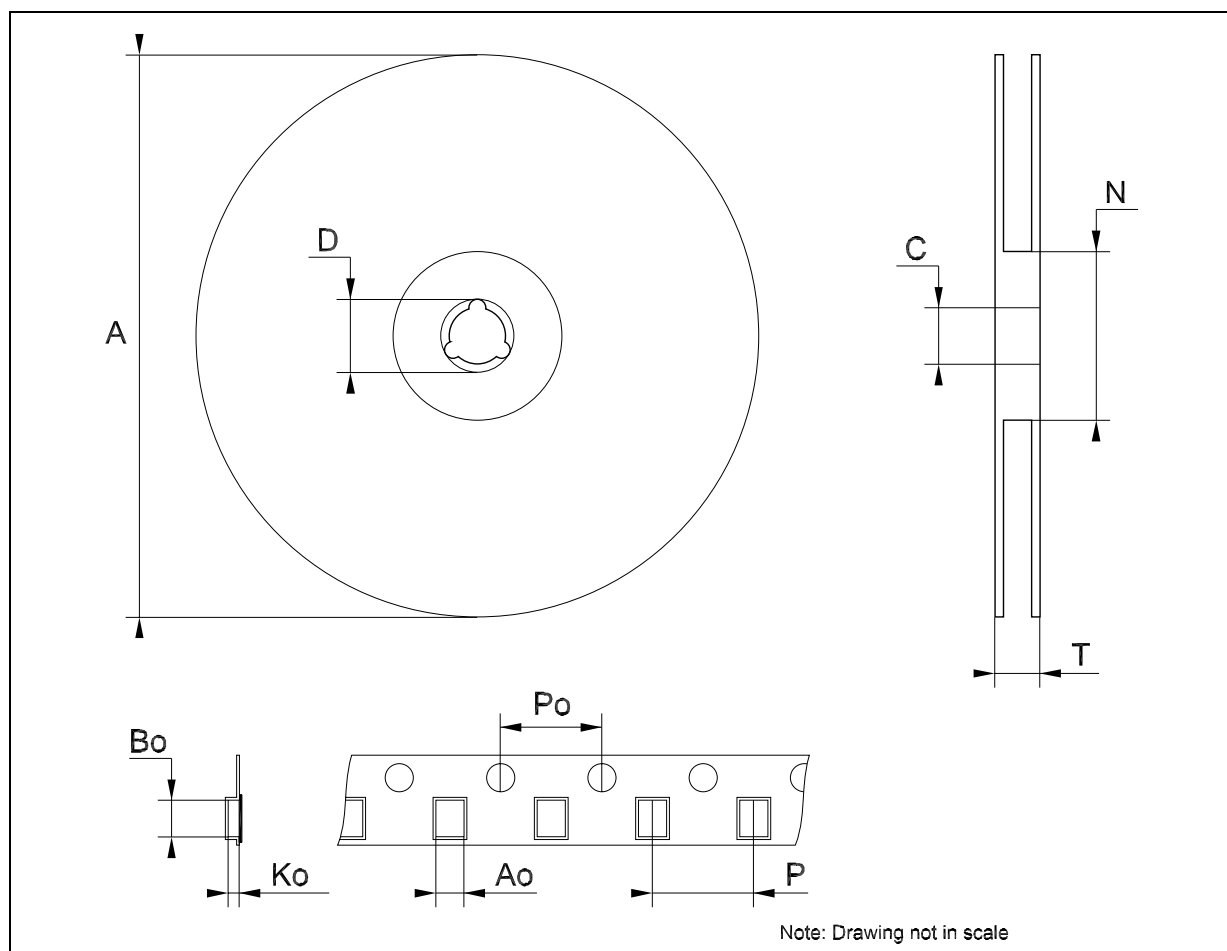
## TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



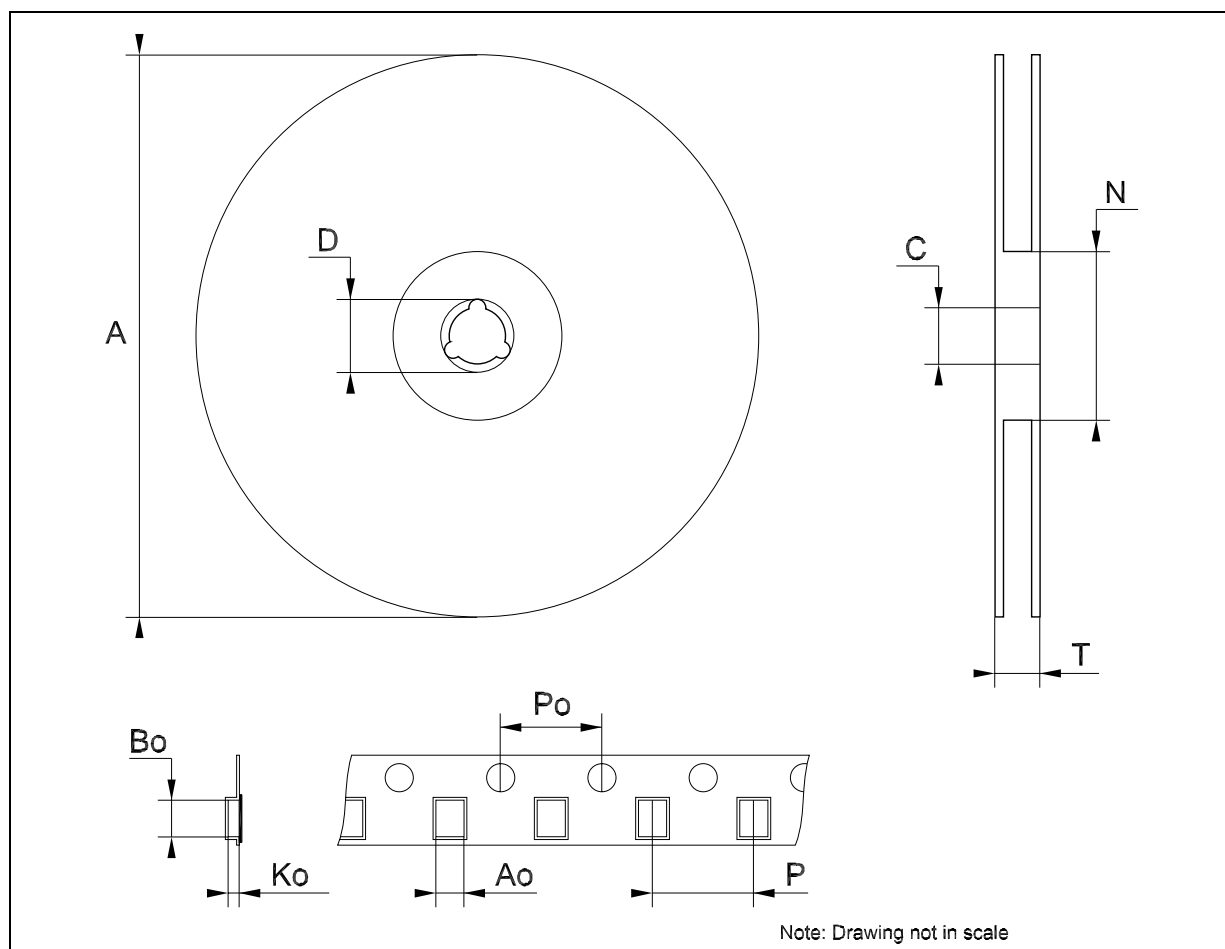
## Tape &amp; Reel SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



## Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



**Table 10: Revision History**

Date	Revision	Description of Changes
15-Sep-2004	5	Ordering Codes Revision - pag. 1.

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