

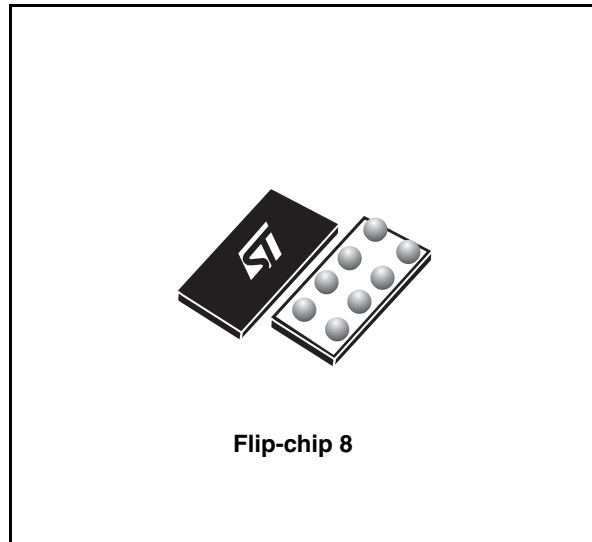
Triple buffer/driver with open drain

Features

- 5 V tolerant inputs
- High speed: $t_{PD} = 3.7$ ns (max.) at $V_{CC} = 3.3$ V
- Low power dissipation:
 - $I_{CC} = 10$ μ A (max.) at $T_A = 85$ °C
- Power down protection on inputs and outputs
- Operating voltage range:
 - $V_{CC} (opr) = 1.65$ to 5.5 V
- Latch-up performance exceeds 300 mA (JESD 17)
- ESD performance
 - 2000-V human body model (JESD 22 A114-A)
 - 200-V machine model (JESD 22 A115-A)
 - 1000-V charge device model (JESD 22 C101)

Applications

- Mobile phones



Description

The 74LX3G07 is a low voltage CMOS triple buffer/driver (open drain) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The internal circuit composed of 2 stages including buffer output, provides high noise immunity and stable output.

Power down protection is provided on input and 0 to 7 V can be accepted on input with no regards to the supply voltage. This device can be used to interface 5 to 3 V.

Table 1. Device summary

Order code	Package	Packaging
74LX3G07BJR	Flip-chip 8	Tape and reel

1 Pin connection

Figure 1. Pin connection and IEC symbols

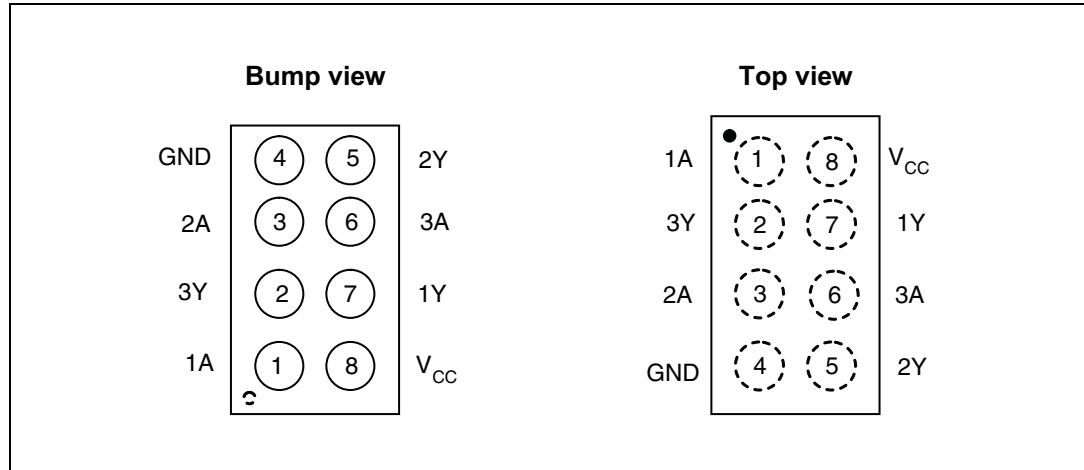


Table 2. Pin assignments

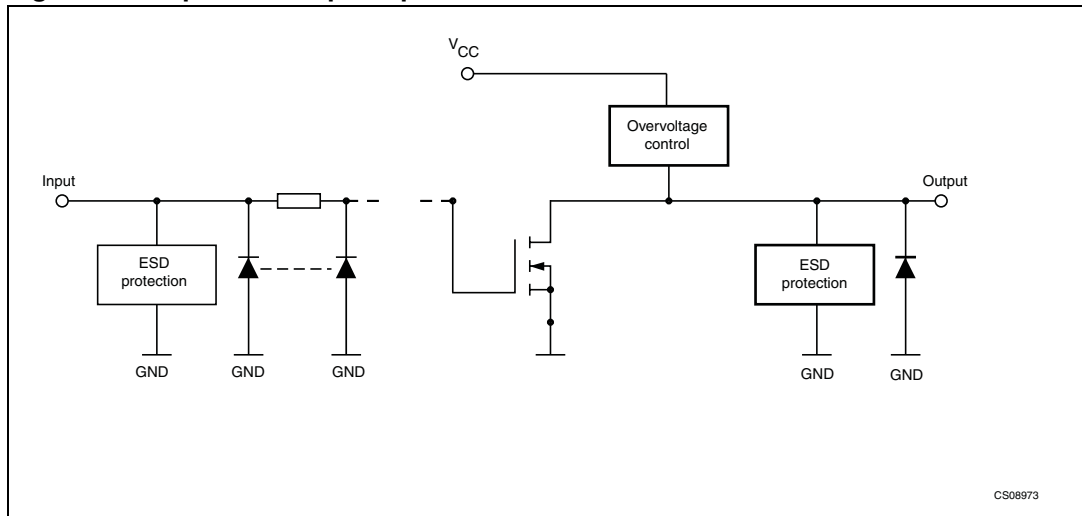
Pin number	Symbol	Name and function
1	1A	Data input 1
2	3Y	Data output 3
3	2A	Data input 2
4	GND	Ground (0V)
5	2Y	Data output 2
6	3A	Data input 3
7	1Y	Data output 1
8	V _{CC}	Positive supply voltage

Table 3. Truth table

nA	nY
L	L
H	Z

Z: High impedance

Figure 2. Input and output equivalent circuit



2 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to +7.0	V
V_O	DC output voltage ($V_{CC} = 0$ V)	-0.5 to +7.0	V
V_O	DC output voltage (high or low state)	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	- 50	mA
I_{OK}	DC output diode current	- 50	mA
I_O	DC output current	± 50	mA
I_{CC}	DC supply current per supply pin	± 100	mA
I_{GND}	DC ground current per supply pin	± 100	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

2.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 5.5	V
V_I	Input voltage	0 to 5.5	V
V_O	Output voltage ($V_{CC} = 0$ V)	0 to 5.5	V
V_O	Output voltage (high or low state)	0 to V_{CC}	V
I_{OL}	High or low level output current ($V_{CC} = 4.5$ to 5.5 V)	+ 32	mA
I_{OL}	High or low level output current ($V_{CC} = 3.0$ to 3.6 V)	+24	mA
I_{OL}	High or low level output current ($V_{CC} = 2.7$ to 3.0 V)	+12	mA
I_{OL}	High or low level output current ($V_{CC} = 2.3$ to 2.7 V)	+8	mA
I_{OL}	High or low level output current ($V_{CC} = 1.65$ to 2.3 V)	+4	mA
T_{op}	Operating temperature	-40 to 85	°C
dt/dv	Input rise and fall time	0 to 10	ns/V

3 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value		Unit
		V _{CC} (V)		-40 to 85 °C		
				Min	Max	
V _{IH}	High level input voltage	1.65 – 1.95		0.65 V _{CC}		V
		2.3 – 2.7		0.7 V _{CC}		
		3.0 – 5.5		0.7 V _{CC}		
V _{IL}	Low level input voltage	1.65 – 1.95			0.35 V _{CC}	V
		2.3 – 2.7			0.3 V _{CC}	
		3.0 – 5.5			0.3 V _{CC}	
V _{OL}	Low level output voltage	1.65 – 4.5	I _O = 100 µA		0.1	V
		1.65	I _O = 4 mA		0.45	
		2.3	I _O = 8 mA		0.3	
		3.0	I _O = 16 mA		0.4	
			I _O = 24 mA		0.55	
		4.5	I _O = 32 mA		0.55	
I _{OZ}	High impedance output leakage current	3.6	V _I = 5.5 V		±10	µA
I _I	Input leakage current	1.65 – 5.5	V _I = 0 – 5.5 V		±5	µA
I _{off}	Power off leakage current	0	V _I or V _O = 5.5 V		10	µA
I _{CC}	Quiescent supply current	1.65 – 5.5	V _I = V _{CC} or GND		10	µA
		3.6	V _I or V _O = 3.6 to 5.5 V		±10	

Table 7. AC electrical characteristics

Symbol	Parameter	Test conditions				Value		Unit
		V _{CC} (V)	C _L (pF)	R ₁ (Ω)	t _s = t _r (ns)	-40 to 85 °C		
						Min	Max	
t _{PLZ}	Propagation delay time	1.65 – 1.95	30	1000	2.0	1.5	7.8	ns
		2.3 – 2.7	30	500	2.0	1.0	4.3	
		3.0 – 3.6	50	500	2.5	1.1	3.7	
		4.5 – 5.5	50	500	2.5	1.0	2.9	
t _{PZL}	Propagation delay time	1.65 – 1.95	30	1000	2.0	1.5	7.8	ns
		2.3 – 2.7	30	500	2.0	1.0	4.3	
		3.0 – 3.6	50	500	2.5	1.1	3.7	
		4.5 – 5.5	50	500	2.5	1.0	2.9	

Table 8. Capacitive characteristics

Symbol	Parameter	Test conditions		Value			Unit
		V _{CC} (V)		T _A = 25 °C			
				Min	Typ	Max	
C _{IN}	Input capacitance	3.3	V _{IN} = 0 or V _{CC}		2.5		pF
C _{OUT}	Output capacitance	3.3	V _{IN} = 0 or V _{CC}		4		pF
C _{PD}	Power dissipation capacitance ⁽¹⁾	1.8	f _{IN} = 10 MHz		8		pF
		2.5			8		
		3.3			8		

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to test circuit). Average operating current can be obtained by the following equation: I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}

Figure 3. Test circuit

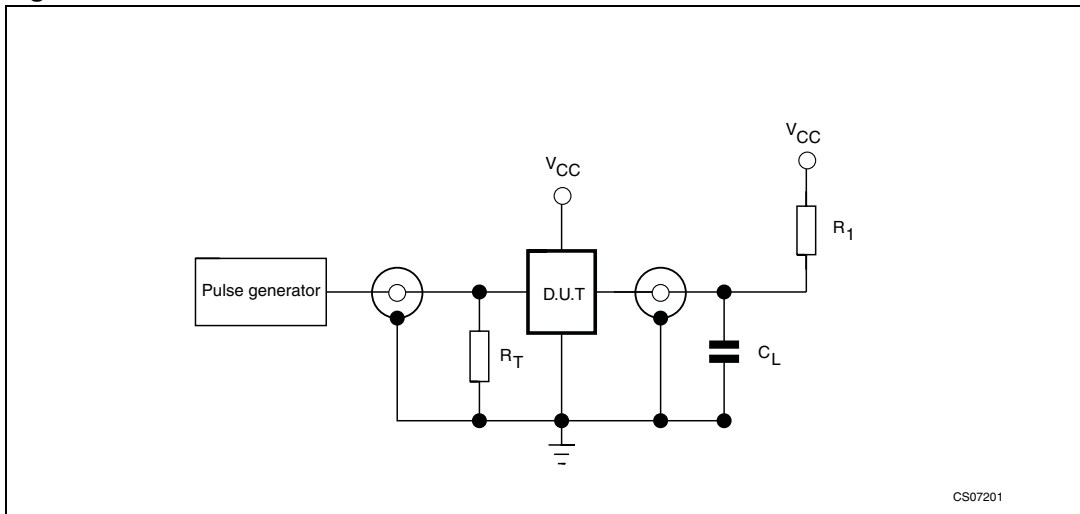
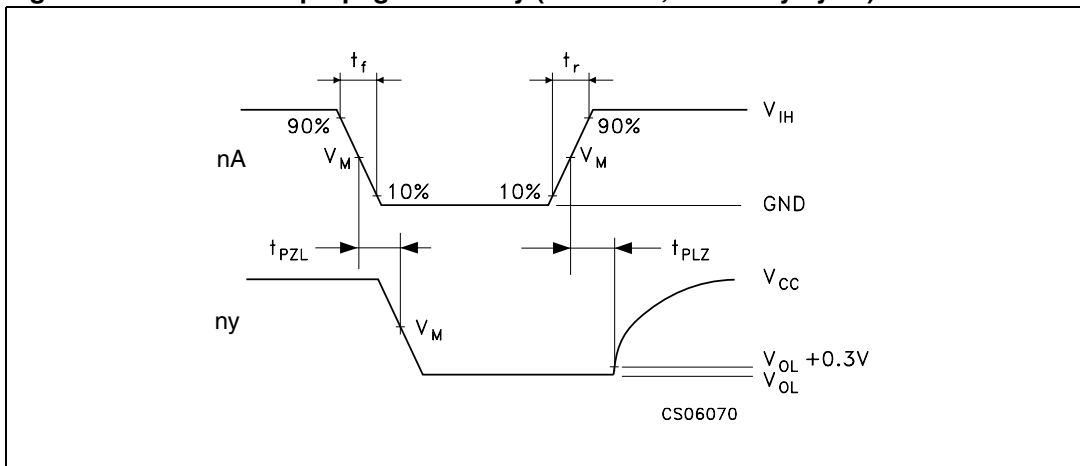


Table 9. Test circuit and waveform symbol value

Symbol	V _{CC}		
	1.65 – 1.95 V	2.3 – 2.7 V	2.7 – 5.5 V
C _L	30 pF	30 pF/ 50 pF	50 pF
R1	1000 Ω	500 Ω	500 Ω
V _{IH}	V _{CC}	V _{CC}	V _{CC}
V _M	V _{CC} /2	V _{CC} /2	V _{CC} /2
t _r = t _f	< 2.0 ns	< 2.0 ns	< 2.5 ns

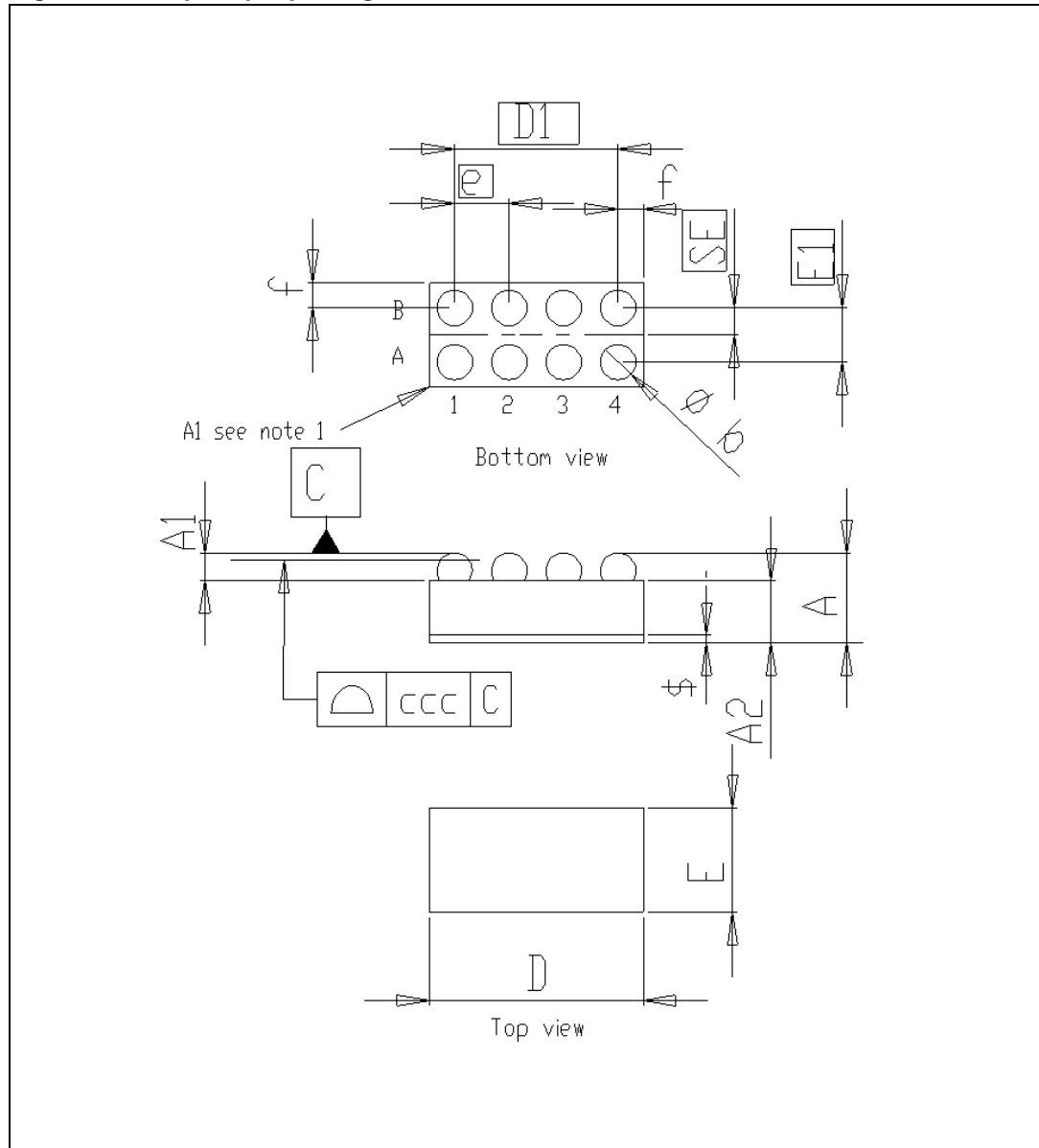
Figure 4. Waveform: propagation delay (f = 1 MHz; 50% duty cycle)



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 5. Flip-chip 8 package outline



1. Drawing not to scale.

Table 10. Flip-chip 8 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.535	0.58	0.625
A1	0.18	0.205	0.23
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	1.85	1.9	1.95
D1		1.5	
e	0.45	0.5	0.55
E	0.85	0.9	0.95
E1	0.45	0.5	0.55
SE		0.25	
f	0.19	0.2	0.21
ccc		0.08	

Figure 6. Flip-chip 8 footprint

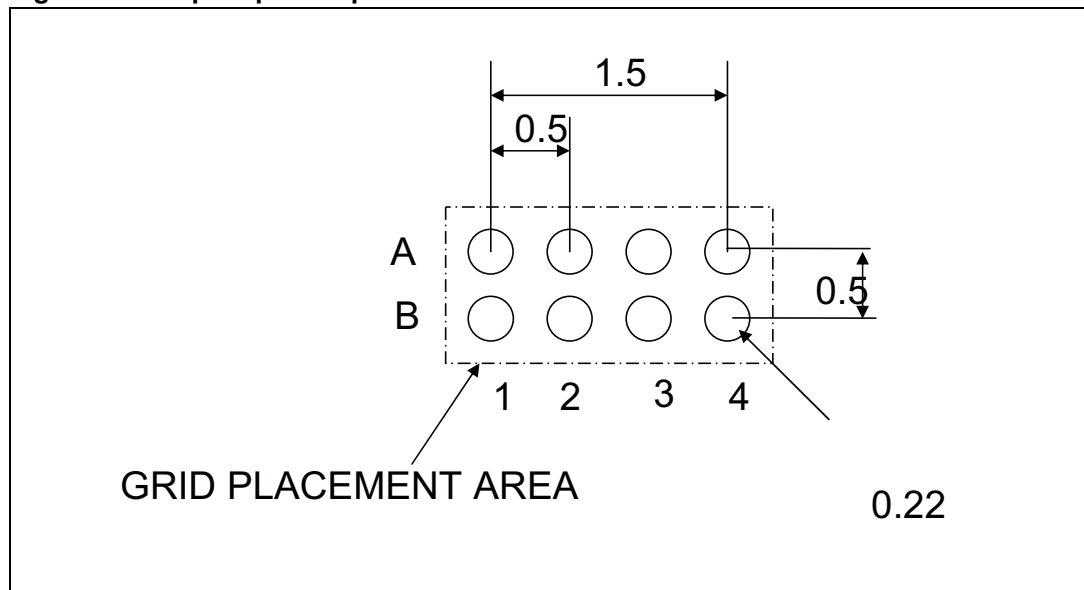


Figure 7. Flip-chip 8 tape and reel

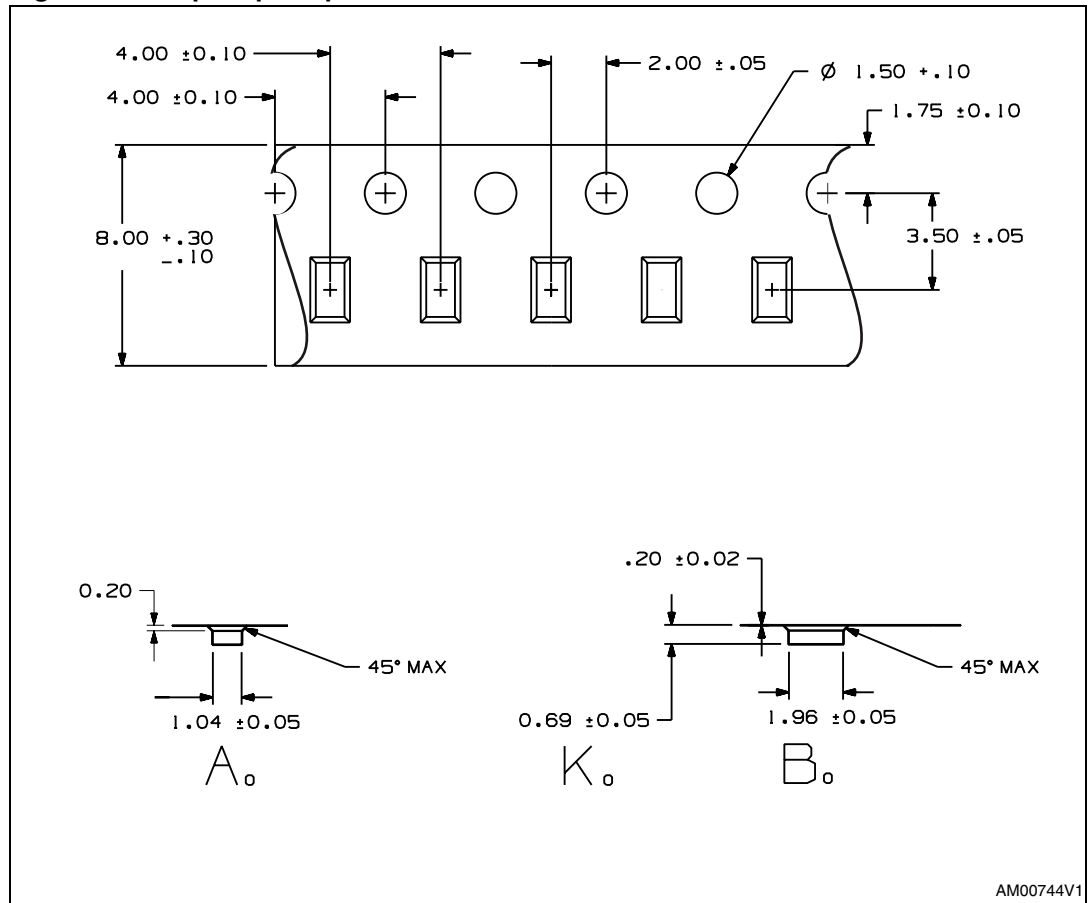


Figure 8. Tape orientation

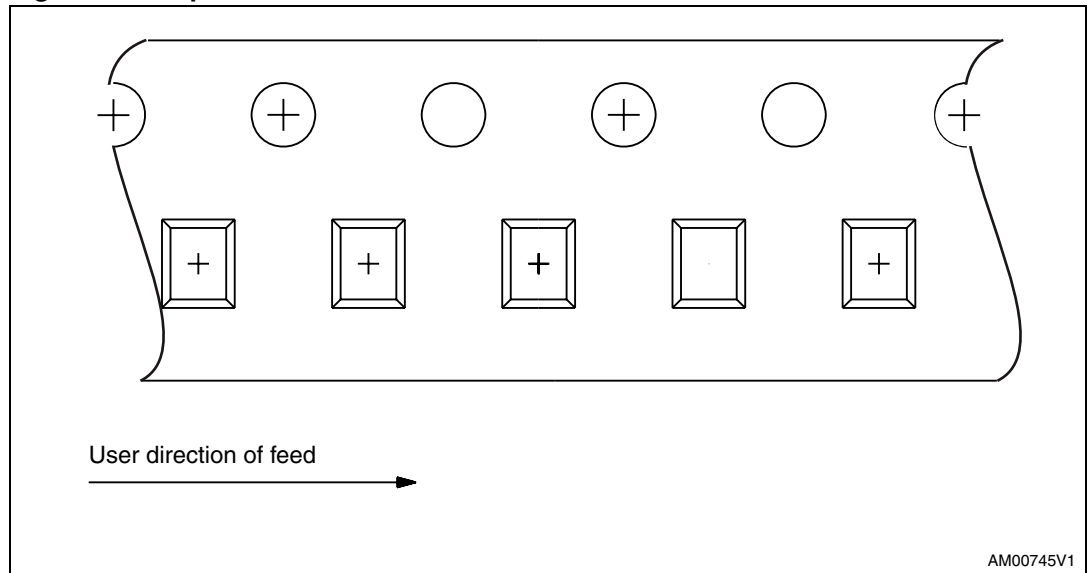
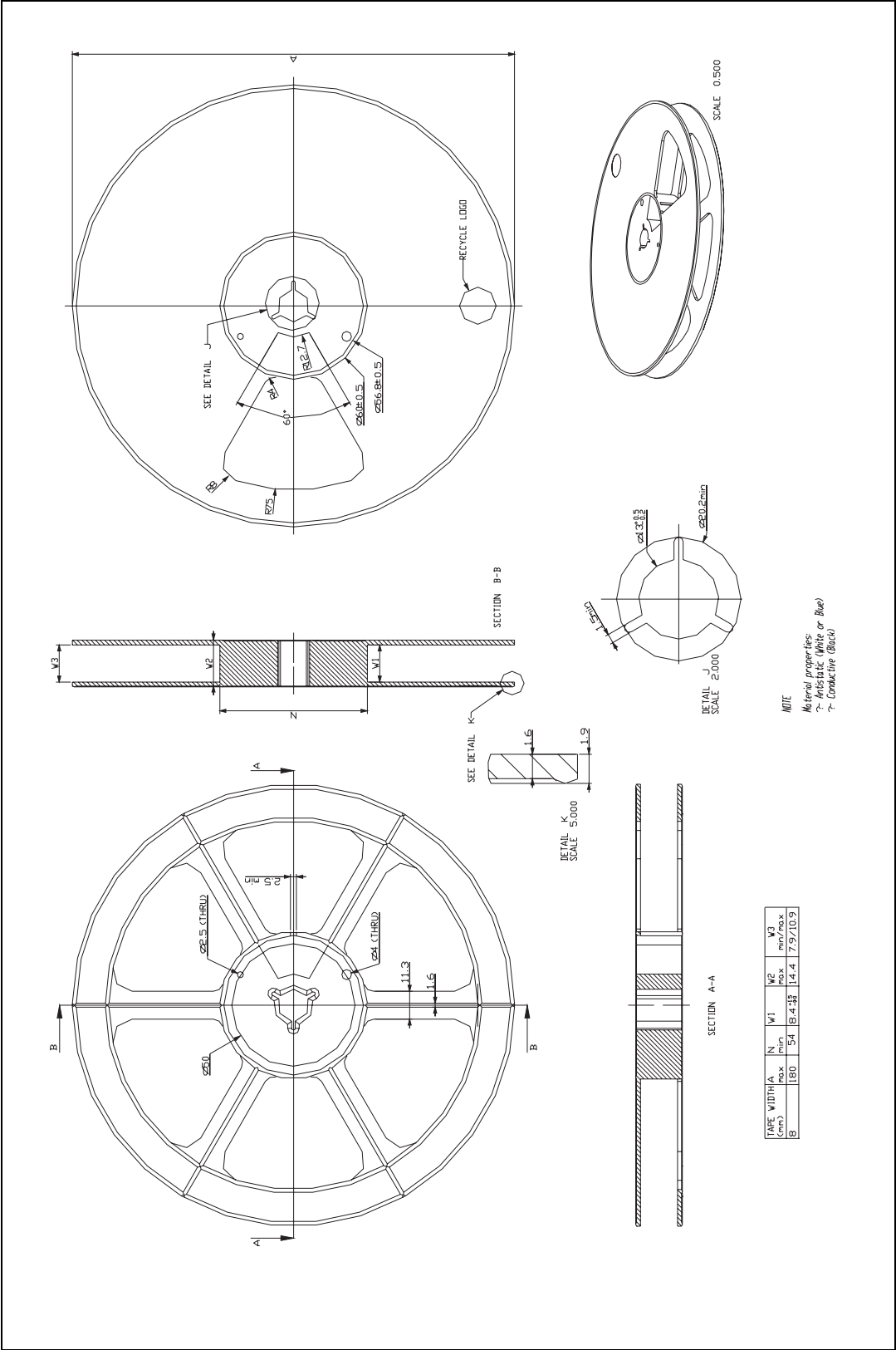


Figure 9. Reel information



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
10-Jul-2008	1	Initial release.
19-Mar-2009	2	Preliminary status promoted to datasheet. Updated Section 4: Package mechanical data .

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