EMIF06-VID01C2

IPAD™

6 line low capacitance EMI filter and ESD protection

Main application

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU board

Description

The EMIF06-VID01C2 is a 6 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The Flip-Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

Benefits

- High efficiency EMI filtering (-40db @ 900MHz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming: 2.92mm x 1.29mm
- Very thin package: 0.69 mm
- High efficiency in ESD suppression on inputs pins (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging
- Lead free package

Complies with the following standards:

IEC 61000-4-2

level 4 input pins	15 kV	(air discharge)
	8 kV	(contact discharge

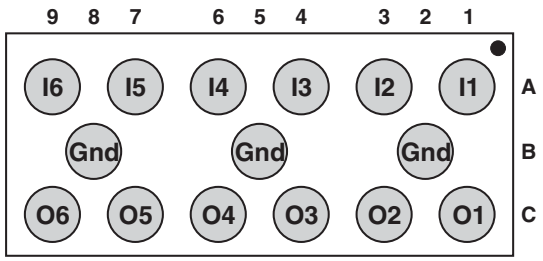
MIL STD 883E - Method 3015-6 Class 3

Lead free coated Flip-Chip (15 Bumps)

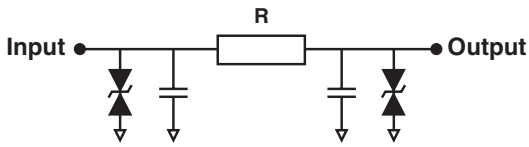
Order code

Part Number	Marking
EMIF06-VID01C2	GR

Pin identities (bump side)



Circuit configuration



R = 100Ω
C_{LINE} = 16pF typ. @ 3V

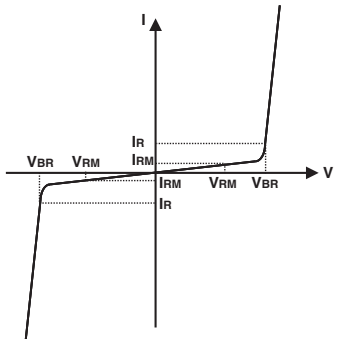
1 Characteristics

Table 1. Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical Characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
R	Series resistance between Input and Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			500	nA
R	I = 10 mA	80	100	120	Ω
C_{line}	V_R = 3 V DC 1 MHz V_{OSC} = 30 mV		16	19	pF

Figure 1. S21 (db) attenuation measurement

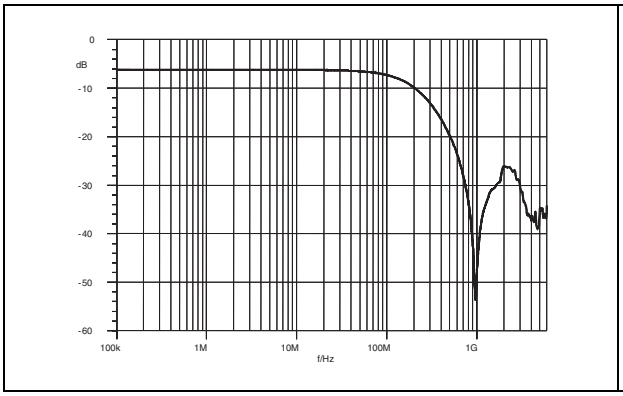


Figure 2. Analog crosstalk measurement

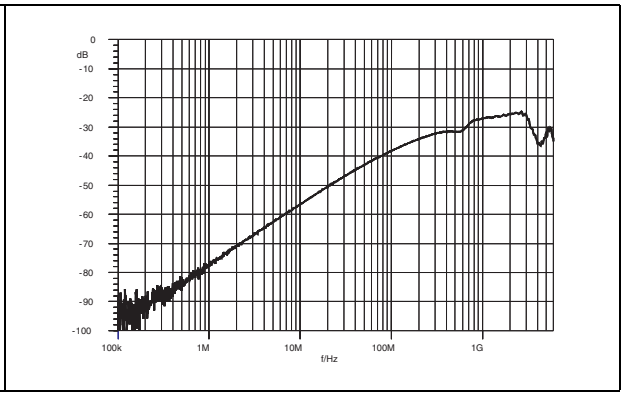


Figure 3. ESD response to IEC 61000-4-2 (+15kV air discharge) on one input (Vin) and on one output (Vout)

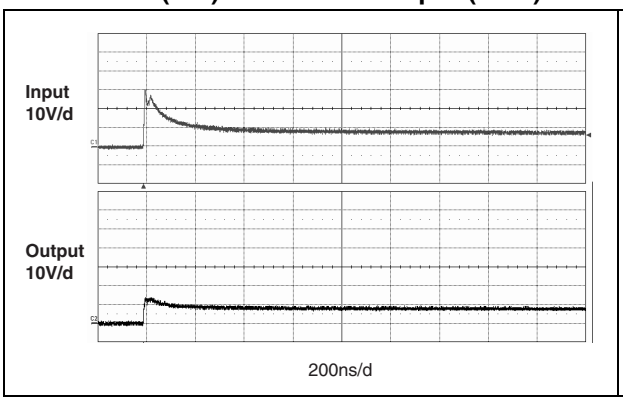


Figure 4. ESD response to IEC 61000-4-2 (-15kV air discharge) on one input (Vin) and on one output (Vout)

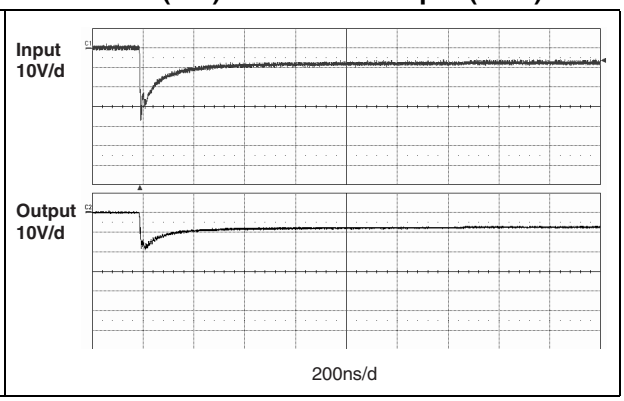
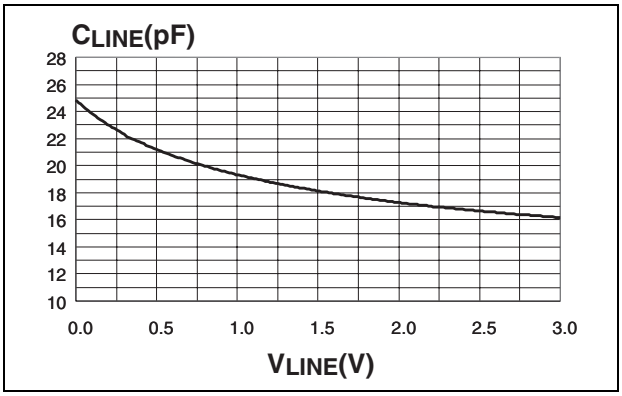


Figure 5. Junction capacitance versus reverse voltage applied (typical values)



2 Ordering information scheme

EMIF yy - xxx zz Cx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
C = Coated Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm

3 Package information

Figure 6. Flip-Chip Dimensions

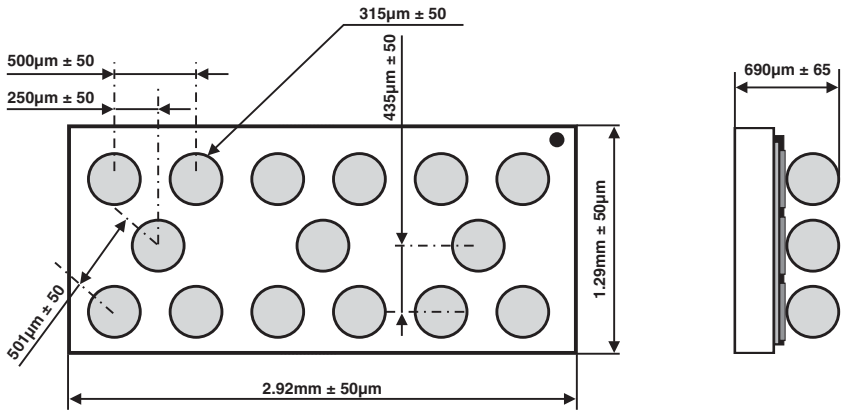


Figure 7. Footprint recommendations **Figure 8. Marking**

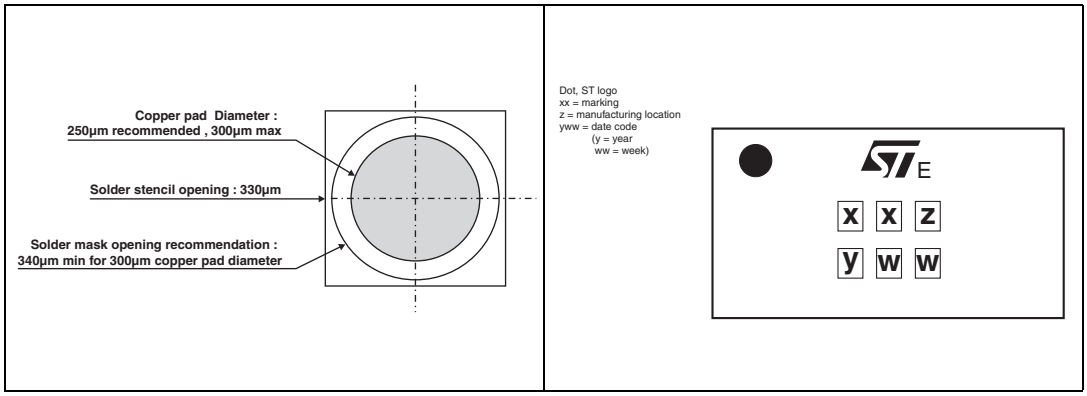
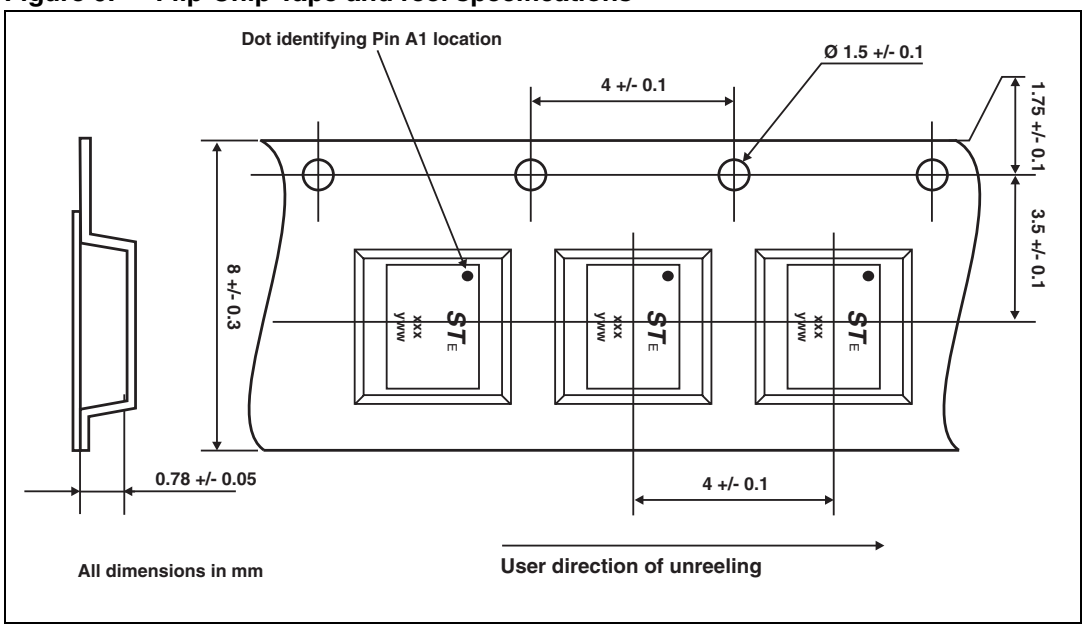


Figure 9. Flip-Chip Tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More packing informations are available in the application note

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-VID01C2	GR	Flip-Chip	5.9 mg	5000	Tape and reel 7”

5 Revision history

Date	Revision	Changes
12-Aug-2005	1	First issue.
01-Jun-2006	2	Reformatted to current standards. Modified marking illustration to remove dimensions. Depth dimension changed in Figure 9.

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