EMIF10-COM01C2

IPAD™

EMI Filter including ESD protection

Main product characteristics

EMI filtering and ESD protection for:

- Computers and printers
- Communication systems
- Mobile phones

Description

The EMIF10-COM01C2 is a highly integrated device designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 Flip-Chip packaging means the package size is equal to the die size.

Additionally, this filter includes an ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

Benefits

- EMI symmetrical (I/O) low-pass filter
- Coating resin on flat side
- Very low PCB space consuming: < 6 mm^2
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input and output pins
- High reliability offered by monolithic integration
- Lead free package

Complies with the following standards:

IEC 61000-4-2 level 4

15 kV (air discharge)

8 kV (contact discharge)

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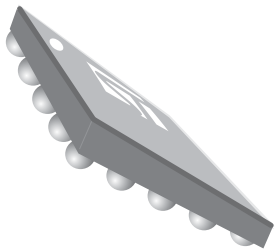


Lead free coated Flip-Chip (25 Bumps)

Order code

Part Number	Marking
EMIF10-COM01C2	FE

Figure 1. Pin configuration (Bump side)

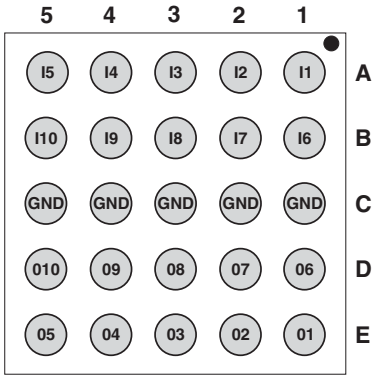
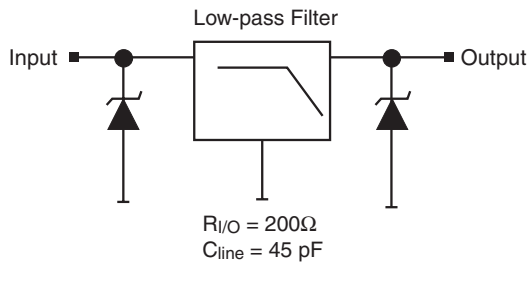


Figure 2. Basic cell configuration



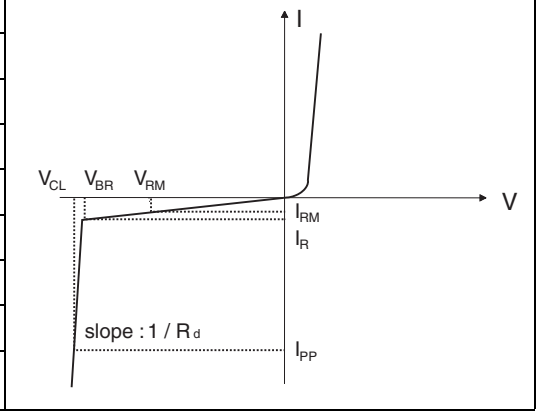
1 Characteristics

Table 1. Absolute Ratings (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical Characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Resistance between Input and Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			500	nA
R_d	I_{PP} = 10 A, t_p = 2.5 µs		1		Ω
$R_{I/O}$		180	200	220	Ω
C_{line}	At 0 V bias		45	50	pF
t_{LH}	V_{input} = 2.8 V R_{load} = 100 kΩ			25	ns

Figure 3. S21(db) attenuation measurement(1)

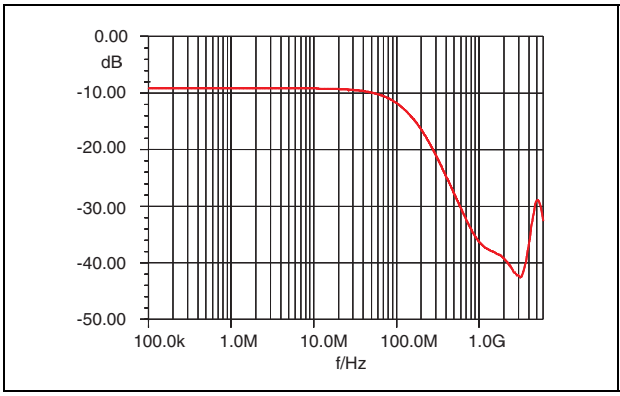
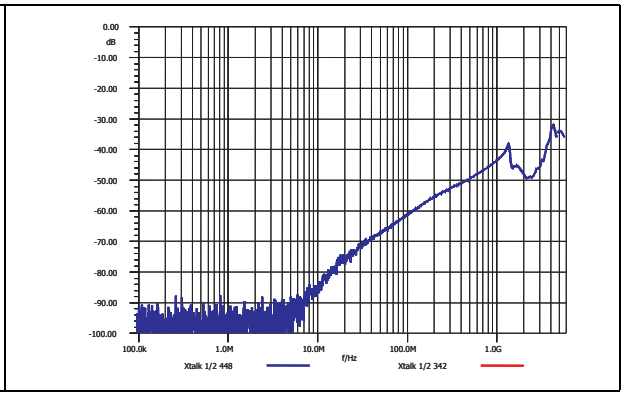


Figure 4. Analog crosstalk



1. Spikes at high frequencies are induced by the PCB layout

Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

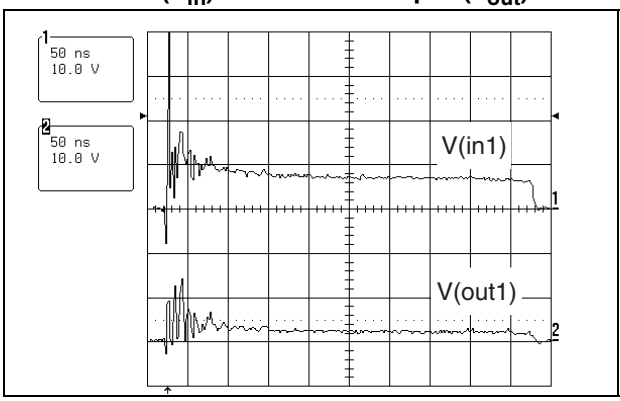


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

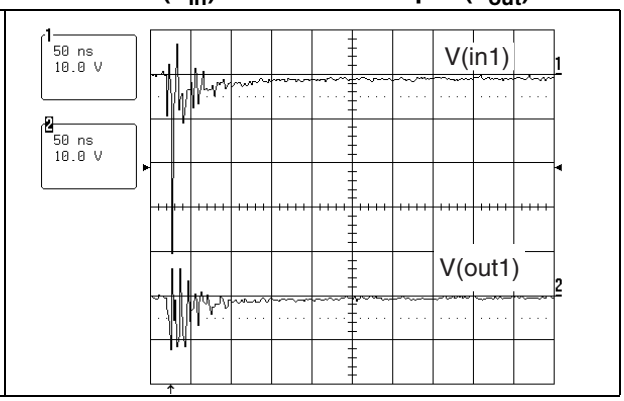


Figure 7. Rise time measurement

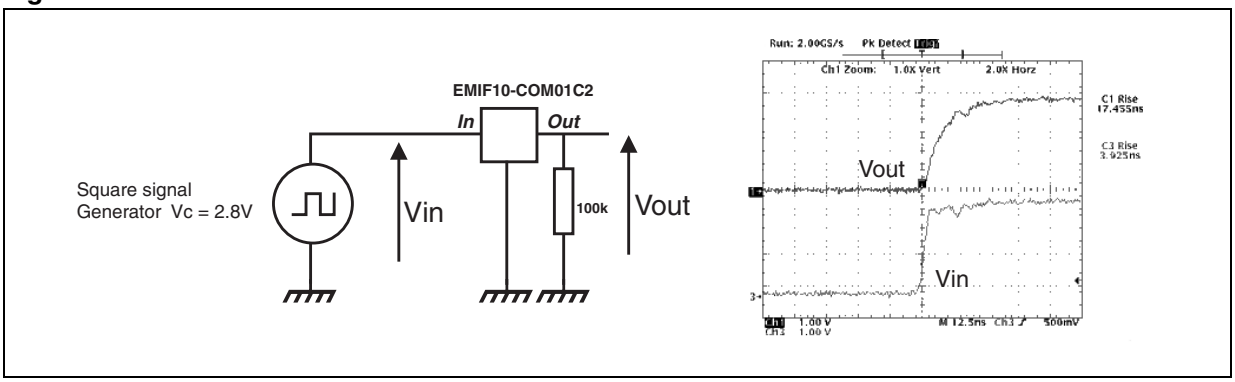


Figure 8. Capacitance versus reverse applied voltage

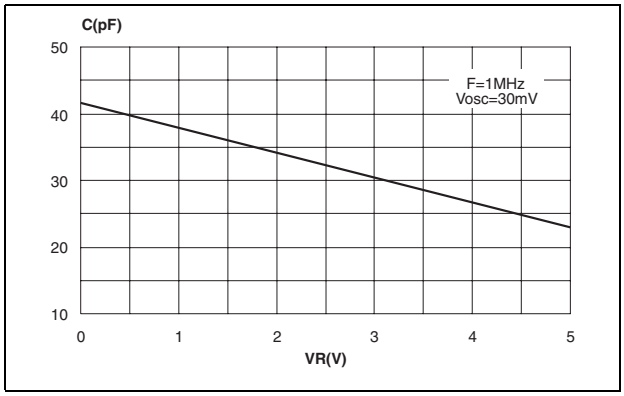
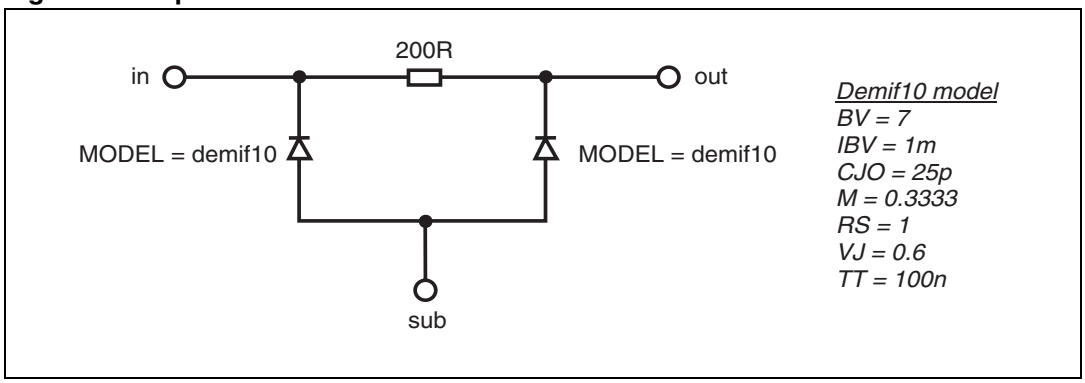


Figure 9. Aplac model



1.1 PCB grounding recommendations

In order to ensure a good efficiency in terms of ESD protection and filtering behavior, we recommend to implement microvias (100 µm dia.) between the GND bumps and the GND layer. GND bumps can be connected together in PCB layer 1, and in addition, if possible, use through hole vias (200 µm dia.) in both sides of filter to improve contact to GND (layer). This layout will minimize the distance to the ground and thus parasitic inductances. In addition, we recommend to have GND plane wherever possible.

2 Ordering Information Scheme

EMIF yy - xxx zz Cx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
C = coated flip-chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm

3 Package information

Figure 10. Flip-Chip package dimensions

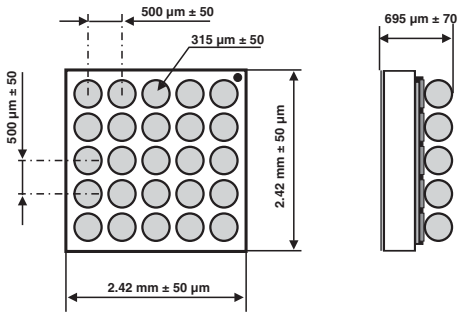


Figure 11. Foot print recommendations **Figure 12. Marking**

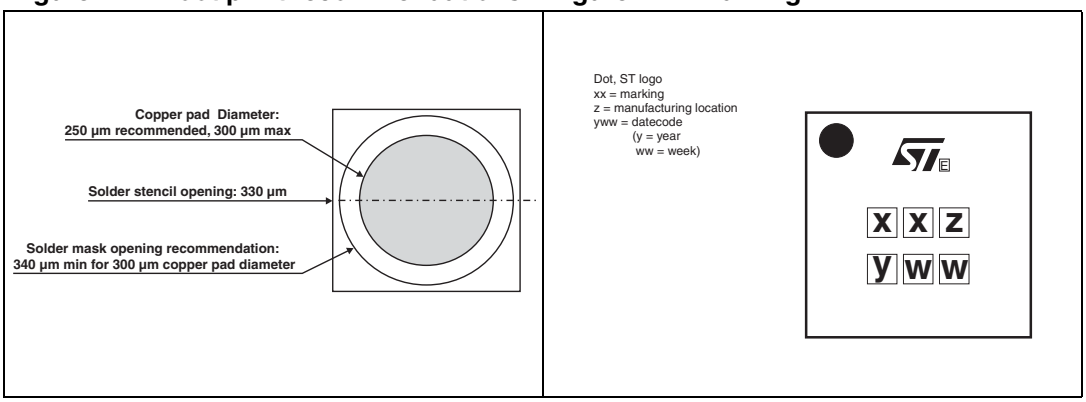
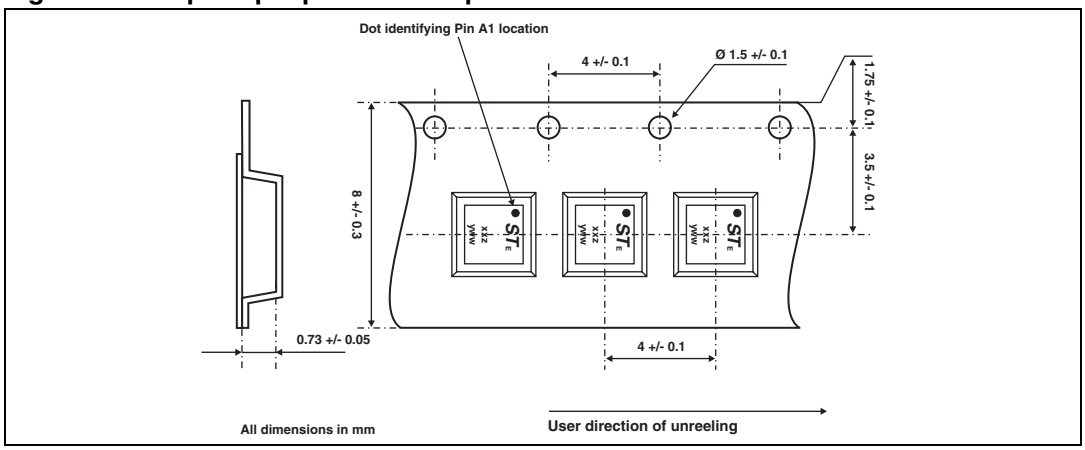


Figure 13. Flip-Chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Note: More informations are available in the application notes:

AN1235: "Flip-Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-COM01C2	FE	Flip-Chip	8.3 mg	5000	Tape and reel

5 Revision history

Date	Revision	Description of Changes
12-Jul-2005	1	First issue.
12-Aug-2005	2	Lead free added in Benefits on page 1. ECOPACK statement added on page 6.
27-Jan-2006	3	Improved graphics to show coating. Updated attenuation measurement graphic (Figure 3). Weight corrected.
04-Apr-2006	4	Reformatted to current standard. Pin identification in Figure 1 updated.

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