EMIF10-LCD01C2

10 LINE EMI FILTER AND ESD PROTECTION

IPAD™

MAIN PRODUCT CHARACTERISTICS:

Where EMI filtering in ESD sensitive equipment is required :

- LCD for Mobile phones
- Computers and printers
- Communication systems
- MCU Boards

DESCRIPTION

The EMIF10-LCD01C2 is a 10 line highly integrated devices designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences. The EMIF10 flip chip packaging means the package size is equal to the die size.
This filter includes an ESD protection circuitry, which prevents the device from destruction when subjected to ESD surges up 15kV.

BENEFITS

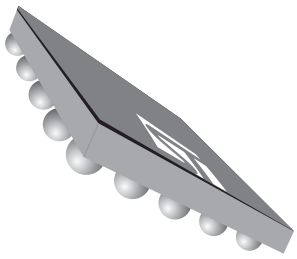
- EMI symmetrical (I/O) low-pass filter
- High efficiency in EMI filtering
- Very low PCB space consuming: < 7mm²
- Coating resin on back side
- Very thin package: 0.69 mm
- High efficiency in ESD suppression on input pins (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration and wafer level packaging.
- Lead free package

COMPLIES WITH THE FOLLOWING STANDARDS:

IEC61000-4-2:

Level 4 input pins 15kV (air discharge)
8kV (contact discharge)
Level 1 output pins 2kV (air discharge)
2kV (contact discharge)

MIL STD 833E - Method 3015-6 Class 3



Lead free coated Flip-Chip (25 bumps)

Figure 1: Pin Configuration (bump side)

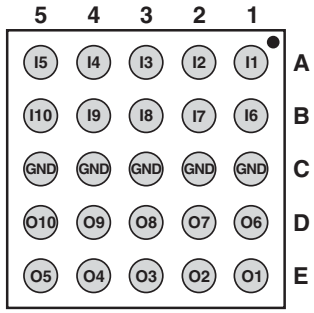


Figure 2: Basic Cell Configuration

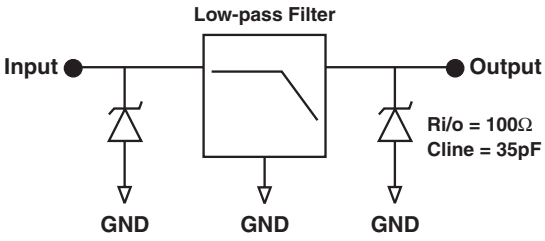


Table 1: Order Code

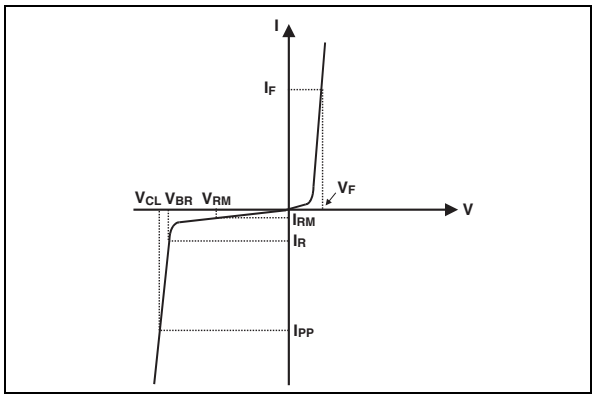
Part Number	Marking
EMIF10-LCD01C2	FL

Table 2: Absolute Maximum Ratings (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 3: Electrical Characteristics (T_{amb} = 25°C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
Cline	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3V			500	nA
$R_{I/O}$		90	100	110	Ω
Cline	@ 0V bias		28	35	pF
Rt / Ft	Induced rise and fall time 10-90% at 26 MHz frequency signal V = 1.9 V (Rt / Ft input 1 ns, 50Ω impedance generator)		8 (1)		ns

(1) guaranteed by design

Figure 3: S21(dB) all lines attenuation measurement and Aplac simulation

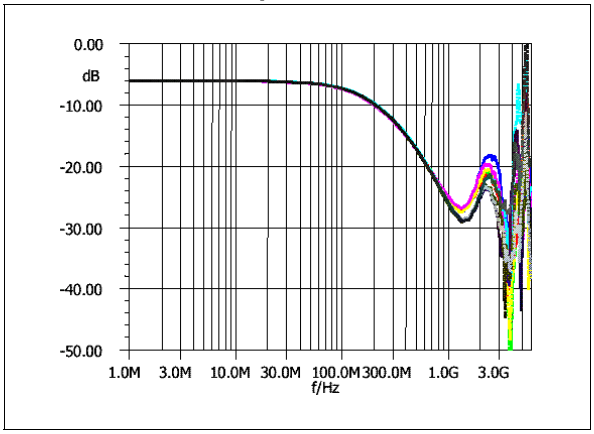


Figure 4: Analog cross talk measurements

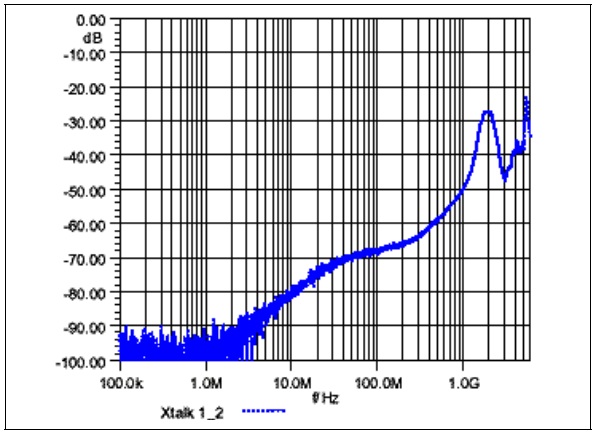


Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input and on one output

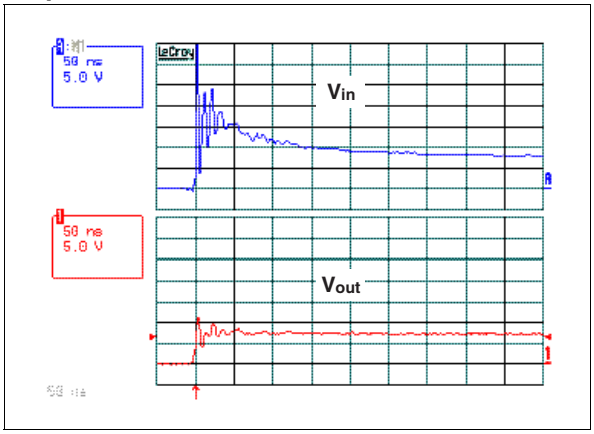


Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input and on one output

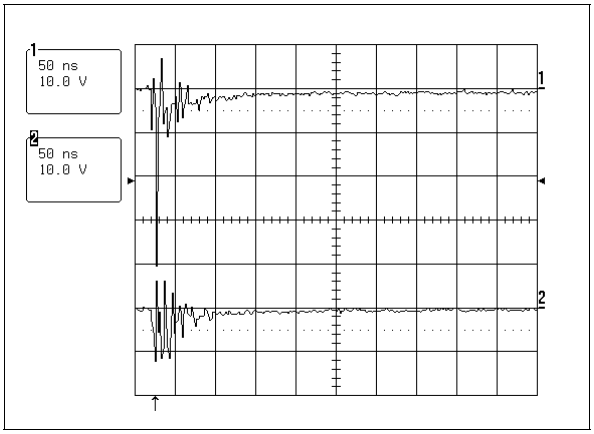


Figure 7: Line capacitance versus applied voltage

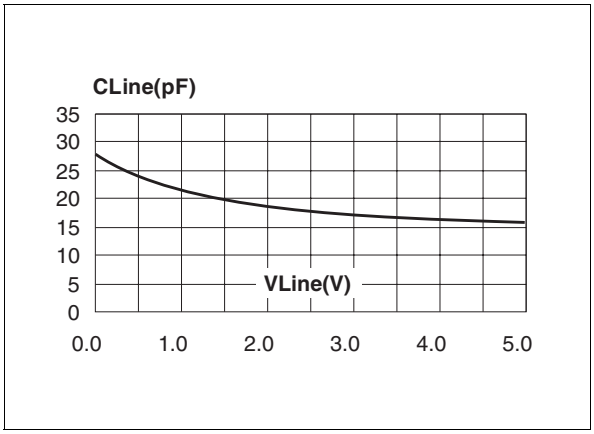


Figure 8: Rise time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator)

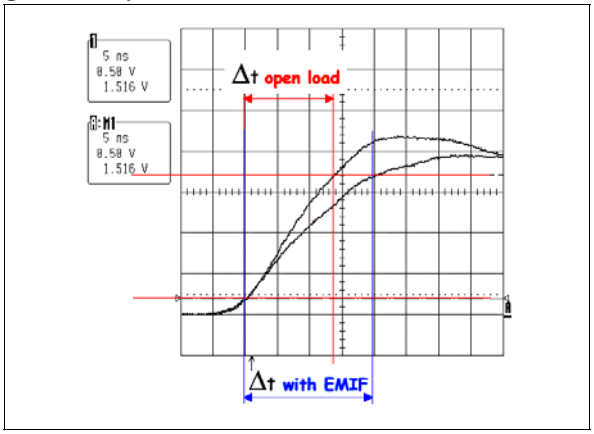


Figure 9: Fall time 10-90% measurements with 1.9V signal at 26 MHz frequency (50Ω generator)

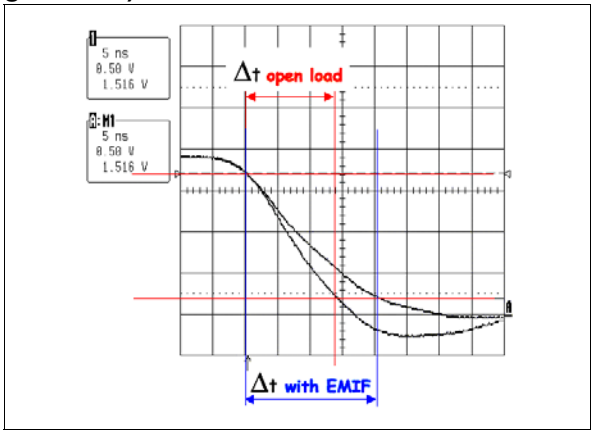
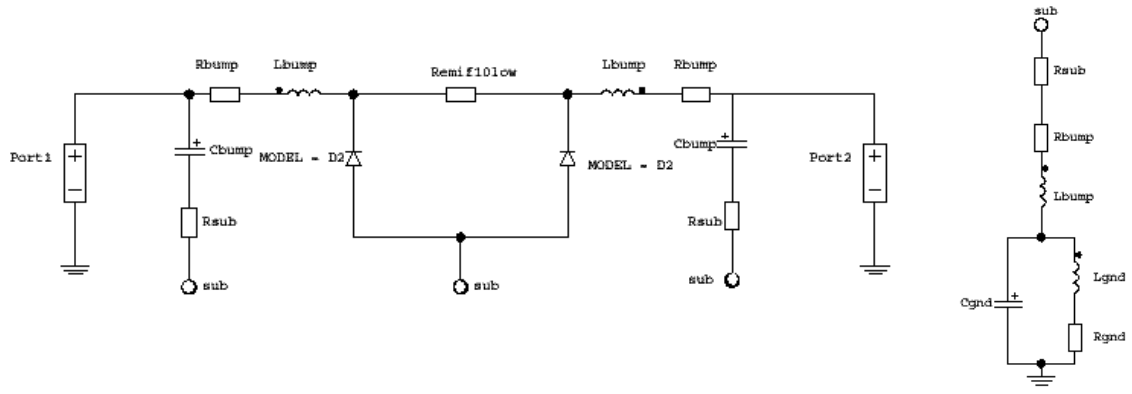


Figure 10: Aplac model



EMIF10-LCD01C1 model

Ground return

Figure 11: Aplac parameters

ZRZ structure
aplacvar Remif10low 100
aplacvar Cemif10flow 17.5pF
Bumps
aplacvar Lbump 50pH
aplacvar Rbump 20m
aplacvar Cbump 1.5pF
Bulk
aplacvar Rsub 100m
Gnd connections
aplacvar Rgnd 100m
aplacvar Lgnd 200pH
aplacvar Cgnd 0.15pF

BV = 7
CJO = Cemif10low
IBV = 1u
IKF = 1000
IS = 10f
ISR = 100p
N = 1
M = 0.3333
RS = 0.015
VJ = 0.6
TT = 50n

Figure 12: Order Code

EMIF yy - xxx zz Cx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10(pF)
or
3 letters = application
2 digits = version

Package
C = Flip-Chip
x = 1: 500µm, Bump = 315µm
= 2: Leadfree Pitch = 500µm, Bump = 315µm
= 3: Leadfree Pitch = 400µm, Bump = 250µm

Figure 13: FLIP-CHIP Package Mechanical Data

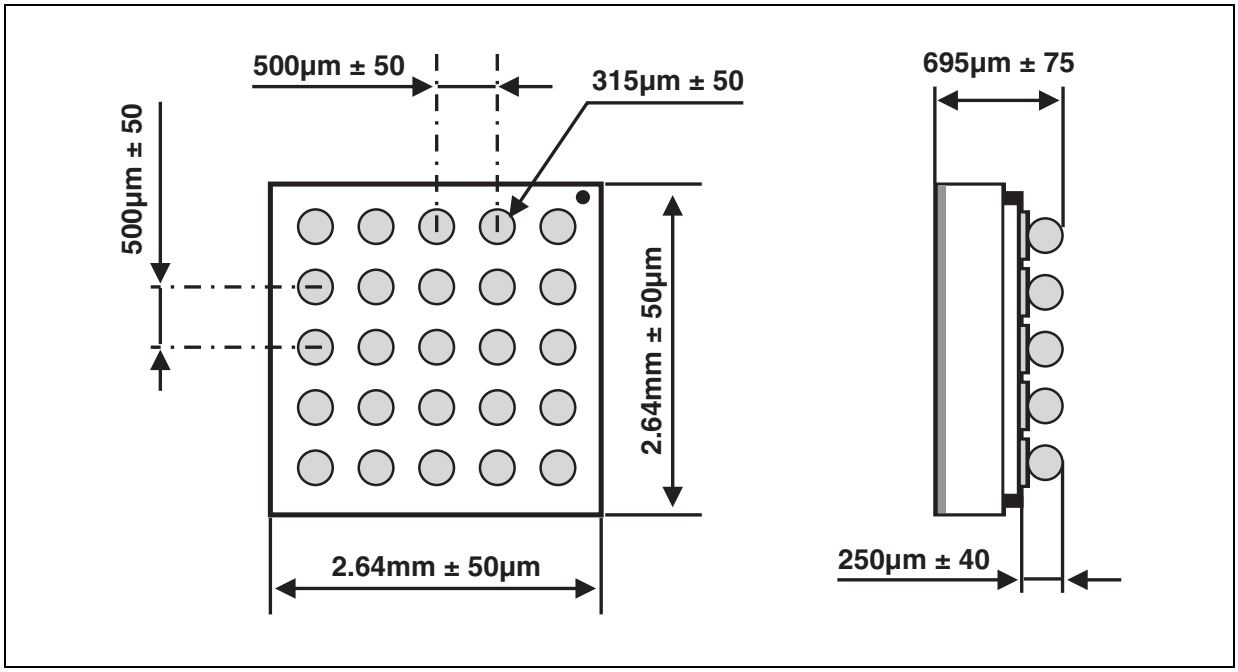


Figure 14: Foot Print Recommendations

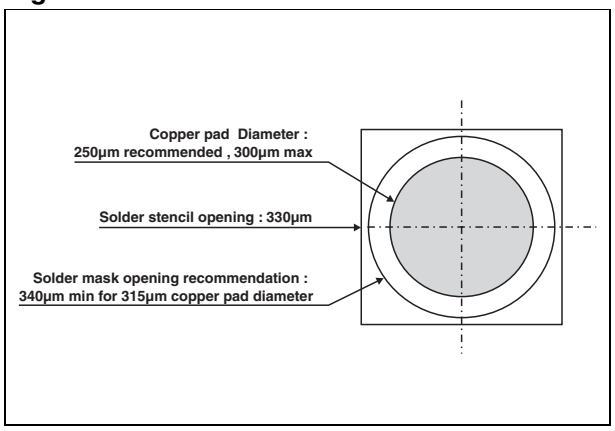


Figure 15: Marking

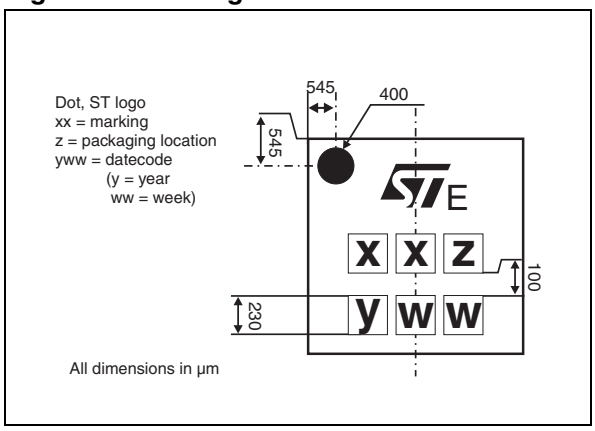
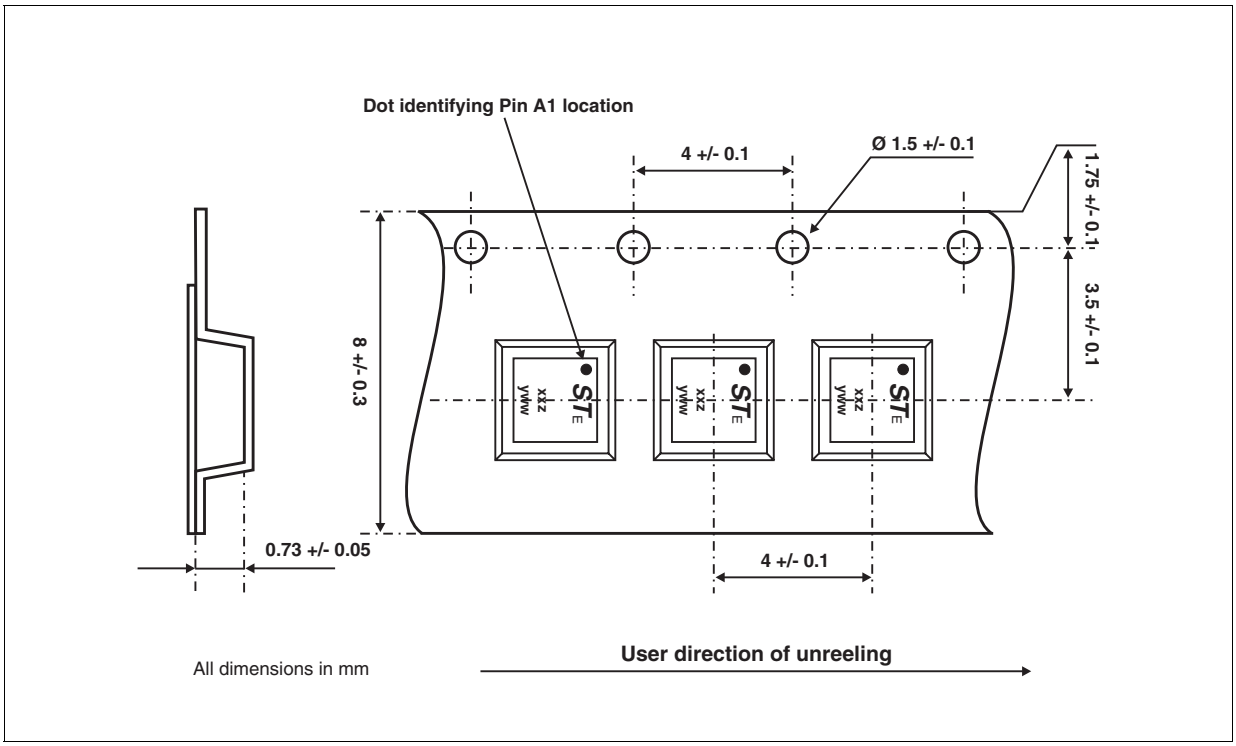


Figure 16: FLIP-CHIP Tape and Reel Specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Part Number	Marking	Package	Weight	Base qty	Delivery mode
EMIF10-LCD01C2	FL	Flip-Chip	9.3 mg	5000	Tape & reel (7”)

Table 4: Ordering Information

Note: Further packing information available in the application notes
- AN1235: "Flip-Chip: Package description and recommandations for use"
- AN1751: "EMI Filters: Recommendations and measurements"

Table 5: Revision History

Date	Revision	Description of Changes
12-Aug-2005	1	First issue