LD49150XX08
LD49150XX10, LD49150XX12

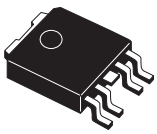
1.5 A very low drop for low output voltage regulator

Features

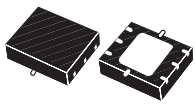
- Input voltage range:
  - V_I = 1.4 V to 5.5 V
  - V_{BIAS} = 3 V to 6 V
- Stable with ceramic capacitor
- ±1.5 % initial tolerance
- Maximum dropout voltage (V_I - V_O) of 200 mV over temperature
- Adjustable output voltage down to 0.8 V
- Ultra fast transient response (up to 10 MHz bandwidth)
- Excellent line and load regulation specifications
- Logic controlled shutdown option
- Thermal shutdown and current limit protection
- Junction temperature range: - 25 °C to 125 °C

Applications

- Graphics processors
- PC add-in cards
- Microprocessor core voltage supply
- Low voltage digital ICs
- High efficiency linear power supplies
- SMPS post regulators



PPAK



DFN6 (3x3 mm)

Description

The LD49150xx is a high-bandwidth, low-dropout, 1.5 A voltage regulator, ideal for powering core voltages of low-power microprocessors. The LD49150xx implements a dual supply configuration allowing for very low output impedance and very fast transient response. The LD49150xx requires a bias input supply and a main input supply, allowing for ultra-low input voltages on the main supply rail. The input supply operates from 1.4 V to 5.5 V and the bias supply requires between 3 V and 6 V for proper operation. The LD49150xx offers fixed output voltages from 0.8 V to 1.8 V and adjustable output voltages down to 0.8 V. The LD49150xx requires a minimum output capacitance for stability, and work optimally with small ceramic capacitors.

Table 1. Device summary

Order codes		Output voltages
PPAK (tape and reel)	DFN6 (tape and reel) (1)	
LD49150PT08R		0.8 V (2)
LD49150PT10R	LD49150PU10R	1.0 V
LD49150PT12R	LD49150PU12R	1.2 V

1. Available on request.
2. Adjustable version.

Contents

1 Typical application circuits

Figure 1. Adjustable version

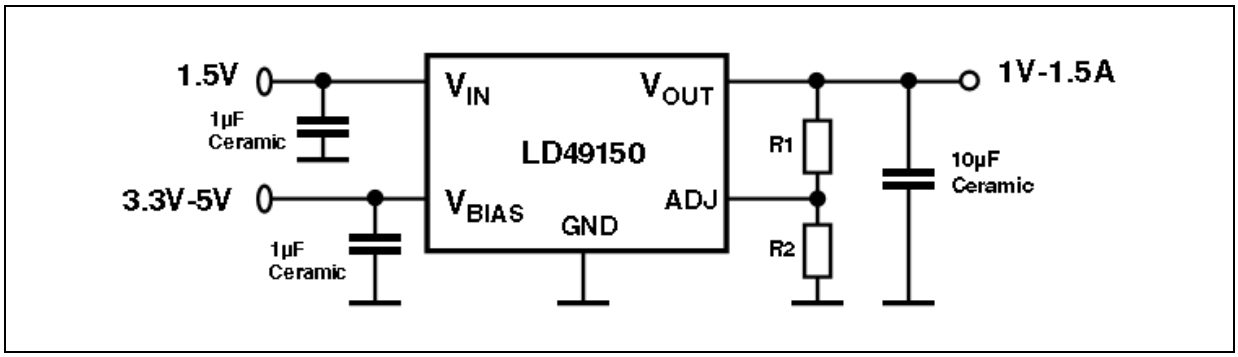
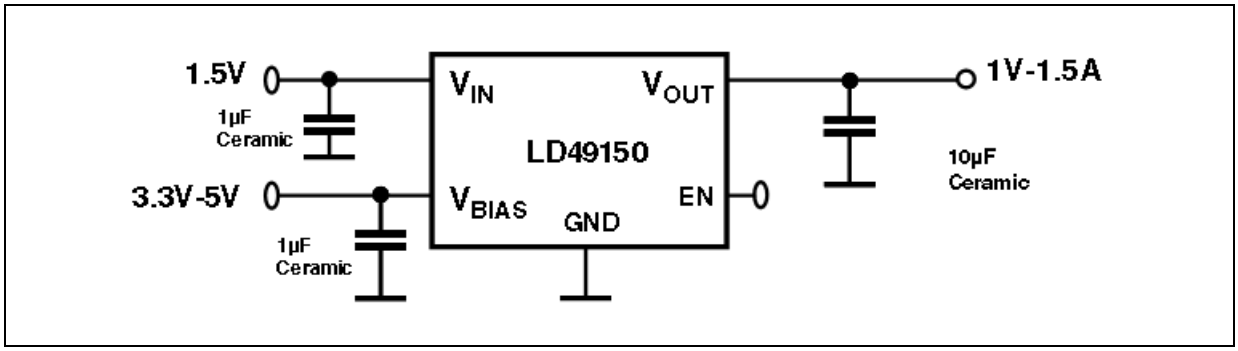


Figure 2. Fixed version with Enable



2 Alternative application circuits

Figure 3. Single supply voltage solution

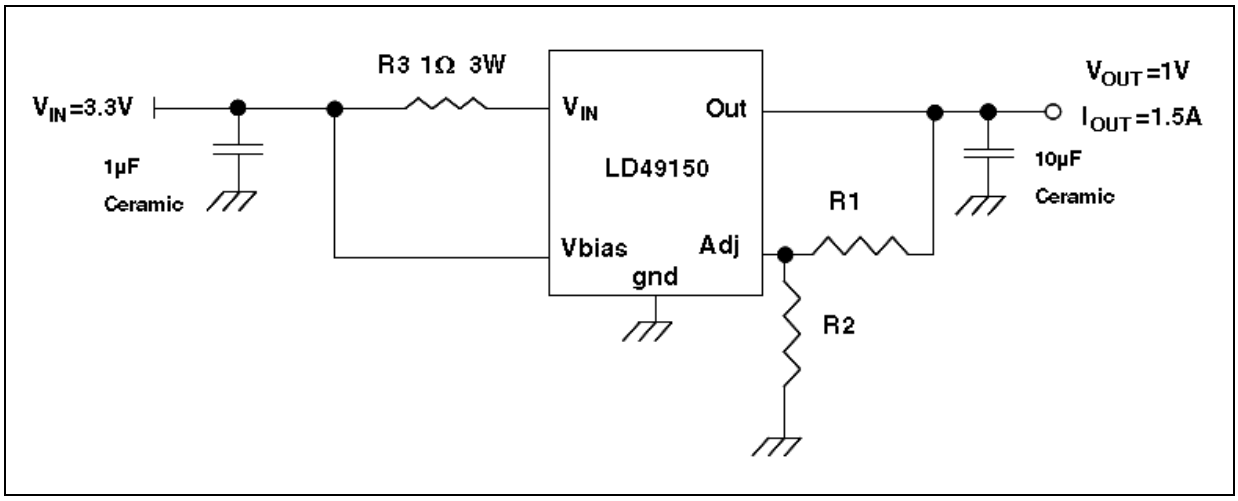
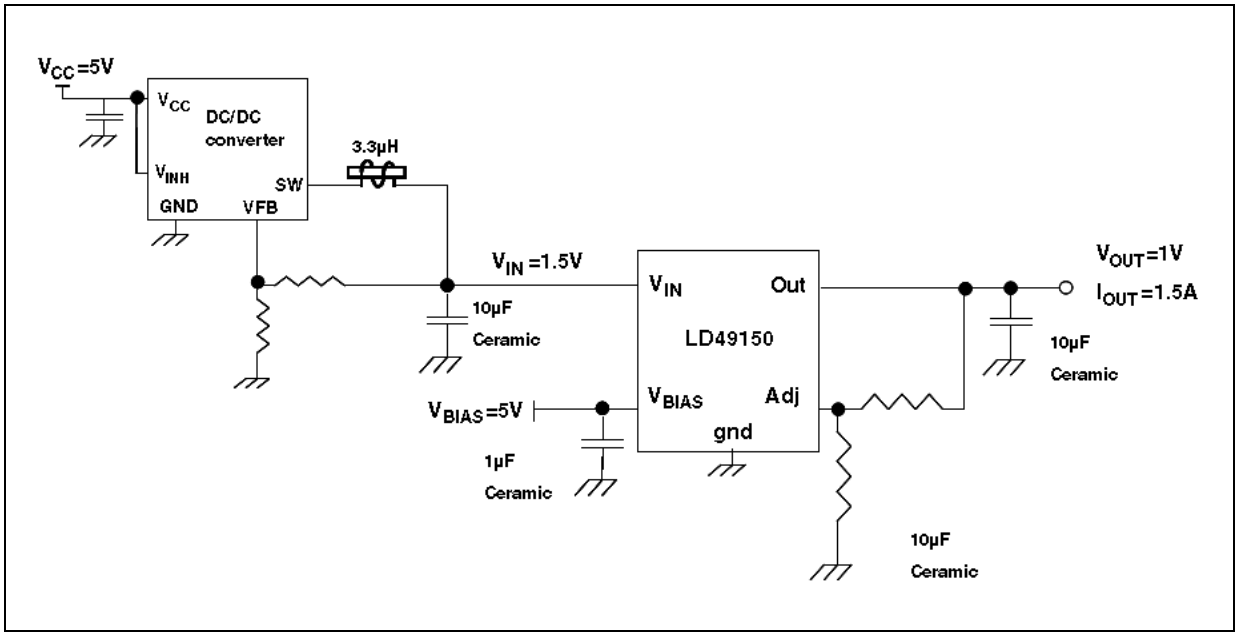
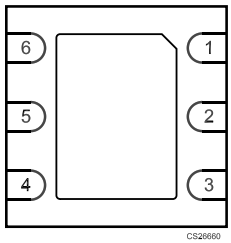


Figure 4. LD49150xx plus DC-DC pre-regulator to reduce power dissipation

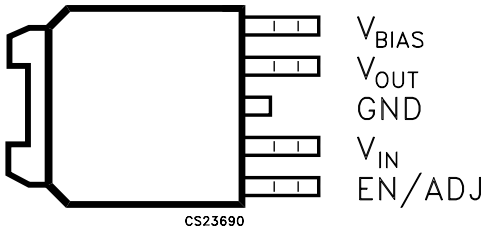


3 Pin configuration

Figure 5. Pin connections (top view for PPAK, bottom view for DFN)



DFN6 (3 x 3 mm)



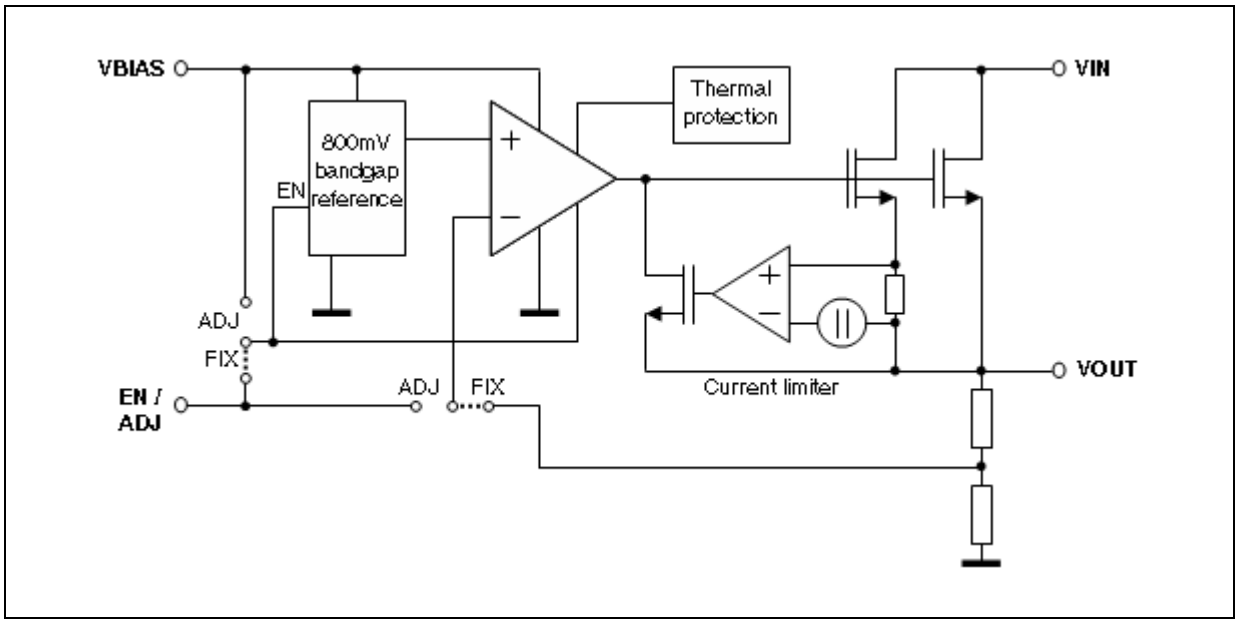
PPAK

Table 2. Pin description

Pin n° for PPAK	Pin n° for DFN	Symbol	Note
1	2	EN	For fixed versions: Enable (Input) - Logic High = Enable, Logic Low = Shutdown.
		ADJ	For adjustable versions: Adjustable regulator feedback input. Connect to resistor voltage divider.
2	3	V_{IN}	Input voltage which supplies current to the output power device.
3	1	GND	Ground (TAB is connected to ground).
4	4	V_{OUT}	Regulator output.
5	6	V_{BIAS}	Input bias voltage for powering all circuitry on the regulator with the exception of the output power device.
	5	N.C.	Not connect.

4 Diagram

Figure 6. Block diagram



5 Maximum ratings

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3 -0.3 to V_{BIAS} + 0.3	V
V_{BIAS}	BIAS supply voltage	-0.3 to 7	V
V_{EN}	Enable input voltage	-0.3 to 7	V
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-50 to 150	°C

1. All the values are referred to ground.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Operating ratings

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	1.4 to 5.5	V
V_{OUT}	Output voltage	0.8 to 4.5	V
V_{BIAS}	BIAS supply voltage	3 to 6	V
V_{EN}	Enable input voltage	0 to V_{BIAS}	V
T_J	Junction temperature range	-25 to 125	°C

6 Electrical characteristics

T_J = - 25 °C to 125 °C, $V_{BIAS} = V_O + 2.1$ V (1); $V_I = V_O$+1 V; $V_{EN} = V_{BIAS}$ (2), I_O = 10 mA; C_I = 1 µF; C_O = 10 µF; C_{BIAS} = 1 µF; unless otherwise specified.
Typical values are referred to T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage accuracy	T_J = 25 °C, fixed voltage options	-1.5		1.5	%
		Over temperature range	-3		3	
V_{LINE}	Line regulation	$V_I = V_O$ + 1 V to 5.5 V	-0.1		0.1	%/V
V_{LOAD}	Load regulation	I_L = 0 mA to 3 A, $V_{BIAS} \geq$ 3 V			1	%
V_{DROP}	Dropout voltage (V_I - V_O)	I_L = 1.5 A			200	mV
V_{DROP}	Dropout voltage (V_{BIAS}- V_O)	I_L = 1.5 A (1)		1.5	2.1	V
I_{GND}	Ground pin current	I_L = 0 mA		4	6	mA
		I_L = 1.5 A		4	6	
I_{GND_SHD}	Ground pin current in shutdown	$V_{EN} \leq$ 0.4 V (2)			5	µA
I_{VBIAS}	Current through V_{BIAS}	I_L = 0 mA		3	5	mA
		I_L = 1.5 A		3	5	
I_L	Current limit	V_O = 0 V	2.5			A
Enable input (2)						
V_{EN}	Enable input threshold (fixed voltage only)	Regulator Enable	1.4			V
		Regulator Shutdown			0.4	
I_{EN}	Enable pin input current			0.1	1	µA
Reference						
V_{REF}	Reference voltage	T_J = 25 °C	0.788	0.8	0.812	V
		Over temperature range	0.776	0.8	0.824	
SVR	Supply voltage rejection	V_I = 2.5 V ± 0.5 V, V_O = 1 V, F = 120 Hz, V_{BIAS} = 3.3 V		68		dB

1. For $V_O \leq$ 1 V, V_{BIAS} dropout specification does not apply due to a minimum 3 V V_{BIAS} input.
2. Fixed output voltage version only.

7 Typical characteristics

Figure 7. Reference voltage vs. temperature

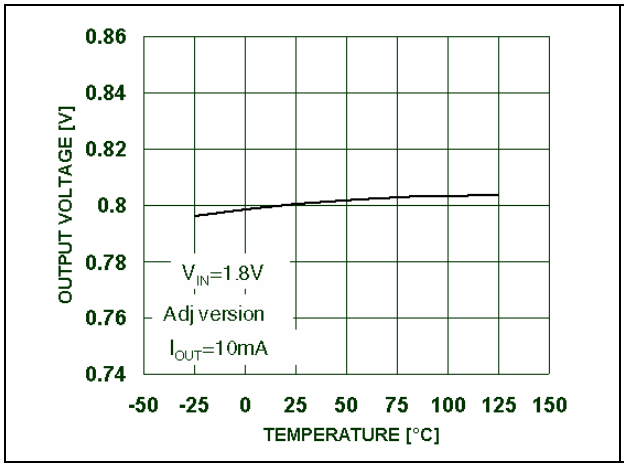


Figure 8. Output voltage vs. temperature

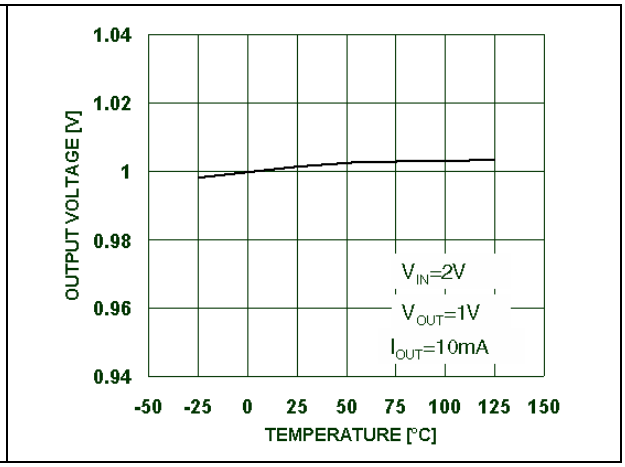


Figure 9. Load regulation vs. temperature

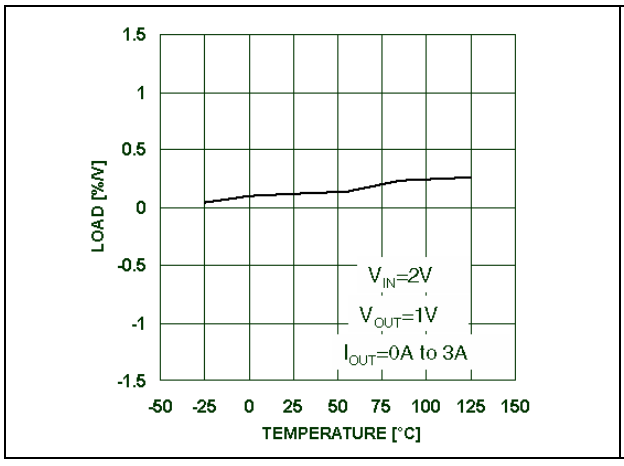


Figure 10. Line regulation vs. temperature

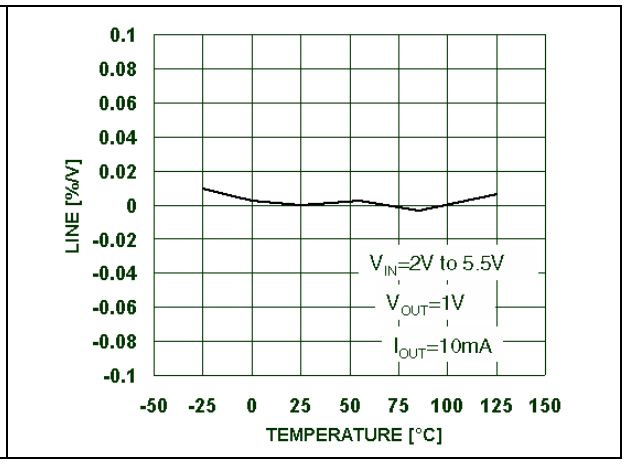


Figure 11. Output voltage vs. input voltage

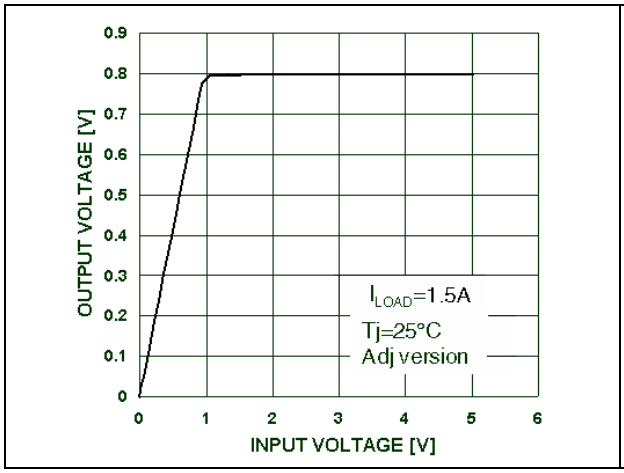


Figure 12. Dropout voltage (V_{IN}-V_{OUT}) vs. temperature

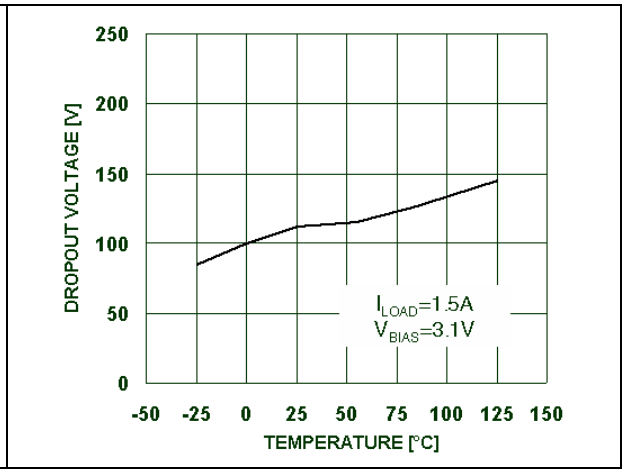


Figure 13. Dropout voltage (V_{IN}-V_{OUT}) vs. temperature

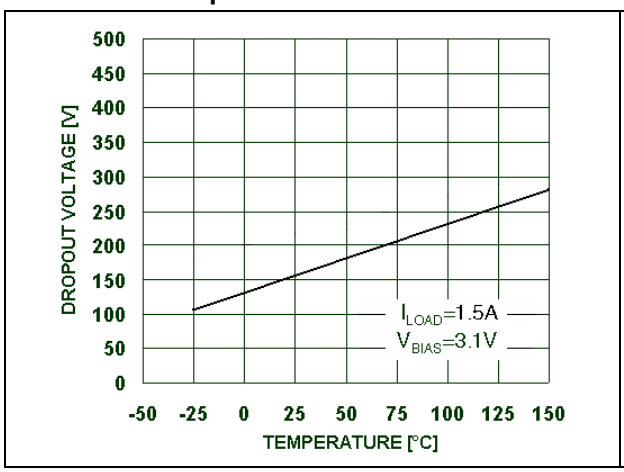


Figure 14. V_{BIAS} pin current vs. temperature

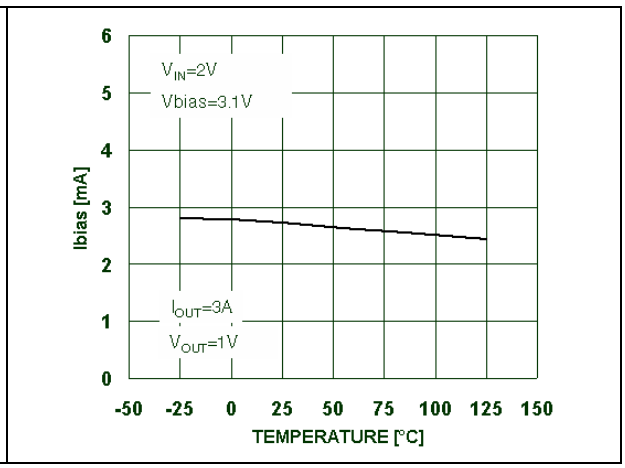


Figure 15. Noise vs. frequency

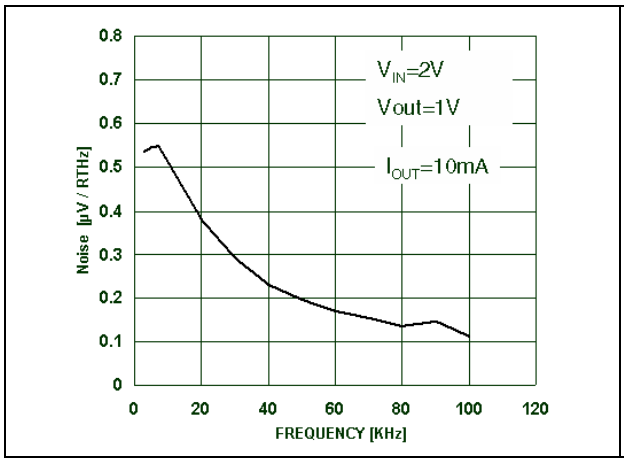


Figure 16. Quiescent current vs. temperature

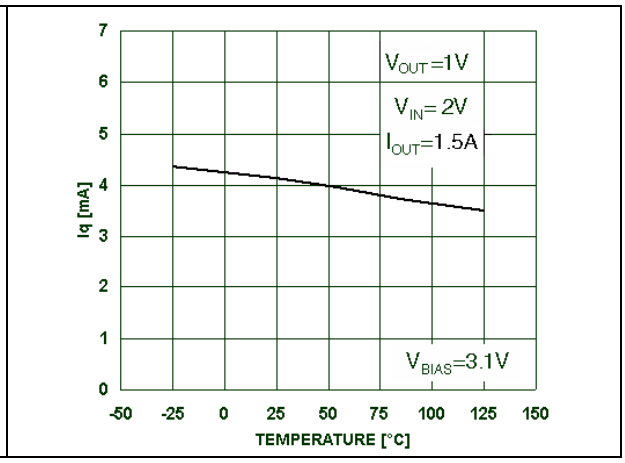


Figure 17. Supply voltage rejection vs. output current

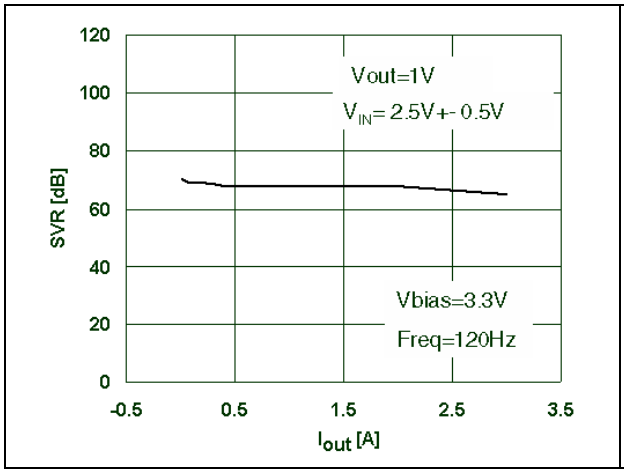


Figure 18. Stability region vs. C_{OUT} & High ESR

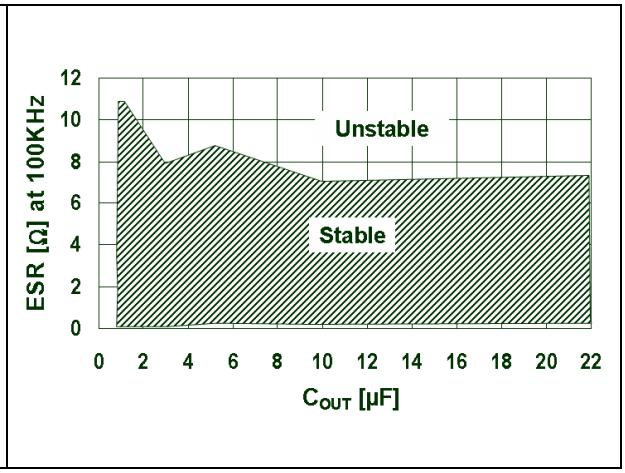


Figure 19. Stability region vs. C_{OUT} & low ESR

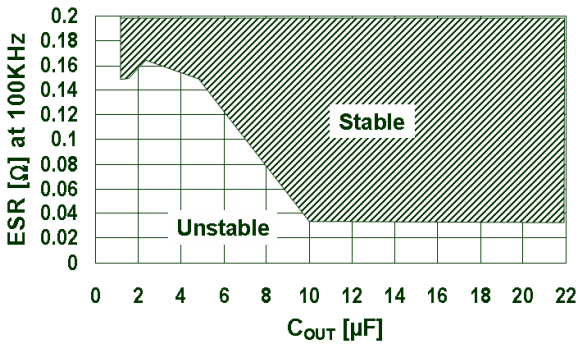
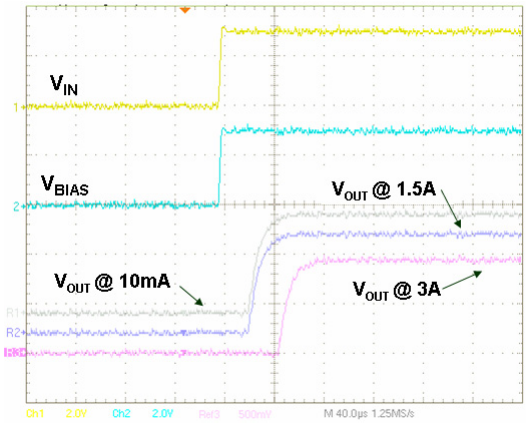
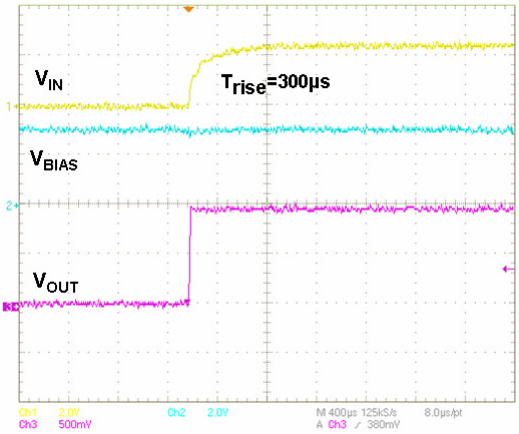


Figure 20. V_{BIAS} & V_{IN} start up transient response (V_{IN} and V_{BIAS} start up at the same time)



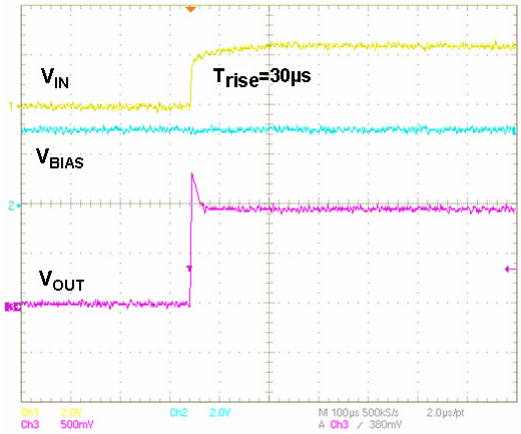
V_{IN}=V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 21. V_{IN} start up transient response (V_{BIAS} start up before V_{IN})



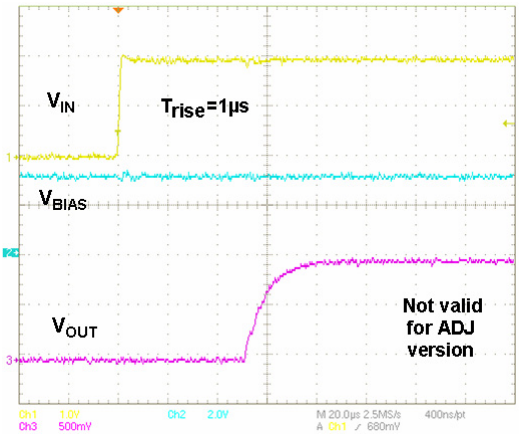
V_{IN}=2.5V, V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 22. V_{IN} start up transient response (V_{BIAS} start up before V_{IN})



V_{IN}=2.5V, V_{BIAS}=V_{INH}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 23. V_{IN} start up transient response (V_{BIAS} start up before V_{IN} and $V_{INH}=V_{IN}$)



$V_{IN}=V_{INH}=2.5V$, $V_{BIAS}=3.1V$, $V_{OUT}=1V$, $C_{OUT}=1\mu F$

8 Application hints

The LD49150xx is an ultra-high performance, low dropout linear regulator, designed for high current application that requires fast transient response. The LD49150xx operates from two input voltages, to reduce dropout voltage. The LD49150xx is designed so that a minimum of external component are necessary.

8.1 Input supply voltage (V_{IN})

V_{IN} provides the power input current to the LD49150xx. The minimum input voltage can be as low as 1.4 V, allowing conversion from very low voltage supplies to achieve low output voltage levels with very low power dissipation.

8.2 Bias supply voltage (V_{BIAS})

The LD49150xx control circuitry is supplied the V_{BIAS} pin which requires a very low bias current (3 mA typ.) even at the maximum output current level (1.5 A). A bypass capacitor on the bias pin is recommended to improve the performance of the LD49150xx during line and load transient. The small ceramic capacitor from V_{BIAS} to ground reduces high frequency noise that could be injected into the control circuitry from the bias rail. In typical applications a 1 µF ceramic chip capacitor may be used. The V_{BIAS} input voltage must be 2.1 V above the output voltage, with a minimum V_{BIAS} input voltage of 3 V.

8.3 External capacitors

To assure regulator stability, input and output capacitors are required as shown in the *1: Typical application circuits*.

8.4 Output capacitor

The LD49150xx requires a minimum output capacitance to maintain stability. A ceramic chip capacitor of at least 1 µF is required. However, specific capacitor selection could be needed to ensure the transient response. A 1 µF ceramic chip capacitor satisfies most applications but 10 µF is recommended to ensure better transient performances. In applications where the V_{IN} level is close to the maximum operating voltage (V_{IN} > 4 V), it is strongly recommended to use an output capacitors of, at least, 10 µF in order to avoid over-voltage stress on the Input/output power pins during short circuit conditions due to parasitic inductive effect. The output capacitor must be located as close as possible to the output pin of the LD49150xx. The ESR (equivalent series resistance) of the output capacitor must be within the "stable" region as shown in the typical characteristics figures. Both ceramic and tantalum capacitors are suitable.

8.5 Minimum load current

The LD49150xx does not require a minimum load to maintain output voltage regulation.

8.6 Power sequencing recommendations

In order to ensure the correct biasing and settling of the regulator internal circuitry during the startup phase, as well as to avoid overvoltage spikes at the output, it is recommended to provide for the correct power sequencing.

As a general rule the V_{IN} and V_{INH} signals timings at startup should be chosen properly, so that they are applied to the device after the V_{BIAS} voltage is already settled at its minimum operative value (see paragraph *8.2: Bias supply voltage (VBIAS)*). This can be achieved, for instance, by avoiding too slow V_{BIAS} rising edges (T_r >10 ms).

Provided that the above condition is satisfied, when fast V_{IN} transient input (T_r < 100 µs) is present, a smooth startup, with limited overvoltage on the output, can be obtained by applying V_{IN} voltage at the same time as the V_{BIAS} voltage (refer to *Figure 20*, *Figure 21* and *Figure 22 on page 11*).

In the fixed voltage versions it is possible to reduce overvoltage spikes during very fast startup (T_r << 100 µs) by pulling the V_{INH} pin up to V_{IN} voltage (see *Figure 23 on page 12*).

8.7 Power dissipation/heatsinking

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS} - V_{OUT} \times I_{OUT}$$

Where:

- V_{IN}, input supply voltage
- V_{BIAS}, bias supply voltage
- V_{OUT}, output voltage
- I_{OUT}, load current

From this data, we can calculate the thermal resistance (θ_{SA}) required for the heat sink using the following formula:

$$\theta_{SA} = (T_J - T_A/P_D) - (\theta_{JC} + \theta_{CS})$$

The maximum allowed temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

The maximum allowable value for junction to ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JAmax} = T_{Rmax} / P_D$$

This part is available for the PPAK package.

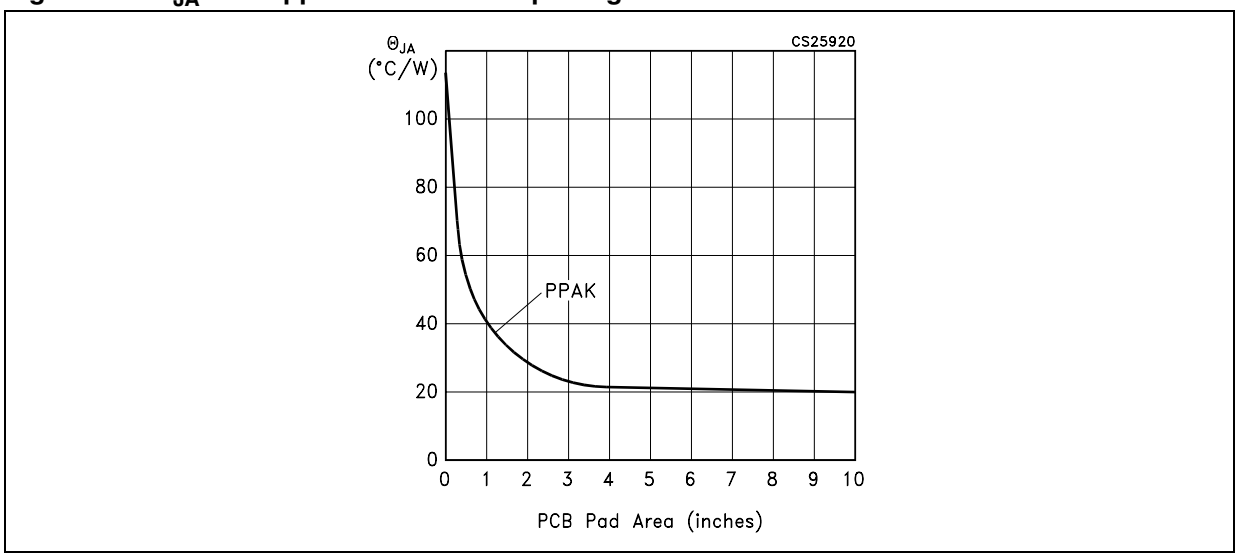
The thermal resistance depends on the amount of copper area or heat sink, and on air flow. If the maximum allowable value of θ_{JA} calculated above is ≥ 100 °C/W for the PPAK package, no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable θ_{JA} falls below these limits, a heat sink is required as described below.

8.8 Heatsinking PPAK package

The PPAK package uses the copper plane on the PCB as a heatsink. The tab of these packages is soldered to the copper plane for heat sinking. It is also possible to use the PCB ground plane a heatsink. This area can be the inner GND layer of a multi-layer PCB, or, in a dual layer PCB, it can be an unbroken GND area on the opposite side where the IC is situated with a dissipating area thermally connected through vias holes, filled by solder.

Figure 26 shows a curve for θ_{JA} of the PPAK package for different copper area sizes, using a typical PCB with 1/16 in thick G10/FR4.

Figure 24. θ_{JA} vs. copper area for PPAK package



8.9 Adjustable regulator design

The LD49150xx adjustable version allows fixing output voltage anywhere between 0.8 V and 4.5 V using two resistors as shown in the typical application circuit. For example, to fix the R_1 resistor value between V_{OUT} and the ADJ pin, the resistor value between ADJ and GND (R_2) is calculated by:

$R_2 = R_1 [0.8/(V_{OUT} - 0.8)]$

Where V_{OUT} is the desired output voltage.

It is suggested to use R1 values lower than 10 kΩ to obtain better load transient performances. Even, higher values up to 100 kΩ are suitable.

8.10 Enable

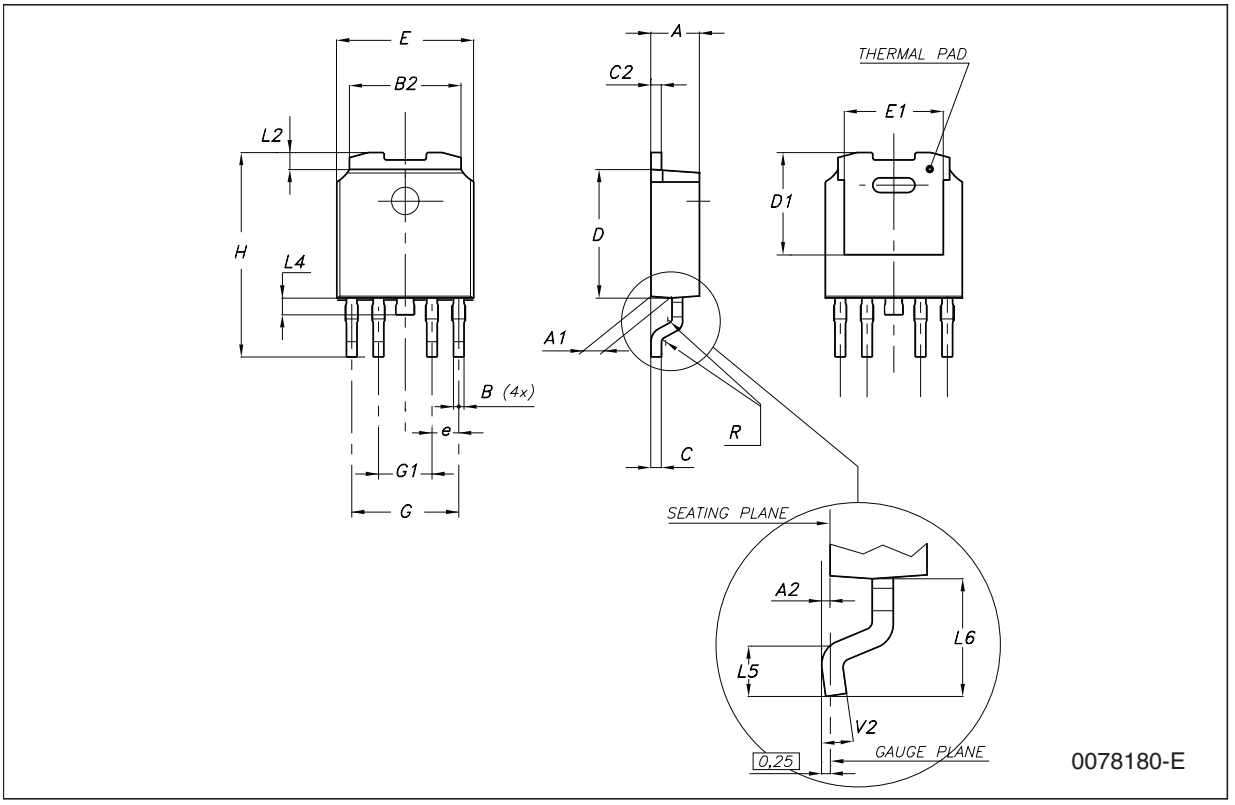
The fixed output voltage versions of LD49150xx feature an active high Enable input (EN) that allows on-off control of the regulator. The EN input threshold is guaranteed between 0.4 V and 1.4 V, for simple logic interfacing. The regulator is set in shut down mode when V_{EN} < 0.4 V and it is in operating mode (V_{OUT} activated) when V_{EN} > 1.4 V. If not in use, the EN pin must be tied directly to the V_{IN} to keep the regulator continuously activated. The En pin must not be left at high impedance.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

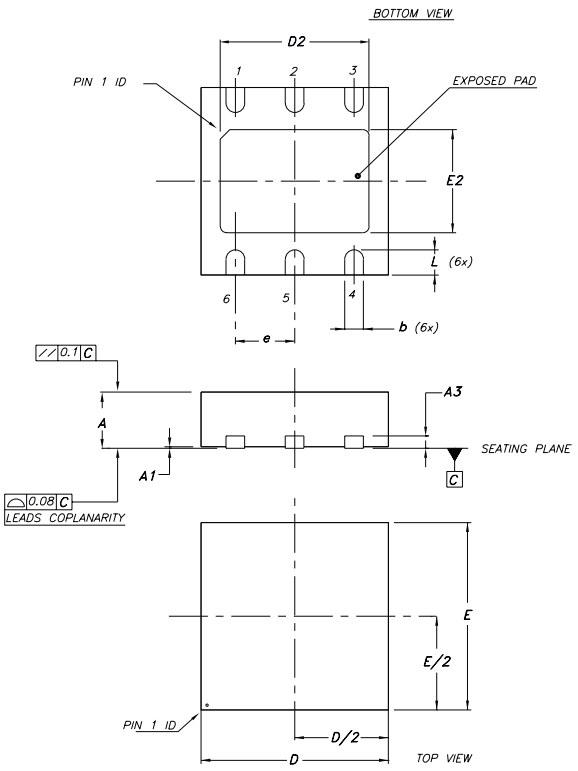
PPAK mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.4		0.6	0.015		0.023
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.201	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		1.27			0.050	
G	4.9		5.25	0.193		0.206
G1	2.38		2.7	0.093		0.106
H	9.35		10.1	0.368		0.397
L2		0.8	1		0.031	0.039
L4	0.6		1	0.023		0.039
L5	1			0.039		
L6		2.8			0.110	



DFN6 (3x3 mm) mechanical data

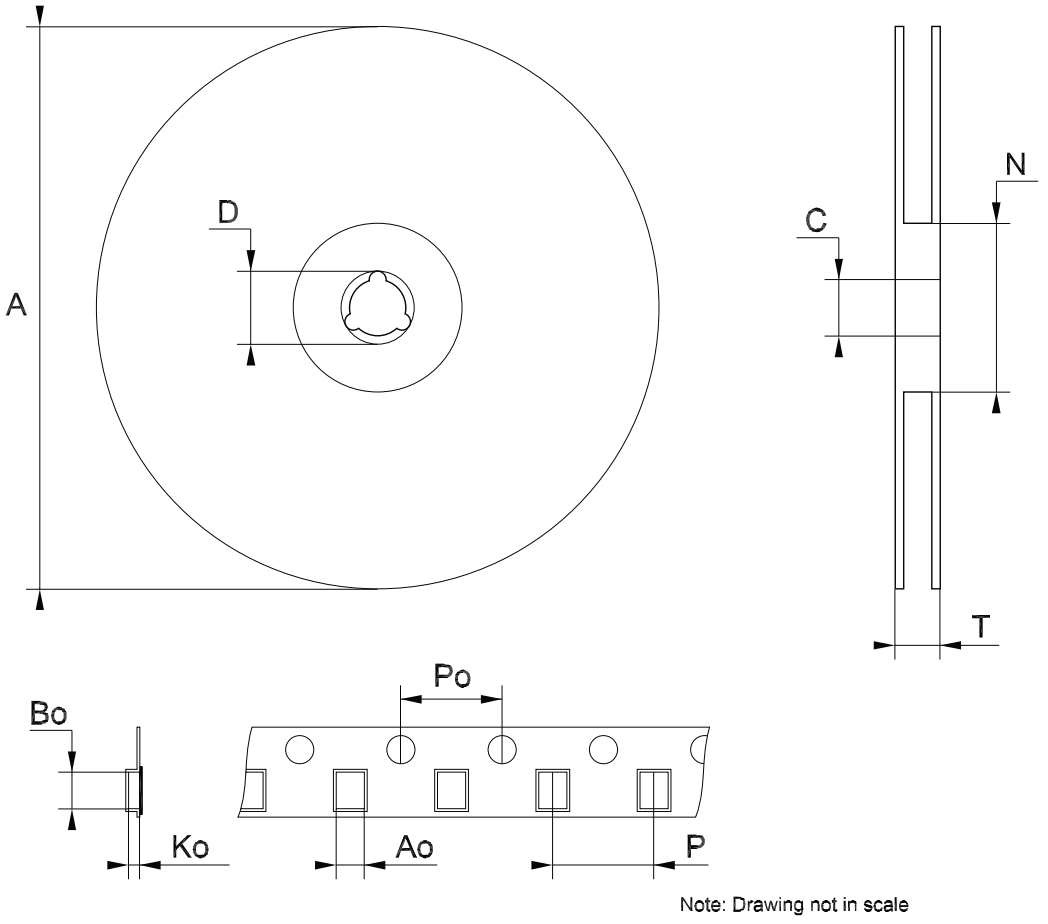
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20			0.008	
b	0.23	0.30	0.38	0.009	0.012	0.015
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.23	2.38	2.48	0.088	0.094	0.098
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50	1.65	1.75	0.059	0.065	0.069
e		0.95			0.037	
L	0.30	0.40	0.50	0.012	0.016	0.020



7946637A

Tape & reel DPAK-PPAK mechanical data

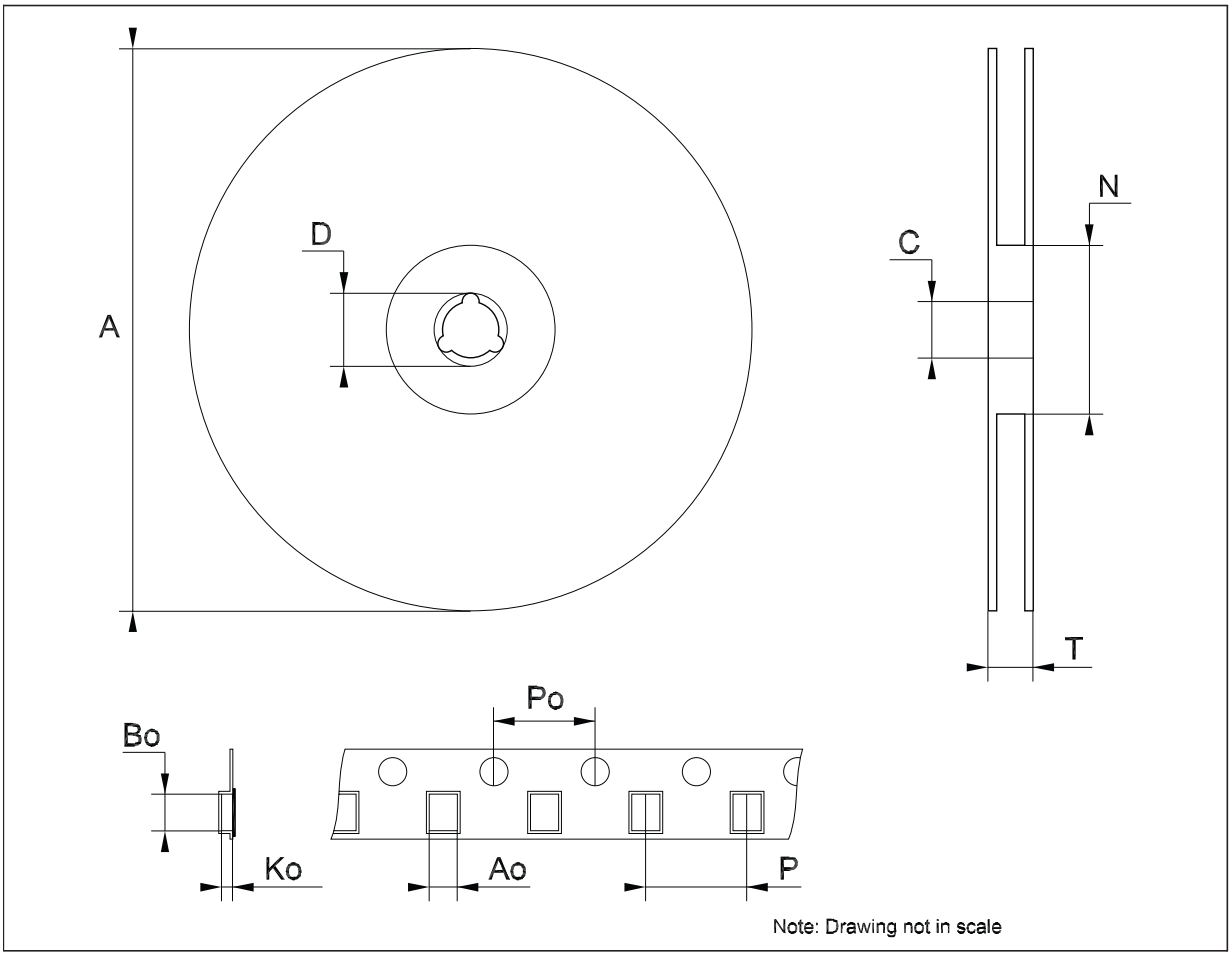
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.80	6.90	7.00	0.268	0.272	0.2.76
Bo	10.40	10.50	10.60	0.409	0.413	0.417
Ko	2.55	2.65	2.75	0.100	0.104	0.105
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	7.9	8.0	8.1	0.311	0.315	0.319



Note: Drawing not in scale

Tape & reel QFNxx/DFNxx (3x3) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			180			7.087
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao		3.3			0.130	
Bo		3.3			0.130	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

10 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Apr-2007	1	Initial release.
12-Jan-2009	2	Added new package DFN6 (3x3 mm) and mechanical data.
29-Jun-2010	3	Modified *Section 8.6: Power sequencing recommendations on page 14*.

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