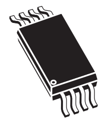
M24C32-DF M24C32-W M24C32-R M24C32-F

32-Kbit serial I²C bus EEPROM

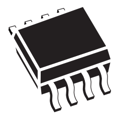
Datasheet – production data

Features

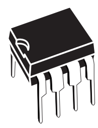
- Compatible with all I²C bus modes:
  - 1 MHz Fast-mode Plus
  - 400 kHz Fast mode
  - 100 kHz Standard mode
- Memory array:
  - 32 Kbit (4 Kbytes) of EEPROM
  - Page size: 32 bytes
  - Additional Write lockable page (M24C32-D order codes)
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Single supply voltage: 1.7 V to 5.5 V
- Operating temperature range: from -40 °C up to +85 °C
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-year data retention
- Packages
  - RoHS compliant and halogen-free (ECOPACK®)



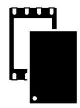
TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width



PDIP8 (BN)



UFDFPN8
(MB, MC)

This is information on a product in full production. www.st.com

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1 Description

The M24C32 is a 32-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 4 K × 8 bits.

The M24C32-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M24C32-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

The M24C32-D offers an additional page, named the Identification Page (32 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

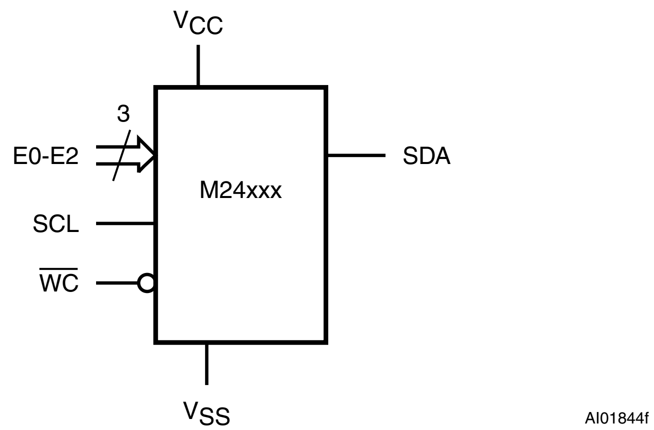
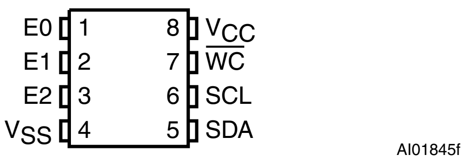


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections



1. DU: Don't Use (if connected, must be connected to V_{SS})
2. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

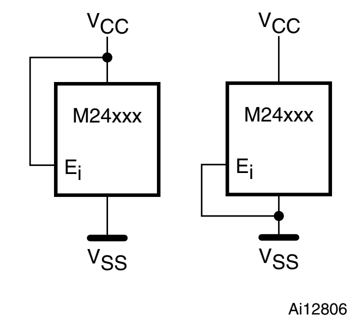
2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 11* indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see *Table 2*). These inputs must be tied to V_{CC} or V_{SS}, as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the internal reset threshold voltage, the device stops responding to any instruction sent to it.

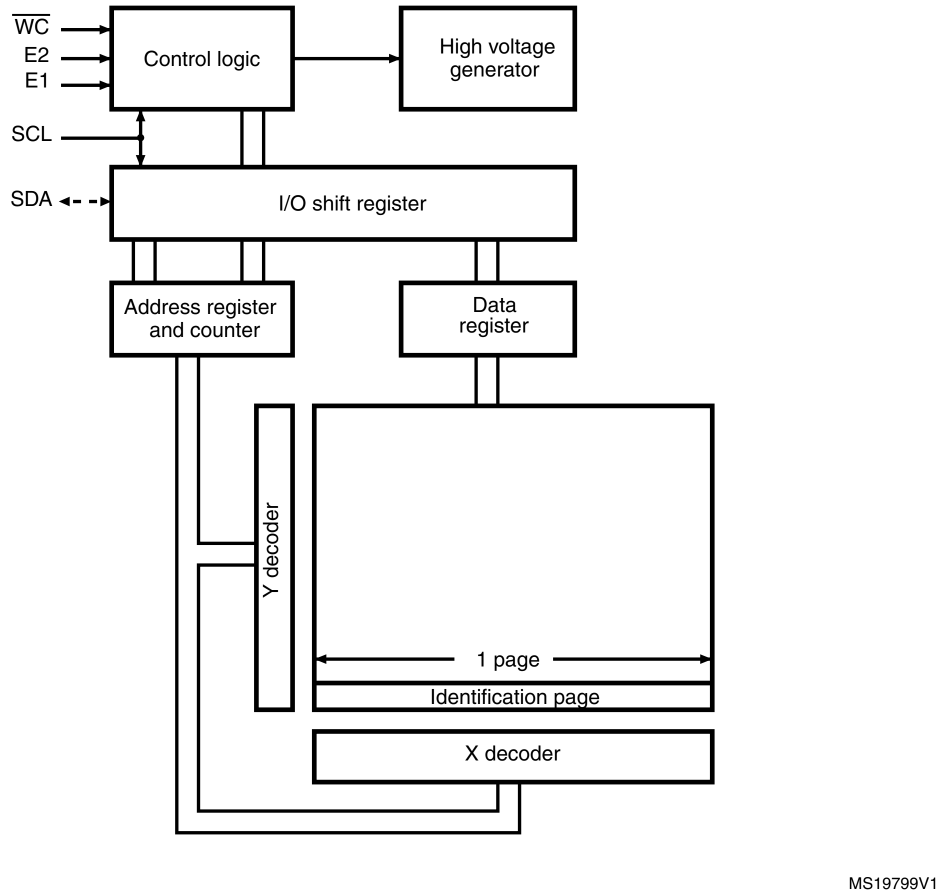
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown in *Figure 4*.

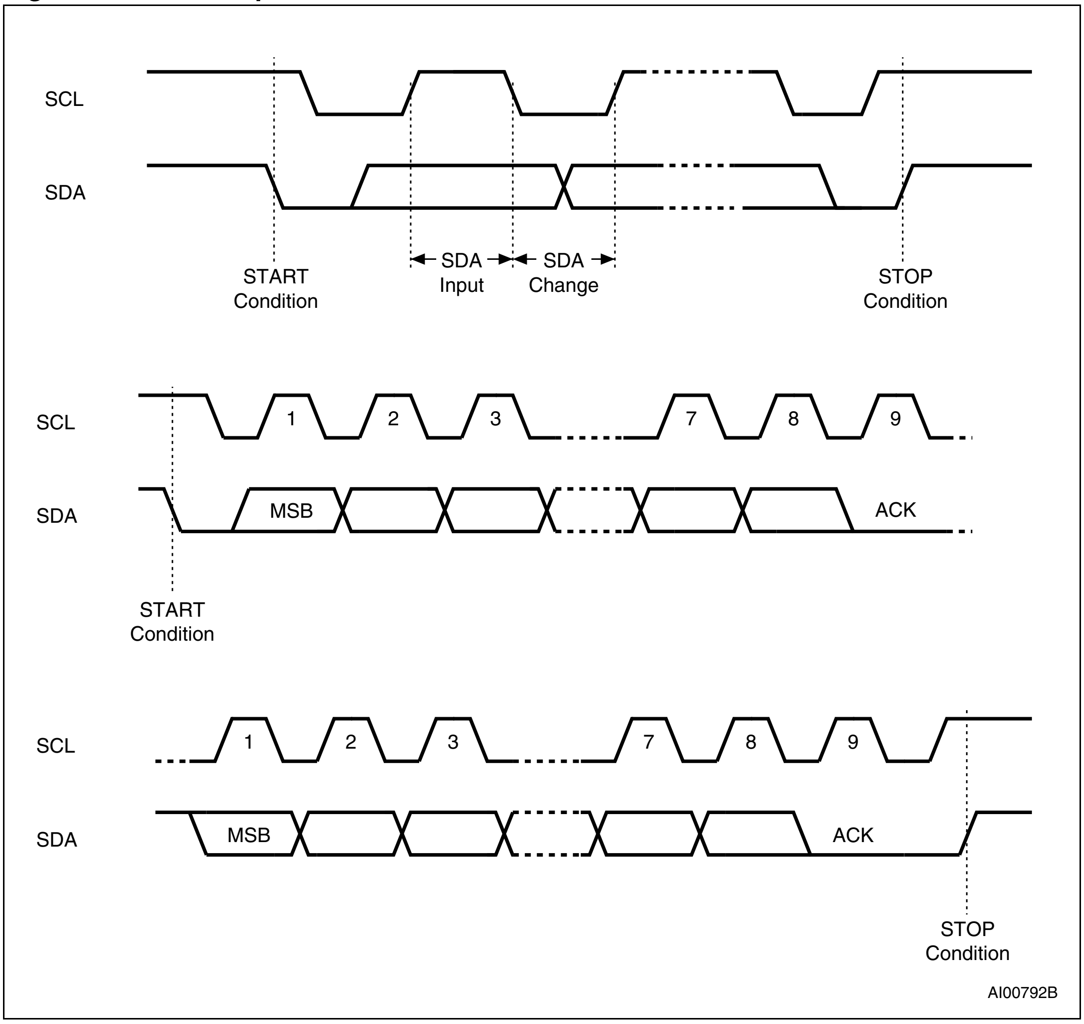
Figure 4. Block diagram



4 Device operation

The device supports the I^{2}C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 5. I^{2}C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 8* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			R$\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	R$\overline{W}$
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	R$\overline{W}$

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared with the value read on input pins E0,E1,E2.

When the device select code is received, the device only responds if the Chip Enable address is the same as the value on its Chip Enable E2,E1,E0 inputs.

The 8th bit is the Read/$\overline{\text{Write}}$ bit (R$\overline{\text{W}}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 6*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 4. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10^{th} bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

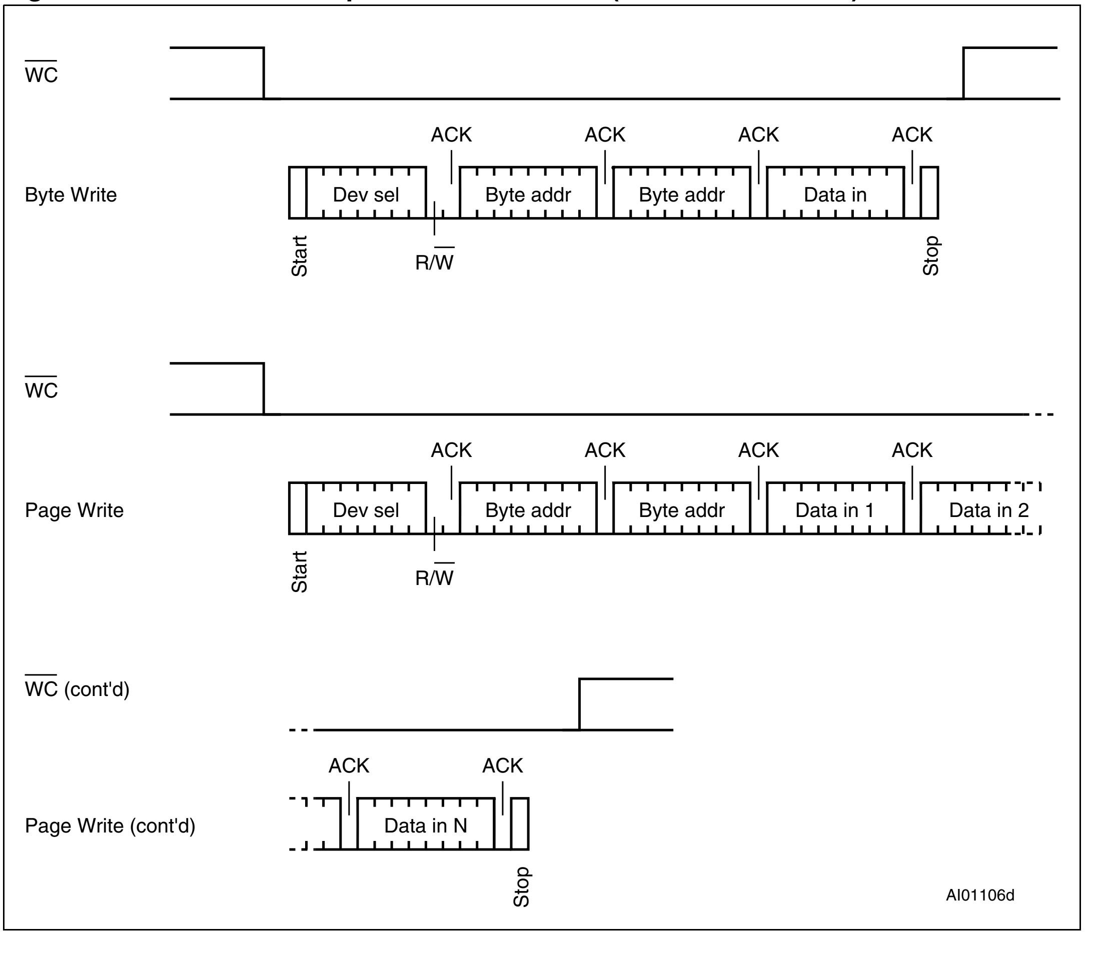
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 7*.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 6*.

Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



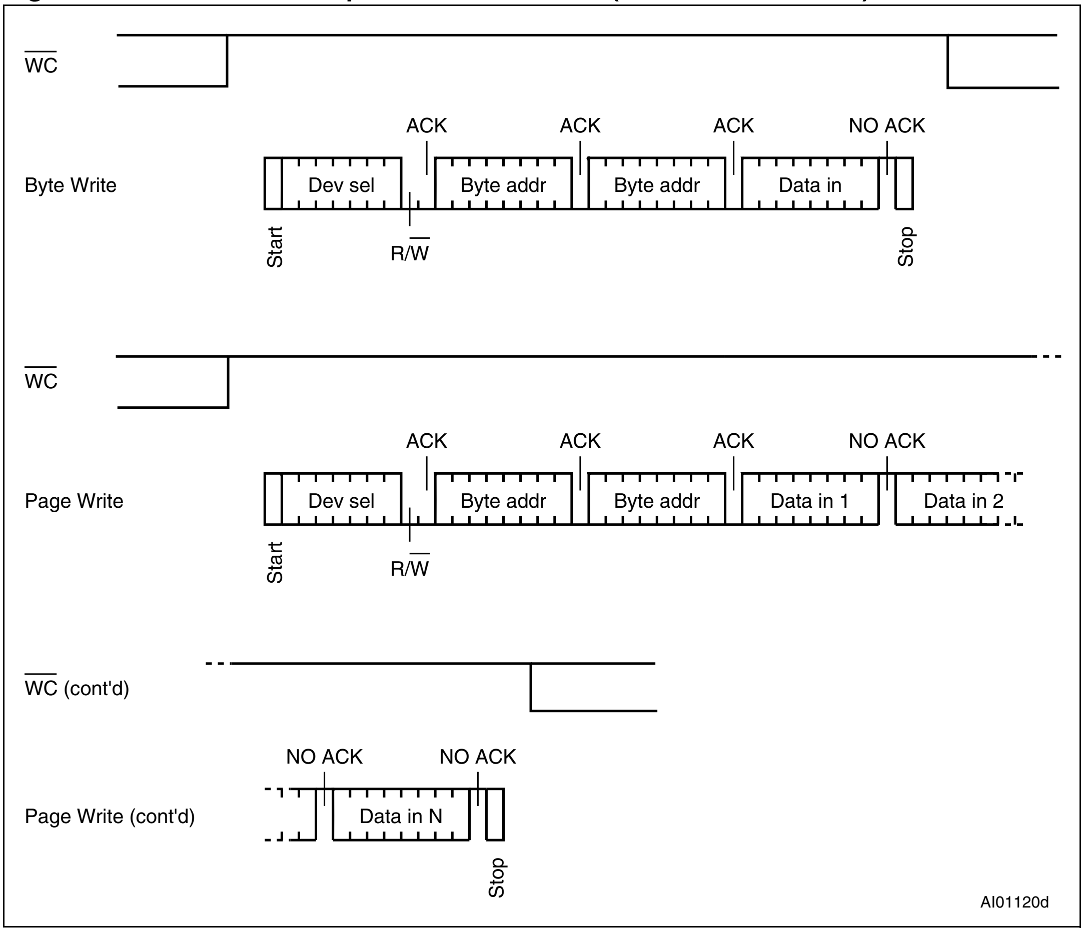
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, b16-b5, are the same. If more bytes are sent than will fit up to the end of the page, a condition known as “roll-over” occurs. In case of roll-over, the first bytes of the page are overwritten.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{\text{WC}}$) is low. If Write Control ($\overline{\text{WC}}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 7*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write mode sequences with $\overline{\text{WC}}$ = 1 (data write inhibited)



5.1.3 Write Identification Page (M24C32-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/A5 are don't care except for address bit A10 which must be ‘0’. LSB address bits A4/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

5.1.4 Lock Identification Page (M24C32-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.1.5 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[a]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[a]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in *Table 11: Cycling performance by groups of four bytes*.

a. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

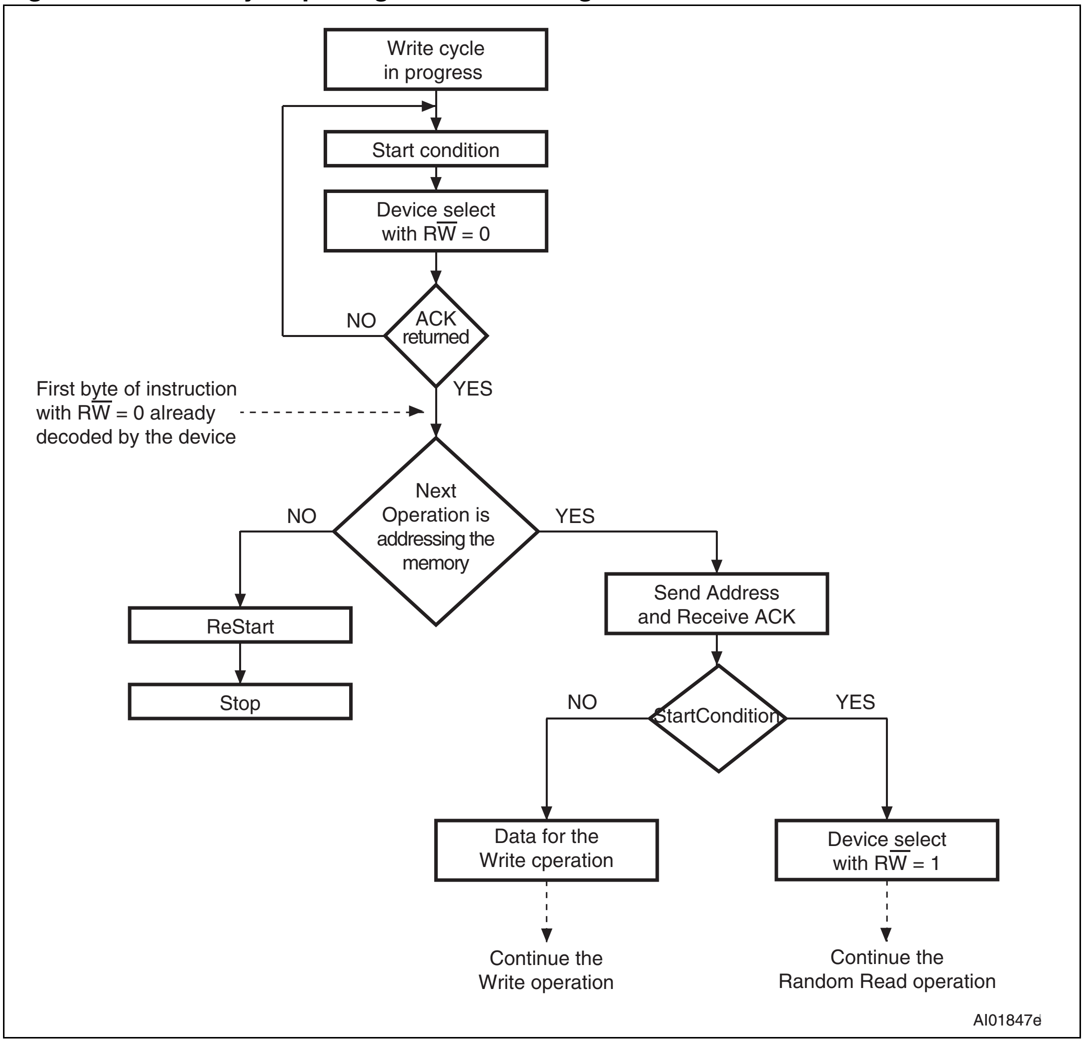
5.1.6 Minimizing Write delays by polling on ACK

The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 8. Write cycle polling flowchart using ACK



1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

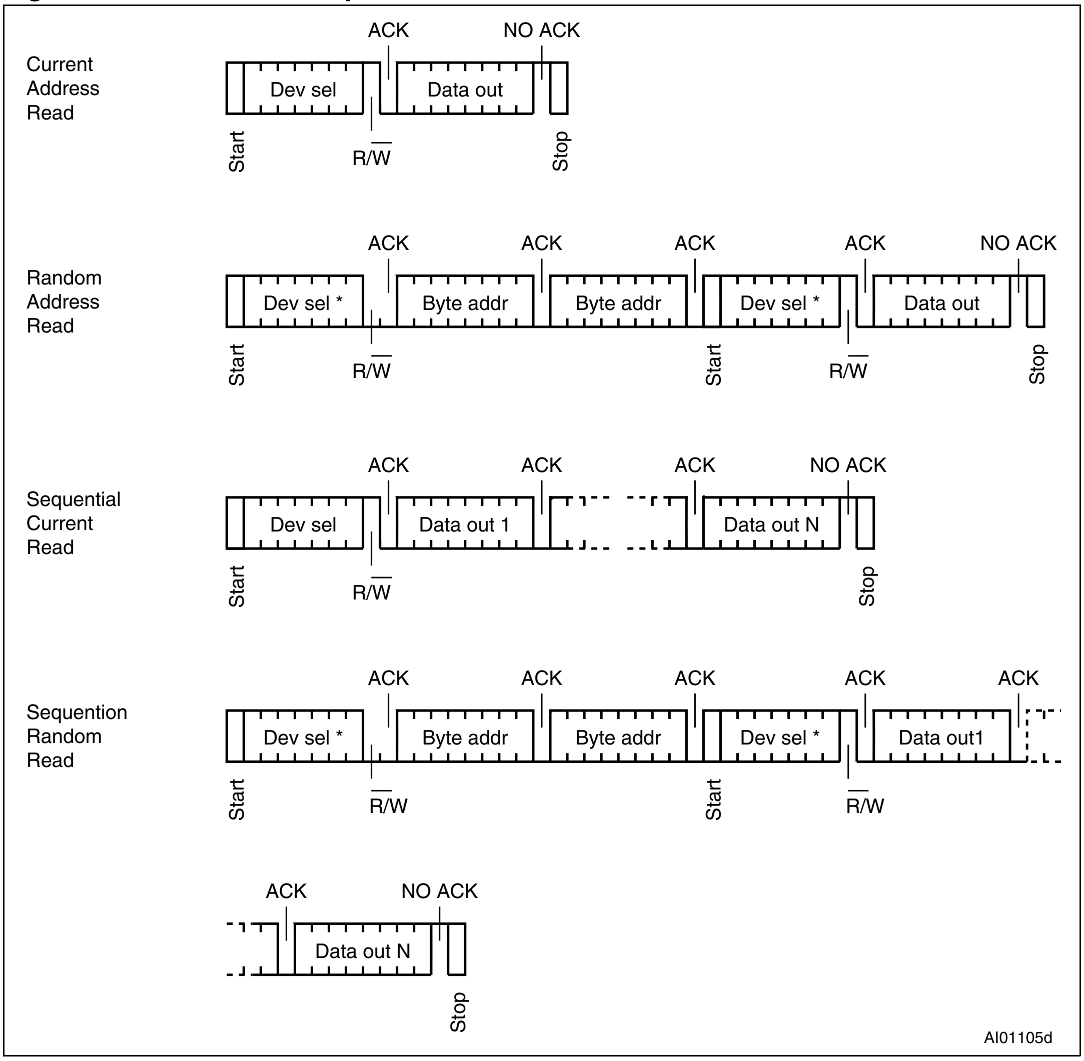
5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 9. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.3 Read Identification Page (M24C32-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.4 Read the lock status (M24C32-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6 Initial delivery state

The device is delivered with all bits set to 1 (both in the memory array and in the Identification page - that is, each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
	PDIP-specific lead temperature during soldering		260(2)	°C
V_{IO}	Input or output range	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(3)	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on pin pairs, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. **Operating conditions (voltage range W)**

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 7. **Operating conditions (voltage range R)**

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 8. **Operating conditions (voltage range F)**

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 9. **AC measurement conditions**

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time		50	ns
	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 10. **AC measurement I/O waveform**

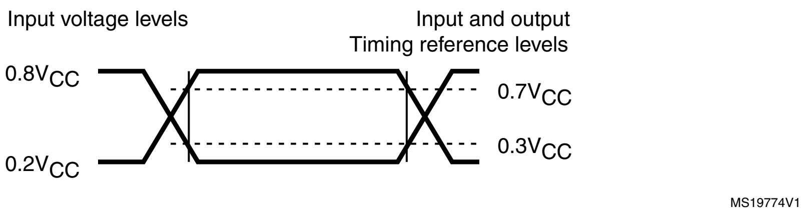


Table 10. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$)(2)	$V_{IN} < 0.3\ V_{CC}$	30		kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500		kΩ

1. Characterized only, not tested in production.
2. E2, E1, E0 input impedance when the memory is selected (after a Start condition).

Table 11. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition(1)	Max.	Unit
Ncycle	Write cycle endurance(2)	TA ≤ 25 °C, 1.8 V < V_{CC} < 5.5 V	4,000,000	Write cycle(3)
		TA = 85 °C, 1.8 V < V_{CC} < 5.5 V	1,200,000	

1. Cycling performance for products identified by process letter K.
2. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.
3. A Write cycle is executed when either a Page Write, a Byte Write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to *Section 5.1.5: ECC (Error Correction Code) and Write cycling*.

Table 12. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	TA = 55 °C	200	Year

1. For products identified by process letter K. The data retention is not tested in production but defined from characterization and qualification results.

Table 13. DC characteristics (M24C32-W, device grade 6)

Symbol	Parameter	Test conditions (see *Table 6*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)		2	mA
		2.5 V < V_{CC} < 5.5 V, f_c = 1 MHz(1) (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		5(4)	µA
V_{IL}	Input low voltage (SCL, SDA, WC)		–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA)		$0.7V_{CC}$	6.5	V
	Input high voltage (WC, E2, E1, E0)		$0.7V_{CC}$	V_{CC}+0.6	
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Only for devices operating at f_C max = 1 MHz (see *Table 17*)
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
4. The new M24C32-W devices (identified by the process letter K) offer I_{CC1} = 3µA (max)

Table 14. DC characteristics (M24C32-R, device grade 6)

Symbol	Parameter	Test conditions(1) (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz(2)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V < V_{CC} < 2.5 V		3(3)	mA
I_{CC1}	Standby supply current	Device not selected(4), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V

1. If the application uses the voltage range R device with 2.5 V < V_{cc} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 13* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see *Table 17*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 15. DC characteristics (M24C32-F, device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz[2]		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.7 V < V_{CC} < 2.5 V		3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.7 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.7 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.7 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V		0.2	V

1. If the application uses the voltage range F device with 2.5 V < Vcc < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 13* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see *Table 17*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 16. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100(5)	-	ns
t_{CLQV}(6)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL}(7)(1)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}(8)(1)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Internal Write cycle duration	-	5	ms
t_{NS}(2)		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80(9)	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. The previous product identified by process letter P was specified with t_{CLQX} = 200 ns (min). Both values offer a safe margin compared to the I²C specification recommendations.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 11*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
9. The previous M24C32 device (identified by process letter P) offers t_{NS} = 100 ns (max), while the current M24C32 device offers t_{NS} = 80 ns (max). Both products offer a safe margin compared to the 50 ns minimum value recommended by the I²C specification.

Table 17. 1 MHz AC characteristics

Symbol	Alt.	Parameter[1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	[2]	[2]	ns
t_{XL1XL2}	t_F	Input signal fall time	[2]	[2]	ns
t_{QL1QL2}[3]	t_F	SDA (out) fall time	20[4]	120	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}[5][6]	t_{AA}	Clock low to next data valid (access time)		450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL}[7][3]	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}[8][3]	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	5	ms
t_{NS}[3]		Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. Only for M24C32 devices identified by the process letter K (devices qualified at 1 MHz).
2. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when $f_C < 1$ MHz.
3. Characterized only, not tested in production.
4. With C_L = 10 pF
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 5*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.

Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

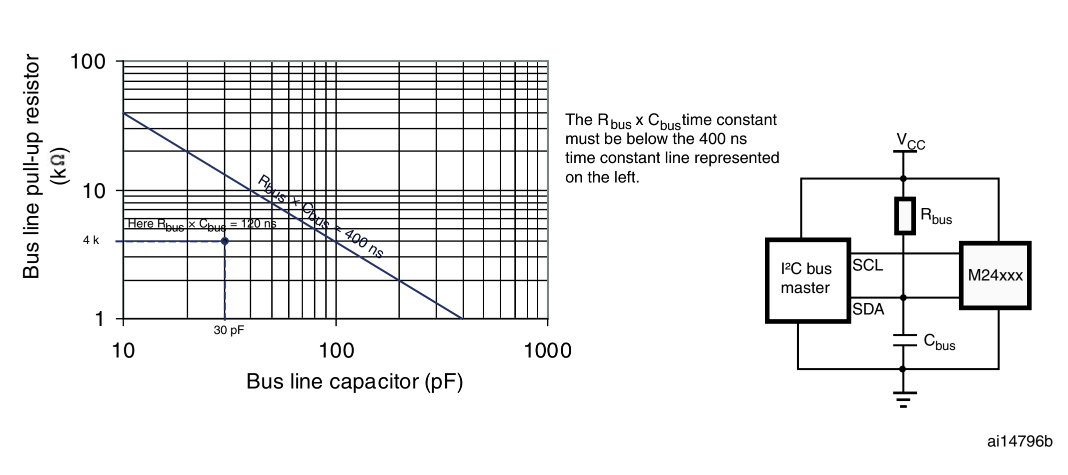


Figure 12. Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I^2C bus at maximum frequency f_C = 1MHz

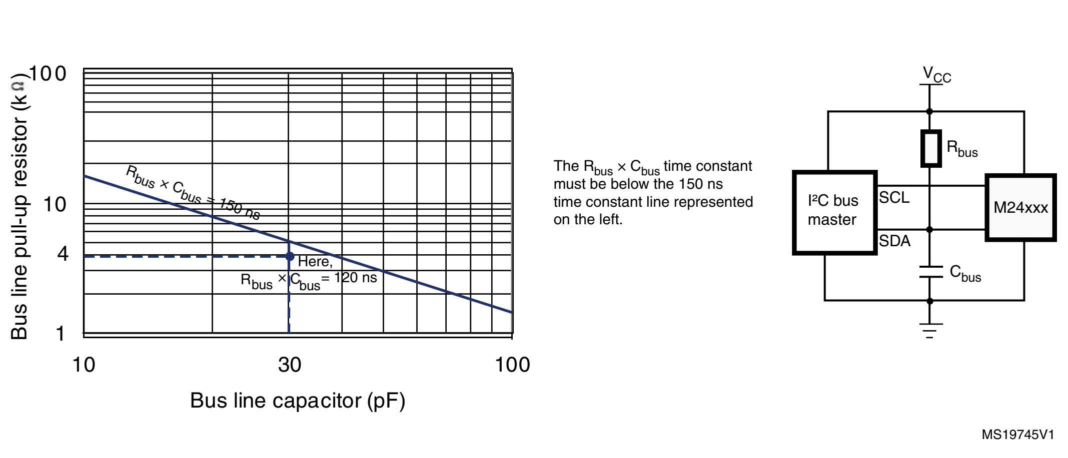
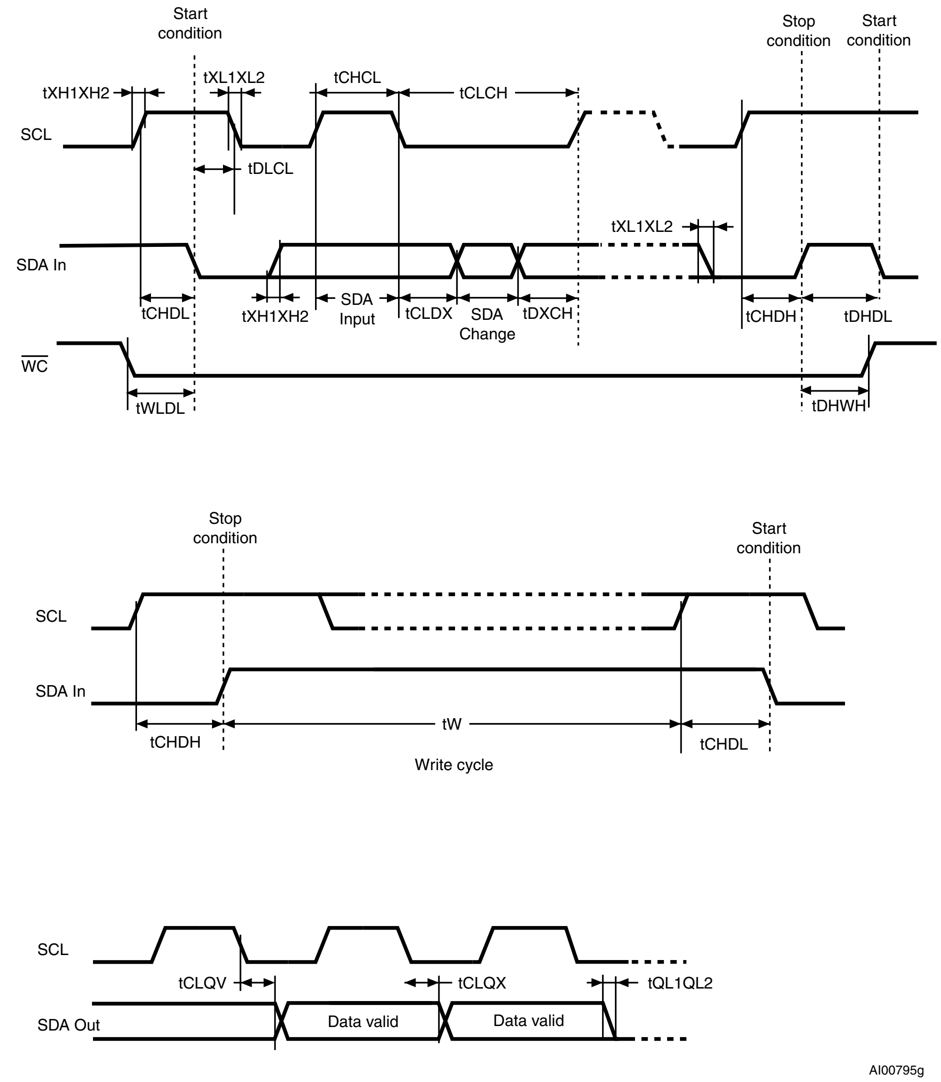


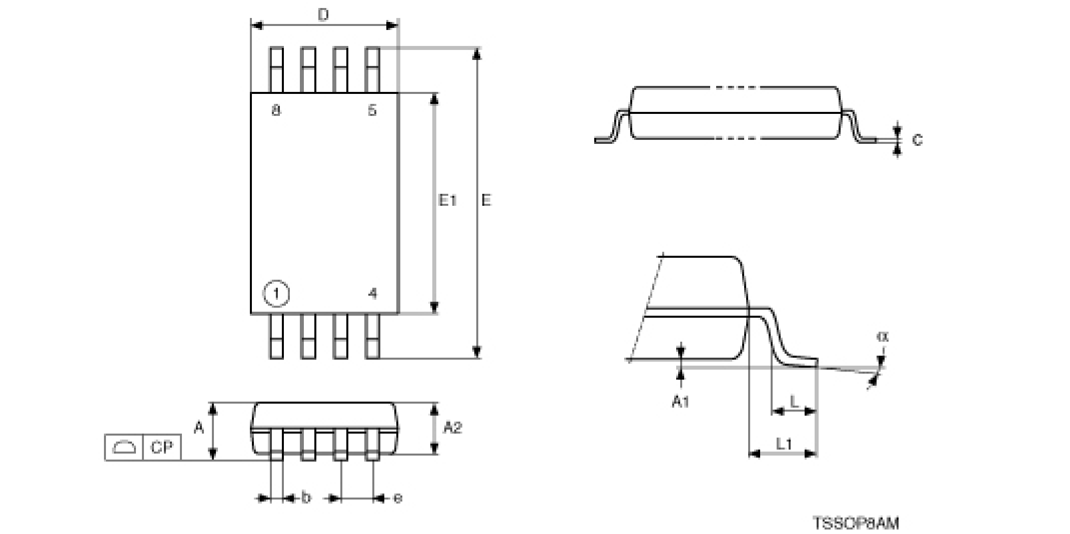
Figure 13. AC waveforms



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. TSSOP8 – 8-lead thin shrink small outline, package outline



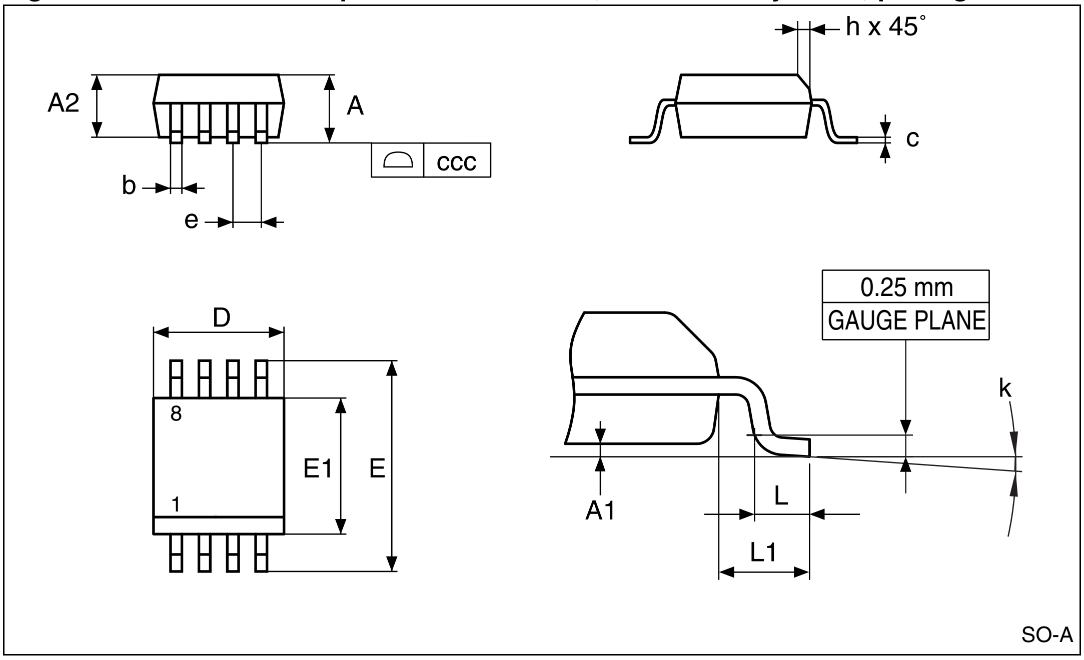
1. Drawing is not to scale.

Table 18. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 15. SO8N – 8 lead plastic small outline, 150 mils body width, package outline



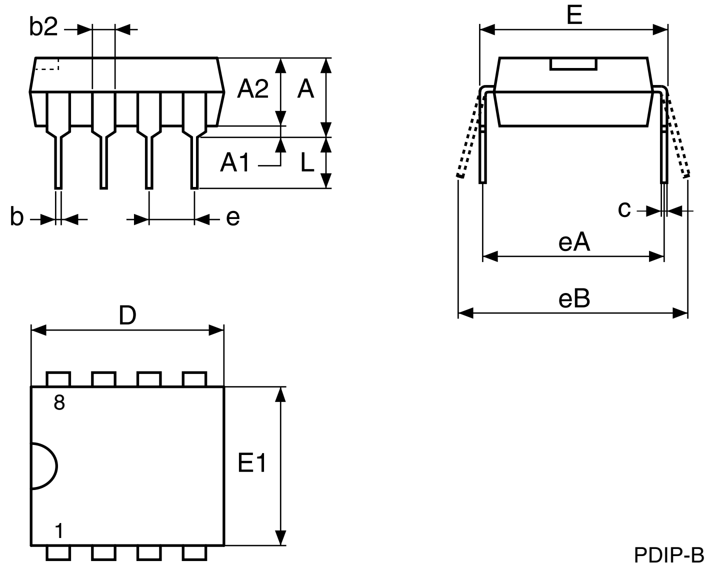
1. Drawing is not to scale.

Table 19. SO8N – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270			0.0500		
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 16. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package outline



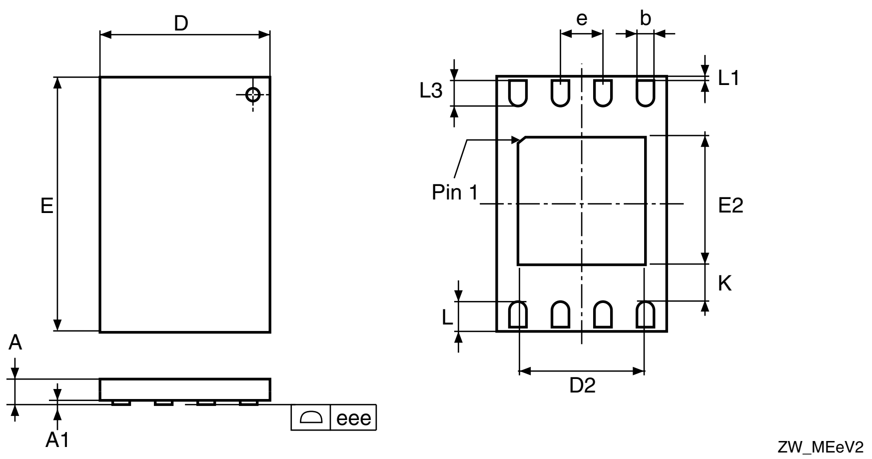
1. Drawing is not to scale.

Table 20. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.2098
A1		0.38			0.0150	
A2	3.30	2.92	4.95	0.1299	0.1150	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.0220
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.20	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.3650	0.3551	0.4000
E	7.87	7.62	8.26	0.3098	0.3000	0.3252
E1	6.35	6.10	7.11	0.2500	0.2402	0.2799
e	2.54	–	–	0.1000	–	–
eA	7.62	–	–	0.3000	–	–
eB			10.92			0.4299
L	3.30	2.92	3.81	0.1299	0.1150	0.1500

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 17. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 21. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

10 Part numbering

Table 22. Ordering information scheme

Example: M24C32-D W MN 6 T P /P

Device type

M24 = I²C serial access EEPROM

Device function

C32 = 32 Kbit (4096 x 8)

Device family

Blank: Without Identification page
-D: With additional Identification page

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V
R = V_{CC} = 1.8 V to 5.5 V
F = V_{CC} = 1.7 V to 5.5 V

Package

BN = PDIP8[(1)]
MN = SO8 (150 mil width)[(2)]
DW = TSSOP8 (169 mil width)[(2)]
MC = UFDFPN8 (MLP8)

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

Option

blank = standard packing
T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process

/P or /K[(3)] = Manufacturing technology code

1. RoHS-compliant (ECOPACK1®)
2. RoHS-compliant and halogen-free (ECOPACK2®)
3. The process letter is not used when ordering the device, but this letter appears on the packing.

For a list of available options (speed, package, etc.) or for further information on any aspect of the devices, please contact your nearest ST sales office.

11 Revision history

Table 23. Document revision history

Date	Revision	Changes
22-Dec-1999	2.3	TSSOP8 package in place of TSSOP14 (pp 1, 2, OrderingInfo, PackageMechData).
28-Jun-2000	2.4	TSSOP8 package data corrected
31-Oct-2000	2.5	References to Temperature Range 3 removed from Ordering Information Voltage range -S added, and range -R removed from text and tables throughout.
20-Apr-2001	2.6	Lead Soldering Temperature in the Absolute Maximum Ratings table amended Write Cycle Polling Flow Chart using ACK illustration updated References to PSDIP changed to PDIP and Package Mechanical data updated
16-Jan-2002	2.7	Test condition for I_{LI} made more precise, and value of I_{LI} for E2-E0 and $\overline{WC}$ added -R voltage range added
02-Aug-2002	2.8	Document reformatted using new template. TSSOP8 (3x3mm² body size) package (MSOP8) added. 5ms write time offered for 5V and 2.5V devices
04-Feb-2003	2.9	SO8W package removed. -S voltage range removed
27-May-2003	2.10	TSSOP8 (3x3mm² body size) package (MSOP8) removed
22-Oct-2003	3.0	Table of contents, and Pb-free options added. Minor wording changes in Summary Description, Power-On Reset, Memory Addressing, Write Operations, Read Operations. V_{IL}(min) improved to -0.45V.
01-Jun-2004	4.0	Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade clarified
04-Nov-2004	5.0	Product List summary table added. Device Grade 3 added. 4.5-5.5V range is Not for New Design. Some minor wording changes. AEC-Q100-002 compliance. t_{NS}(max) changed. V_{IL}(min) is the same on all input pins of the device. Z_{WCL} changed.
05-Jan-2005	6.0	UFDFPN8 package added. Small text changes.

Table 23. Document revision history (continued)

Date	Revision	Changes
29-Jun-2006	7	Document converted to new ST template. M24C32 and M24C64 products (4.5 to 5.5V supply voltage) removed. M24C64 and M24C32 products (1.7 to 5.5V supply voltage) added. *Section 2.3: Chip Enable (E2, E1, E0)* and *Section 2.4: Write Control (WC)* modified, *Section 2.6: Supply voltage (V_{CC})* added and replaces *Power On Reset: VCC Lock-Out Write Protect* section. T_A added, *Note 1* updated and T_{LEAD} specified for PDIP packages in *Table 6: Absolute maximum ratings*. I_{CC0} added, I_{CC} voltage conditions changed and I_{CC1} specified over the whole voltage range in *Table 13: DC characteristics (M24xxx-W, device grade 6)*. I_{CC0} added, I_{CC} frequency conditions changed and I_{CC1} specified over the whole voltage range in *Table 15: DC characteristics (M24xxx-R - device grade 6)*. t_W modified in *Table 16: AC characteristics*. SO8N package specifications updated (see *Figure 15* and *Table 20*). Device grade 5 added, B and P Process letters added to *Table 23: Ordering information scheme*. Small text changes.
03-Jul-2006	8	I_{CC1} modified in *Table 13: DC characteristics (M24xxx-W, device grade 6)*. *Note 1* added to *Table 16: DC characteristics (M24xxx-F)* and table title modified.
17-Oct-2006	9	UFDFPN8 package specifications updated (see *Table 21*). M24128-BW- and M24128-BR part numbers added. Generic part number corrected in *Features on page 1*. I_{CC0} corrected in *Table 13* and *Table 14*. Packages are ECOPACK® compliant.
27-Apr-2007	10	Available packages and temperature ranges by product specified in *Table 22*, *Table 24* and *Table 25*. Notes modified below *Table 11: Input parameters*. V_{IH} max modified in DC characteristics tables (see *Table 14*, *Table 15*, *Table 15* and *Table 16*). C process code added to *Table 23: Ordering information scheme*. For M24xxx-R (1.8 V to 5.5 V range) products assembled from July 2007 on, t_W will be 5 ms (see *Table 16: AC characteristics*.
27-Nov-2007	11	Small text changes. *Section 2.5: V_{SS} ground* and *Section 4.11: ECC (Error Correction Code) and Write cycling* added. V_{IL} and V_{IH} modified in *Table 15: DC characteristics (M24xxx-R - device grade 6)*. JEDEC standard reference updated below *Table 6: Absolute maximum ratings*. Package mechanical data inch values calculated from mm and rounded to 4 decimal digits (see *Section 8: Package mechanical data*).

Table 23. Document revision history (continued)

Date	Revision	Changes
18-Dec-2007	12	Added *Section 2.6.2: Power-up conditions*, updated *Section 2.6.3: Device reset*, and *Section 2.6.4: Power-down conditions* in *Section 2.6: Supply voltage (V_{CC})*. Updated *Figure 4: I²C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})*. Replace M24128 and M24C64 by M24128-BFMB6 and M24C64-FMB6, respectively, in *Section 4.11: ECC (Error Correction Code) and Write cycling*. Added temperature grade 6 in *Table 9: Operating conditions (M24xxx-F)*. Updated test conditions for I_{LO} and V_{LO} in *Table 13: DC characteristics (M24xxx-W, device grade 6)*, *Table 14: DC characteristics (M24xxx-W - device grade 3)*, and *Table 15: DC characteristics (M24xxx-R - device grade 6)*. Test condition updated for I_{LO}, and V_{IH} and V_{IL} differentiate for 1.8 V ≤ V_{CC} < 2.5 V and 2.5 V ≤V_{CC} < 5.5 V in *Table 16: DC characteristics (M24xxx-F)*. Updated *Table 16: AC characteristics*, and *Table 17: AC characteristics (M24xxx-F)*. Updated *Figure 13: AC waveforms*. Added M24128-BF in *Table 25: Available M24C32 products (package, voltage range, temperature grade)*. Process B removed from *Table 23: Ordering information scheme*.
30-May-2008	13	Small text changes. C *Process* option and Blank *Plating technology* option removed from *Table 23: Ordering information scheme*.
15-Jul-2008	14	WLCSP package added (see *Figure 3: WLCSP connections (top view, marking side, with balls on the underside)* and *Section 8: Package mechanical data*). *Section 4.11: ECC (Error Correction Code) and Write cycling* updated.
16-Sep-2008	15	I_{OL} added to *Table 6: Absolute maximum ratings*. *Table 24: Available M24C32 products (package, voltage range, temperature grade)* and *Table 25: Available M24C32 products (package, voltage range, temperature grade)* updated.
05-Jan-2009	16	I2C modes supported specified in *Features on page 1*. Note removed from *Table 16: DC characteristics (M24xxx-F)*. Small text changes.

Table 23. Document revision history (continued)

Date	Revision	Changes
30-Nov-2009	17	64 and 128 Kbit densities removed. *Section 2.6.2: Power-up conditions* updated. *Figure 4: I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* updated. I_{CC1} and V_{IH} updated in *Table 13: DC characteristics (M24xxx-W, device grade 6)*, *Table 14: DC characteristics (M24xxx-W - device grade 3)*, *Table 15: DC characteristics (M24xxx-R - device grade 6)* and *Table 16: DC characteristics (M24xxx-F)*. *Table 16: AC characteristics* modified. *Figure 13: AC waveforms* modified. Note added below *Figure 17: UFDFPN8 (MLP8) – 8-lead ultra thin fine pitch dual flat package no lead 2 × 3mm, package outline*. Small text changes.
18-Mar-2011	18	Added: – M24C32-DF and all information concerning the Identification Page: sections *4.9*, *4.10*, *4.17*, *4.18* – ECC section *4.11* – AC table with clock frequency of 1 MHz (*Table 18*) – *Table 4: Device select code* Updated: – *Section 1: Description* – *Section 4.5: Memory addressing* – *Section 4.18: Read the lock status (M24C32-D)* – *Table 6: Absolute maximum ratings* – AC/DC tables *13*, *17* with values specific to the device identified with process letter K Deleted: – *Table 2: Device select code* – *Table 23: Available M24C32 products (package, voltage range, temperature grade)*
14-Sep-2011	19	Updated: – *Figure 4: I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* – *Figure 5: I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* Added t_{WLDL} and t_{DHWH} in: – *Table 17: 400 kHz AC characteristics* – *Table 18: 1 MHz AC characteristics* – *Figure 13: AC waveforms* Minor text changes.
21-May-2012	20	Datasheet split into: – M24C32-DF, M24C32-W, M24C32-R,M24C32-F (this datasheet) for standard products (range 6), – M24C32-125 datasheet for automotive products (range 3).