# M41T256Y

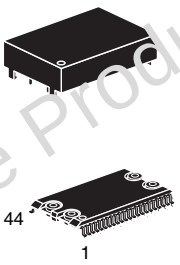
## 256Kbit (32K x 8) serial RTC

**Not For New Design**

## Features

- 5V operating voltage
- Serial interface supports extended $I^2C$ bus addressing (400kHz)
- Automatic switchover and deselect circuitry
- Power-fail deselect voltages:
  - M41T256Y: $V_{CC}$ = 4.5 V to 5.5V; $V_{PFD}$ = 4.2V < $V_{PFD}$ < 4.5V
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year
- Programmable software clock calibration
- 32,752 bytes of general purpose RAM
- Microprocessor power-on reset
- Holds microprocessor in reset until supply voltage reaches stable operating level
- Automatic address-incrementing
- Tamper indication circuit with time-stamp
- Sleep mode function
- Available in ST's 44-lead SNAPHAT® SOIC - mates with ST's removable/replaceable SNAPHAT® battery/crystal top (ordered separately)
- RoHS compliant
  - Lead-free second level interconnect

SNAPHAT (SH)
crystal/battery




SOH44 (MH)

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# 1 Summary

The M41T256Y Serial TIMEKEEPER® SRAM is a low power 256Kbit static CMOS SRAM organized as 32K words by 8 bits. A built-in 32.768kHz oscillator (external crystal controlled) and 8 bytes of the SRAM (see *Table 3 on page 18*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format.

Addresses and data are transferred serially via a two line, bi-directional $I^2C$ interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

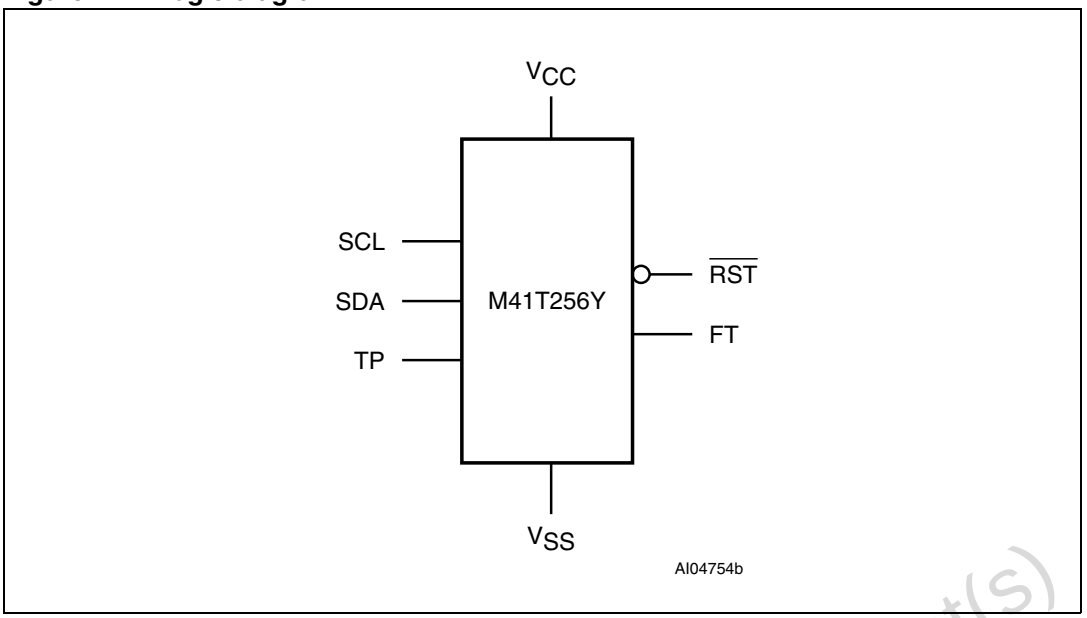
The M41T256Y has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a lithium button-cell supply when a power failure occurs. Functions available to the user include a non-volatile, time-of-day clock/calendar, and power-on reset. The eight clock address locations contain the year, month, date, day, hour, minute, second, and tenths/hundredths of seconds in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically. The first clock address location (7FF8h) stores the clock software calibration settings as well as the write clock bit.

The M41T256Y is supplied in a 44-lead SOIC SNAPHAT® package (MH - which integrates both crystal and battery in a single SNAPHAT top). The 44-pin, 330mil SOIC provides sockets with gold-plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface-mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion. The 44-pin SOIC and crystal/battery packages are shipped separately in plastic, anti-static tubes or in Tape & Reel form. For the 44-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4Txx-BR12SH” (see *Table 14 on page 28*).

**Caution:** Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium, button-cell battery.

**Figure 1. Logic diagram**




1. For 44-pin SNAPHAT (MT) package only.

**Table 1. Signal names**

| | |
|---|---|
| FT | Frequency test (open drain) |
| $\overline{RST}$ | Reset output (open drain) |
| SCL | Serial clock input |
| SDA | Serial data input/output |
| $V_{CC}$ | Supply voltage |
| $V_{SS}$ | Ground |
| TP | Tamper input |

**Figure 2. 44-pin SOIC (MH - snaphat)**

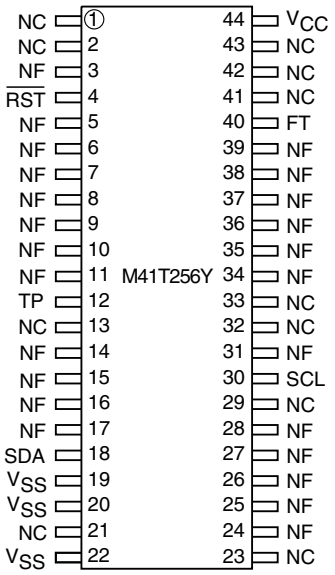
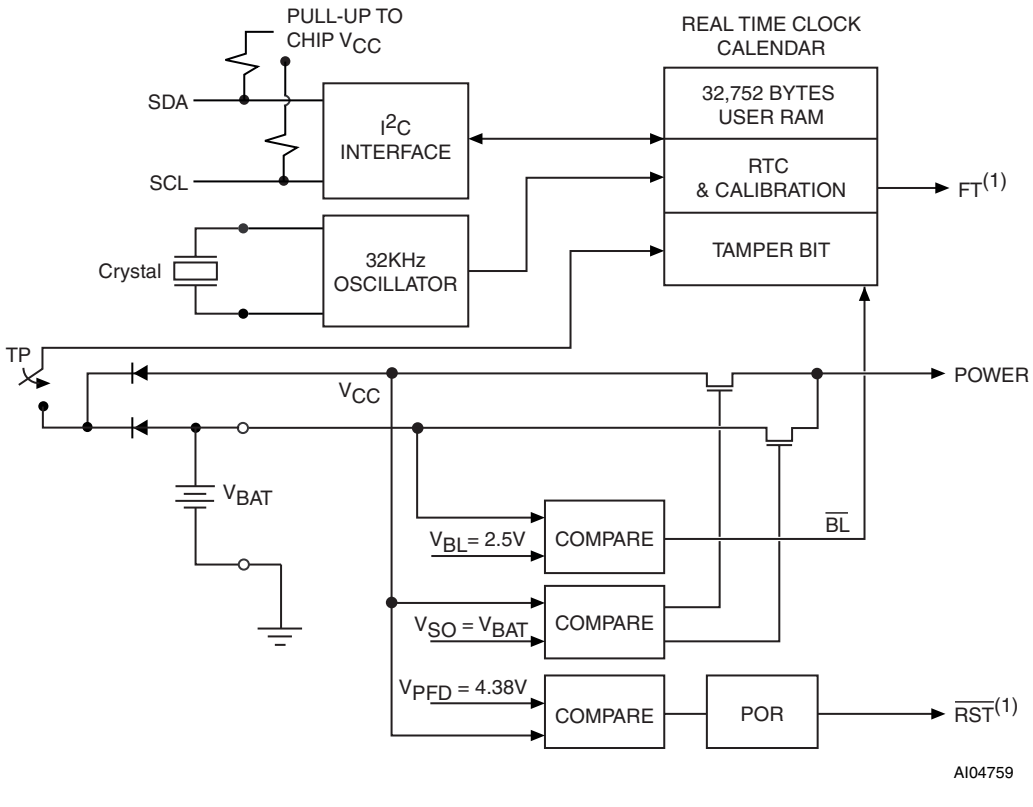



**Figure 3. Block diagram**




1. Open drain output

# 2 Operating modes

The M41T256Y clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 256K bytes contained in the device can then be accessed sequentially in the following order:

0-7FEF = General purpose RAM

7FF0-7FF6 = Reserved

7FF7h = Tenths/hundredths register

7FF8h = Control register

7FF9h = Seconds register

7FFAh = Minutes register

7FFBh = Hour register

7FFCh = Tamper/day register

7FFDh = Date register

7FFEh = Month register

7FFFh = Year register

The M41T256Y clock continually monitors $V_{CC}$ for an out-of tolerance condition. Should $V_{CC}$ fall below $V_{PFD}$, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system. When $V_{CC}$ falls below $V_{SO}$, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and $V_{CC}$ rises above $V_{SO}$, the battery is disconnected, and the power supply is switched to external $V_{CC}$. Write protection continues until $V_{CC}$ reaches $V_{PFD}$ plus $t_{REC}$.

For more information on Battery Storage Life refer to Application Note AN1012.

## 2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

### 2.1.1 Bus not busy

Both data and clock lines remain High.

### 2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

### 2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

### 2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

### 2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge clock pulse. This acknowledge clock pulse is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable Low during the High period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line High to enable the master to generate the STOP condition.

**Figure 4. Serial bus data transfer sequence**

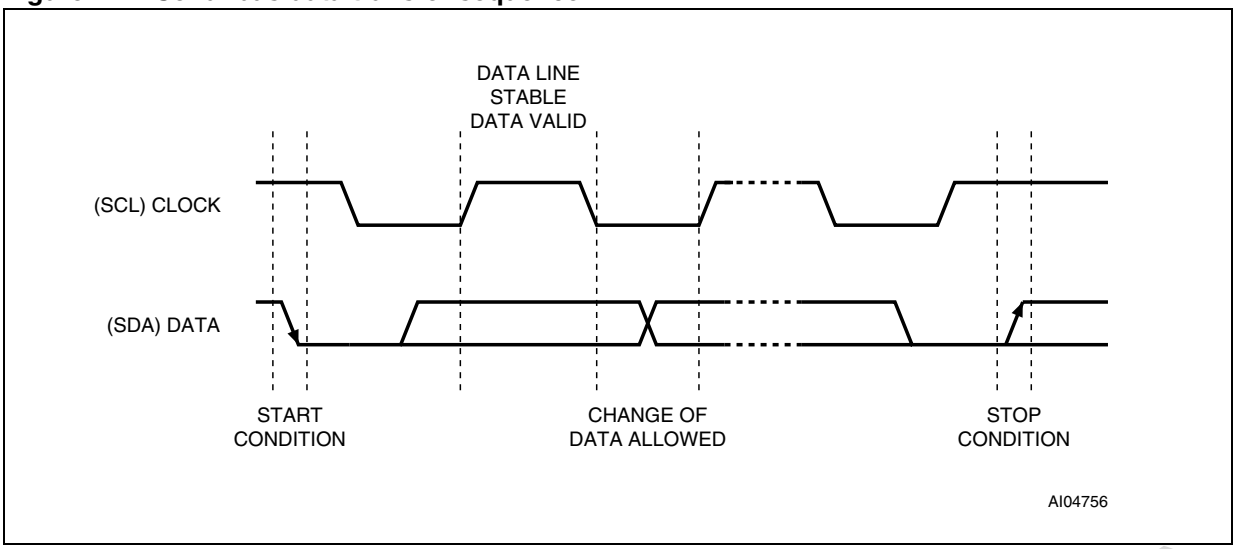



**Figure 5. Acknowledgement sequence**

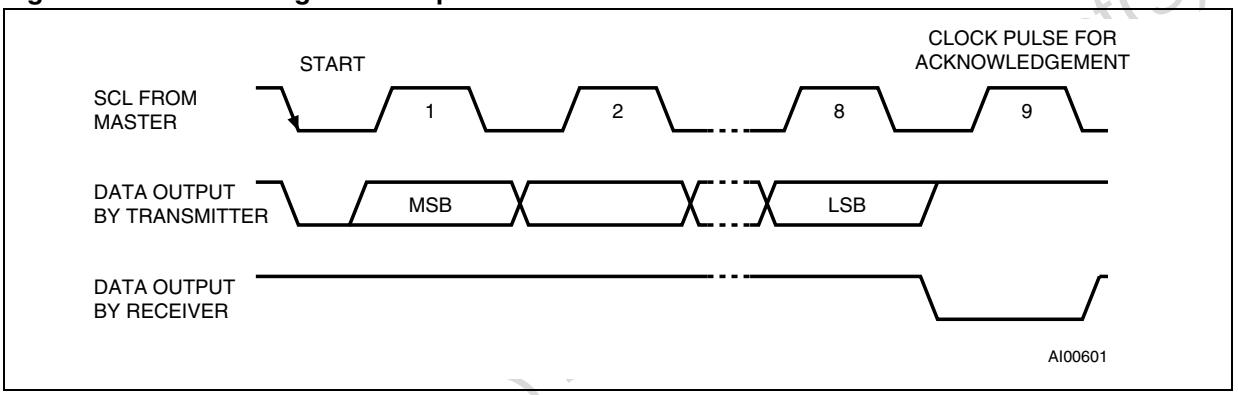


**Figure 6. Bus timing requirements sequence**

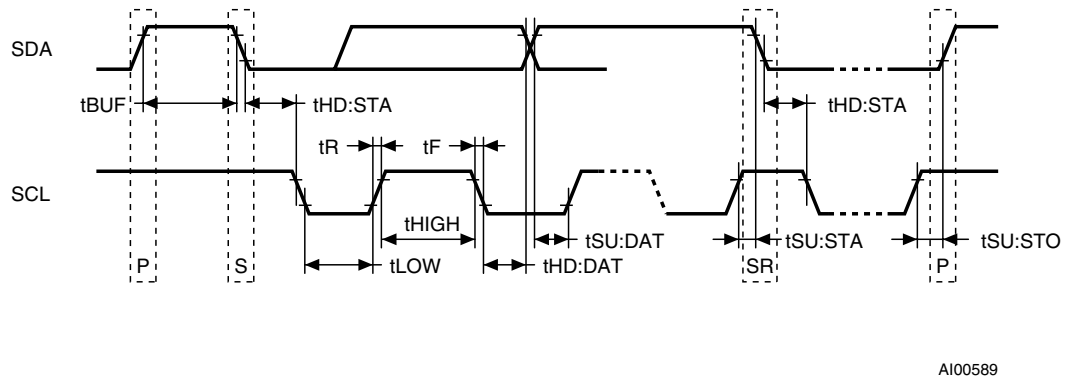



**Table 2. AC characteristics**

| Symbol | Parameter[1] | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | 400 | kHz |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start | 1.3 | | µs |
| $t_F$ | SDA and SCL fall time | | 300 | ns |
| $t_{HD:DAT}$ | Data hold time | 0 | | µs |
| $t_{HD:STA}$ | START condition hold time (after this period the first clock pulse is generated) | 600 | | ns |
| $t_{HIGH}$ | Clock high period | 600 | | ns |
| $t_{LOW}$ | Clock low period | 1.3 | | µs |
| $t_R$ | SDA and SCL rise time | | 300 | ns |
| $t_{SU:DAT}$[2] | Data setup time | 100 | | ns |
| $t_{SU:STA}$ | START condition setup time (only relevant for a repeated start condition) | 600 | | ns |
| $t_{SU:STO}$ | STOP condition setup time | 600 | | ns |

1. Valid for ambient operating temperature: $T_A$ = –25 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300ns max) of the falling edge of SCL

## 2.2 Read mode

In this mode the master reads the M41T256Y slave after setting the slave address (see *Figure 7 on page 13*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the Acknowledge Bit, the byte addresses A(0) and A(1) are written to the on-chip address pointer (MSB of address byte A(0) is a “Don’t care”). Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T256Y slave transmitter will now place the data byte at address An+1 on the bus, the

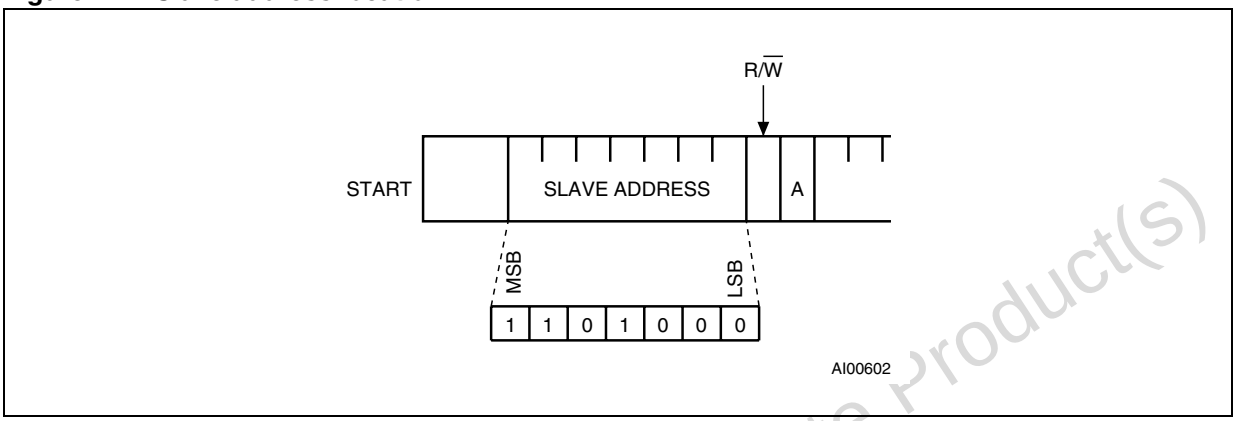
master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter (see *Figure 8 on page 14*).

*Note: Address pointer will wrap around from maximum address to minimum address if consecutive READ or WRITE cycles are performed.*

An alternate READ mode may also be implemented whereby the master reads the M41T256Y slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 9 on page 14*).

**Figure 7. Slave address location**




*Note: The most significant bit is sent first.*

**Figure 8. Read mode sequence**

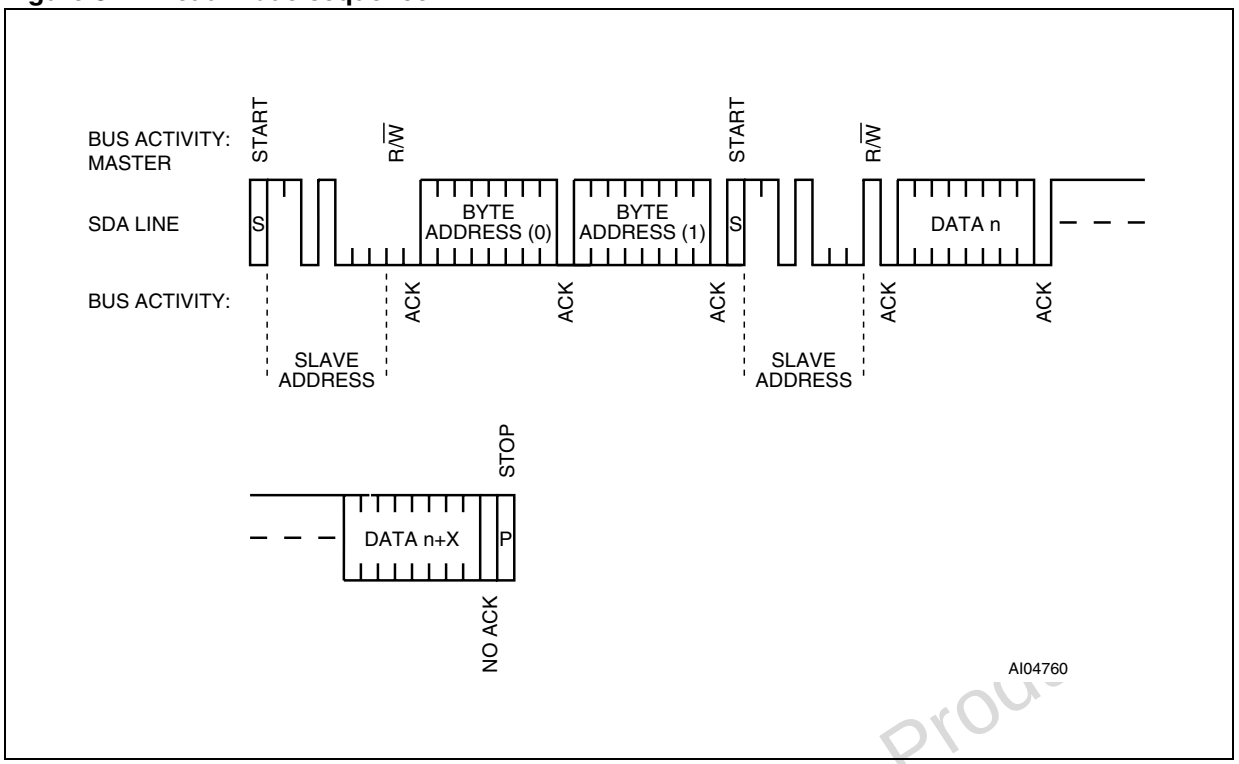
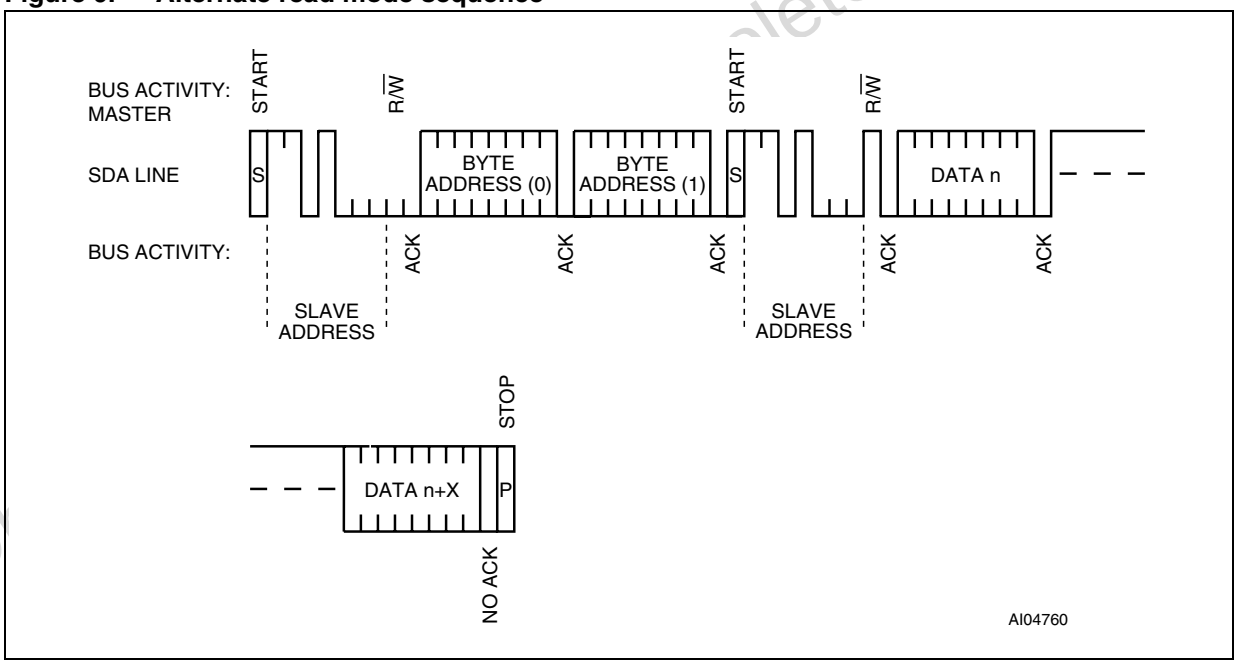



**Figure 9. Alternate read mode sequence**

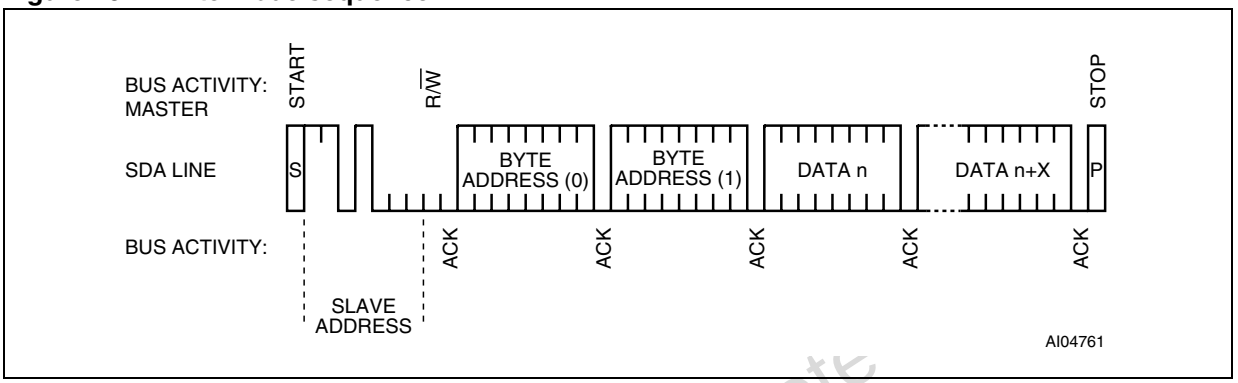


## 2.3 Write mode

In this mode the master transmitter transmits to the M41T256Y slave receiver. Bus protocol is shown in *Figure 10 on page 15*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that byte addresses A(0) and A(1) will follow and is to be written to the on-chip address pointer (MSB of address byte A(0) is a “Don’t care”).

The data byte to be written to the memory is strobed in next and the internal address pointer is incremented to the next memory location within the RAM on the reception of an acknowledge bit. The M41T256Y slave receiver will send an acknowledge bit to the master transmitter after it has received the slave address (see *Figure 7 on page 13*) and again after it has received each address byte.

**Figure 10. Write mode sequence**




## 2.4 Data retention mode

With valid $V_{CC}$ applied, the M41T256Y can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T256Y will automatically deselect, write protecting itself when $V_{CC}$ falls between $V_{PFD}$ (max) and $V_{PFD}$ (min). This is accomplished by internally inhibiting access to the clock registers. At this time, the reset pin ($\overline{RST}$) is driven active and will remain active until $V_{CC}$ returns to nominal levels. When $V_{CC}$ falls below the battery back-up switchover voltage ($V_{SO}$), power input is switched from the $V_{CC}$ pin to the external battery and the clock registers and SRAM are maintained from the attached battery supply.

All outputs become high impedance. On power up, when $V_{CC}$ returns to a nominal value, write protection continues for $t_{REC}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 14 on page 25*).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

## 2.5 Sleep mode

In order to minimize the battery current draw while in storage, the M41T256Y provides the user with a battery “sleep mode,” which disconnects the RAM memory array from the external Lithium battery normally used to provide non-volatile operation in the absence of $V_{CC}$. This can significantly extend the lifetime of the battery, when non-volatile operation is not needed.

*Note: The sleep mode will remove power from the RAM array only and not affect the data retention of the TIMEKEEPER Registers (7FF0h through 7FFFh - this includes the Calibration Register).*

The sleep mode (SLP) Bit located in register 7FF8h (D6), must be set to a '1' by the user while the device is powered by $V_{CC}$. This will “arm” the sleep mode latch, but not actually disconnect the RAM array from power until the next power-down cycle. This protects the user from immediate data loss in the event he inadvertently sets the SLP Bit. Once $V_{CC}$ falls below $V_{SO}$ ($V_{BAT}$), the sleep mode circuit will be engaged and the RAM array will be isolated from the battery, resulting in both a lower battery current, and a loss of RAM data.

*Note: Upon initial battery attach or initial power application without the battery, the state of the SLP Bit will be undetermined. Therefore, the SLP Bit should be initialized to '0' by the user.*

Additional current reduction can be achieved by setting the STOP (ST) Bit in register 7FF9h (D7), turning off the clock oscillator. This combination will result in the longest possible battery life, but also loss of time and data. When the device is again powered-up, the user should first read the SLP Bit to determine if the device is currently in sleep mode, then reset the bit to '0' in order to disable the sleep mode (this will NOT be automatically taken care of during the power-up).

*Note: See AN1570, “M41T256Y Sleep Mode Function” for more information on sleep mode and battery lifetimes.*

# 3 Clock operation

Year, month, and date are contained in the last three registers of the TIMEKEEPER® register map (see *Table 3 on page 18*). Bits D0 through D2 of the next register contain the day (day of week). Finally, there are the registers containing the seconds, minutes, and hours, respectively. The first clock register is the control register (this is described in the clock calibration section).

The nine clock registers may be read one byte at a time, or in a sequential block. The control register (Address location 7FF8h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the nine clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the read.

## 3.1 Reading the clock

The nine byte clock register (see *Table 3 on page 18*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (7FF9h to 7FFFh). The update will resume either due to a stop condition or when the pointer increments to a RAM address.

This prevents reading data in transition. The TIMEKEEPER® cells in the register map are only data registers and not actual clock counters, so updating the registers can be halted without disturbing the clock itself.

## 3.2 Setting the clock

Bit D7 of the control register (7FF8h) is the write clock bit. Setting the write clock bit to a '1' will allow the user to write the desired day, date, and time data in 24-hour BCD format. Resetting the write clock bit to a '0' then transfers the values of all time registers (7FF8h-7FFFh) to the actual clock counters and resets the internal divider (or clock) chain.

*Note: The tenths/hundredths of seconds register will automatically be reset to zero when the WRITE clock bit is set.*

Other register bits such as FT, TEB, and ST may be written without setting the WC Bit. In such cases, the clock data will be undisturbed and will retain their previous values.

## 3.3 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The stop bit (ST) is the most significant bit of the seconds register. Setting it to '1' stops the oscillator. Setting it to '0' restarts the oscillator in approximately one second.

Table 3. TIMEKEEPER® register map

| Address | Data | | | | | | | | Function/Range BCD Format | |
|---|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| 7FFFh | 10 years | | | | Year | | | | Year | 00-99 |
| 7FFEh | 0 | 0 | 0 | 10M | Month | | | | Month | 01-12 |
| 7FFDh | 0 | 0 | 10 date | | Date: Day of Month | | | | Date | 01-31 |
| 7FFCh | BL | FT | TEB | TB | 0 | Day of Week | | | Tamper/day | 0-1/01-07 |
| 7FFBh | 0 | 0 | 10 hours | | Hours (24 Hour Format) | | | | Hours | 00-23 |
| 7FFAh | 0 | 10 minutes | | | Minutes | | | | Minutes | 00-59 |
| 7FF9h | ST | 10 seconds | | | Seconds | | | | Seconds | 00-59 |
| 7FF8h | WC | SLP | S | Calibration | | | | | Control | |
| 7FF7h | 0.1 Seconds | | | | 0.01 Seconds | | | | Seconds | 00-99 |
| 7FF6h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF5h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF4h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF3h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF2h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF1h | X | X | X | X | X | X | X | X | Reserved | |
| 7FF0h | X | X | X | X | X | X | X | X | Reserved | |

Keys:

S = Sign bit
FT = Frequency test bit
ST = Stop bit
WC = Write clock bit
X = '1' or '0'
BL = Battery low flag (read only bit)
TB = Tamper bit (read only bit)
TEB = Tamper enable bit
0 = Must be set to '0'
SLP = Sleep mode bit

*Note: 7FF0h through 7FF6h are invalid addresses and when read will return arbitrary data.*



## 3.4 Power-on reset

The M41T256Y continuously monitors $V_{CC}$. When $V_{CC}$ falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for $t_{REC}$ after $V_{CC}$ passes $V_{PFD}$ (max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

## 3.5 Tamper indication circuit

The M41T256Y provides an independent input pin, the tamper pin (TP) which can be used to monitor a signal which can result in the setting of the tamper bit (TB) if the tamper enable bit (TEB) is set to a '1.'

The tamper pin is triggered by being connected to $V_{CC}/V_{BAT}$ through an external switch. This switch is normally open in the application, allowing the pin to be “floating” (internally latched to $V_{SS}$ when TEB is set). When this switch is closed (connecting the pin to $V_{CC}/V_{BAT}$), the tamper bit will be immediately set. This allows the user to determine if the device has been physically moved or tampered with. The tamper bit is a “read only” bit and is reset only by taking the tamper pin to ground and resetting the tamper enable bit to '0.'

This function operates both under normal power, and in battery back-up. If the switch closes during a power-down condition, the bit will still be set correctly.

*Note: Upon initial battery attach or initial power application without the battery, the state of TEB (and TB) will be undetermined. Therefore TEB must be initialized to a '0.'*

## 3.6 Tamper event time-stamp

If a tamper occurs, not only will the tamper bit be set, but the event will also automatically be time-stamped. This is accomplished by freezing the normal update of the clock registers (7FF7h through 7FFFh) immediately following a tamper event. Thus, when tampering occurs, the user may first read the time registers to determine exactly when the tamper event occurred, then re-enable the clock update to the current time (and reset the Tamper Bit, TB) by resetting the tamper enable bit (TEB).

The time update will then resume, and after either a stop condition or incrementing the address pointer to a RAM address and back, the clock can be read to determine the current time.

*Note: The tamper bit (TB) must always be set to '0' in order to read the current time.*

## 3.7 Calibrating the clock

The M41T256Y is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. The devices are tested not exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. When the calibration circuit is properly employed, accuracy improves to better than +1/–2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 11 on page 20*). Therefore, the M41T256Y design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 12 on page 20*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register (7FF8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one

second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

**Figure 11. Crystal accuracy across temperature**

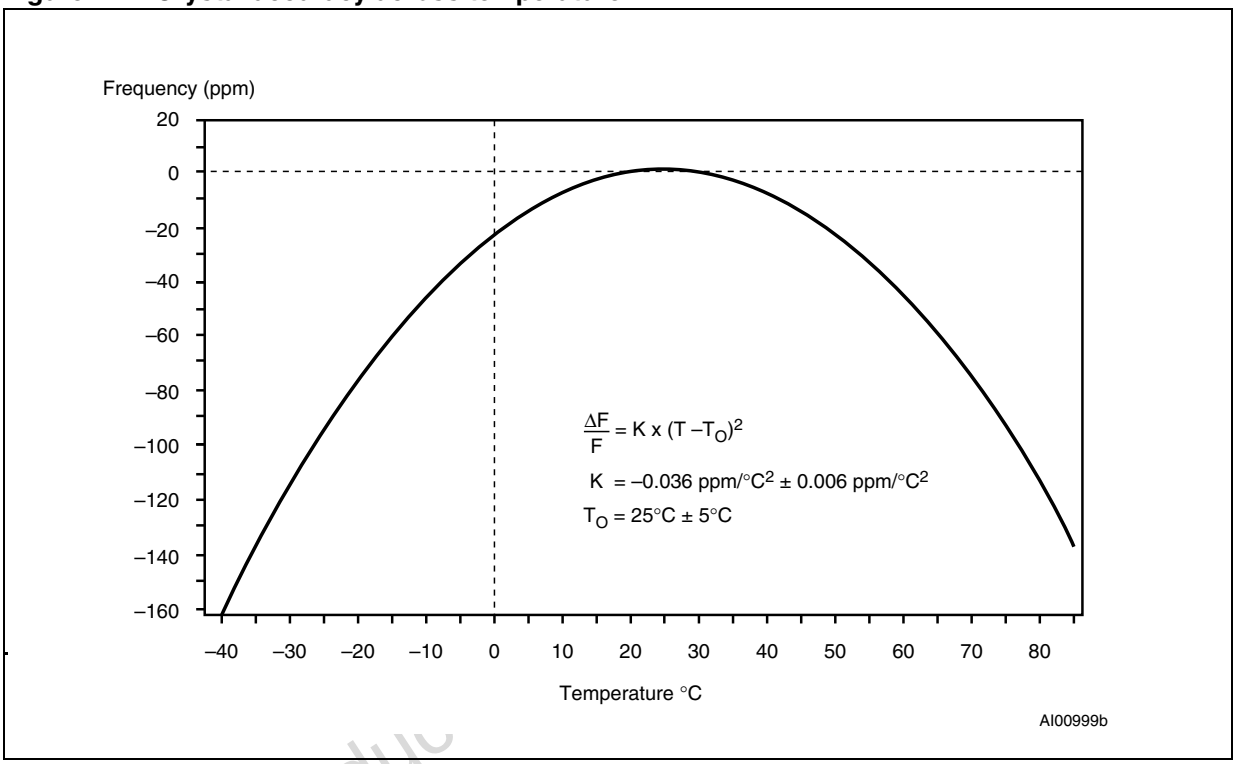
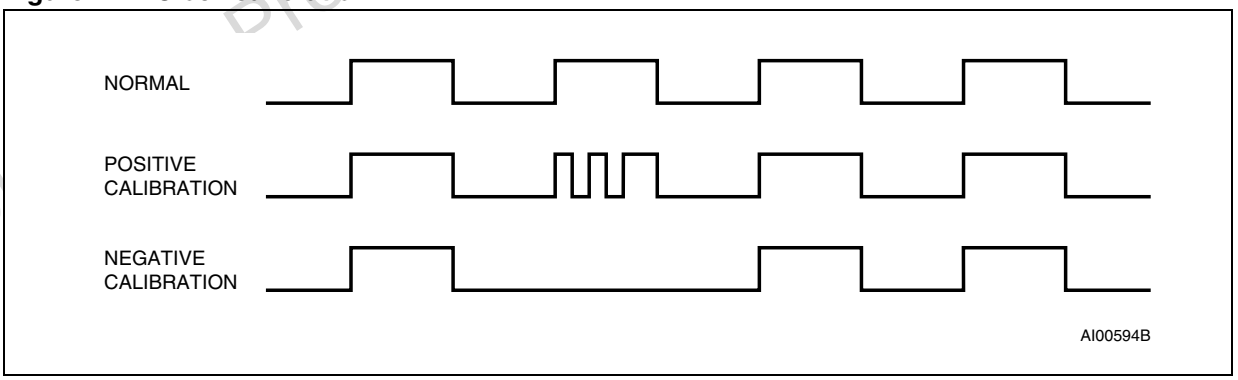



**Figure 12. Clock calibration**




Two methods are available for ascertaining how much calibration a given M41T256Y may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note AN934: TIMEKEEPER CALIBRATION. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the FT pin. The pin will toggle at 512Hz, when the stop bit (ST) is '0,' and the frequency test bit (FT) is '1.'

Any deviation from 512Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The FT pin is an open drain output which requires a pull-up resistor to $V_{CC}$ for proper operation. A 500 to 10k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

## 3.8 Battery low warning

The M41T256Y automatically performs battery voltage monitoring upon power-up. The battery low (BL) bit, bit D7 of day register, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, during the next power-up sequence.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed. The battery may be replaced while $V_{CC}$ is applied to the device.

The M41T256Y only monitors the battery when a nominal $V_{CC}$ is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

## 3.9 Preferred power-on/battery attach defaults

See *Table 4*, below.

**Table 4. Preferred default values**

| Condition | WC | TEB(1) | TB(1) | FT | ST(1) | SLP(1) |
|---|---|---|---|---|---|---|
| Battery attach or initial power-up | 0 | X | X | 0 | X | X |
| Power-cycling (with battery) | 0 | UC | UC | 0 | UC | UC |

1. X = Undetermined; UC = Unchanged

# 4 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 5. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $T_{STG}$ | Storage temperature ($V_{CC}$ off, oscillator off) | SNAPHAT® | –40 to 85 | °C |
| | | SOIC | –55 to 125 | °C |
| $T_{SLD}$(1) | Lead solder temperature for 10 seconds | | 260 | °C |
| $V_{IO}$ | Input or output voltages | | –0.3 to $V_{CC}$ + 0.3 | V |
| $V_{CC}$ | Supply voltage | | –0.3 to 7.0 | V |
| $I_O$ | Output current | | 20 | mA |
| $P_D$ | Power dissipation | | 1 | W |

1. For SO package, standard (SnPb) lead finish: Reflow at peak temperature of 225°C (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

   For SO package, Lead-free (Pb-free) lead finish: Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

**Caution:** *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

**Caution:** *Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.*

# 5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in *Table 6: DC and AC measurement conditions*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 6. DC and AC measurement conditions**

| Parameter | M41T256Y |
|---|---|
| $V_{CC}$ Supply voltage | 4.5 to 5.5V |
| Ambient operating temperature | –25 to 70°C |
| Load capacitance ($C_L$) | 100pF |
| Input rise and fall times | ≤ 50ns |
| Input pulse voltages | $0.2V_{CC}$ to $0.8V_{CC}$ |
| Input and output timing ref. voltages | $0.3V_{CC}$ to $0.7V_{CC}$ |

**Figure 13. AC testing input/output waveforms**

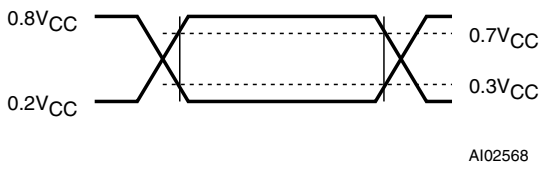



**Table 7. Capacitance**

| Symbol | Parameter(1) and (2) | Min | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | | 7 | pF |
| | Input capacitance (tamper pin) | | 1000 | pF |
| $C_{IO}$(3) | Input / output capacitance | | 10 | pF |
| $t_{LP}$ | Low-pass filter input time constant (SDA and SCL) | | 50 | ns |

1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected.

**Table 8. DC characteristics**

| Sym | Parameter | Test condition(1) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{BAT}$ | Battery current OSC ON | $T_A$ = 25°C, $V_{CC}$ = 0V, $V_{BAT}$ = 3.0V | | 1.5 | 1.9 | µA |
| | Battery current OSC OFF | | | 1.0 | 1.4 | µA |
| $I_{CC1}$ | Supply current | f = 400kHz | | 1.4 | 3.0 | mA |
| $I_{CC2}$ | Supply current (standby) | SCL, SDA = $V_{CC}$ – 0.3V | | 1.0 | 2.5 | mA |
| $I_{LI}$ | Input leakage current | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | | | ±1 | µA |
| $I_{LO}$(2) | Output leakage current | 0V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | | ±1 | µA |
| $V_{IH}$ | Input high voltage | | 0.7$V_{CC}$ | | $V_{CC}$ + 0.3 | V |
| $V_{IHB}$ | Input high voltage in battery back-up for tamper pin | | $V_{BAT}$ – $V_{diode}$ | | $V_{BAT}$ | V |
| $V_{IL}$ | Input low voltage | | –0.3 | | 0.3$V_{CC}$ | V |
| $V_{BAT}$ | Battery voltage | | 2.5 | | 3.5 | V |
| $V_{OH}$ | Output high voltage | | | | $V_{CC}$ + 0.3 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 3.0mA | | | 0.4 | V |
| | Output low voltage (open drain)(3) | $I_{OL}$ = 10mA | | | 0.4 | V |
| $V_{PFD}$ | Power fail deselect | | 4.20 | | 4.50 | V |
| $V_{SO}$ | Battery back-up switchover | | | $V_{BAT}$ | | V |
| $R_{SW}$ | Switch resistance on tamper pin | | | | 500 | W |

1. Valid for ambient operating temperature: $T_A$ = –25 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. Outputs deselected.
3. For $\overline{RST}$ and FT pin (open drain).

**Table 9. Crystal electrical characteristics (externally supplied)**

| Symbol | Parameter(1) | Typ | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_0$ | Resonant frequency | 32.768 | | | kHz |
| $R_S$ | Series resistance | | | 35 | kΩ |
| $C_L$ | Load capacitance | 12.5 | | | pF |

1. Load capacitors are integrated within the M41T256Y. Circuit board layout considerations for the 32.768kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.

**Figure 14. Power down/up mode AC waveforms**

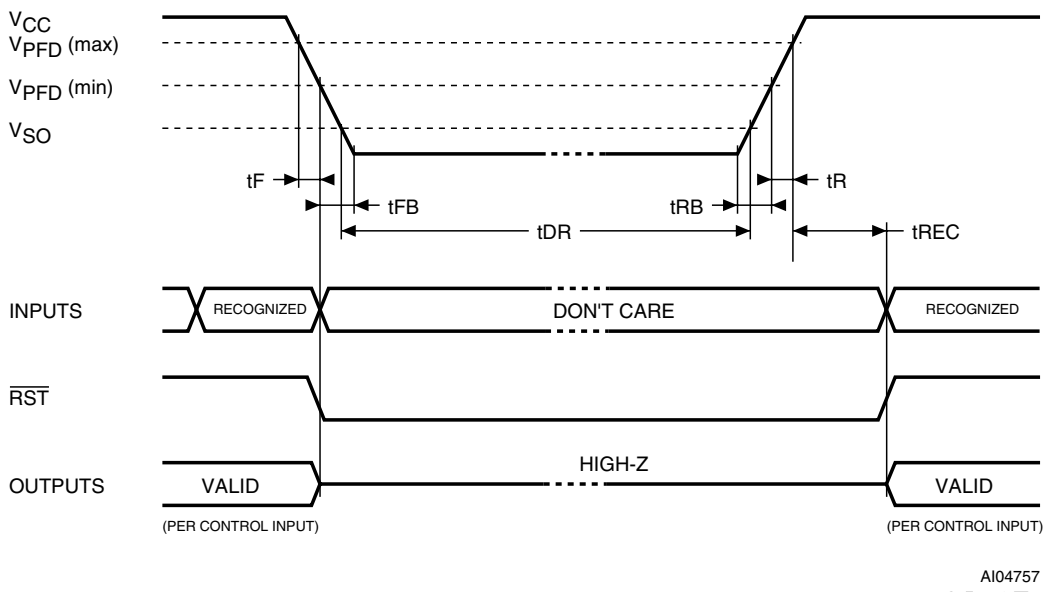



**Table 10. Power down/up AC characteristics**

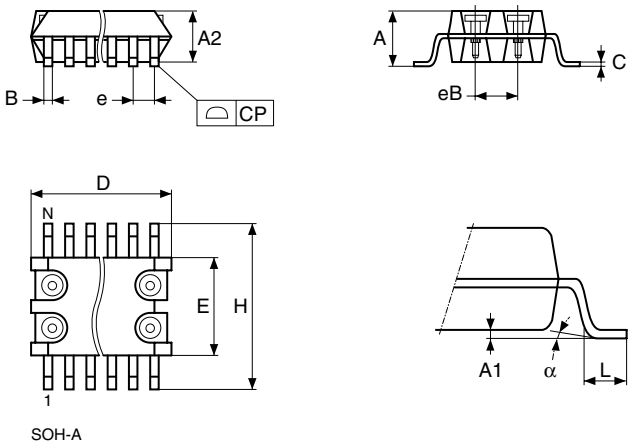
| Symbol | Parameter[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_F$[2] | $V_{PFD}$ (max) to $V_{PFD}$ (min) $V_{CC}$ fall time | 300 | | | µs |
| $t_{FB}$[3] | $V_{PFD}$ (min) to $V_{SS}$ $V_{CC}$ fall time | 10 | | | µs |
| $t_R$ | $V_{PFD}$ (min) to $V_{PFD}$ (max) $V_{CC}$ rise time | 10 | | | µs |
| $t_{RB}$ | $V_{SS}$ to $V_{PFD}$ (min) $V_{CC}$ rise time | 1 | | | µs |
| $t_{REC}$ | Power up deselect time | 40 | | 200 | ms |
| $t_{DR}$ | Expected data retention time (OSC on, sleep mode off) | 7.2[4] | | | years |

1. Valid for ambient operating temperature: $T_A$ = –25 to 70°C; $V_{CC}$ = 4.5 to 5.5V (except where noted).
2. $V_{PFD}$ (max) to $V_{PFD}$ (min) fall time of less than tF may result in deselection/write protection not occurring until 200µs after $V_{CC}$ passes $V_{PFD}$ (min).
3. $V_{PFD}$ (min) to $V_{SS}$ fall time of less than $t_{FB}$ may cause corruption of RAM data.
4. At 25°C and $V_{CC}$ = 0V with the oscillator running and using M4T32-BR12SH SNAPHAT battery top.

# 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 15. SOH44 – 44-lead plastic small outline, SNAPHAT, package outline**

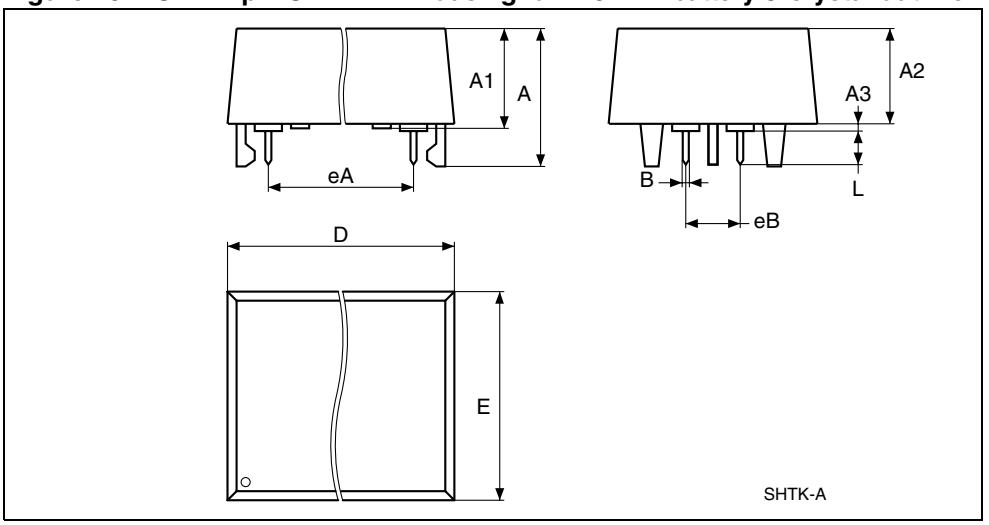



*Note: Drawing is not to scale.*

**Table 11. SOH44 – 44-lead plastic small outline, SNAPHAT, package mech. data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 3.05 | | | 0.120 |
| A1 | | 0.05 | 0.36 | | 0.002 | 0.014 |
| A2 | | 2.34 | 2.69 | | 0.092 | 0.106 |
| B | | 0.36 | 0.46 | | 0.014 | 0.018 |
| C | | 0.15 | 0.32 | | 0.006 | 0.012 |
| D | | 17.71 | 18.49 | | 0.697 | 0.728 |
| E | | 8.23 | 8.89 | | 0.324 | 0.350 |
| e | 0.81 | – | – | 0.032 | – | – |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| H | | 11.51 | 12.70 | | 0.453 | 0.500 |
| L | | 0.41 | 1.27 | | 0.016 | 0.050 |
| a | | 0° | 8° | | 0° | 8° |
| N | 44 | | | 44 | | |
| CP | | | 0.10 | | | 0.004 |

**Figure 16. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal outline**




*Note: Drawing is not to scale.*

**Table 12. SH – 4-pin SNAPHAT housing for 120mAh battery & crystal, mechanical data**

| Symb | mm | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 10.54 | | | 0.415 |
| A1 | | 8.00 | 8.51 | | 0.315 | .0335 |
| A2 | | 7.24 | 8.00 | | 0.285 | 0.315 |
| A3 | | | 0.38 | | | 0.015 |
| B | | 0.46 | 0.56 | | 0.018 | 0.022 |
| D | | 21.21 | 21.84 | | 0.835 | 0.860 |
| E | | 17.27 | 18.03 | | 0.680 | .0710 |
| eA | | 15.55 | 15.95 | | 0.612 | 0.628 |
| eB | | 3.20 | 3.61 | | 0.126 | 0.142 |
| L | | 2.03 | 2.29 | | 0.080 | 0.090 |

# 7 Part numbering

**Table 13. Ordering information scheme**

Example: M41T 256Y MT 7 E

**Device type**

M41T

**Supply voltage and write protect voltage**

256Y = $V_{CC}$ = 4.5 to 5.5V; $V_{PFD}$ = 4.2 to 4.5V

**Package**

MH(1) = SOH44

**Temperature range**

7 = –25 to 70°C

**Shipping method**

E = Lead-free package (ECOPACK®), tubes

F = Lead-free package (ECOPACK®), tape & reel

1. The SOIC package (SOH44) requires the SNAPHAT® battery package which is ordered separately under the part number “M4Txx-BR12SH” in plastic tubes (see *Table 14*).

**Caution:** Do not place the SNAPHAT battery package “M4TXX-BR12SH” in conductive foam as it will drain the lithium button-cell battery.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

**Table 14. SNAPHAT® battery table**

| Part Number | Description | Package |
|---|---|---|
| M4T32-BR12SH | Lithium battery (120mAh) SNAPHAT | SH |

# 8 Revision history

**Table 15. Document revision history**

| Date | Version | Revision Details |
|---|---|---|
| February 2002 | 1.0 | First Issue |
| 26-Apr-02 | 1.1 | Addition of “Tamper Event Time-Stamp” text |
| 31-May-02 | 1.2 | Add Sleep Mode, 44-pin with SNAPHAT package (Figure *2, 5, 19, 20*; Table *1, 5, 14, 15, 12, 13*). |
| 03-Jul-02 | 1.3 | Modify Crystal Electrical Characteristics table footnotes (Table *9*). |
| 12-Jul-02 | 1.4 | Added programmable Sleep Mode information to document (Figure *3*, *4*, *5*, *6*; Table *3*, *4*) |
| 29-Jul-02 | 1.5 | Add “Hatless” to package description (Figure *1*,*18*) and Table *14*, *11*) |
| 20-Dec-02 | 2.0 | $I_{CC}$ Characteristics changed (Table *8*); Document promoted to “Datasheet” |
| 04-Jan-03 | 2.1 | Add $V_{OL}$ value (Table *8*) |
| 26-Mar-03 | 2.2 | Update test condition (Table *10*) |
| 15-Jun-04 | 3.0 | Reformatted; add Lead-free information; update characteristics (Figure *14*; Table *5*, *14*) |
| 16-Apr-2007 | 4 | Reformatted document. Updated packaging references that only 44-lead SNAPHAT available (cover page, *Summary*, *Figure 1*, *Table 1*, *Table 13*). Updated *Table 9*, *10*. |
| 09-Nov-2007 | 5 | Added lead-free second level interconnect information to cover page and *Section 6: Package mechanical data*; product status “Not for New Design”; updated *Table 13*. |

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