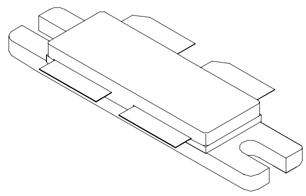
SD56120M

RF POWER Transistors, LDMOST plastic family
N-Channel enhancement-mode lateral MOSFETs

General features

- Excellent thermal stability
- Common source configuration Push-pull
- P_{OUT} = 120W with 13dB gain @ 860MHz / 32V
- BeO free package
- Internal input matching

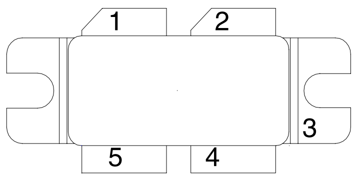


M252
Epoxy sealed

Description

The SD56120M is a common source N-Channel enhancement-mode lateral Field-Effect RF power transistor designed for broadband commercial and industrial applications at frequencies up to 1.0 GHz. The SD56120M is designed for high gain and broadband performance operating in common source mode at 32 V. Its internal matching makes it ideal for TV broadcast applications requiring high linearity.

Pin connection



1. Drain
2. Drain
3. Source
4. Gate
5. Gate

Order codes

Part number	Package	Branding
SD56120M	M252	SD56120M

Contents

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-Source Voltage	65	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current	14	A
P_{DISS}	Power Dissipation (@ Tc = 70°C)	236	W
Tj	Max. Operating Junction Temperature	200	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.55	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 3. Static (per section)

Symbol	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V I_{DS} = 10 mA	65			V
I_{DSS}	V_{GS} = 0 V V_{DS} = 28 V			1	µA
I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	V_{DS} = 28 V I_D = 100 mA	2.0		5.0	V
$V_{DS(ON)}$	V_{GS} = 10 V I_D = 3 A		0.7	0.8	V
G_{FS}	V_{DS} = 10 V I_D = 3 A		3		mho
C_{ISS}(1)	V_{GS} = 0 V V_{DS} = 28 V f = 1 MHz		221		pF
C_{OSS}	V_{GS} = 0 V V_{DS} = 28 V f = 1 MHz		48.9		pF
C_{RSS}	V_{GS} = 0 V V_{DS} = 28 V f = 1 MHz		2.25		pF

1. Includes Internal Input Moscap.

2.2 Dynamic

Table 4. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 32V I_{DQ} = 400 mA f = 860MHz	120			W
G_{PS}	V_{DD} = 32V I_{DQ} = 400 mA P_{OUT} = 120 W,f = 860MHz	13	16		dB
h_D	V_{DD} = 32V I_{DQ} = 400 mA P_{OUT} = 120 W,f = 860MHz	50			%
Load mismatch	V_{DD} = 32V I_{DQ} = 400 mA P_{OUT} = 120 W,f = 860MHz All phase angles	10:1			VSWR

3 Impedances

Figure 1. Current conventions

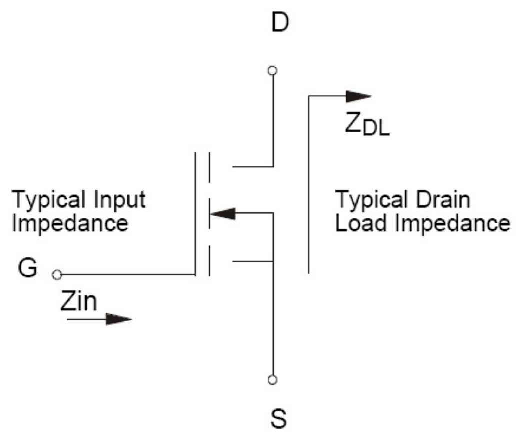


Table 5. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
860 MHz	5.57 + j 3.488	4.21 - j 2.88

Note: Measured drain to drain and gate to gate respectively.

4 Typical performance

Figure 2. Capacitance vs drain voltage

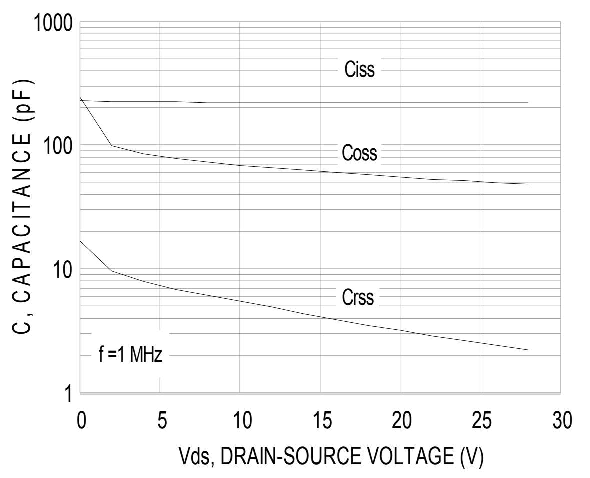


Figure 3. Gate-source voltage vs case temperature

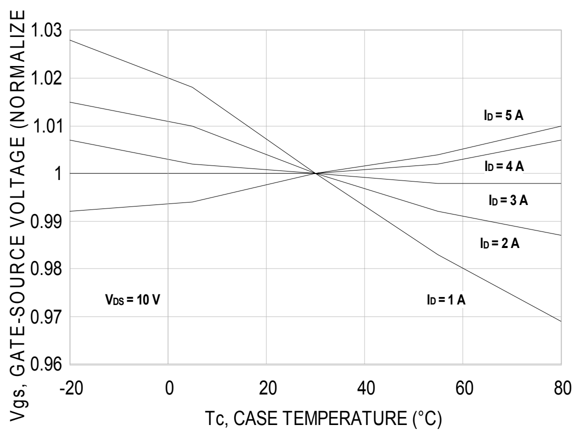


Figure 4. Drain current vs gate voltage

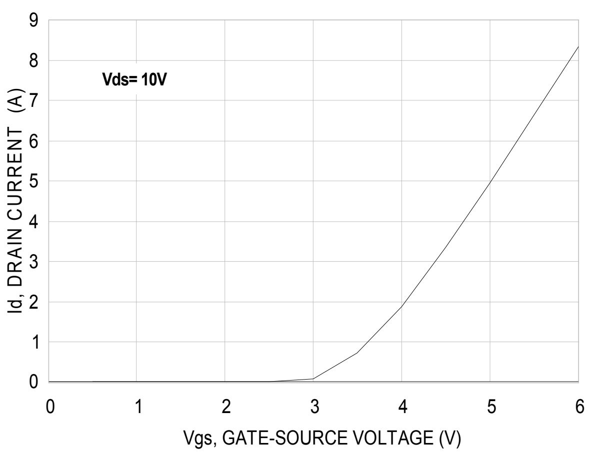


Figure 5. Output power & efficiency vs input power

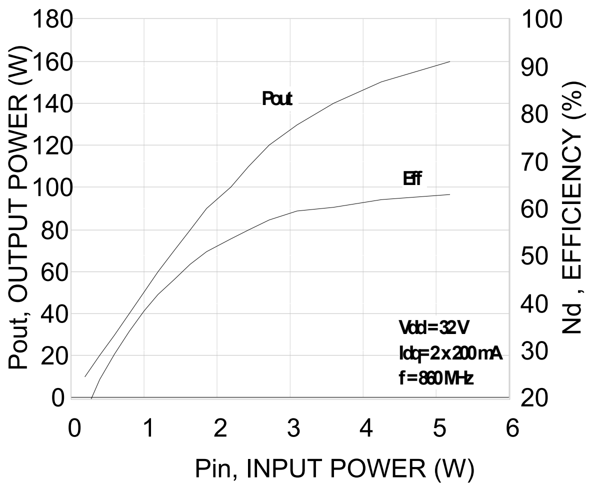


Figure 6. Power gain vs output power

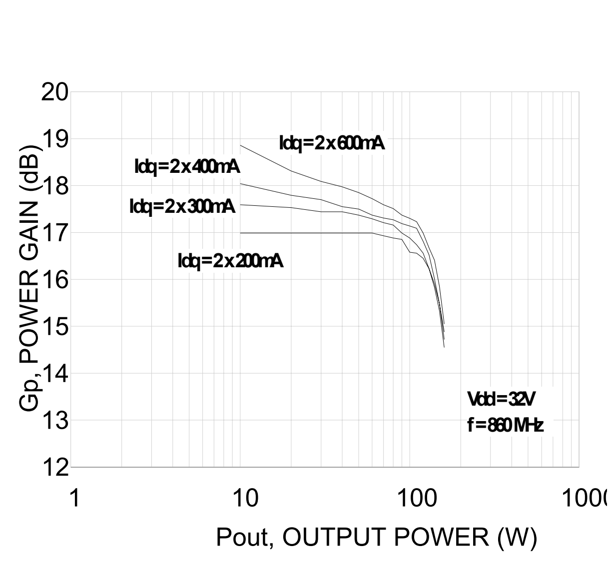


Figure 7. Intermodulation distortion vs output power

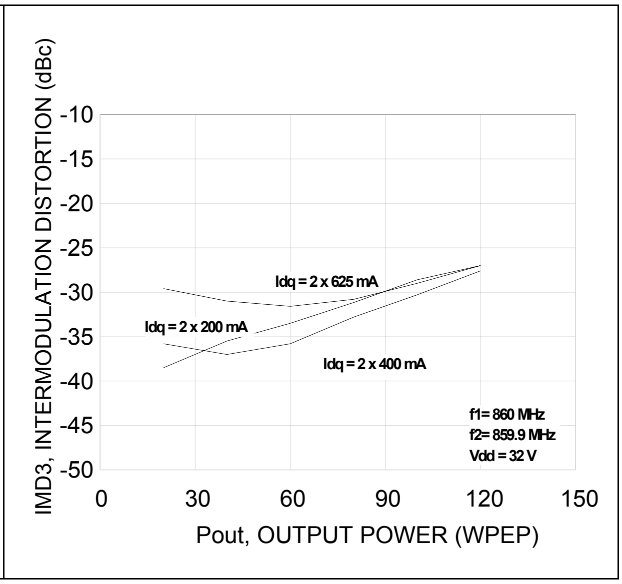
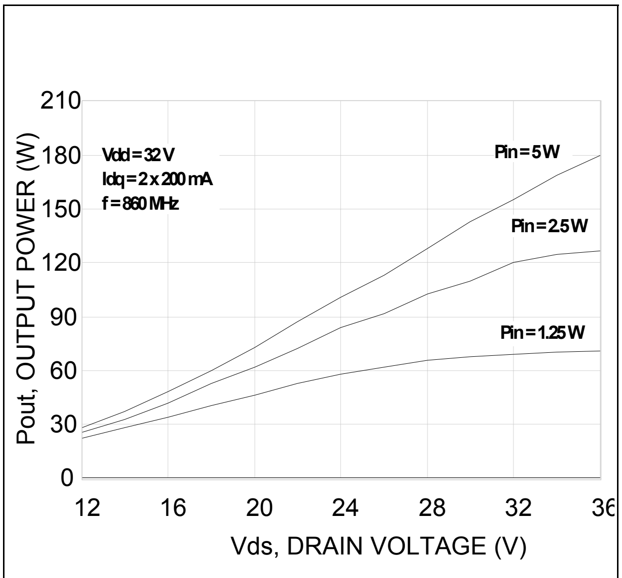
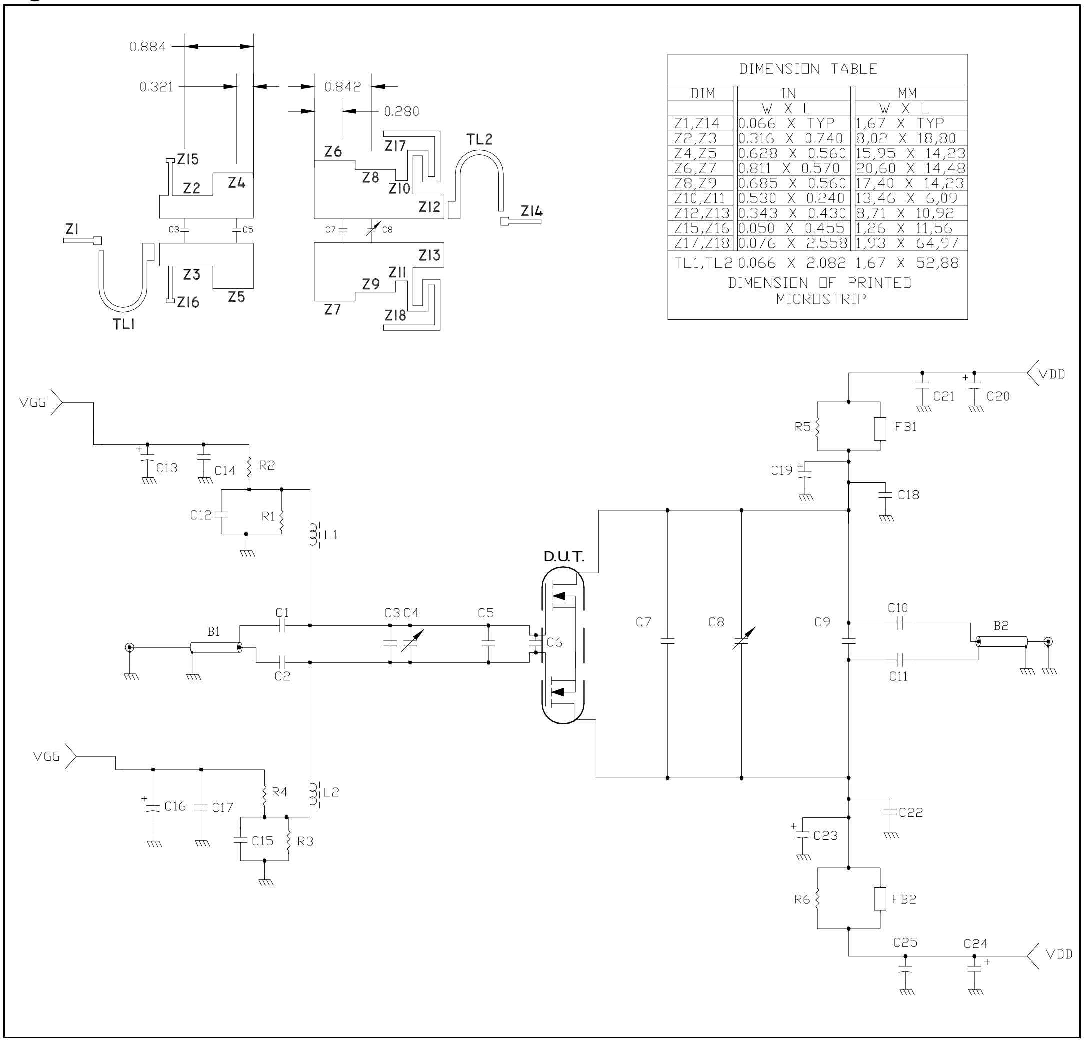


Figure 8. Output power vs drain voltage



Test circuit

Figure 9. Test circuit schematic



DIMENSION TABLE

DIM	IN W X L	MM W X L
Z1,Z14	0.066 X TYP	1,67 X TYP
Z2,Z3	0.316 X 0.740	8,02 X 18,80
Z4,Z5	0.628 X 0.560	15,95 X 14,23
Z6,Z7	0.811 X 0.570	20,60 X 14,48
Z8,Z9	0.685 X 0.560	17,40 X 14,23
Z10,Z11	0.530 X 0.240	13,46 X 6,09
Z12,Z13	0.343 X 0.430	8,71 X 10,92
Z15,Z16	0.050 X 0.455	1,26 X 11,56
Z17,Z18	0.076 X 2.558	1,93 X 64,97
TL1,TL2	0.066 X 2.082	1,67 X 52,88

DIMENSION OF PRINTED MICROSTRIP

1 *C3 and C4 adjacent to each other*

2 *Gap between ground & transmission line = 0.056 [1.42] TYP.*

Table 6. Test circuit component part list

Component	Description
C1, C2, C10, C11	51 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C3	9.1 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C4, C8	0.6 - 4.5 GIGATRIM VARIABLE CAPACITOR
C5, C9	5.6 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C6	12 pF ATC 100A SURFACE MOUNT CERAMIC CHIP CAPACITOR
C7	13 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C12, C15, C18, C22	91 pF ATC 100B SURFACE MOUNT CERAMIC CHIP CAPACITOR
C13, C16, C20, C24	10 µF 50V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
C14, C17, C21, C25	0.1 µF 500V SURFACE MOUNT CERAMIC CHIP CAPACITOR
C19, C23	100 µF 63V ALUMINUM ELECTROLYTIC RADIAL LEAD CAPACITOR
R1, R2, R3, R4	200 OHM 1/4 W SURFACE MOUNT CHIP RESISTOR
R5, R6	1.8 OHM 1/4 W SURFACE MOUNT CHIP RESISTOR
B1, B2	BALUN, 25 OHM SEMI-RIDGE OD="0.141", 2.37 LG COAXIAL CABLE OR EQUIVALENT
L1, L2	CHIP INDICATOR 10 nH SURFACE MOUNT COIL
FB1, FB2	SURFACE MOUNT EMI SHIELD BEAD
PCB	WOVEN GLASS REINFORCED / CERAMIC FILLED 0.030" THK εr = 3.48, 2 Oz ED CU BOTH SIDES

Figure 10. Test fixture

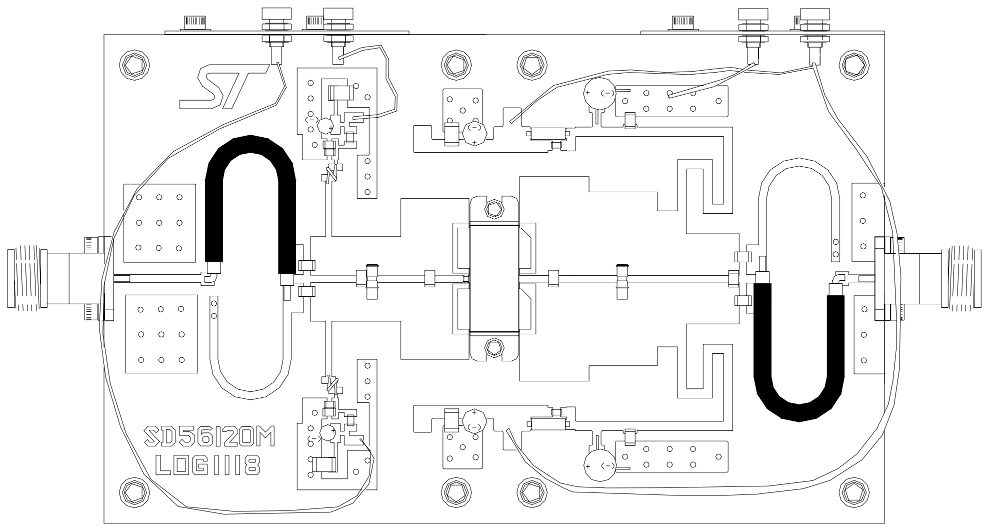
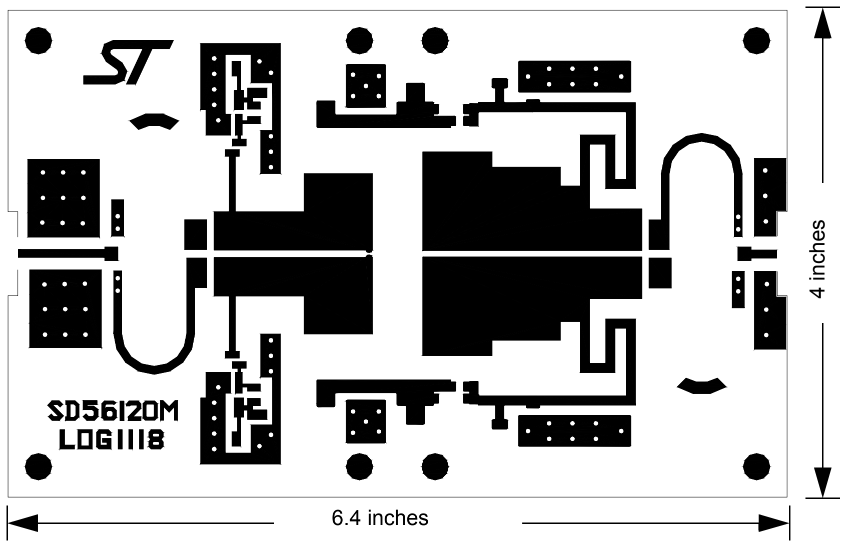


Figure 11. Test circuit photomaster



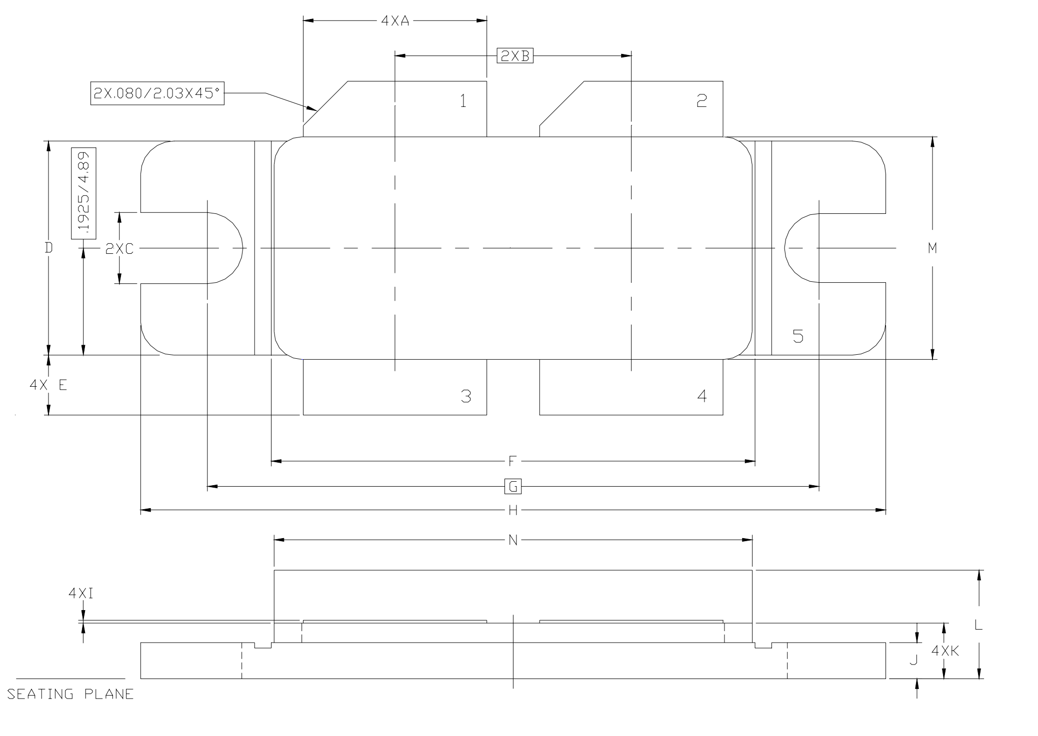
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 7. M252 (.400 x .860 4L BAL N/HERM W/FLG) mechanical data

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	8.13		8.64	.320		.340
B		10.80			.425	
C	3.00		3.30	.118		.130
D	9.65		9.91	.380		.390
E	2.16		2.92	.085		.115
F	21.97		22.23	.865		.875
G		27.94			1.100	
H	33.91		34.16	1.335		1.345
I	0.10		0.15	.004		.006
J	1.52		1.78	.060		.070
K	2.36		2.74	.093		.108
L	4.57		5.33	.180		.210
M	9.96		10.34	.392		.407
N	21.64		22.05	.852		.868

Figure 12. Package dimensions



Controlling dimension: Inches

Ref. 7145054A

6 Revision history

Table 8. Revision history

Date	Revision	Changes
13-Jul-2006	10	New template, added lead free info