

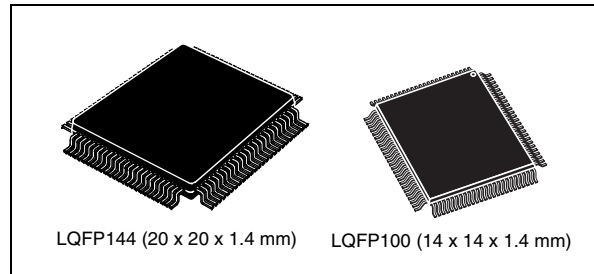


SPC560P44L3, SPC560P44L5 SPC560P50L3, SPC560P50L5

32-bit Power Architecture[®] based MCU with 576 KB Flash memory and 40 KB SRAM for automotive chassis and safety applications

Features

- 64 MHz, single issue, 32-bit CPU core complex (e200z0h)
 - Compliant with Power Architecture[®] embedded category
 - Variable Length Encoding (VLE)
- Memory organization
 - Up to 512 KB on-chip code flash memory with ECC and erase/program controller
 - Additional 64 (4 × 16) KB on-chip data flash memory with ECC for EEPROM emulation
 - Up to 40 KB on-chip SRAM with ECC
- Fail safe protection
 - Programmable watchdog timer
 - Non-maskable interrupt
 - Fault collection unit
- Nexus L2+ interface
- Interrupts
 - 16-channel eDMA controller
 - 16 priority level controller
- General purpose I/Os individually programmable as input, output or special function
- 2 general purpose eTimer units
 - 6 timers each with up/down count capabilities
 - 16-bit resolution, cascadable counters
 - Quadrature decode with rotation direction flag
 - Double buffer input capture and output compare
- Communications interfaces
 - 2 LINFlex channels (LIN 2.1)
 - 4 DSPI channels with automatic chip select generation
 - 1 FlexCAN interface (2.0B Active) with 32 message objects



- 1 safety port based on FlexCAN with 32 message objects and up to 7.5 Mbit/s capability; usable as second CAN when not used as safety port
- 1 FlexRay[™] module (V2.1) with selectable dual or single channel support, 32 message objects and up to 10 Mbit/s (512 KB device only)
- Two 10-bit analog-to-digital converters (ADC)
 - 2 × 11 input channels, + 4 shared channels
 - Conversion time < 1 μs including sampling time at full precision
 - Programmable ADC Cross Triggering Unit (CTU)
 - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- 1 FlexPWM unit: 8 complementary or independent outputs with ADC synchronization signals

Table 1. Device summary

Package	Order code	
	448 KB Flash	576 KB Flash
LQFP144	SPC560P44L5CEFA SPC560P44L5CEFB	SPC560P50L5CEFA SPC560P50L5CEFB SPC560P50L5BEAB
LQFP100	SPC560P44L3CEFA SPC560P44L3CEFB	SPC560P50L3CEFA SPC560P50L3CEFB SPC560P50L3BEAB

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1 Introduction

1.1 Document overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC560P44/50 series of microcontroller units (MCUs). It also describes the device features and highlights important electrical and physical characteristics. For functional characteristics, refer to the device reference manual.

1.2 Description

This 32-bit system-on-chip (SoC) automotive microcontroller family is the latest achievement in integrated automotive application controllers. It belongs to an expanding range of automotive-focused products designed to address chassis applications—specifically, electrical hydraulic power steering (EHPS) and electric power steering (EPS)—as well as airbag applications.

This family is one of a series of next-generation integrated automotive microcontrollers based on the Power Architecture technology.

The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

1.3 Device comparison

[Table 2](#) provides a summary of different members of the SPC560P44Lx, SPC560P50Lx family and their features—relative to full-featured version—to enable a comparison among the family members and an understanding of the range of functionality offered within this family.

Table 2. SPC560P44Lx, SPC560P50Lx device comparison

Feature		SPC560P44	SPC560P50
Code flash memory (with ECC)		384 KB	512 KB
Data flash memory / EE option (with ECC)		64 KB	
SRAM (with ECC)		36 KB	40 KB
Processor core		32-bit e200z0h	
Instruction set		VLE (variable length encoding)	
CPU performance		0–64 MHz	
FMPLL (frequency-modulated phase-locked loop) module		2	
INTC (interrupt controller) channels		147	
PIT (periodic interrupt timer)		1 (includes four 32-bit timers)	
eDMA (enhanced direct memory access) channels		16	
FlexRay		Yes ⁽¹⁾	
FlexCAN (controller area network)		2 ⁽²⁾⁽³⁾	
Safety port		Yes (via second FlexCAN module)	
FCU (fault collection unit)		Yes	
CTU (cross triggering unit)		Yes	
eTimer		2 (16-bit, 6 channels)	
FlexPWM (pulse-width modulation) channels		8 (capturing on X-channels)	
ADC (analog-to-digital converter)		2 (10-bit, 15-channel ⁽⁴⁾)	
LINFlex		2	
DSPI (deserial serial peripheral interface)		4	
CRC (cyclic redundancy check) unit		Yes	
JTAG controller		Yes	
Nexus port controller (NPC)		Yes (Level 2+)	
Supply	Digital power supply ⁽⁵⁾	3.3 V or 5 V single supply with external transistor	
	Analog power supply	3.3 V or 5 V	
	Internal RC oscillator	16 MHz	
	External crystal oscillator	4–40 MHz	
Packages		LQFP100, LQFP144	
Temperature	Standard ambient temperature	–40 to 125 °C	

- 32 message buffers, selectable single or dual channel support
- Each FlexCAN module has 32 message buffers.
- One FlexCAN module can act as a Safety Port with a bit rate as high as 7.5 Mbit/s.
- Four channels shared between the two ADCs
- The different supply voltages vary according to the part number ordered.

SPC560P44Lx, SPC560P50Lx is available in two configurations having different features: full-featured and airbag. [Table 3](#) shows the main differences between the two versions.

Table 3. SPC560P44Lx, SPC560P50Lx device configuration differences

Feature	Full-featured	Airbag
CTU (cross triggering unit)	Yes	No
FlexPWM	Yes	No
FlexRay	Yes	No
FMPLL (frequency-modulated phase-locked loop) module	2 (one FMPLL, one for FlexRay)	1 (only FMPLL)

1.4 Block diagram

[Figure 1](#) shows a top-level block diagram of the SPC560P44Lx, SPC560P50Lx MCU.

Figure 1. SPC560P44Lx, SPC560P50Lx block diagram

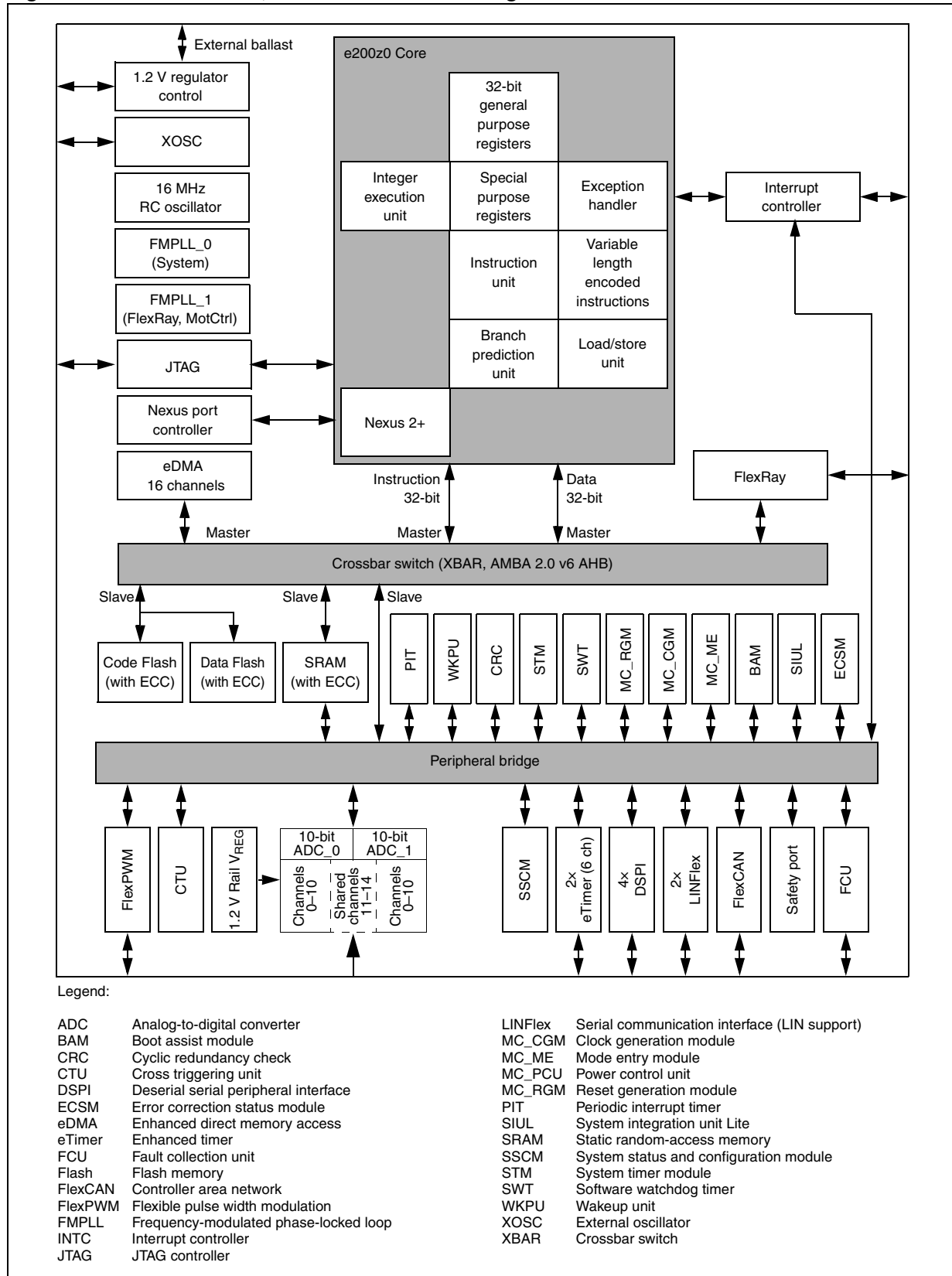


Table 4. SPC560P44Lx, SPC560P50Lx series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to-digital converter
Boot assist module (BAM)	Block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Controller area network (FlexCAN)	Supports the standard CAN communications protocol
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports; supports a 32-bit address bus width and a 32-bit data bus width
Cyclic redundancy check (CRC)	CRC checksum generator
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "n" programmable channels
Enhanced timer (eTimer)	Provides enhanced programmable up/down modulo counting
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
External oscillator (XOSC)	Provides an output clock used as input reference for FMPLL_0 or as reference clock for specific modules depending on system needs
Fault collection unit (FCU)	Provides functional safety to the device
Flash memory	Provides non-volatile storage for program code, constants and variables
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with minimum load on CPU
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Peripheral bridge (PBRIDGE)	Interface between the system bus and on-chip peripherals
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 4. SPC560P44Lx, SPC560P50Lx series block summary (continued)

Block	Function
Pulse width modulator (FlexPWM)	Contains four PWM submodules, each of which is capable of controlling a single half-bridge power stage and two fault input channels
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up to 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR ⁽¹⁾ and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, 1 of which can cause non-maskable interrupt requests or wakeup events

1. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.5 Feature details

1.5.1 High performance e200z0 core processor

The e200z0 Power Architecture core provides the following features:

- High performance e200z0 core processor for managing peripherals and interrupts
- Single issue 4-stage pipeline in-order execution 32-bit Power Architecture CPU
- Harvard architecture
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
 - Results in smaller code size footprint
 - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
 - 1 cycle load latency
 - Misaligned access support
 - No load-to-use pipeline bubbles
- Thirty-two 32-bit general purpose registers (GPRs)
- Separate instruction bus and load/store bus Harvard architecture
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs
- Long cycle time instructions, except for guarded loads, do not increase interrupt latency
- Extensive system development support through Nexus debug port
- Non-maskable interrupt support

1.5.2 Crossbar switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 32-bit data bus width.

The crossbar allows for two concurrent transactions to occur from any master port to any slave port; but one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic will select the higher priority master and grant it ownership of the slave port. All other masters requesting that slave port will be stalled until the higher priority master completes its transactions. Requesting masters will be treated with equal priority and will be granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access.

The crossbar provides the following features:

- 4 master ports:
 - e200z0 core complex Instruction port
 - e200z0 core complex Load/Store Data port
 - eDMA
 - FlexRay
- 3 slave ports:
 - Flash memory (code flash and data flash)
 - SRAM
 - Peripheral bridge
- 32-bit internal address, 32-bit internal data paths
- Fixed Priority Arbitration based on Port Master
- Temporary dynamic priority elevation of masters

1.5.3 Enhanced direct memory access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware micro architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels support independent 8, 16 or 32-bit single value or block transfers
- Supports variable sized queues and circular queues
- Source and destination address registers are independently configured to either post-increment or to remain constant
- Each transfer is initiated by a peripheral, CPU, or eDMA channel request
- Each eDMA channel can optionally send an interrupt request to the CPU on completion of a single value or block transfer
- DMA transfers possible between system memories, DSPs, ADC, FlexPWM, eTimer and CTU
- Programmable DMA channel multiplexer for assignment of any DMA source to any available DMA channel with as many as 30 request sources
- eDMA abort operation through software

1.5.4 Flash memory

The SPC560P44Lx, SPC560P50Lx provides as much as 576 KB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 32-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit wide prefetch buffers. Prefetch buffer hits allow no-wait responses. Normal flash memory array accesses are registered and are forwarded to the system bus on the following cycle, incurring two wait-states.

The flash memory module provides the following features:

- As much as 576 KB flash memory
 - 8 blocks (32 KB + 2×16 KB + 32 KB + 32 KB + 3×128 KB) code flash
 - 4 blocks (16 KB + 16 KB + 16 KB + 16 KB) data flash
 - Full Read While Write (RWW) capability between code and data flash
- Four 128-bit wide prefetch buffers to provide single cycle in-line accesses (prefetch buffers can be configured to prefetch code or data or both)
- Typical flash memory access time: 0 wait states for buffer hits, 2 wait states for page buffer miss at 64 MHz
- Hardware managed flash memory writes handled by 32-bit RISC Krypton engine
- Hardware and software configurable read and write access protections on a per-master basis
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (up to 31 additional cycles) allowing use for emulation of other memory types.
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page sizes
 - Code flash memory: 128 bits (4 words)
 - Data flash memory: 32 bits (1 word)
- ECC with single-bit correction, double-bit detection for data integrity
 - Code flash memory: 64-bit ECC
 - Data flash memory: 32-bit ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Censorship protection scheme to prevent flash memory content visibility
- Hardware support for EEPROM emulation

1.5.5 Static random access memory (SRAM)

The SPC560P44Lx, SPC560P50Lx SRAM module provides up to 40 KB of general-purpose memory.

The SRAM module provides the following features:

- Supports read/write accesses mapped to the SRAM from any master
- Up to 40 KB general purpose SRAM
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait state for 8- and 16-bit writes if back to back with a read to same memory block

1.5.6 Interrupt controller (INTC)

The interrupt controller (INTC) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems. The INTC handles 147 selectable-priority interrupt sources.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR has to be executed. It also provides a wide number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol (PCP) for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the same resource can not preempt each other.

The INTC provides the following features:

- Unique 9-bit vector for each separate interrupt source
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority: modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
- 2 external high priority interrupts directly accessing the main core and I/O processor (IOP) critical interrupt mechanism

1.5.7 System status and configuration module (SSCM)

The system status and configuration module (SSCM) provides central device functionality.

The SSCM includes these features:

- System configuration and status
 - Memory sizes/status
 - Device mode and security status
 - Determine boot vector
 - Search code flash for bootable sector
 - DMA status
- Debug status port enable and selection
- Bus and peripheral abort enable/disable

1.5.8 System clocks and clock generation

The following list summarizes the system clock and clock generation on the SPC560P44Lx, SPC560P50Lx:

- Lock detect circuitry continuously monitors lock status
- Loss of clock (LOC) detection for PLL outputs
- Programmable output clock divider ($\div 1$, $\div 2$, $\div 4$, $\div 8$)
- FlexPWM module and eTimer module can run on an independent clock source
- On-chip oscillator with automatic level control
- Internal 16 MHz RC oscillator for rapid start-up and safe mode: supports frequency trimming by user application

1.5.9 Frequency-modulated phase-locked loop (FMPLL)

The FMPLL allows the user to generate high speed system clocks from a 4–40 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

The PLL has the following major features:

- Input clock frequency: 4–40 MHz
- Maximum output frequency: 64 MHz
- Voltage controlled oscillator (VCO)—frequency 256–512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Frequency-modulated PLL
 - Modulation enabled/disabled through software
 - Triangle wave modulation
- Programmable modulation depth ($\pm 0.25\%$ to $\pm 4\%$ deviation from center frequency): programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation

1.5.10 Main oscillator

The main oscillator provides these features:

- Input frequency range: 4–40 MHz
- Crystal input mode or oscillator input mode
- PLL reference

1.5.11 Internal RC oscillator

This device has an RC ladder phase-shift oscillator. The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared by the stable bandgap reference voltage.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- $\pm 5\%$ variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup

1.5.12 Periodic interrupt timer (PIT)

The PIT module implements these features:

- 4 general purpose interrupt timers
- 32-bit counter resolution
- Clocked by system clock frequency
- Each channel can be used as trigger for a DMA request

1.5.13 System timer module (STM)

The STM module implements these features:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.14 Software watchdog timer (SWT)

The SWT has the following features:

- 32-bit time-out register to set the time-out period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.5.15 Fault collection unit (FCU)

The FCU provides an independent fault reporting mechanism even if the CPU is malfunctioning.

The FCU module has the following features:

- FCU status register reporting the device status
- Continuous monitoring of critical fault signals
- User selection of critical signals from different fault sources inside the device
- Critical fault events trigger 2 external pins (user selected signal protocol) that can be used externally to reset the device and/or other circuitry (for example, safety relay or FlexRay transceiver)
- Faults are latched into a register

1.5.16 System integration unit – Lite (SIUL)

The SPC560P44Lx, SPC560P50Lx SIUL controls MCU pad configuration, external interrupt, general purpose I/O (GPIO), and internal peripheral multiplexing.

The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized general purpose input output (GPIO) control of as many as 80 input/output pins and 26 analog input-only pads (package dependent)
- All GPIO pins can be independently configured to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins (except ADC channels) can be alternatively configured as both general purpose input or output pins
- ADC channels support alternative configuration as general purpose inputs
- Direct readback of the pin value is supported on all pins through the SIUL
- Configurable digital input filter that can be applied to some general purpose input pins for noise elimination: as many as 4 internal functions can be multiplexed onto 1 pin

1.5.17 Boot and censorship

Different booting modes are available in the SPC560P44Lx, SPC560P50Lx: booting from internal flash memory and booting via a serial link.

The default booting scheme uses the internal flash memory (an internal pull-down is used to select this mode). Optionally, the user can boot via FlexCAN or LINFlex (using the boot assist module software).

A censorship scheme is provided to protect the content of the flash memory and offer increased security for the entire device.

A password mechanism is designed to grant the legitimate user access to the non-volatile memory.

Boot assist module (BAM)

The BAM is a block of read-only one-time programmed memory and is identical for all SPC560Pxx devices that are based on the e200z0h core. The BAM program is executed every time the device is powered on if the alternate boot mode has been selected by the user.

The BAM provides the following features:

- Serial bootloading via FlexCAN or LINFlex
- Ability to accept a password via the used serial communication channel to grant the legitimate user access to the non-volatile memory

1.5.18 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC560P44Lx, SPC560P50Lx.

The sources of the ECC errors are:

- Flash memory
- SRAM

1.5.19 Peripheral bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access privilege level per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianness swap capability

1.5.20 Controller area network (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU contains one controller area network (FlexCAN) module. This module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module contains 32 message buffers.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Up to 8-bytes data length
 - Programmable bit rate up to 1 Mbit/s
- 32 message buffers of up to 8-bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
 - Supports configuration of multiple mailboxes to form message queues of scalable depth
 - Arbitration scheme according to message ID or message buffer number
 - Internal arbitration to guarantee no inner or outer priority inversion
 - Transmit abort procedure and notification
- Receive features
 - Individual programmable filters for each mailbox
 - 8 mailboxes configurable as a six-entry receive FIFO
 - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
 - System clock
 - Direct oscillator clock to avoid PLL jitter

1.5.21 Safety port (FlexCAN)

The SPC560P44Lx, SPC560P50Lx MCU has a second CAN controller synthesized to run at high bit rates to be used as a safety port. The CAN module of the safety port provides the following features:

- Identical to the FlexCAN module
- Bit rate as fast as 7.5 Mbit/s at 60 MHz CPU clock using direct connection between CAN modules (no physical transceiver required)
- 32 message buffers of up to 8 bytes data length
- Can be used as a second independent CAN module

1.5.22 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1
- 32 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as Tx, Rx or RxFIFO
- Message buffer size configurable
- Message filtering for all message buffers based on FrameID, cycle count and message ID
- Programmable acceptance filters for RxFIFO message buffers

1.5.23 Serial communication interface module (LINFlex)

The LINFlex (local interconnect network flexible) on the SPC560P44Lx, SPC560P50Lx features the following:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0, and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
 - Autonomous LIN frame handling
 - Message buffer to store Identifier and as much as 8 data bytes
 - Supports message length as long as 64 bytes
 - Detection and flagging of LIN errors (sync field, delimiter, ID parity, bit framing, checksum, and time-out)
 - Classic or extended checksum calculation
 - Configurable Break duration as long as 36-bit times
 - Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
 - Diagnostic features: Loop back; Self Test; LIN bus stuck dominant detection
 - Interrupt-driven operation with 16 interrupt sources
- LIN slave mode features
 - Autonomous LIN header handling
 - Autonomous LIN response handling
- UART mode
 - Full-duplex operation
 - Standard non return-to-zero (NRZ) mark/space format
 - Data buffers with 4-byte receive, 4-byte transmit
 - Configurable word length (8-bit or 9-bit words)
 - Error detection and flagging
 - Parity, Noise and Framing errors
 - Interrupt-driven operation with four interrupt sources
 - Separate transmitter and receiver CPU interrupt sources
 - 16-bit programmable baud-rate modulus counter and 16-bit fractional
 - 2 receiver wake-up methods

1.5.24 Deserial serial peripheral interface (DSPI)

The deserial serial peripheral interface (DSPI) module provides a synchronous serial interface for communication between the SPC560P44Lx, SPC560P50Lx MCU and external devices.

The DSPI modules provide these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 20 chip select lines available
 - 8 on DSPI_0
 - 4 each on DSPI_1, DSPI_2 and DSPI_3
- 8 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.25 Pulse width modulator (FlexPWM)

The pulse width modulator module (PWM) contains four PWM submodules, each capable of controlling a single half-bridge power stage. There are also four fault channels.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), permanent magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

The FlexPWM block implements the following features:

- 16-bit resolution for center, edge-aligned, and asymmetrical PWMs
- Maximum operating clock frequency of 120 MHz
- PWM outputs can operate as complementary pairs or independent channels
- Can accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
 - Integral reload rates from 1 to 16
 - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Write protection for critical registers
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a “Force Out” event
- PWMX pin can optionally output a third PWM signal from each submodule
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual-edge capture functionality
- eDMA support with automatic reload
- 2 fault inputs
- Capture capability for PWMA, PWMB, and PWMX channels not supported

1.5.26 eTimer

The SPC560P44Lx, SPC560P50Lx includes two eTimer modules. Each module provides six 16-bit general purpose up/down timer/counter units with the following features:

- Maximum operating clock frequency of 120 MHz
- Individual channel capability
 - Input capture trigger
 - Output compare
 - Double buffer (to capture rising edge and falling edge)
 - Separate prescaler for each counter
 - Selectable clock source
 - 0–100% pulse measurement
 - Rotation direction flag (Quad decoder mode)
- Maximum count rate
 - External event counting: max. count rate = peripheral clock/2
 - Internal clock counting: max. count rate = peripheral clock
- Counters are:
 - Cascadable
 - Preloadable
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Pins available as GPIO when timer functionality not in use

1.5.27 Analog-to-digital converter (ADC) module

The ADC module provides the following features:

Analog part:

- 2 on-chip AD converters
 - 10-bit AD resolution
 - 1 sample and hold unit per ADC
 - Conversion time, including sampling time, less than 1 μ s (at full precision)
 - Typical sampling time is 150 ns min. (at full precision)
 - Differential non-linearity error (DNL) ± 1 LSB
 - Integral non-linearity error (INL) ± 1.5 LSB
 - TUE < 3 LSB
 - Single-ended input signal up to 5.0 V
 - The ADC and its reference can be supplied with a voltage independent from V_{DDIO}
 - The ADC supply can be equal or higher than V_{DDIO}
 - The ADC supply and the ADC reference are not independent from each other (they are internally bonded to the same pad)
 - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles

Digital part:

- 2 × 13 input channels including 4 channels shared between the 2 converters
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location,
- 2 modes of operation: Normal mode or CTU control mode
- Normal mode features
 - Register-based interface with the CPU: control register, status register, 1 result register per channel
 - ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
 - Selectable priority between software and hardware injected commands
 - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
 - DMA compatible interface
- CTU control mode features
 - Triggered mode only
 - 4 independent result queues (2 × 16 entries, 2 × 4 entries)
 - Result alignment circuitry (left justified; right justified)
 - 32-bit read mode allows to have channel ID on one of the 16-bit part
 - DMA compatible interfaces

1.5.28 Cross triggering unit (CTU)

The cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Double buffered trigger generation unit with as many as eight independent triggers generated from external triggers
- Trigger generation unit configurable in sequential mode or in triggered mode
- Each Trigger can be appropriately delayed to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection

1.5.29 Nexus development interface (NDI)

The NDI (Nexus Development Interface) block provides real-time development support capabilities for the SPC560P44Lx, SPC560P50Lx Power Architecture based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI

block is an integration of several individual Nexus blocks that are selected to provide the development support interface for this device. The NDI block interfaces to the host processor and internal busses to provide development support as per the IEEE-ISTO 5001-2003 Class 2+ standard. The development support provided includes access to the MCU's internal memory map and access to the processor's internal registers during run time.

The Nexus Interface provides the following features:

- Configured via the IEEE 1149.1
- All Nexus port pins operate at V_{DDIO} (no dedicated power supply)
- Nexus 2+ features supported
 - Static debug
 - Watchpoint messaging
 - Ownership trace messaging
 - Program trace messaging
 - Real time read/write of any internally memory mapped resources through JTAG pins
 - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
 - Watchpoint triggering, watchpoint triggers program tracing
- Auxiliary Output Port
 - 4 MDO (Message Data Out) pins
 - MCKO (Message Clock Out) pin
 - 2 \overline{MSEO} (Message Start/End Out) pins
 - $\overline{EVT0}$ (Event Out) pin
- Auxiliary Input Port
 - $\overline{EVT1}$ (Event In) pin

1.5.30 Cyclic redundancy check (CRC)

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC module features:

- Support for CRC-16-CCITT (x_{25} protocol):
 - $x^{16} + x^{12} + x^5 + 1$
- Support for CRC-32 (Ethernet protocol):
 - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.31 IEEE 1149.1 JTAG controller

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 4 pins (TDI, TMS, TCK, TDO)
- Selectable modes of operation include JTAGC/debug or normal system operation.
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
 - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD
- A 5-bit instruction register that supports the additional following public instructions:
 - ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

1.5.32 On-chip voltage regulator (VREG)

The on-chip voltage regulator module provides the following features:

- Uses external NPN (negative-positive-negative) transistor
- Regulates external 3.3 V /5.0 V down to 1.2 V for the core logic
- Low voltage detection on the internal 1.2 V and I/O voltage 3.3 V

2 Package pinouts and signal descriptions

2.1 Package pinouts

The LQFP pinouts are shown in the following figures.

Figure 2. 144-pin LQFP pinout – Full featured configuration (top view)

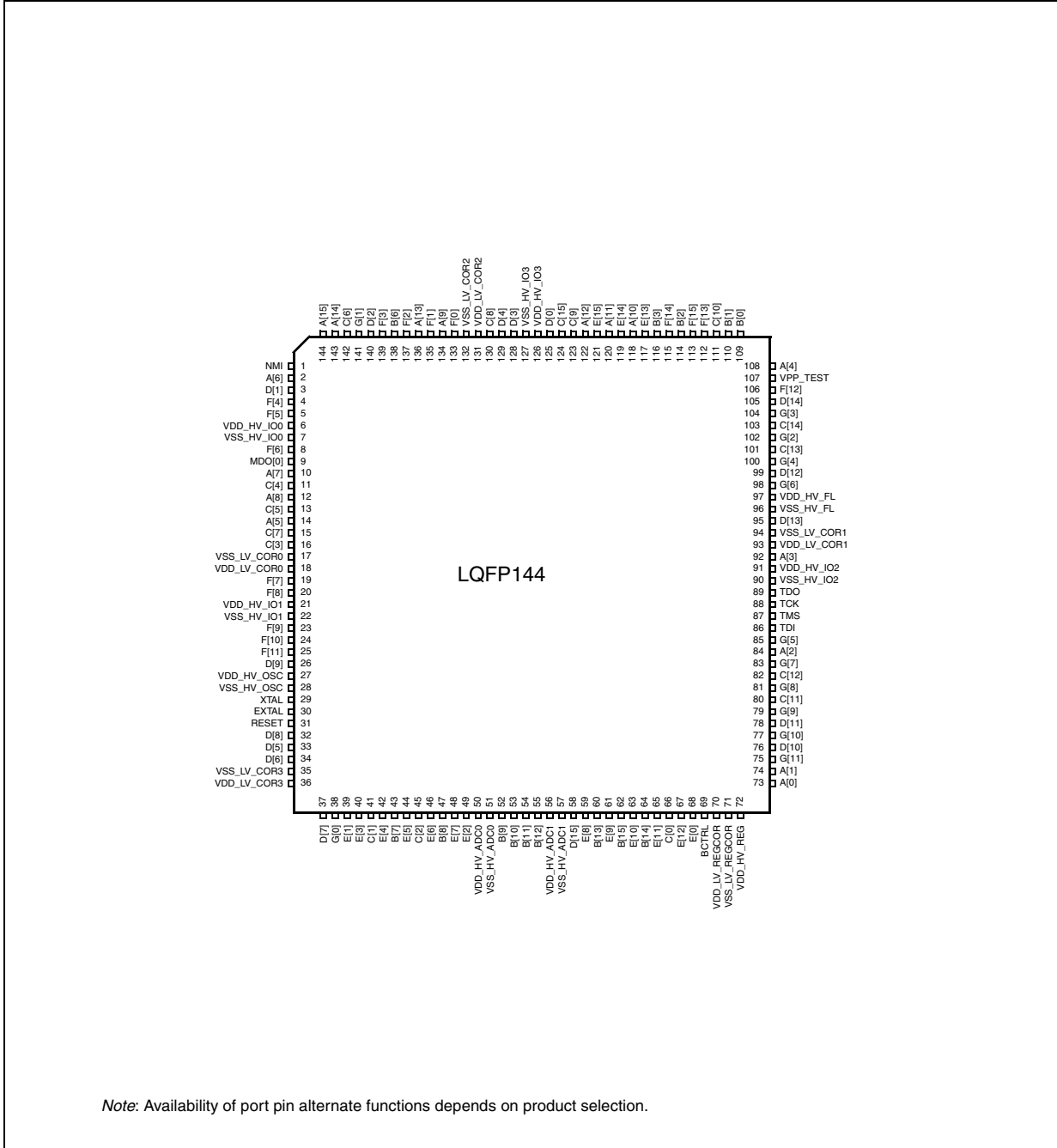
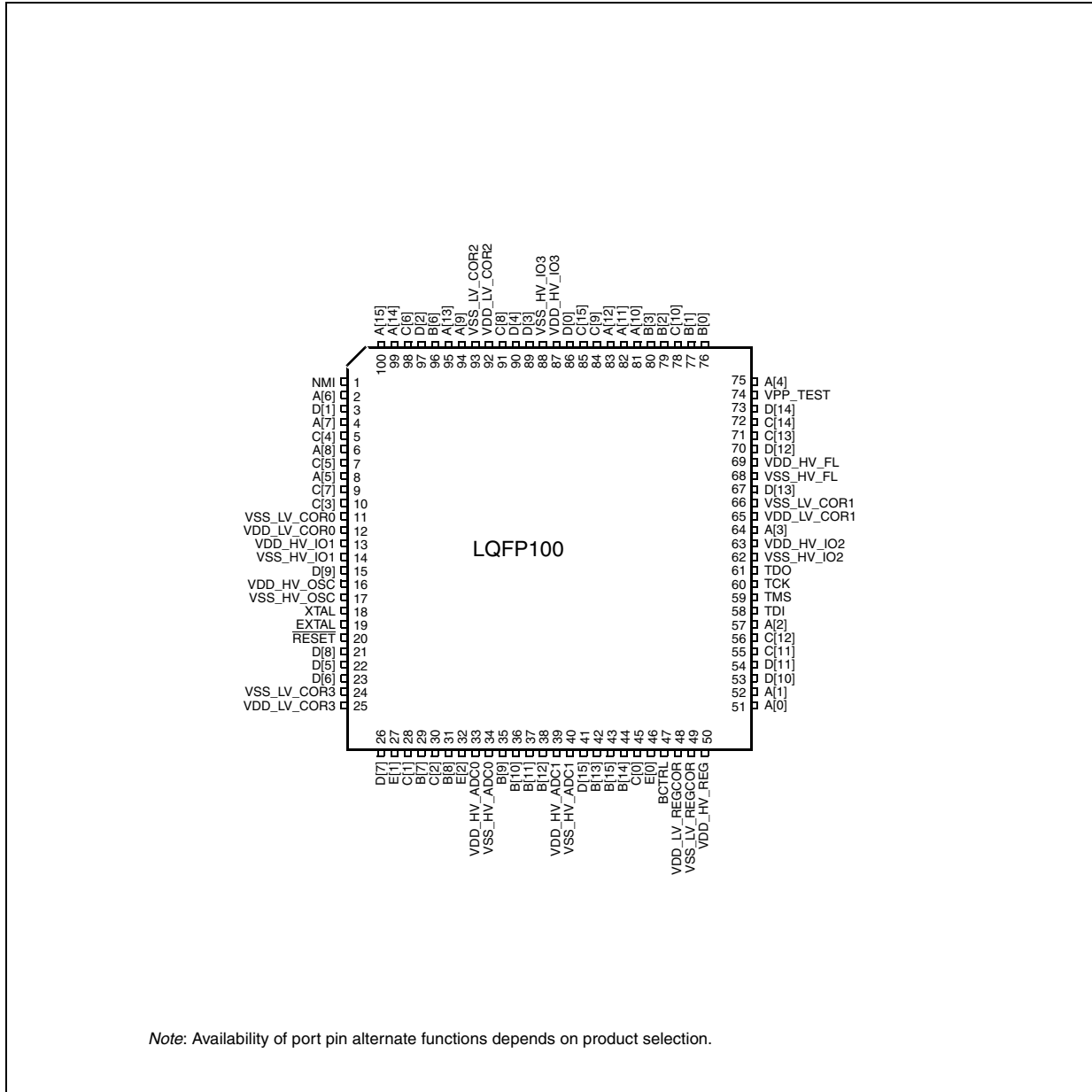
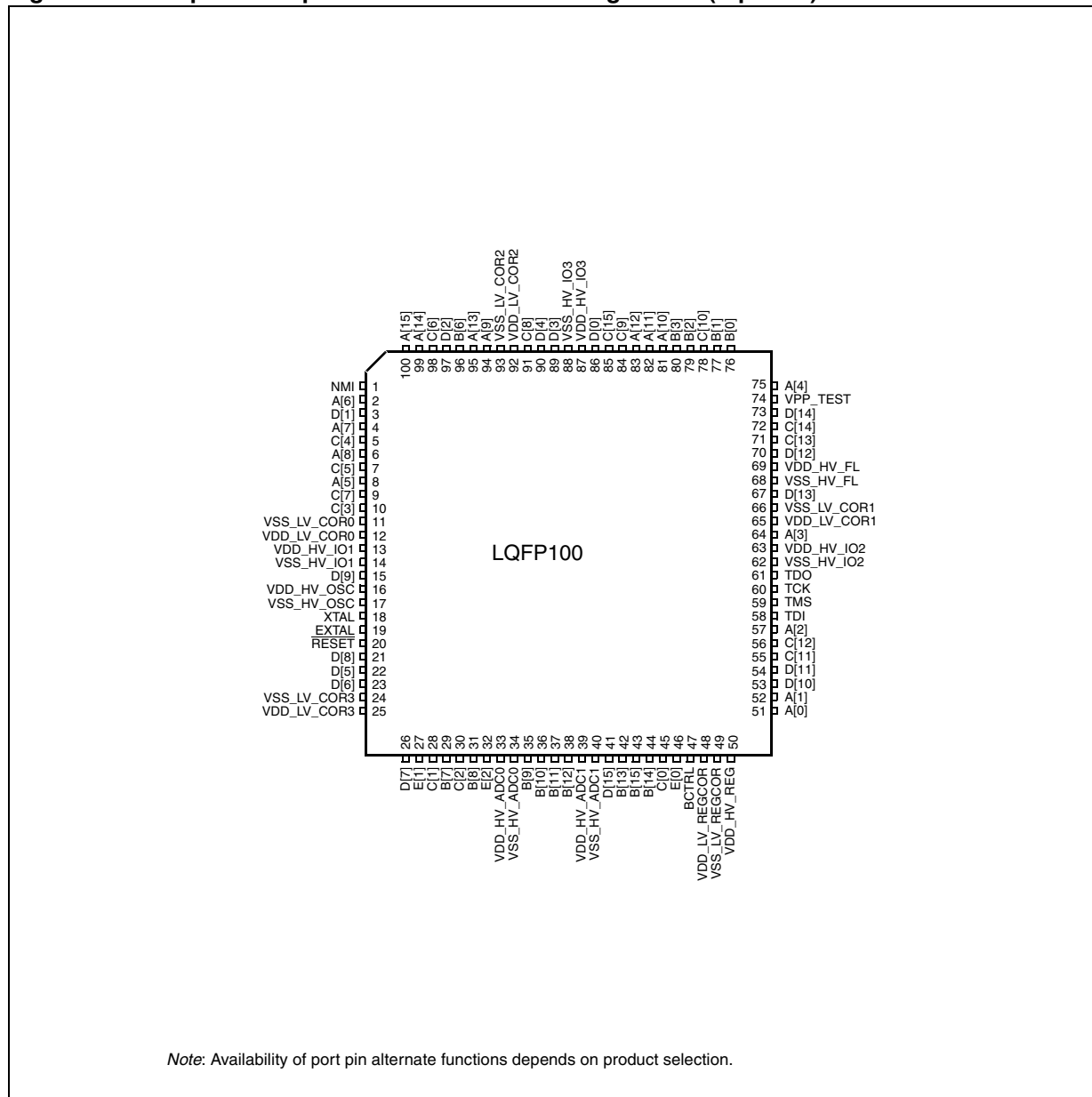


Figure 3. 100-pin LQFP pinout – Airbag configuration (top view)



Note: Availability of port pin alternate functions depends on product selection.

Figure 4. 100-pin LQFP pinout – Full featured configuration (top view)



2.2 Pin description

The following sections provide signal descriptions and related information about the functionality and configuration of the SPC560P44Lx, SPC560P50Lx devices.

2.2.1 Power supply and reference voltage pins

[Table 5](#) lists the power supply and reference voltage for the SPC560P44Lx, SPC560P50Lx devices.

Table 5. Supply pins

Supply		Pin	
Symbol	Description	100-pin	144-pin
VREG control and power supply pins. Pins available on 100-pin and 144-pin package.			
BCTRL	Voltage regulator external NPN ballast base control pin	47	69
V _{DD_HV_REG} (3.3 V or 5.0 V)	Voltage regulator supply voltage	50	72
V _{DD_LV_REGCOR}	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and V _{SS_LV_REGCOR} .	48	70
V _{SS_LV_REGCOR}	1.2 V decoupling pins for core logic and regulator feedback. Decoupling capacitor must be connected between this pins and V _{DD_LV_REGCOR} .	49	71
ADC_0/ADC_1 reference and supply voltage. Pins available on 100-pin and 144-pin package.			
V _{DD_HV_ADC0} ⁽¹⁾	ADC_0 supply and high reference voltage	33	50
V _{SS_HV_ADC0}	ADC_0 ground and low reference voltage	34	51
V _{DD_HV_ADC1}	ADC_1 supply and high reference voltage	39	56
V _{SS_HV_ADC1}	ADC_1 ground and low reference voltage	40	57
Power supply pins (3.3 V or 5.0 V). All pins available on 144-pin package. Five pairs (V _{DD} ; V _{SS}) available on 100-pin package.			
V _{DD_HV_IO0} ⁽²⁾	Input/Output supply voltage	—	6
V _{SS_HV_IO0} ⁽²⁾	Input/Output ground	—	7
V _{DD_HV_IO1}	Input/Output supply voltage	13	21
V _{SS_HV_IO1}	Input/Output ground	14	22
V _{DD_HV_IO2}	Input/Output supply voltage	63	91
V _{SS_HV_IO2}	Input/Output ground	62	90
V _{DD_HV_IO3}	Input/Output supply voltage	87	126
V _{SS_HV_IO3}	Input/Output ground	88	127
V _{DD_HV_FL}	Code and data flash supply voltage	69	97
V _{SS_HV_FL}	Code and data flash supply ground	68	96
V _{DD_HV_OSC}	Crystal oscillator amplifier supply voltage	16	27
V _{SS_HV_OSC}	Crystal oscillator amplifier ground	17	28
Power supply pins (1.2 V). All pins available on 100-pin and 144-pin package.			
V _{DD_LV_COR0}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV_COR} pin.	12	18
V _{SS_LV_COR0}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{DD_LV_COR} pin.	11	17

Table 5. Supply pins (continued)

Supply		Pin	
Symbol	Description	100-pin	144-pin
V _{DD_LV_COR1}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV_COR} pin.	65	93
V _{SS_LV_COR1}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{DD_LV_COR} pin.	66	94
V _{DD_LV_COR2}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{SS_LV_COR} pin.	92	131
V _{SS_LV_COR2}	1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest V _{DD_LV_COR} pin.	93	132
V _{DD_LV_COR3}	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and V _{SS_LV_COR3} .	25	36
V _{SS_LV_COR3}	1.2 V Decoupling pins for on-chip PLL modules. Decoupling capacitor must be connected between this pin and V _{DD_LV_COR3} .	24	35

1. Analog supply/ground and high/low reference lines are internally physically separate, but are shorted via a double-bonding connection on V_{DD_HV_ADCx}/V_{SS_HV_ADCx} pins.
2. Not available on 100-pin package.

2.2.2 System pins

[Table 5](#) and [Table 6](#) contain information on pin functions for the SPC560P44Lx, SPC560P50Lx devices. The pins listed in [Table 6](#) are single-function pins. The pins shown in [Table 7](#) are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

Table 6. System pins

Symbol	Description	Direction	Pad speed ⁽¹⁾		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
Dedicated pins. Available on 100-pin and 144-pin package.						
MDO[0]	Nexus Message Data Output—line 0	Output only	Fast		—	9
NMI	Non-Maskable Interrupt	Input only	Slow	—	1	1
XTAL	Analog output of the oscillator amplifier circuit; needs to be grounded if oscillator is used in bypass mode	—	—	—	18	29
EXTAL	<ul style="list-style-type: none"> – Analog input of oscillator amplifier circuit, when oscillator not in bypass mode – Analog input for clock generator when oscillator in bypass mode 	—	—	—	19	30

Table 6. System pins (continued)

Symbol	Description	Direction	Pad speed ⁽¹⁾		Pin	
			SRC = 0	SRC = 1	100-pin	144-pin
TMS	JTAG state machine control	Bidirectional	Slow	Fast	59	87
TCK	JTAG clock	Input only	Slow	—	60	88
TDI	Test Data In	Input only	Slow	Medium	58	86
TDO	Test Data Out	Output only	Slow	Fast	61	89
Reset pin, available on 100-pin and 144-pin package.						
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt trigger characteristics and noise filter	Bidirectional	Medium	—	20	31
Test pin, available on 100-pin and 144-pin package.						
VPP_TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.	—	—	—	74	107

1. SCR values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

2.2.3 Pin muxing

[Table 7](#) defines the pin list and muxing for the SPC560P44Lx, SPC560P50Lx devices.

Each row of [Table 7](#) shows all the possible ways of configuring each pin, via alternate functions. The default function assigned to each pin after reset is the ALT0 function.

SPC560P44Lx, SPC560P50Lx devices provide four main I/O pad types, depending on the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved NEXUS debugging capability.
- *Symmetric pads* are designed to meet FlexRay requirements.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance. For more information, see the datasheet's "Pad AC Specifications" section.

Table 7. Pin muxing

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 —	GPIO[0] ETC[0] SCK F[0] EIRQ[0]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	51	73
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 —	GPIO[1] ETC[1] SOUT F[1] EIRQ[1]	SIUL eTimer_0 DSPI_2 FCU_0 SIUL	I/O I/O O O I	Slow	Medium	52	74
A[2] ⁽⁶⁾	PCR[2]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[2] ETC[2] — A[3] SIN ABS[0] EIRQ[2]	SIUL eTimer_0 — FlexPWM_0 DSPI_2 MC_RGM SIUL	I/O I/O — O I I I	Slow	Medium	57	84
A[3] ⁽⁶⁾	PCR[3]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[3] ETC[3] CS0 B[3] ABS[2] EIRQ[3]	SIUL eTimer_0 DSPI_2 FlexPWM_0 MC_RGM SIUL	I/O I/O I/O O I I	Slow	Medium	64	92

**Table 7. Pin muxing (continued)**

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
A[4] ⁽⁶⁾	PCR[4]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[4] ETC[0] CS1 ETC[4] FAB EIRQ[4]	SIUL eTimer_1 DSPI_2 eTimer_0 MC_RGM SIUL	I/O I/O O I/O I I	Slow	Medium	75	108
A[5]	PCR[5]	ALT0 ALT1 ALT2 ALT3 —	GPIO[5] CS0 ETC[5] CS7 EIRQ[5]	SIUL DSPI_1 eTimer_1 DSPI_0 SIUL	I/O I/O I/O O I	Slow	Medium	8	14
A[6]	PCR[6]	ALT0 ALT1 ALT2 ALT3 —	GPIO[6] SCK — — EIRQ[6]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	Slow	Medium	2	2
A[7]	PCR[7]	ALT0 ALT1 ALT2 ALT3 —	GPIO[7] SOUT — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	Slow	Medium	4	10
A[8]	PCR[8]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[8] — — — SIN EIRQ[8]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	Slow	Medium	6	12

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
A[9]	PCR[9]	ALT0 ALT1 ALT2 ALT3 —	GPIO[9] CS1 — B[3] FAULT[0]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — O I	Slow	Medium	94	134
A[10]	PCR[10]	ALT0 ALT1 ALT2 ALT3 —	GPIO[10] CS0 B[0] X[2] EIRQ[9]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O I/O I/O I	Slow	Medium	81	118
A[11]	PCR[11]	ALT0 ALT1 ALT2 ALT3 —	GPIO[11] SCK A[0] A[2] EIRQ[10]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O I/O I/O I/O I	Slow	Medium	82	120
A[12]	PCR[12]	ALT0 ALT1 ALT2 ALT3 —	GPIO[12] SOUT A[2] B[2] EIRQ[11]	SIUL DSPI_2 FlexPWM_0 FlexPWM_0 SIUL	I/O O I/O I/O I	Slow	Medium	83	122
A[13]	PCR[13]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[13] — B[2] — SIN FAULT[0] EIRQ[12]	SIUL — FlexPWM_0 — DSPI_2 FlexPWM_0 SIUL	I/O — I/O — I I I	Slow	Medium	95	136



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
A[14]	PCR[14]	ALT0 ALT1 ALT2 ALT3 —	GPIO[14] TXD ETC[4] — EIRQ[13]	SIUL Safety Port_0 eTimer_1 — SIUL	I/O O I/O — I	Slow	Medium	99	143
A[15]	PCR[15]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[15] — ETC[5] — RXD EIRQ[14]	SIUL — eTimer_1 — Safety Port_0 SIUL	I/O — I/O — I I	Slow	Medium	100	144
Port B (16-bit)									
B[0]	PCR[16]	ALT0 ALT1 ALT2 ALT3 —	GPIO[16] TXD ETC[2] DEBUG[0] EIRQ[15]	SIUL FlexCAN_0 eTimer_1 SSCM SIUL	I/O O I/O — I	Slow	Medium	76	109
B[1]	PCR[17]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[17] — ETC[3] DEBUG[1] RXD EIRQ[16]	SIUL — eTimer_1 SSCM FlexCAN_0 SIUL	I/O — I/O — I I	Slow	Medium	77	110
B[2]	PCR[18]	ALT0 ALT1 ALT2 ALT3 —	GPIO[18] TXD — DEBUG[2] EIRQ[17]	SIUL LIN_0 — SSCM SIUL	I/O O — — I	Slow	Medium	79	114

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[3]	PCR[19]	ALT0 ALT1 ALT2 ALT3 —	GPIO[19] — — DEBUG[3] RXD	SIUL — — SSCM LIN_0	I/O — — — I	Slow	Medium	80	116
B[6]	PCR[22]	ALT0 ALT1 ALT2 ALT3 —	GPIO[22] CLKOUT CS2 — EIRQ[18]	SIUL MC_CGL DSPI_2 — SIUL	I/O O O — I	Slow	Medium	96	138
B[7]	PCR[23]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[23] — — — AN[0] RXD	SIUL — — — ADC_0 LIN_0	Input only	—	—	29	43
B[8]	PCR[24]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[24] — — — AN[1] ETC[5]	SIUL — — — ADC_0 eTimer_0	Input only	—	—	31	47
B[9]	PCR[25]	ALT0 ALT1 ALT2 ALT3 —	GPIO[25] — — — AN[11]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	35	52



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[10]	PCR[26]	ALT0 ALT1 ALT2 ALT3 —	GPIO[26] — — — AN[12]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	36	53
B[11]	PCR[27]	ALT0 ALT1 ALT2 ALT3 —	GPIO[27] — — — AN[13]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	37	54
B[12]	PCR[28]	ALT0 ALT1 ALT2 ALT3 —	GPIO[28] — — — AN[14]	SIUL — — — ADC_0 / ADC_1	Input only	—	—	38	55
B[13]	PCR[29]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[29] — — — AN[0] RXD	SIUL — — — ADC_1 LIN_1	Input only	—	—	42	60
B[14]	PCR[30]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[30] — — — AN[1] ETC[4] EIRQ[19]	SIUL — — — ADC_1 eTimer_0 SIUL	Input only	—	—	44	64

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
B[15]	PCR[31]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[31] — — — AN[2] EIRQ[20]	SIUL — — — ADC_1 SIUL	Input only	—	—	43	62
Port C (16-bit)									
C[0]	PCR[32]	ALT0 ALT1 ALT2 ALT3 —	GPIO[32] — — — AN[3]	SIUL — — — ADC_1	Input only	—	—	45	66
C[1]	PCR[33]	ALT0 ALT1 ALT2 ALT3 —	GPIO[33] — — — AN[2]	SIUL — — — ADC_0	Input only	—	—	28	41
C[2]	PCR[34]	ALT0 ALT1 ALT2 ALT3 —	GPIO[34] — — — AN[3]	SIUL — — — ADC_0	Input only	—	—	30	45
C[3]	PCR[35]	ALT0 ALT1 ALT2 ALT3 —	GPIO[35] CS1 ETC[4] TXD EIRQ[21]	SIUL DSPI_0 eTimer_1 LIN_1 SIUL	I/O O I/O O I	Slow	Medium	10	16



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[4]	PCR[36]	ALT0 ALT1 ALT2 ALT3 —	GPIO[36] CS0 X[1] DEBUG[4] EIRQ[22]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O I/O — I	Slow	Medium	5	11
C[5]	PCR[37]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[37] SCK — DEBUG[5] FAULT[3] EIRQ[23]	SIUL DSPI_0 — SSCM FlexPWM_0 SIUL	I/O I/O — — I I	Slow	Medium	7	13
C[6]	PCR[38]	ALT0 ALT1 ALT2 ALT3 —	GPIO[38] SOUT B[1] DEBUG[6] EIRQ[24]	SIUL DSPI_0 FlexPWM_0 SSCM SIUL	I/O I/O O — I	Slow	Medium	98	142
C[7]	PCR[39]	ALT0 ALT1 ALT2 ALT3 —	GPIO[39] — A[1] DEBUG[7] SIN	SIUL — FlexPWM_0 SSCM DSPI_0	I/O — I/O — I	Slow	Medium	9	15
C[8]	PCR[40]	ALT0 ALT1 ALT2 ALT3 —	GPIO[40] CS1 — CS6 FAULT[2]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	91	130



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[9]	PCR[41]	ALT0 ALT1 ALT2 ALT3 —	GPIO[41] CS3 — X[3] FAULT[2]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — I/O I	Slow	Medium	84	123
C[10]	PCR[42]	ALT0 ALT1 ALT2 ALT3 —	GPIO[42] CS2 — A[3] FAULT[1]	SIUL DSPI_2 — FlexPWM_0 FlexPWM_0	I/O O — I/O I	Slow	Medium	78	111
C[11]	PCR[43]	ALT0 ALT1 ALT2 ALT3	GPIO[43] ETC[4] CS2 CS0	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O I/O	Slow	Medium	55	80
C[12]	PCR[44]	ALT0 ALT1 ALT2 ALT3	GPIO[44] ETC[5] CS3 CS1	SIUL eTimer_0 DSPI_2 DSPI_3	I/O I/O O O	Slow	Medium	56	82
C[13]	PCR[45]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[45] ETC[1] — — EXT_IN EXT_SYNC	SIUL eTimer_1 — — CTU_0 FlexPWM_0	I/O I/O — — I I	Slow	Medium	71	101
C[14]	PCR[46]	ALT0 ALT1 ALT2 ALT3	GPIO[46] ETC[2] EXT_TGR —	SIUL eTimer_1 CTU_0 —	I/O I/O O —	Slow	Medium	72	103



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
C[15]	PCR[47]	ALT0	GPIO[47]	SIUL	I/O	Slow	Symmetric	85	124
		ALT1	CA_TR_EN	FlexRay_0	O				
		ALT2	ETC[0]	eTimer_1	I/O				
		ALT3	A[1]	FlexPWM_0	I/O				
		—	EXT_IN	CTU_0	I				
—	EXT_SYNC	FlexPWM_0	I						
Port D (16-bit)									
D[0]	PCR[48]	ALT0	GPIO[48]	SIUL	I/O	Slow	Symmetric	86	125
		ALT1	CA_TX	FlexRay_0	O				
		ALT2	ETC[1]	eTimer_1	I/O				
		ALT3	B[1]	FlexPWM_0	I/O				
D[1]	PCR[49]	ALT0	GPIO[49]	SIUL	I/O	Slow	Medium	3	3
		ALT1	—	—	—				
		ALT2	ETC[2]	eTimer_1	I/O				
		ALT3	EXT_TRG	CTU_0	O				
		—	CA_RX	FlexRay_0	I				
D[2]	PCR[50]	ALT0	GPIO[50]	SIUL	I/O	Slow	Medium	97	140
		ALT1	—	—	—				
		ALT2	ETC[3]	eTimer_1	I/O				
		ALT3	X[3]	FlexPWM_0	I/O				
		—	CB_RX	FlexRay_0	I				
D[3]	PCR[51]	ALT0	GPIO[51]	SIUL	I/O	Slow	Symmetric	89	128
		ALT1	CB_TX	FlexRay_0	O				
		ALT2	ETC[4]	eTimer_1	I/O				
		ALT3	A[3]	FlexPWM_0	O				

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[4]	PCR[52]	ALT0 ALT1 ALT2 ALT3	GPIO[52] CB_TR_EN ETC[5] B[3]	SIUL FlexRay_0 eTimer_1 FlexPWM_0	I/O O I/O O	Slow	Symmetric	90	129
D[5]	PCR[53]	ALT0 ALT1 ALT2 ALT3	GPIO[53] CS3 F[0] SOUT	SIUL DSPI_0 FCU_0 DSPI_3	I/O O O O	Slow	Medium	22	33
D[6]	PCR[54]	ALT0 ALT1 ALT2 ALT3 —	GPIO[54] CS2 SCK — FAULT[1]	SIUL DSPI_0 DSPI_3 — FlexPWM_0	I/O O I/O — I	Slow	Medium	23	34
D[7]	PCR[55]	ALT0 ALT1 ALT2 ALT3 —	GPIO[55] CS3 F[1] CS4 SIN	SIUL DSPI_1 FCU_0 DSPI_0 DSPI_3	I/O O O O I	Slow	Medium	26	37
D[8]	PCR[56]	ALT0 ALT1 ALT2 ALT3 —	GPIO[56] CS2 — CS5 FAULT[3]	SIUL DSPI_1 — DSPI_0 FlexPWM_0	I/O O — O I	Slow	Medium	21	32
D[9]	PCR[57]	ALT0 ALT1 ALT2 ALT3	GPIO[57] X[0] TXD —	SIUL FlexPWM_0 LIN_1 —	I/O I/O O —	Slow	Medium	15	26

**Table 7. Pin muxing (continued)**

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
D[10]	PCR[58]	ALT0 ALT1 ALT2 ALT3	GPIO[58] A[0] CS0 —	SIUL FlexPWM_0 DSPI_3 —	I/O I/O I/O —	Slow	Medium	53	76
D[11]	PCR[59]	ALT0 ALT1 ALT2 ALT3	GPIO[59] B[0] CS1 SCK	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O I/O O I/O	Slow	Medium	54	78
D[12]	PCR[60]	ALT0 ALT1 ALT2 ALT3 —	GPIO[60] X[1] — — RXD	SIUL FlexPWM_0 — — LIN_1	I/O I/O — — I	Slow	Medium	70	99
D[13]	PCR[61]	ALT0 ALT1 ALT2 ALT3	GPIO[61] A[1] CS2 SOUT	SIUL FlexPWM_0 DSPI_3 DSPI_3	I/O I/O O O	Slow	Medium	67	95
D[14]	PCR[62]	ALT0 ALT1 ALT2 ALT3 —	GPIO[62] B[1] CS3 — SIN	SIUL FlexPWM_0 DSPI_3 — DSPI_3	I/O I/O O — I	Slow	Medium	73	105
D[15]	PCR[63]	ALT0 ALT1 ALT2 ALT3 —	GPIO[63] — — — AN[4]	SIUL — — — ADC_1	— — — — —	—	—	41	58



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port E(16-bit)									
E[0]	PCR[64]	ALT0 ALT1 ALT2 ALT3 —	GPIO[64] — — — AN[5]	SIUL — — — ADC_1	Input only	—	—	46	68
E[1]	PCR[65]	ALT0 ALT1 ALT2 ALT3 —	GPIO[65] — — — AN[4]	SIUL — — — ADC_0	Input only	—	—	27	39
E[2]	PCR[66]	ALT0 ALT1 ALT2 ALT3 —	GPIO[66] — — — AN[5]	SIUL — — — ADC_0	Input only	—	—	32	49
E[3]	PCR[67]	ALT0 ALT1 ALT2 ALT3 —	GPIO[67] — — — AN[6]	SIUL — — — ADC_0	Input only	—	—	—	40
E[4]	PCR[68]	ALT0 ALT1 ALT2 ALT3 —	GPIO[68] — — — AN[7]	SIUL — — — ADC_0	Input only	—	—	—	42

**Table 7. Pin muxing (continued)**

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[5]	PCR[69]	ALT0 ALT1 ALT2 ALT3 —	GPIO[69] — — — AN[8]	SIUL — — — ADC_0	Input only	—	—	—	44
E[6]	PCR[70]	ALT0 ALT1 ALT2 ALT3 —	GPIO[70] — — — AN[9]	SIUL — — — ADC_0	Input only	—	—	—	46
E[7]	PCR[71]	ALT0 ALT1 ALT2 ALT3 —	GPIO[71] — — — AN[10]	SIUL — — — ADC_0	Input only	—	—	—	48
E[8]	PCR[72]	ALT0 ALT1 ALT2 ALT3 —	GPIO[72] — — — AN[6]	SIUL — — — ADC_1	Input only	—	—	—	59
E[9]	PCR[73]	ALT0 ALT1 ALT2 ALT3 —	GPIO[73] — — — AN[7]	SIUL — — — ADC_1	Input only	—	—	—	61

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[10]	PCR[74]	ALT0 ALT1 ALT2 ALT3 —	GPIO[74] — — — AN[8]	SIUL — — — ADC_1	Input only	—	—	—	63
E[11]	PCR[75]	ALT0 ALT1 ALT2 ALT3 —	GPIO[75] — — — AN[9]	SIUL — — — ADC_1	Input only	—	—	—	65
E[12]	PCR[76]	ALT0 ALT1 ALT2 ALT3 —	GPIO[76] — — — AN[10]	SIUL — — — ADC_1	Input only	—	—	—	67
E[13]	PCR[77]	ALT0 ALT1 ALT2 ALT3 —	GPIO[77] SCK — — EIRQ[25]	SIUL DSPI_3 — — SIUL	I/O I/O — — I	Slow	Medium	—	117
E[14]	PCR[78]	ALT0 ALT1 ALT2 ALT3 —	GPIO[78] SOUT — — EIRQ[26]	SIUL DSPI_3 — — SIUL	I/O O — — I	Slow	Medium	—	119



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
E[15]	PCR[79]	ALT0	GPIO[79]	SIUL	I/O	Slow	Medium	—	121
		ALT1	—	—	—				
		ALT2	—	—	—				
		ALT3	—	—	—				
		—	SIN	DSPI_3	I				
—	EIRQ[27]	SIUL	I						
Port F (16-bit)									
F[0]	PCR[80]	ALT0	GPIO[80]	SIUL	I/O	Slow	Medium	—	133
		ALT1	DBG0	FlexRay_0	O				
		ALT2	CS3	DSPI_3	O				
		ALT3	—	—	—				
		—	EIRQ[28]	SIUL	I				
F[1]	PCR[81]	ALT0	GPIO[81]	SIUL	I/O	Slow	Medium	—	135
		ALT1	DBG1	FlexRay_0	O				
		ALT2	CS2	DSPI_3	O				
		ALT3	—	—	—				
		—	EIRQ[29]	SIUL	I				
F[2]	PCR[82]	ALT0	GPIO[82]	SIUL	I/O	Slow	Medium	—	137
		ALT1	DBG2	FlexRay_0	O				
		ALT2	CS1	DSPI_3	O				
		ALT3	—	—	—				
		—	—	—	—				
F[3]	PCR[83]	ALT0	GPIO[83]	SIUL	I/O	Slow	Medium	—	139
		ALT1	DBG3	FlexRay_0	O				
		ALT2	CS0	DSPI_3	I/O				
		ALT3	—	—	—				
		—	—	—	—				


Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[4]	PCR[84]	ALT0 ALT1 ALT2 ALT3	GPIO[84] MDO[3] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	4
F[5]	PCR[85]	ALT0 ALT1 ALT2 ALT3	GPIO[85] MDO[2] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	5
F[6]	PCR[86]	ALT0 ALT1 ALT2 ALT3	GPIO[86] MDO[1] — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	8
F[7]	PCR[87]	ALT0 ALT1 ALT2 ALT3	GPIO[87] MCKO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	19
F[8]	PCR[88]	ALT0 ALT1 ALT2 ALT3	GPIO[88] MSEO1 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	20
F[9]	PCR[89]	ALT0 ALT1 ALT2 ALT3	GPIO[89] MSEO0 — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	23

**Table 7. Pin muxing (continued)**

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
F[10]	PCR[90]	ALT0 ALT1 ALT2 ALT3	GPIO[90] EVTO — —	SIUL NEXUS_0 — —	I/O O — —	Slow	Fast	—	24
F[11]	PCR[91]	ALT0 ALT1 ALT2 ALT3 —	GPIO[91] — — — EVTI	SIUL — — — NEXUS_0	I/O — — — I	Slow	Medium	—	25
F[12]	PCR[92]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[3] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	106
F[13]	PCR[93]	ALT0 ALT1 ALT2 ALT3	GPIO[92] ETC[4] — —	SIUL eTimer_1 — —	I/O I/O — —	Slow	Medium	—	112
F[14]	PCR[94]	ALT0 ALT1 ALT2 ALT3	GPIO[94] TXD — —	SIUL LIN_1 — —	I/O O — —	Slow	Medium	—	115
F[15]	PCR[95]	ALT0 ALT1 ALT2 ALT3 —	GPIO[95] — — — RXD	SIUL — — — LIN_1	I/O — — — I	Slow	Medium	—	113

Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
Port G (12-bit)									
G[0]	PCR[96]	ALT0 ALT1 ALT2 ALT3 —	GPIO[96] F[0] — — EIRQ[30]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	38
G[1]	PCR[97]	ALT0 ALT1 ALT2 ALT3 —	GPIO[97] F[1] — — EIRQ[31]	SIUL FCU_0 — — SIUL	I/O O — — I	Slow	Medium	—	141
G[2]	PCR[98]	ALT0 ALT1 ALT2 ALT3	GPIO[98] X[2] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	102
G[3]	PCR[99]	ALT0 ALT1 ALT2 ALT3	GPIO[99] A[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	104
G[4]	PCR[100]	ALT0 ALT1 ALT2 ALT3	GPIO[100] B[2] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	100
G[5]	PCR[101]	ALT0 ALT1 ALT2 ALT3	GPIO[101] X[3] — —	SIUL FlexPWM_0 — —	I/O I/O — —	Slow	Medium	—	85



Table 7. Pin muxing (continued)

Port pin	Pad configuration register (PCR)	Alternate function ⁽¹⁾⁽²⁾	Functions	Peripheral ⁽³⁾	I/O direction ⁽⁴⁾	Pad speed ⁽⁵⁾		Pin No.	
						SRC = 0	SRC = 1	100-pin	144-pin
G[6]	PCR[102]	ALT0 ALT1 ALT2 ALT3	GPIO[102] A[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	98
G[7]	PCR[103]	ALT0 ALT1 ALT2 ALT3	GPIO[103] B[3] — —	SIUL FlexPWM_0 — —	I/O O — —	Slow	Medium	—	83
G[8]	PCR[104]	ALT0 ALT1 ALT2 ALT3 —	GPIO[104] — — — FAULT[0]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	81
G[9]	PCR[105]	ALT0 ALT1 ALT2 ALT3 —	GPIO[105] — — — FAULT[1]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	79
G[10]	PCR[106]	ALT0 ALT1 ALT2 ALT3 —	GPIO[106] — — — FAULT[2]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	77
G[11]	PCR[107]	ALT0 ALT1 ALT2 ALT3 —	GPIO[107] — — — FAULT[3]	SIUL — — — FlexPWM_0	I/O — — — I	Slow	Medium	—	75

1. ALTO is the primary (default) function for each port after reset.
2. Alternate functions are chosen by setting the values of the PCR[PA] bitfields inside the SIU module. PCR[PA] = 00 → ALT0; PCR[PA] = 01 → ALT1; PCR[PA] = 10 → ALT2; PCR[PA] = 11 → ALT3. This is intended to select the output functions; to use one of the input-only functions, the PCR[IBE] bit must be written to '1', regardless of the values selected in the PCR[PA] bitfields. For this reason, the value corresponding to an input only function is reported as "—".
3. Module included on the MCU.
4. Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMI[PADSELx] bitfields inside the SIUL module.
5. Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
6. Weak pull down during reset.

3 Electrical characteristics

3.1 Introduction

This section contains device electrical characteristics as well as temperature and power considerations.

This microcontroller contains input protection against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level (V_{DD} or V_{SS}). This can be done by the internal pull-up or pull-down resistors, which are provided by the device for most general purpose pins.

The following tables provide the device characteristics and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

Caution: All of the following parameter values can vary depending on the application and must be confirmed during silicon characterization or silicon reliability trial.

3.2 Parameter classification

The electrical parameters are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 8](#) are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute maximum ratings

Table 9. Absolute maximum ratings⁽¹⁾

Symbol		Parameter	Conditions	Value		Unit
				Min	Max ⁽²⁾	
V _{SS}	SR	Device ground	—	0	0	V
V _{DD_HV_IOx} ⁽³⁾	SR	3.3 V / 5.0 V input/output supply voltage with respect to ground (V _{SS})	—	-0.3	6.0	V
V _{SS_HV_IOx}	SR	Input/output ground voltage with respect to ground (V _{SS})	—	-0.1	0.1	V
V _{DD_HV_FL}	SR	3.3 V / 5.0 V code and data flash supply voltage with respect to ground (V _{SS})	—	-0.3	6.0	V
			Relative to V _{DD_HV_IOx}		V _{DD_HV_IOx} + 0.3	
V _{SS_HV_FL}	SR	Code and data flash ground with respect to ground (V _{SS})	—	-0.1	0.1	V
V _{DD_HV_OSC}	SR	3.3 V / 5.0 V crystal oscillator amplifier supply voltage with respect to ground (V _{SS})	—	-0.3	6.0	V
			Relative to V _{DD_HV_IOx}		V _{DD_HV_IOx} + 0.3	
V _{SS_HV_OSC}	SR	3.3 V / 5.0 V crystal oscillator amplifier reference voltage with respect to ground (V _{SS})	—	-0.1	0.1	V
V _{DD_HV_REG}	SR	3.3 V / 5.0 V voltage regulator supply voltage with respect to ground (V _{SS})	—	-0.3	6.0	V
			Relative to V _{DD_HV_IOx}		V _{DD_HV_IOx} + 0.3	
V _{DD_HV_ADC0} ⁽⁴⁾	SR	3.3 V / 5.0 V ADC_0 supply and high reference voltage with respect to ground (V _{SS})	V _{DD_HV_REG} < 2.7 V	-0.3	V _{DD_HV_REG} + 0.3	V
			V _{DD_HV_REG} > 2.7 V		6.0	
V _{SS_HV_ADC0}	SR	ADC_0 ground and low reference voltage with respect to ground (V _{SS})	—	-0.1	0.1	V
V _{DD_HV_ADC1} ⁽⁴⁾	SR	3.3 V / 5.0 V ADC_0 supply and high reference voltage with respect to ground (V _{SS})	V _{DD_HV_REG} < 2.7 V	-0.3	V _{DD_HV_REG} + 0.3	V
			V _{DD_HV_REG} > 2.7 V		6.0	
V _{SS_HV_ADC1}	SR	ADC_1 ground and low reference voltage with respect to ground (V _{SS})	—	-0.1	0.1	V
TV _{DD}	SR	Slope characteristics on all V _{DD} during power up ⁽⁵⁾ with respect to ground (V _{SS})	—	0.5	—	V/μs
			—	—	3	V/s

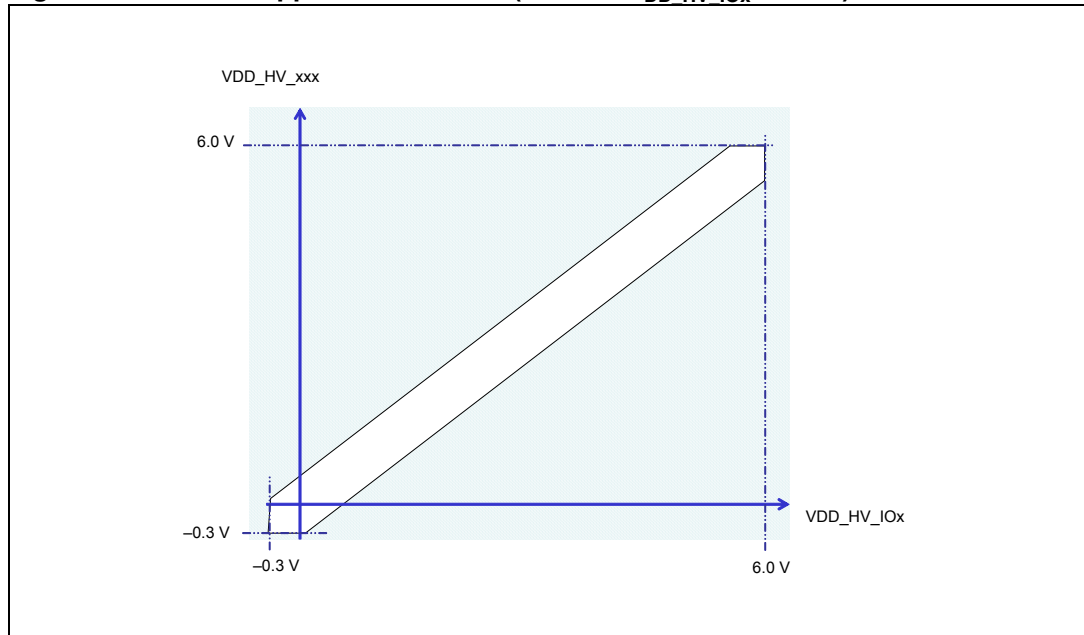
Table 9. Absolute maximum ratings⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Value		Unit	
			Min	Max ⁽²⁾		
V _{IN}	SR	Voltage on any pin with respect to ground (V _{SS_HV_IOx}) with respect to ground (V _{SS})	—	-0.3	6.0	V
					Relative to V _{DD_HV_IOx}	
I _{INJPAD}	SR	Injected input current on any pin during overload condition	—	-10	10	mA
I _{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	mA
I _{VDD_LV}	SR	Low voltage static current sink through V _{DD_LV}	—	—	155	mA
T _{STG}	SR	Storage temperature	—	-55	150	°C
T _J	SR	Junction temperature under bias	—	-40	150	°C

1. Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
3. The difference between each couple of voltage supplies must be less than 300 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 300 \text{ mV}$.
4. The difference between ADC voltage supplies must be less than 300 mV, $|V_{DD_HV_ADC1} - V_{DD_HV_ADC0}| < 300 \text{ mV}$.
5. Guaranteed by device validation

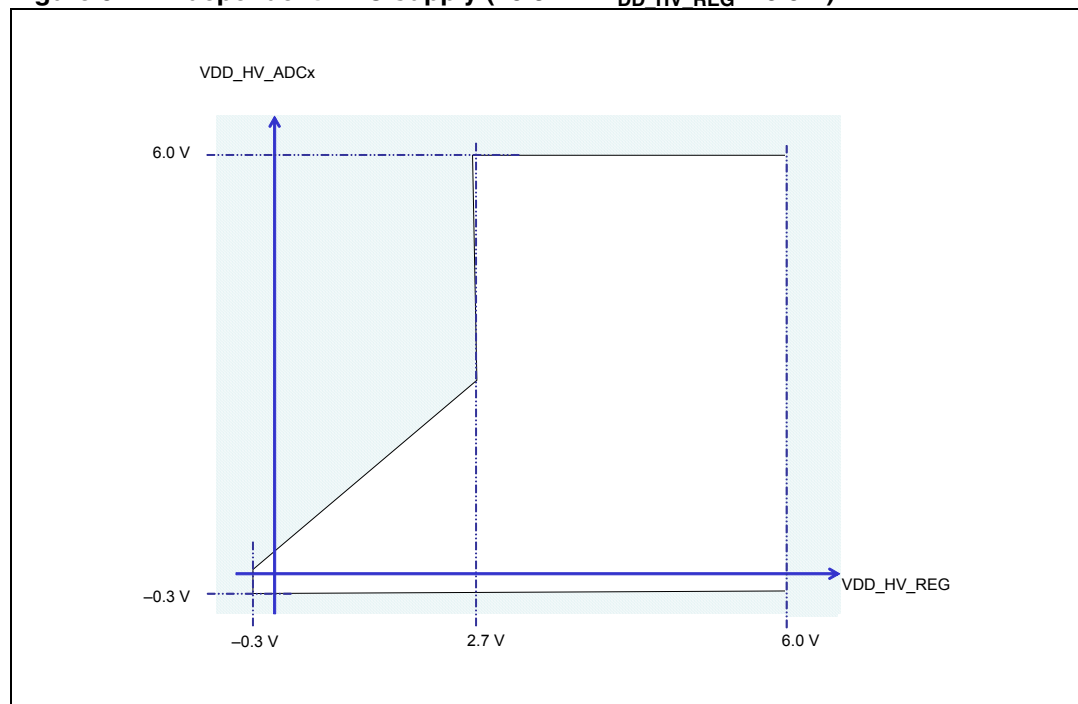
Figure 5 shows the constraints of the different power supplies.

Figure 5. Power supplies constraints ($-0.3 \text{ V} \leq V_{DD_HV_IOx} \leq 6.0 \text{ V}$)



The SPC560P44Lx, SPC560P50Lx supply architecture allows of having ADC supply managed independently from standard V_{DD_HV} supply. *Figure 6* shows the constraints of the ADC power supply.

Figure 6. Independent ADC supply ($-0.3\text{ V} \leq V_{DD_HV_REG} \leq 6.0\text{ V}$)



3.4 Recommended operating conditions

Table 10. Recommended operating conditions (5.0 V)

Symbol	Parameter	Conditions	Value		Unit	
			Min	Max ⁽¹⁾		
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD_HV_IOx}^{(2)}$	SR	5.0 V input/output supply voltage	—	4.5	5.5	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FL}$	SR	5.0 V code and data flash supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{SS_HV_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	5.0 V crystal oscillator amplifier supply voltage	—	4.5	5.5	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	

Table 10. Recommended operating conditions (5.0 V) (continued)

Symbol	Parameter	Conditions	Value		Unit	
			Min	Max ⁽¹⁾		
V _{SS_HV_OSC}	SR	5.0 V crystal oscillator amplifier reference voltage	—	0	0	V
V _{DD_HV_REG}	SR	5.0 V voltage regulator supply voltage	—	4.5	5.5	V
		Relative to V _{DD_HV_IOx}	V _{DD_HV_IOx} - 0.1	V _{DD_HV_IOx} + 0.1		
V _{DD_HV_ADC0} ⁽³⁾	SR	5.0 V ADC_0 supply and high reference voltage	—	4.5	5.5	V
		Relative to V _{DD_HV_REG}	V _{DD_HV_REG} - 0.1	—		
V _{SS_HV_ADC0}	SR	ADC_0 ground and low reference voltage	—	0	0	V
V _{DD_HV_ADC1} ⁽³⁾	SR	5.0 V ADC_1 supply and high reference voltage	—	4.5	5.5	V
		Relative to V _{DD_HV_REG}	V _{DD_HV_REG} - 0.1	—		
V _{SS_HV_ADC1}	SR	ADC_1 ground and low reference voltage	—	0	0	V
V _{DD_LV_REGCOR} ⁽⁴⁾⁽⁵⁾	CC	Internal supply voltage	—	—	—	V
V _{SS_LV_REGCOR} ⁽⁴⁾	SR	Internal reference voltage	—	0	0	V
V _{DD_LV_CORx} ⁽⁴⁾⁽⁵⁾	CC	Internal supply voltage	—	—	—	V
V _{SS_LV_CORx} ⁽⁴⁾	SR	Internal reference voltage	—	0	0	V
T _A	SR	Ambient temperature under bias	f _{CPU} = 64 MHz	-40	105	°C
			f _{CPU} = 60 MHz	-40	125	

1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.
2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100$ mV.
3. The difference between ADC voltage supplies must be less than 100 mV, $|V_{DD_HV_ADC1} - V_{DD_HV_ADC0}| < 100$ mV.
4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds (V_{SS_LV_xxx}) must be shorted to high voltage grounds (V_{SS_HV_xxx}) and the low voltage supply pins (V_{DD_LV_xxx}) must be connected to the external ballast emitter.
5. The low voltage supplies (V_{DD_LV_xxx}) are not all independent.

V_{DD_LV_COR1} and V_{DD_LV_COR2} are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, V_{SS_LV_COR1} and V_{SS_LV_COR2} are internally shorted.

V_{DD_LV_REGCOR} and V_{DD_LV_REGCORx} are physically shorted internally, as are V_{SS_LV_REGCOR} and V_{SS_LV_CORx}.

Table 11. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max ⁽¹⁾	
V_{SS}	SR	Device ground	—	0	0	V
$V_{DD_HV_IOx}^{(2)}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FL}$	SR	3.3 V code and data flash supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{SS_HV_FL}$	SR	Code and data flash ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
			Relative to $V_{DD_HV_IOx}$	$V_{DD_HV_IOx} - 0.1$	$V_{DD_HV_IOx} + 0.1$	
$V_{DD_HV_ADC0}^{(3)}$	SR	3.3 V ADC_0 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG} - 0.1$	5.5	
$V_{SS_HV_ADC0}$	SR	ADC_0 ground and low reference voltage	—	0	0	V
$V_{DD_HV_ADC1}^{(3)}$	SR	3.3 V ADC_1 supply and high reference voltage	—	3.0	5.5	V
			Relative to $V_{DD_HV_REG}$	$V_{DD_HV_REG} - 0.1$	5.5	
$V_{SS_HV_ADC1}$	SR	ADC_1 ground and low reference voltage	—	0	0	V
$V_{DD_LV_REGCOR}^{(4)(5)}$	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_REGCOR}^{(4)}$	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}^{(4)(5)}$	CC	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}^{(4)}$	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} = 64 \text{ MHz}$	-40	105	°C
			$f_{CPU} = 60 \text{ MHz}$	-40	125	

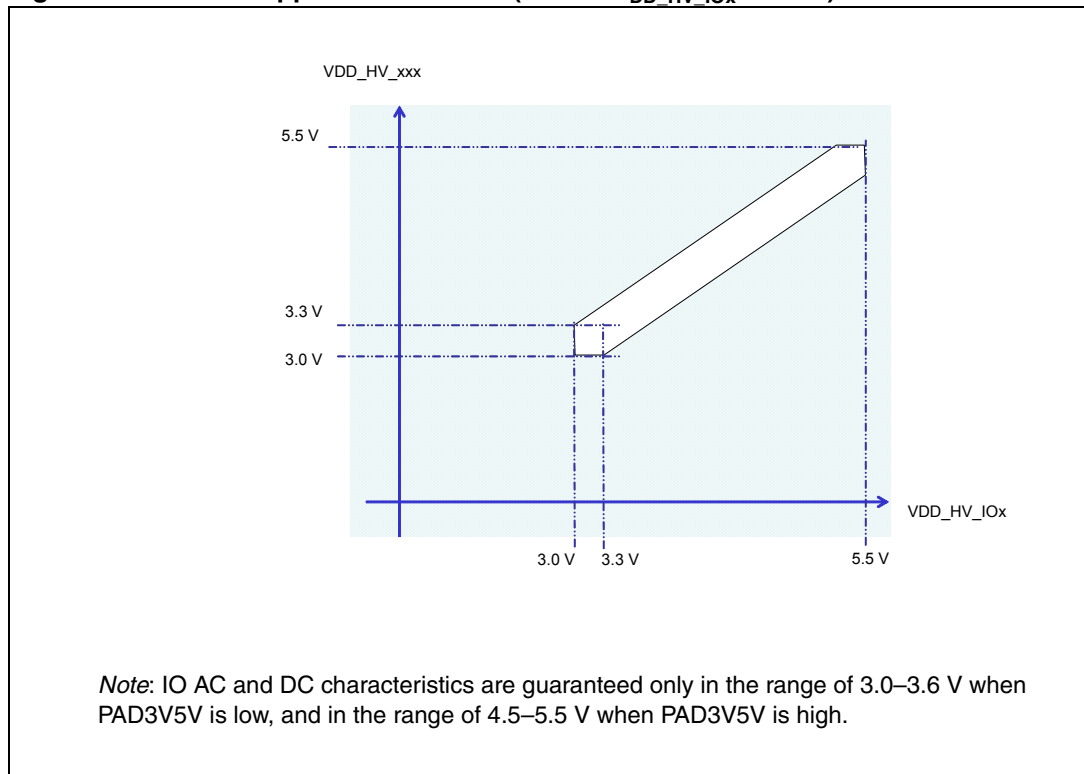
1. Parametric figures can be out of specification when voltage drops below 4.5 V, however, guaranteeing the full functionality. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_IOy} - V_{DD_HV_IOx}| < 100 \text{ mV}$.

3. The difference between each couple of voltage supplies must be less than 100 mV, $|V_{DD_HV_ADC1} - V_{DD_HV_ADC0}| < 100$ mV. As long as that condition is met, ADC_0 and ADC_1 can be operated at 5 V with the rest of the device operating at 3.3 V.
 4. To be connected to emitter of external NPN. Low voltage supplies are not under user control—they are produced by an on-chip voltage regulator—but for the device to function properly the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter.
 5. The low voltage supplies ($V_{DD_LV_xxx}$) are not all independent.
- $V_{DD_LV_COR1}$ and $V_{DD_LV_COR2}$ are shorted internally via double bonding connections with lines that provide the low voltage supply to the data flash module. Similarly, $V_{SS_LV_COR1}$ and $V_{SS_LV_COR2}$ are internally shorted.
- $V_{DD_LV_REGCOR}$ and $V_{DD_LV_REGCORx}$ are physically shorted internally, as are $V_{SS_LV_REGCOR}$ and $V_{SS_LV_CORx}$.

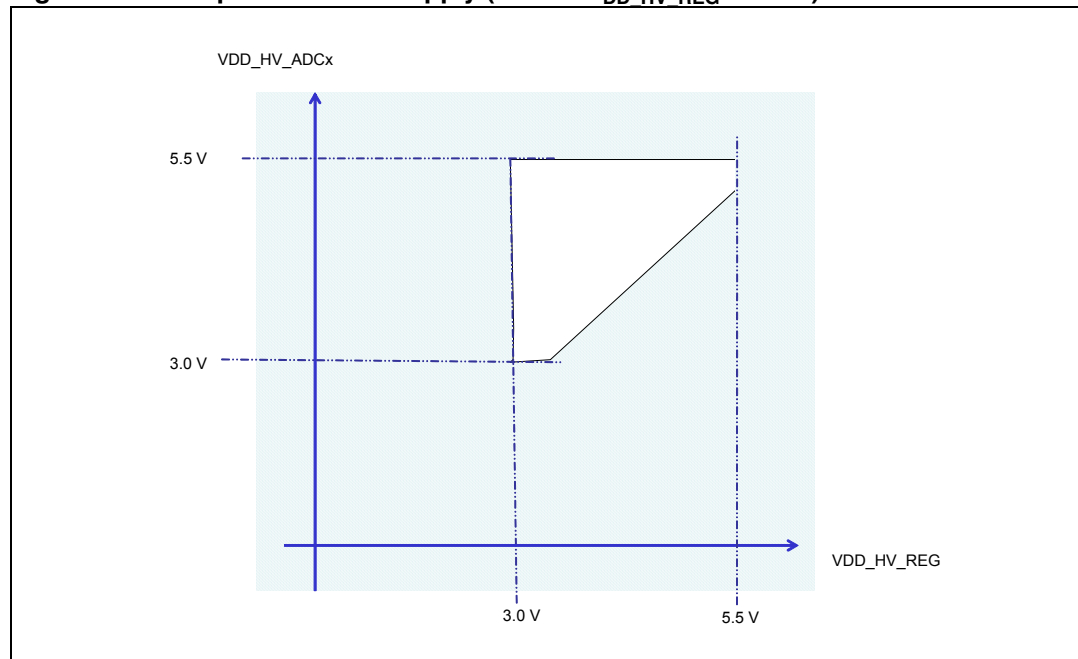
Figure 7 shows the constraints of the different power supplies.

Figure 7. Power supplies constraints ($3.0\text{ V} \leq V_{DD_HV_IOx} \leq 5.5\text{ V}$)



The SPC560P44Lx, SPC560P50Lx supply architecture allows the ADC supply to be managed independently from the standard V_{DD_HV} supply. Figure 8 shows the constraints of the ADC power supply.

Figure 8. Independent ADC supply ($3.0\text{ V} \leq V_{DD_HV_REG} \leq 5.5\text{ V}$)



3.5 Thermal characteristics

3.5.1 Package thermal characteristics

Table 12. Thermal characteristics for 144-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
R _{θJA}	Thermal resistance junction-to-ambient, natural convection ⁽¹⁾	Single layer board—1s	54.2	°C/W
		Four layer board—2s2p	44.4	°C/W
R _{θJB}	Thermal resistance junction-to-board ⁽²⁾	Four layer board—2s2p	29.9	°C/W
R _{θJCtop}	Thermal resistance junction-to-case (top) ⁽³⁾	Single layer board—1s	9.3	°C/W
Ψ _{JB}	Junction-to-board, natural convection ⁽⁴⁾	Operating conditions	30.2	°C/W
Ψ _{JC}	Junction-to-case, natural convection ⁽⁵⁾	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

Table 13. Thermal characteristics for 100-pin LQFP

Symbol	Parameter	Conditions	Typical value	Unit
R _{θJA}	Thermal resistance junction-to-ambient, natural convection ⁽¹⁾	Single layer board—1s	47.3	°C/W
		Four layer board—2s2p	35.3	°C/W
R _{θJB}	Thermal resistance junction-to-board ⁽²⁾	Four layer board—2s2p	19.1	°C/W
R _{θJctop}	Thermal resistance junction-to-case (top) ⁽³⁾	Single layer board—1s	9.7	°C/W
Ψ _{JB}	Junction-to-board, natural convection ⁽⁴⁾	Operating conditions	19.1	°C/W
Ψ _{JC}	Junction-to-case, natural convection ⁽⁵⁾	Operating conditions	0.8	°C/W

1. Junction-to-ambient thermal resistance determined per JEDEC JESD51-7. Thermal test board meets JEDEC specification for this package.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Thermal characterization parameter indicating the temperature difference between the board and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.
5. Thermal characterization parameter indicating the temperature difference between the case and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JC.

3.5.2 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from [Equation 1](#):

$$\text{Equation 1} \quad T_J = T_A + (R_{\theta JA} * P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- R_{θJA} = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in [Equation 2](#) as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$\text{Equation 2} \quad R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- R_{θJA} = junction to ambient thermal resistance (°C/W)
- R_{θJC} = junction to case thermal resistance (°C/W)
- R_{θCA} = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using [Equation 3](#):

Equation 3 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 U.S.A.
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.6 Electromagnetic interference (EMI) characteristics

Table 14. EMI testing specifications

Symbol	Parameter	Conditions	Clocks	Frequency	Level (Max)	Unit
V_{EME}	Radiated emissions	Device configuration, test conditions and EM testing per standard IEC61967-2	f_{OSC} 8 MHz f_{CPU} 64 MHz No PLL frequency modulation	150 kHz–150 MHz	16	dB μ V
				150–1000 MHz	15	
				IEC Level	M	
		Supply voltage = 5 V DC Ambient temperature = 25 °C Worst-case orientation	f_{OSC} 8 MHz f_{CPU} 64 MHz 1% PLL frequency modulation	150 kHz–150 MHz	15	dB μ V
				150–1000 MHz	14	
				IEC Level	M	

3.7 Electrostatic discharge (ESD) characteristics

Table 15. ESD ratings⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	SR Electrostatic discharge (Human Body Model)	—	2000	V
$V_{ESD(CDM)}$	SR Electrostatic discharge (Charged Device Model)	—	750 (corners)	V
			500 (other)	

- All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
- A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3.8 Power management electrical characteristics

3.8.1 Voltage regulator electrical characteristics

The internal voltage regulator requires an external NPN (BCP56, BCP68, BCX68 or BC817) ballast to be connected as shown in [Figure 9](#) and [Figure 10](#). Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Note: The voltage regulator output cannot be used to drive external circuits. Output pins are to be used only for decoupling capacitance.

$V_{DD_LV_COR}$ must be generated using internal regulator and external NPN transistor. It is not possible to provide $V_{DD_LV_COR}$ through external regulator.

For the SPC560P44Lx, SPC560P50Lx microcontroller, 10 μ F should be placed between each of the three $V_{DD_LV_CORx}/V_{SS_LV_CORx}$ supply pairs and also between the $V_{DD_LV_REGCOR}/V_{SS_LV_REGCOR}$ pair. Additionally, 40 μ F should be placed between the $V_{DD_HV_REG}/V_{SS_HV_REG}$ pins.

$V_{DD} = 3.0\text{ V to }3.6\text{ V} / 4.5\text{ V to }5.5\text{ V}$, $T_A = -40\text{ to }125\text{ °C}$, unless otherwise specified.

Figure 9. Configuration without resistor on base

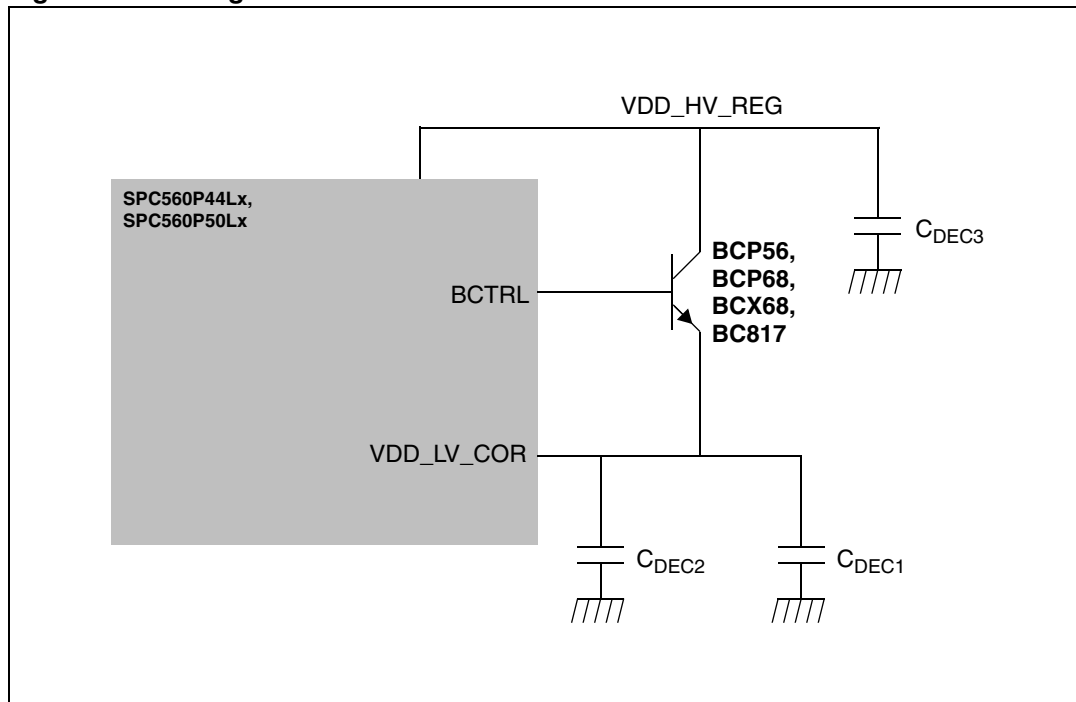


Table 16. Voltage regulator electrical characteristics (configuration without resistor on base)

Symbol	C	Parameter	Conditions	Value			Unit	
				Min	Typ	Max		
$V_{DD_LV_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	Post-trimming	1.15	—	1.32	V
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances	40	56	—	μ F
R_{REG}	SR	—	Resulting ESR of all four C_{DEC1}	Absolute maximum value between 100 kHz and 10 MHz	—	—	45	m Ω
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances of 100 nF each	400	—	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	—	40	—	—	μ F

Figure 10. Configuration with resistor on base

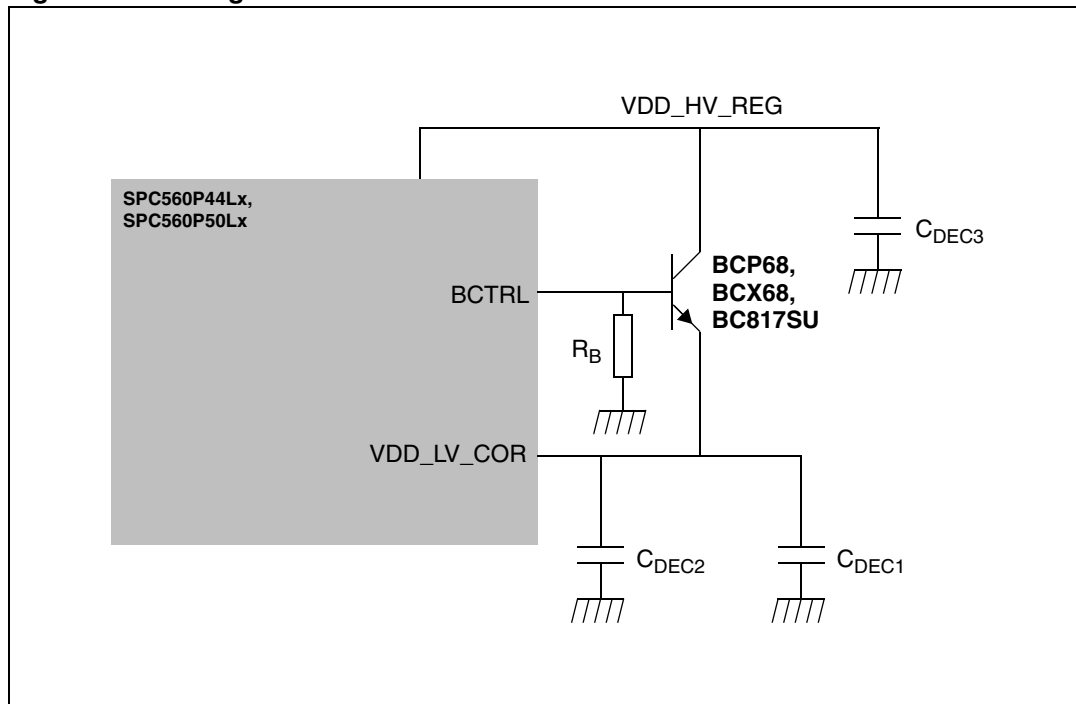


Table 17. Voltage regulator electrical characteristics (configuration with resistor on base)

Symbol	C	Parameter	Conditions	Value			Unit	
				Min	Typ	Max		
$V_{DD_LV_REGCOR}$	CC	P	Output voltage under maximum load run supply current configuration	1.15	—	1.32	V	
R_B	SR	—	External resistance on bipolar junction transistor (BJT) base	18	—	22	k Ω	
C_{DEC1}	SR	—	External decoupling/stability ceramic capacitor	Bipolar BCP68 or BCX68 or BC817. Three capacitances of 10 μ F	19.5	30	—	μ F
				Bipolar BC817. One capacitance of 22 μ F	14.3	22	—	μ F
R_{REG}	SR	—	Resulting ESR of either one or all three C_{DEC1}	—	—	45	m Ω	
C_{DEC2}	SR	—	External decoupling/stability ceramic capacitor	4 capacitances of 440 nF each	1200	1760	—	nF
C_{DEC3}	SR	—	External decoupling/stability ceramic capacitor on VDD_HV_REG	2 capacitances of 10 μ F each	2×10	—	—	μ F

3.8.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V_{DD} and the V_{DD_LV} voltage while device is supplied:

- POR monitors V_{DD} during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V_{DD} to ensure device reset below minimum functional supply
- LVDHV5 monitors V_{DD} when application uses device in the $5.0V \pm 10\%$ range
- LVDLVCOR monitors low voltage digital power domain

Table 18. Low voltage monitor electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value		Unit
				Min	Max	
V_{PORH}	T	Power-on reset threshold	—	1.5	2.7	V
V_{PORUP}	P	Supply for functional POR module	$T_A = 25\text{ }^\circ\text{C}$	1.0	—	V
$V_{REGLVDMOK_H}$	P	Regulator low voltage detector high threshold	—	—	2.95	V
$V_{REGLVDMOK_L}$	P	Regulator low voltage detector low threshold	—	2.6	—	V
$V_{FLLVDMOK_H}$	P	Flash low voltage detector high threshold	—	—	2.95	V
$V_{FLLVDMOK_L}$	P	Flash low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDMOK_H}$	P	I/O low voltage detector high threshold	—	—	2.95	V
$V_{IOLVDMOK_L}$	P	I/O low voltage detector low threshold	—	2.6	—	V
$V_{IOLVDM5OK_H}$	P	I/O 5V low voltage detector high threshold	—	—	4.4	V
$V_{IOLVDM5OK_L}$	P	I/O 5V low voltage detector low threshold	—	3.8	—	V
$V_{MLVDDOK_H}$	P	Digital supply low voltage detector high	—	—	1.145	V
$V_{MLVDDOK_L}$	P	Digital supply low voltage detector low	—	1.08	—	V

1. $V_{DD} = 3.3V \pm 10\% / 5.0V \pm 10\%$, $T_A = -40\text{ }^\circ\text{C}$ to $T_{A\text{ MAX}}$, unless otherwise specified

3.9 Power up/down sequencing

To prevent an overstress event or a malfunction within and outside the device, the SPC560P44Lx, SPC560P50Lx implements the following sequence to ensure each module is started only when all conditions for switching it ON are available:

- A POWER_ON module working on voltage regulator supply controls the correct start-up of the regulator. This is a key module ensuring safe configuration for all voltage regulator functionality when supply is below 1.5V. Associated POWER_ON (or POR) signal is active low.
- Several low voltage detectors, working on voltage regulator supply monitor the voltage of the critical modules (voltage regulator, I/Os, flash memory and low voltage domain). LVDs are gated low when POWER_ON is active.
- A POWER_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, flash

memory and RC16 oscillator needed during power-up phase and reset phase. When POWER_OK is low the associated module are set into a safe state.

Figure 11. Power-up typical sequence

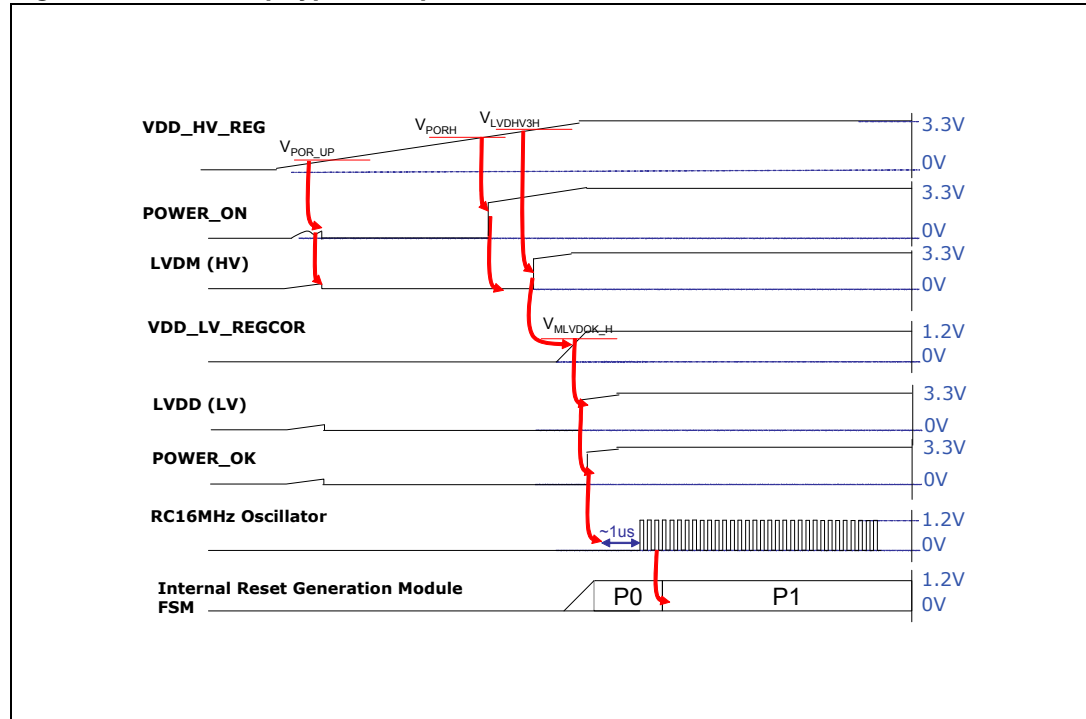


Figure 12. Power-down typical sequence

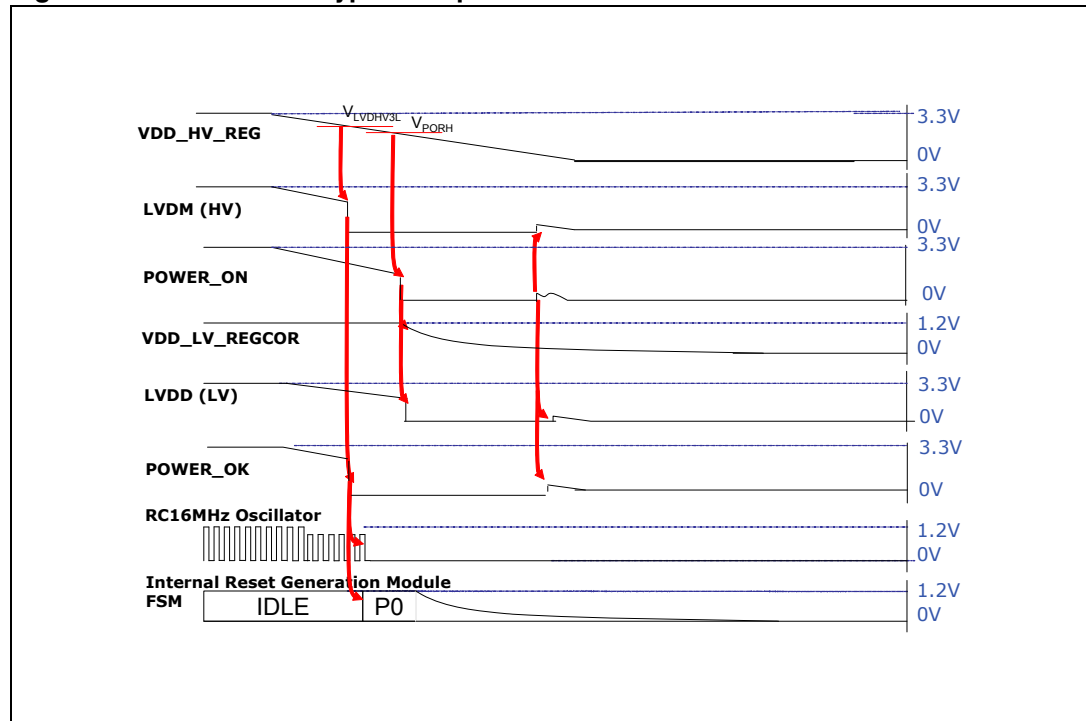
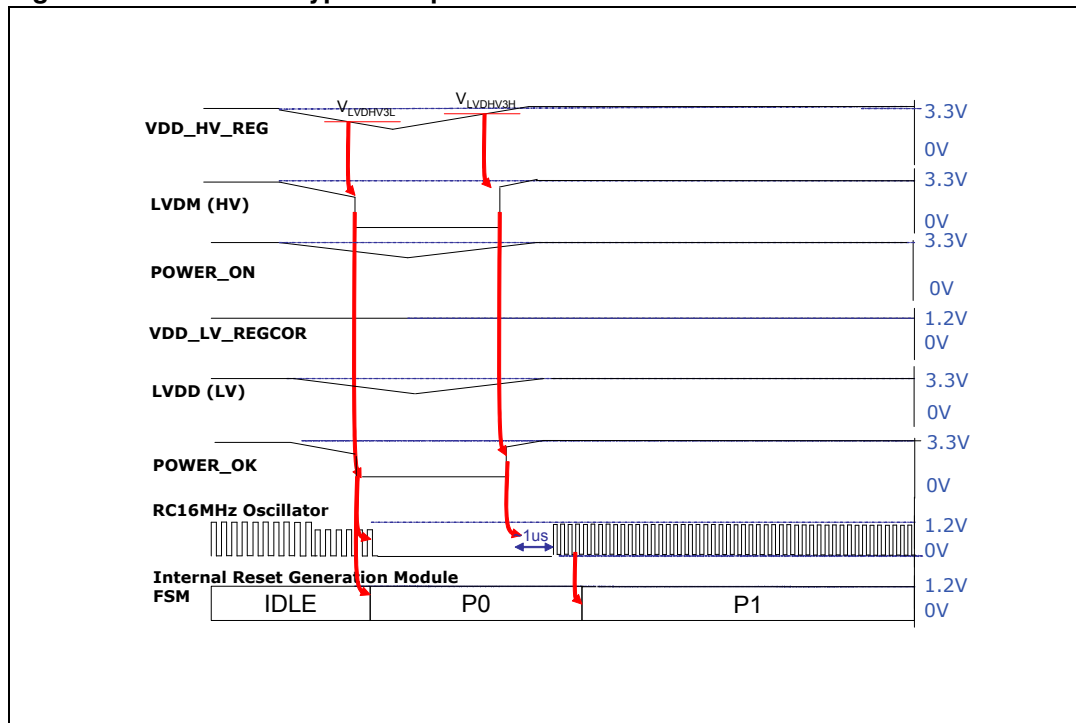


Figure 13. Brown-out typical sequence



3.10 DC electrical characteristics

3.10.1 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the non-volatile user options (NVUSRO) register.

For a detailed description of the NVUSRO register, please refer to the device reference manual.

NVUSRO[PAD3V5V] field description

The DC electrical characteristics are dependent on the PAD3V5V bit value. [Table 19](#) shows how NVUSRO[PAD3V5V] controls the device configuration.

Table 19. PAD3V5V field description

Value ⁽¹⁾	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

1. Default manufacturing value before flash initialization is '1' (3.3 V).

NVUSRO[OSCILLATOR_MARGIN] field description

The fast external crystal oscillator consumption is dependent on the OSCILLATOR_MARGIN bit value. [Table 20](#) shows how NVUSRO[OSCILLATOR_MARGIN] controls the device configuration.

Table 20. OSCILLATOR_MARGIN field description

Value ⁽¹⁾	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

1. Default manufacturing value before flash initialization is '1'.

3.10.2 DC electrical characteristics (5 V)

[Table 21](#) gives the DC electrical characteristics at 5 V ($4.5\text{ V} < V_{DD_HV_IOx} < 5.5\text{ V}$, NVUSRO[PAD3V5V] = 0); see [Figure 14](#).

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V _{IL}	D	Low level input voltage	—	-0.1 ⁽¹⁾	—	V
	P		—	—	0.35 V _{DD_HV_IOx}	V
V _{IH}	P	High level input voltage	—	0.65 V _{DD_HV_IOx}	—	V
	D		—	—	V _{DD_HV_IOx} + 0.1 ⁽¹⁾	V
V _{HYS}	T	Schmitt trigger hysteresis	—	0.1 V _{DD_HV_IOx}	—	V
V _{OL_S}	P	Slow, low level output voltage	I _{OL} = 3 mA	—	0.1 V _{DD_HV_IOx}	V
V _{OH_S}	P	Slow, high level output voltage	I _{OH} = -3 mA	0.8 V _{DD_HV_IOx}	—	V
V _{OL_M}	P	Medium, low level output voltage	I _{OL} = 3 mA	—	0.1 V _{DD_HV_IOx}	V
V _{OH_M}	P	Medium, high level output voltage	I _{OH} = -3 mA	0.8 V _{DD_HV_IOx}	—	V
V _{OL_F}	P	Fast, low level output voltage	I _{OL} = 3 mA	—	0.1 V _{DD_HV_IOx}	V
V _{OH_F}	P	Fast, high level output voltage	I _{OH} = -3 mA	0.8 V _{DD_HV_IOx}	—	V
V _{OL_SYM}	P	Symmetric, low level output voltage	I _{OL} = 3 mA	—	0.1 V _{DD_HV_IOx}	V
V _{OH_SYM}	P	Symmetric, high level output voltage	I _{OH} = -3 mA	0.8 V _{DD_HV_IOx}	—	V
I _{PU}	P	Equivalent pull-up current	V _{IN} = V _{IL}	-130	—	μA
			V _{IN} = V _{IH}	—	-10	
I _{PD}	P	Equivalent pull-down current	V _{IN} = V _{IL}	10	—	μA
			V _{IN} = V _{IH}	—	130	
I _{IL}	P	Input leakage current (all bidirectional ports)	T _A = -40 to 125 °C	-1	1	μA

Table 21. DC electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0) (continued)

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
I_{IL}	P	Input leakage current (all ADC input-only ports)	$T_A = -40$ to 125 °C	-0.5	0.5	μA
C_{IN}	D	Input capacitance	—	—	10	pF

1. "SR" parameter values must not exceed the absolute maximum ratings shown in [Table 9](#).

Table 22. Supply current (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Conditions	Value		Unit
				Typ	Max	
$I_{DD_LV_CORx}$	T	RUN—Maximum mode ⁽¹⁾	$V_{DD_LV_CORx}$ externally forced at 1.3 V	40 MHz	62	77
				64 MHz	71	88
		RUN—Typical mode ⁽²⁾		40 MHz	45	56
				64 MHz	52	65
	P	RUN—Maximum mode ⁽³⁾	$V_{DD_LV_CORx}$ externally forced at 1.3 V	64 MHz	60	75
		HALT mode ⁽⁴⁾	$V_{DD_LV_CORx}$ externally forced at 1.3 V	—	1.5	10
STOP mode ⁽⁵⁾		$V_{DD_LV_CORx}$ externally forced at 1.3 V	—	1	10	
I_{DD_FLASH}	T	Flash during read	$V_{DD_HV_FL}$ at 5.0 V	—	10	12
		Flash during erase operation on 1 flash module	$V_{DD_HV_FL}$ at 5.0 V	—	15	19
I_{DD_ADC}	T	ADC—Maximum mode ⁽¹⁾	$V_{DD_HV_ADC0}$ at 5.0 V $V_{DD_HV_ADC1}$ at 5.0 V $f_{ADC} = 16$ MHz	ADC_1	3.5	5
				ADC_0	3	4
		ADC—Typical mode ⁽²⁾		ADC_1	0.8	1
				ADC_0	0.005	0.006
I_{DD_OSC}	T	Oscillator	V_{DD_OSC} at 5.0 V	8 MHz	2.6	3.2

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode configurations: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP "P" mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.3 DC electrical characteristics (3.3 V)

Table 23 gives the DC electrical characteristics at 3.3 V ($3.0\text{ V} < V_{DD_HV_IOx} < 3.6\text{ V}$, $NVUSRO[PAD3V5V] = 1$); see *Figure 14*.

Table 23. DC electrical characteristics (3.3 V, $NVUSRO[PAD3V5V] = 1$)⁽¹⁾

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Max	
V _{IL}	D	Low level input voltage	—	-0.1 ⁽²⁾	—	V
	P		—	—	0.35 V _{DD_HV_IOx}	V
V _{IH}	P	High level input voltage	—	0.65 V _{DD_HV_IOx}	—	V
	D		—	—	V _{DD_HV_IOx} + 0.1 ⁽²⁾	V
V _{HYS}	T	Schmitt trigger hysteresis	—	0.1 V _{DD_HV_IOx}	—	V
V _{OL_S}	P	Slow, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_S}	P	Slow, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_M}	P	Medium, low level output voltage	I _{OL} = 2 mA	—	0.5	V
V _{OH_M}	P	Medium, high level output voltage	I _{OH} = -2 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_F}	P	Fast, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_F}	P	Fast, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
V _{OL_SYM}	P	Symmetric, low level output voltage	I _{OL} = 1.5 mA	—	0.5	V
V _{OH_SYM}	P	Symmetric, high level output voltage	I _{OH} = -1.5 mA	V _{DD_HV_IOx} - 0.8	—	V
I _{PU}	P	Equivalent pull-up current	V _{IN} = V _{IL}	-130	—	μA
			V _{IN} = V _{IH}	—	-10	
I _{PD}	P	Equivalent pull-down current	V _{IN} = V _{IL}	10	—	μA
			V _{IN} = V _{IH}	—	130	
I _{IL}	P	Input leakage current (all bidirectional ports)	T _A = -40 to 125 °C	—	1	μA
I _{IL}	P	Input leakage current (all ADC input-only ports)	T _A = -40 to 125 °C	—	0.5	μA
C _{IN}	D	Input capacitance	—	—	10	pF

1. These specifications are design targets and subject to change per device characterization.
2. "SR" parameter values must not exceed the absolute maximum ratings shown in *Table 9*.

Table 24. Supply current (3.3 V, NVUSRO[PAD3V5V] = 1)

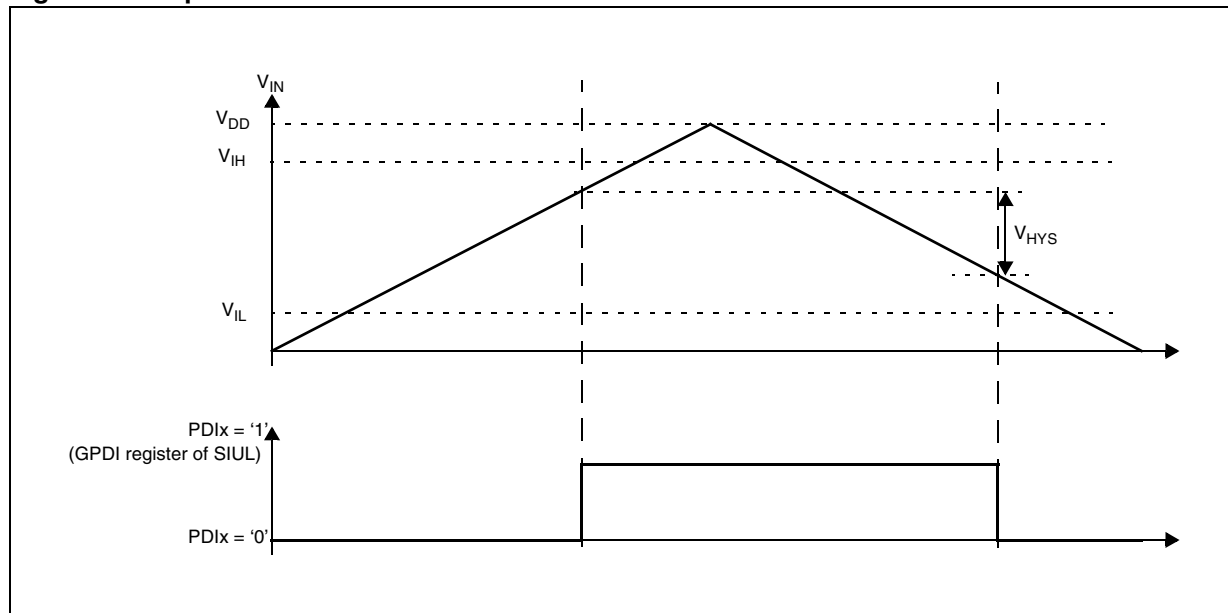
Symbol	C	Parameter	Conditions	Value		Unit
				Typ	Max	
I _{DD_LV_CORx}	T	RUN—Maximum mode ⁽¹⁾	V _{DD_LV_CORx} externally forced at 1.3 V	40 MHz	62	77
				64 MHz	71	89
		RUN—Typical mode ⁽²⁾		40 MHz	45	56
				64 MHz	53	66
	P	RUN—Maximum mode ⁽³⁾	V _{DD_LV_CORx} externally forced at 1.3 V	64 MHz	60	75
		HALT mode ⁽⁴⁾	V _{DD_LV_CORx} externally forced at 1.3 V	—	1.5	10
STOP mode ⁽⁵⁾		V _{DD_LV_CORx} externally forced at 1.3 V	—	1	10	
I _{DD_FLASH}	T	Flash during read on single mode	V _{DD_HV_FL} at 3.3 V	—	8	10
		Flash during erase operation on single mode	V _{DD_HV_FL} at 3.3 V	—	10	12
I _{DD_ADC}	T	ADC—Maximum mode ⁽¹⁾	V _{DD_HV_ADC0} at 3.3 V V _{DD_HV_ADC1} at 3.3 V f _{ADC} = 16 MHz	ADC_1	2.5	4
				ADC_0	2	4
		ADC—Typical mode ⁽²⁾		ADC_1	0.8	1
				ADC_0	0.005	0.006
I _{DD_OSC}	T	Oscillator	V _{DD_OSC} at 3.3 V	8 MHz	2.4	3

1. Maximum mode: FlexPWM, ADCs, CTU, DSPI, LINFlex, FlexCAN, 15 output pins, 1st and 2nd PLL enabled. I/O supply current excluded.
2. Typical mode: DSPI, LINFlex, FlexCAN, 15 output pins, 1st PLL only. I/O supply current excluded.
3. Code fetched from RAM, PLL_0: 64 MHz system clock (x4 multiplier with 16 MHz XTAL), PLL_1 is ON at PHI_div2 = 120 MHz and PHI_div3 = 80 MHz, auxiliary clock sources set that all peripherals receive maximum frequency, all peripherals enabled.
4. Halt mode configurations: code fetched from RAM, code and data flash memories in low power mode, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.
5. STOP “P” mode Device Under Test (DUT) configuration: code fetched from RAM, code and data flash memories OFF, OSC/PLL_0/PLL_1 are OFF, core clock frozen, all peripherals are disabled.

3.10.4 Input DC electrical characteristics definition

Figure 14 shows the DC electrical characteristics behavior as function of time.

Figure 14. Input DC electrical characteristics definition



3.10.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in [Table 25](#).

Table 25. I/O supply segment

Package	Supply segment						
	1	2	3	4	5	6	7
LQFP144	pin8 – pin20	pin23 – pin38	pin39 – pin55	pin58 – pin68	pin73 – pin89	pin92 – pin125	pin128 – pin5
LQFP100	pin15 – pin26	pin27 – pin38	pin41 – pin46	pin51 – pin61	pin64 – pin86	pin89 – pin10	—

[Table 26](#) provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 26. I/O weight

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
NMI	1%	1%	1%	1%
PAD[6]	6%	5%	14%	13%
PAD[49]	5%	4%	14%	12%
PAD[84]	14%	10%	—	—

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[85]	9%	7%	—	—
PAD[86]	9%	6%	—	—
MOD0[0]	12%	8%	—	—
PAD[7]	4%	4%	11%	10%
PAD[36]	5%	4%	11%	9%
PAD[8]	5%	4%	10%	9%
PAD[37]	5%	4%	10%	9%
PAD[5]	5%	4%	9%	8%
PAD[39]	5%	4%	9%	8%
PAD[35]	5%	4%	8%	7%
PAD[87]	12%	9%	—	—
PAD[88]	9%	6%	—	—
PAD[89]	10%	7%	—	—
PAD[90]	15%	11%	—	—
PAD[91]	6%	5%	—	—
PAD[57]	8%	7%	8%	7%
PAD[56]	13%	11%	13%	11%
PAD[53]	14%	12%	14%	12%
PAD[54]	15%	13%	15%	13%
PAD[55]	25%	22%	25%	22%
PAD[96]	27%	24%	—	—
PAD[65]	1%	1%	1%	1%
PAD[67]	1%	1%	—	—
PAD[33]	1%	1%	1%	1%
PAD[68]	1%	1%	—	—
PAD[23]	1%	1%	1%	1%
PAD[69]	1%	1%	—	—
PAD[34]	1%	1%	1%	1%
PAD[70]	1%	1%	—	—
PAD[24]	1%	1%	1%	1%
PAD[71]	1%	1%	—	—
PAD[66]	1%	1%	1%	1%
PAD[25]	1%	1%	1%	1%

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[26]	1%	1%	1%	1%
PAD[27]	1%	1%	1%	1%
PAD[28]	1%	1%	1%	1%
PAD[63]	1%	1%	1%	1%
PAD[72]	1%	1%	—	—
PAD[29]	1%	1%	1%	1%
PAD[73]	1%	1%	—	—
PAD[31]	1%	1%	1%	1%
PAD[74]	1%	1%	—	—
PAD[30]	1%	1%	1%	1%
PAD[75]	1%	1%	—	—
PAD[32]	1%	1%	1%	1%
PAD[76]	1%	1%	—	—
PAD[64]	1%	1%	1%	1%
PAD[0]	23%	20%	23%	20%
PAD[1]	21%	18%	21%	18%
PAD[107]	20%	17%	—	—
PAD[58]	19%	16%	19%	16%
PAD[106]	18%	16%	—	—
PAD[59]	17%	15%	17%	15%
PAD[105]	16%	14%	—	—
PAD[43]	15%	13%	15%	13%
PAD[104]	14%	13%	—	—
PAD[44]	13%	12%	13%	12%
PAD[103]	12%	11%	—	—
PAD[2]	11%	10%	11%	10%
PAD[101]	11%	9%	—	—
PAD[21]	10%	8%	10%	8%
TMS	1%	1%	1%	1%
TCK	1%	1%	1%	1%
PAD[20]	16%	11%	16%	11%
PAD[3]	4%	3%	4%	3%
PAD[61]	9%	8%	9%	8%

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[102]	11%	10%	—	—
PAD[60]	11%	10%	11%	10%
PAD[100]	12%	10%	—	—
PAD[45]	12%	10%	12%	10%
PAD[98]	12%	11%	—	—
PAD[46]	12%	11%	12%	11%
PAD[99]	13%	11%	—	—
PAD[62]	13%	11%	13%	11%
PAD[92]	13%	12%	—	—
VPP_TEST	1%	1%	1%	1%
PAD[4]	14%	12%	14%	12%
PAD[16]	13%	12%	13%	12%
PAD[17]	13%	11%	13%	11%
PAD[42]	13%	11%	13%	11%
PAD[93]	12%	11%	—	—
PAD[95]	12%	11%	—	—
PAD[18]	12%	10%	12%	10%
PAD[94]	11%	10%	—	—
PAD[19]	11%	10%	11%	10%
PAD[77]	10%	9%	—	—
PAD[10]	10%	9%	10%	9%
PAD[78]	9%	8%	—	—
PAD[11]	9%	8%	9%	8%
PAD[79]	8%	7%	—	—
PAD[12]	7%	7%	7%	7%
PAD[41]	7%	6%	7%	6%
PAD[47]	5%	4%	5%	4%
PAD[48]	4%	4%	4%	4%
PAD[51]	4%	4%	4%	4%
PAD[52]	5%	4%	5%	4%
PAD[40]	5%	5%	6%	5%
PAD[80]	9%	8%	—	—
PAD[9]	10%	9%	11%	10%

Table 26. I/O weight (continued)

Pad	LQFP144		LQFP100	
	Weight 5V	Weight 3.3V	Weight 5V	Weight 3.3V
PAD[81]	10%	9%	—	—
PAD[13]	10%	9%	12%	11%
PAD[82]	10%	9%	—	—
PAD[22]	10%	9%	13%	12%
PAD[83]	10%	9%	—	—
PAD[50]	10%	9%	14%	12%
PAD[97]	10%	9%	—	—
PAD[38]	10%	9%	14%	13%
PAD[14]	9%	8%	14%	13%
PAD[15]	9%	8%	15%	13%

3.11 Main oscillator electrical characteristics

The SPC560P44Lx, SPC560P50Lx provides an oscillator/resonator driver.

Table 27. Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0)

Symbol	C	Parameter	Value		Unit	
			Min	Max		
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	6.5	25	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time ⁽¹⁾⁽²⁾	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

Table 28. Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1)

Symbol	C	Parameter	Value		Unit	
			Min	Max		
f_{OSC}	SR	—	Oscillator frequency	4	40	MHz
g_m	—	P	Transconductance	4	20	mA/V
V_{OSC}	—	T	Oscillation amplitude on XTAL pin	1	—	V
t_{OSCSU}	—	T	Start-up time ⁽¹⁾⁽²⁾	8	—	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of XTAL

Table 29. Input clock characteristics

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
f _{OSC}	SR	Oscillator frequency	4	—	40	MHz
f _{CLK}	SR	Frequency in bypass	—	—	64	MHz
t _{rCLK}	SR	Rise/fall time in bypass	—	—	1	ns
t _{DC}	SR	Duty cycle	47.5	50	52.5	%

3.12 FMPLL electrical characteristics

Table 30. FMPLL electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value		Unit	
				Min	Max		
f _{ref_crystal} f _{ref_ext}	D	PLL reference frequency range ⁽²⁾	Crystal reference	4	40	MHz	
f _{PLLIN}	D	Phase detector input frequency range (after pre-divider)	—	4	16	MHz	
f _{FMPLLOUT}	D	Clock frequency range in normal mode	—	16	120	MHz	
f _{FREE}	P	Free-running frequency	Measured using clock division — typically /16	20	150	MHz	
t _{CYC}	D	System clock period	—	—	1 / f _{SYS}	ns	
f _{LORL} f _{LORH}	D	Loss of reference frequency window ⁽³⁾	Lower limit Upper limit	1.6 24	3.7 56	MHz	
f _{SCM}	D	Self-clocked mode frequency ⁽⁴⁾⁽⁵⁾	—	20	150	MHz	
C _{JITTER}	T	CLKOUT period jitter ⁽⁶⁾⁽⁷⁾⁽⁸⁾⁽⁹⁾	Short-term jitter ⁽¹⁰⁾	f _{SYS} maximum	-4	4	% f _{CLKOUT}
			Long-term jitter (avg. over 2 ms interval)	f _{PLLIN} = 16 MHz (resonator), f _{PLLCLK} at 64 MHz, 4000 cycles	—	10	ns
t _{pll}	D	PLL lock time ⁽¹¹⁾⁽¹²⁾	—	—	200	μs	
t _{dc}	D	Duty cycle of reference	—	40	60	%	
f _{LCK}	D	Frequency LOCK range	—	-6	6	% f _{SYS}	
f _{UL}	D	Frequency un-LOCK range	—	-18	18	% f _{SYS}	
f _{CS} f _{DS}	D	Modulation depth	Center spread Down spread	±0.25 -0.5	±4.0 ⁽¹³⁾ -8.0	% f _{SYS}	
f _{MOD}	D	Modulation frequency ⁽¹⁴⁾	—	—	70	kHz	

1. V_{DD_LV_CORx} = 1.2 V ±10%; V_{SS} = 0 V; T_A = -40 to 125 °C, unless otherwise specified

2. Considering operation with PLL not bypassed

3. "Loss of Reference Frequency" window is the reference frequency range outside of which the PLL is in self-clocked mode.

4. Self-clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.
5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. Short term jitter is measured on the clock rising edge at cycle n and cycle $n+4$.
11. This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
12. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
13. This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).
14. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.13 16 MHz RC oscillator electrical characteristics

Table 31. 16 MHz RC oscillator electrical characteristics

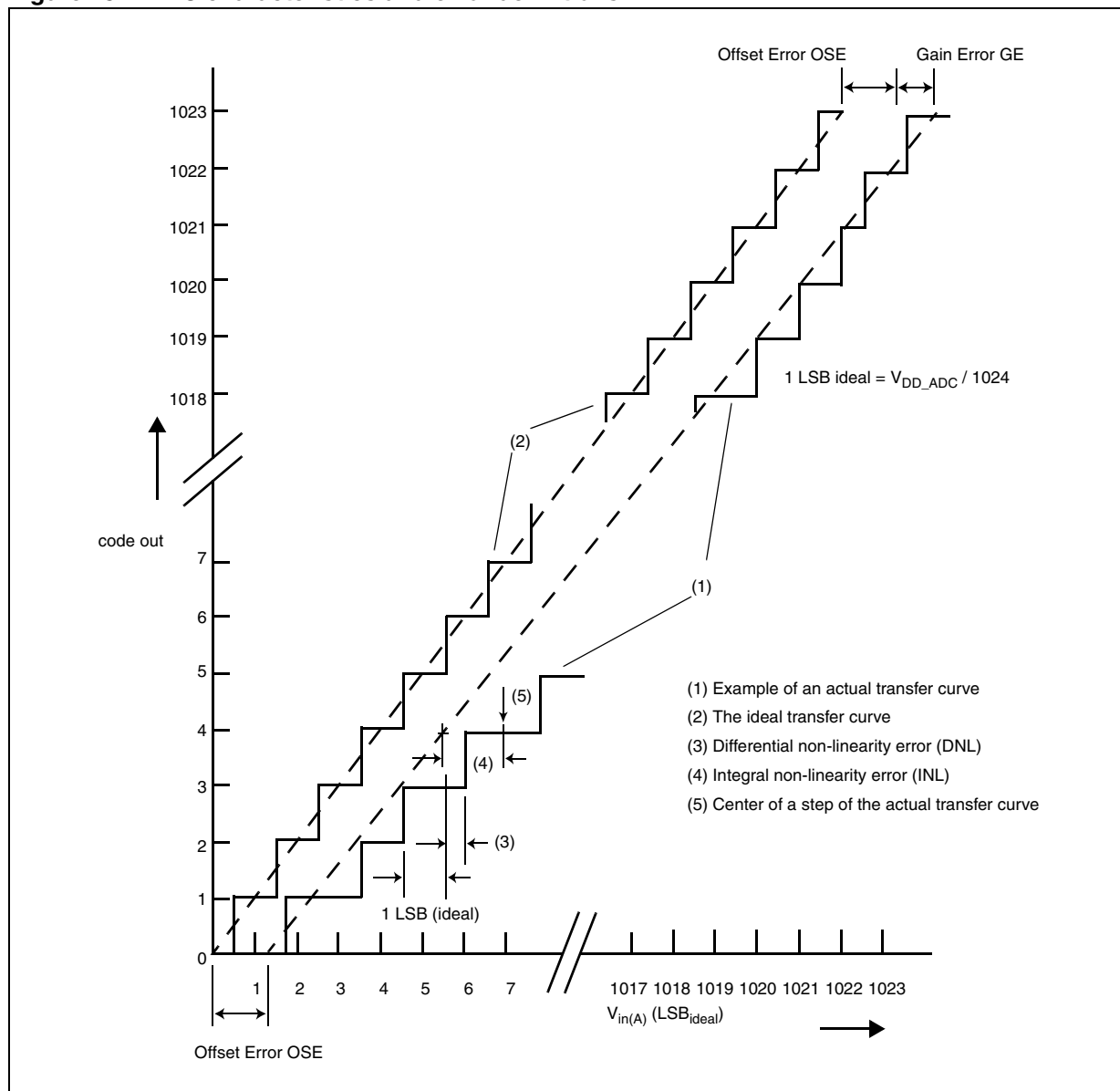
Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
f_{RC}	P	RC oscillator frequency	$T_{\text{A}} = 25\text{ }^{\circ}\text{C}$	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation over temperature and supply with respect to f_{RC} at $T_{\text{A}} = 25\text{ }^{\circ}\text{C}$ in high-frequency configuration	—	–5	—	5	%
Δ_{RCMTRIM}	T	Post Trim Accuracy: The variation of the PTF ⁽¹⁾ from the 16 MHz	$T_{\text{A}} = 25\text{ }^{\circ}\text{C}$	–1	—	1	%
Δ_{RCMSTEP}	T	Fast internal RC oscillator trimming step	$T_{\text{A}} = 25\text{ }^{\circ}\text{C}$	—	1.6	—	%

1. PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

3.14 Analog-to-digital converter (ADC) electrical characteristics

The device provides a 10-bit successive approximation register (SAR) analog-to-digital converter.

Figure 15. ADC characteristics and error definitions



3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the source impedance value of the transducer or circuit supplying the analog signal to be measured.

The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

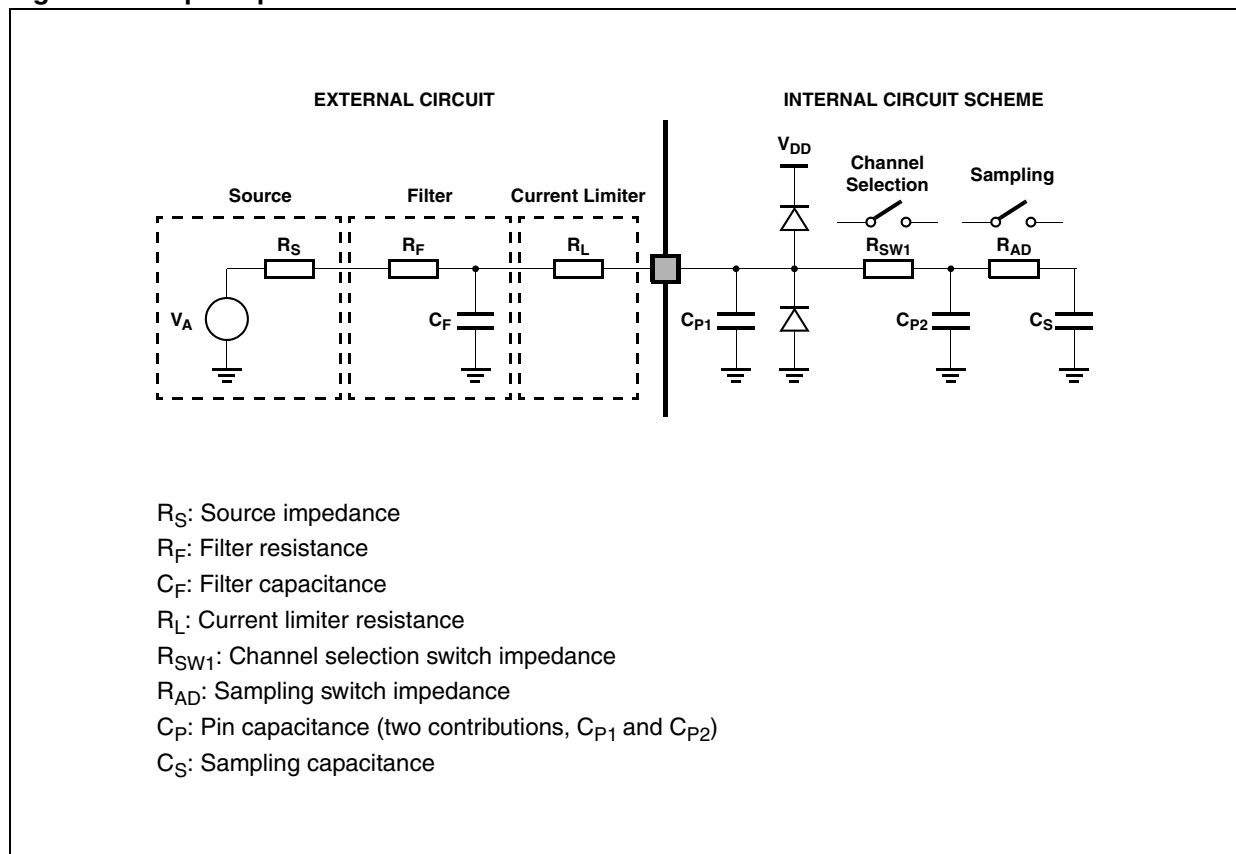
In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the ADC conversion rate, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (fc \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the [Equation 4](#):

Equation 4

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

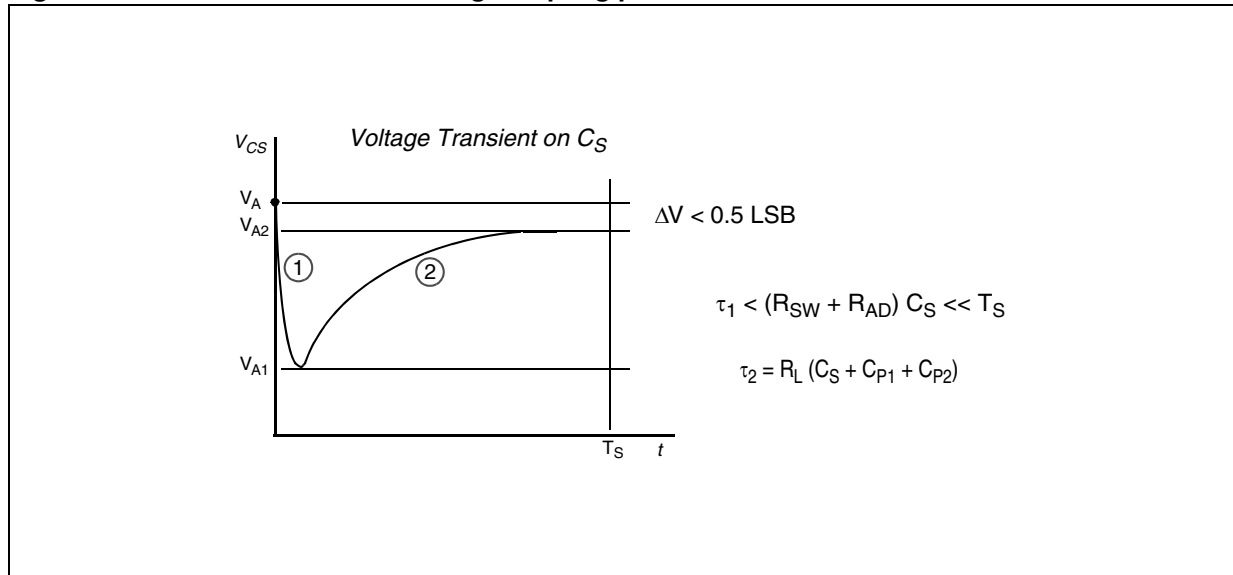
[Equation 4](#) generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

Figure 16. Input equivalent circuit



A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F , C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in [Figure 16](#)): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch closed).

Figure 17. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Equation 5

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

[Equation 5](#) can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

Equation 6

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S , determining a new value of the voltage V_{A1} on the capacitance according to [Equation 7](#):

Equation 7

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L : again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Equation 8

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S , a constraints on R_L sizing is obtained:

Equation 9

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

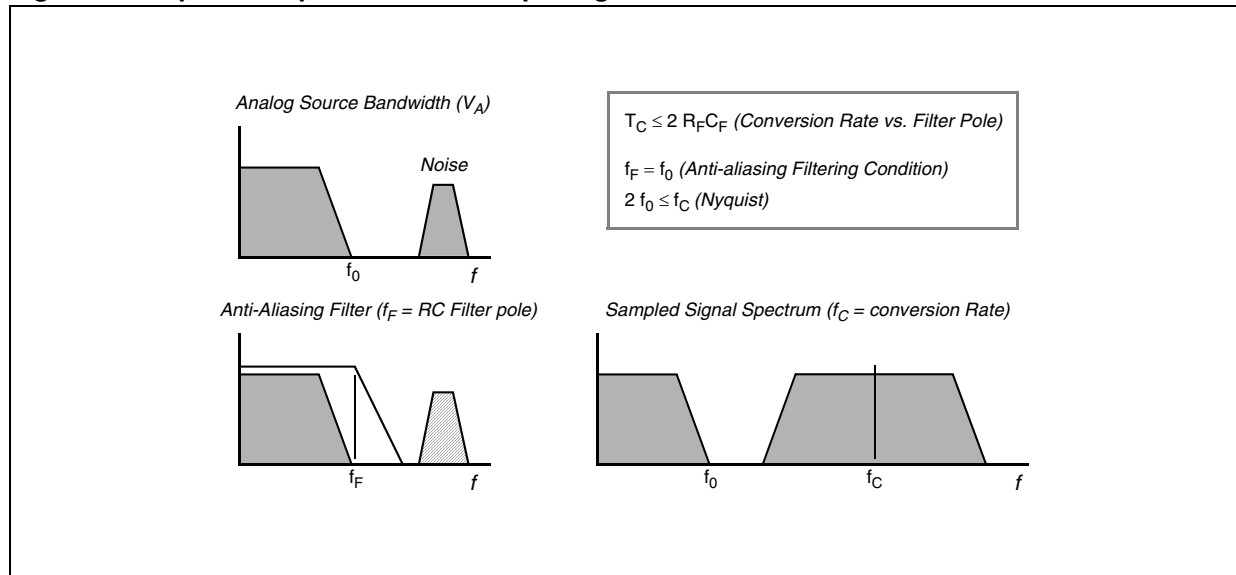
Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1} , C_{P2} and C_S , then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1} . [Equation 10](#) must be respected (charge balance assuming now C_S already charged at V_{A1}):

Equation 10

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A ; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

Figure 18. Spectral representation of input signal



Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter $R_F C_F$ is definitively much higher than the sampling time T_S , so the

charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S ; from the two charge balance equations above, it is simple to derive *Equation 11* between the ideal and real sampled voltage on C_S :

Equation 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Equation 12

$$C_F > 2048 \cdot C_S$$

3.14.2 ADC conversion characteristics

Table 32. ADC conversion characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit	
				Min	Typ	Max		
f_{CK}	SR	—	ADC clock frequency (depends on ADC configuration) (The duty cycle depends on AD_clk ⁽²⁾ frequency)	—	3 ⁽³⁾	—	60	MHz
f_s	SR	—	Sampling frequency	—	—	—	1.53	MHz
t_{ADC_S}	—	D	Sample time ⁽⁴⁾	$f_{ADC} = 20$ MHz, INPSAMP = 3	125	—	—	ns
				$f_{ADC} = 9$ MHz, INPSAMP = 255	—	—	28.2	μ s
t_{ADC_C}	—	P	Conversion time ⁽⁵⁾	$f_{ADC} = 20$ MHz ⁽⁶⁾ , INPCMP = 1	0.650	—	—	μ s
t_{ADC_PU}	SR	—	ADC power-up delay (time needed for ADC to settle exiting from software power down; PWDN bit = 0)	—	—	—	1.5	μ s
C_S ⁽⁷⁾	—	D	ADC input sampling capacitance	—	—	—	2.5	pF
C_{P1} ⁽⁷⁾	—	D	ADC input pin capacitance 1	—	—	—	3	pF
C_{P2} ⁽⁷⁾	—	D	ADC input pin capacitance 2	—	—	—	1	pF
R_{SW1} ⁽⁷⁾	—	D	Internal resistance of analog source	$V_{DD_HV_ADC} = 5$ V \pm 10%	—	—	0.6	k Ω
				$V_{DD_HV_ADC} = 3.3$ V \pm 10%	—	—	3	k Ω
R_{AD} ⁽⁷⁾	—	D	Internal resistance of analog source	—	—	—	2	k Ω

Table 32. ADC conversion characteristics (continued)

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit	
				Min	Typ	Max		
I _{INJ}	—	T	Input current injection	Current injection on one ADC input, different from the converted one. Remains within TUE spec.	-5	—	5	mA
INL	CC	P	Integral non-linearity	No overload	-1.5	—	1.5	LSB
DNL	CC	P	Differential non-linearity	No overload	-1.0	—	1.0	LSB
OSE	CC	T	Offset error	—	—	±1	—	LSB
GE	CC	T	Gain error	—	—	±1	—	LSB
TUE	CC	P	Total unadjusted error without current injection	—	-2.5	—	2.5	LSB
TUE	CC	T	Total unadjusted error with current injection	—	-3	—	3	LSB

1. V_{DD} = 3.3 V to 3.6 V / 4.5 V to 5.5 V, T_A = -40 °C to T_A MAX, unless otherwise specified and analog input voltage from V_{SS_HV_ADCx} to V_{DD_HV_ADCx}.
2. AD_clk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. When configured to allow 60 MHz ADC, the minimum ADC clock speed is 9 MHz, below which precision is lost.
4. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{ADC_S}. After the end of the sample time t_{ADC_S}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{ADC_S} depend on programming.
5. This parameter includes the sample time t_{ADC_S}.
6. 20 MHz ADC clock. Specific prescaler is programmed on MC_PLL_CLK to provide 20 MHz clock to the ADC.
7. See [Figure 16](#).

3.15 Flash memory electrical characteristics

Table 33. Program and erase specifications

Symbol	C	Parameter	Value				Unit
			Min	Typical ⁽¹⁾	Initial max ⁽²⁾	Max ⁽³⁾	
T _{dwprogram}	P	Double Word (64 bits) Program Time ⁽⁴⁾	—	22	50	500	µs
T _{BKPRG}	P	Bank Program (512 KB) ⁽⁴⁾⁽⁵⁾	—	1.45	1.65	33	s
	P	Bank Program (64 KB) ⁽⁴⁾⁽⁵⁾	—	0.18	0.21	4.10	s
T _{16kpperase}	P	16 KB Block Pre-program and Erase Time	—	300	500	5000	ms
T _{32kpperase}	P	32 KB Block Pre-program and Erase Time	—	400	600	5000	ms
T _{128kpperase}	P	128 KB Block Pre-program and Erase Time	—	800	1300	7500	ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
3. The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.



4. Actual hardware programming times. This does not include software overhead.
5. Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 34. Flash memory module life

Symbol	C	Parameter	Conditions	Value		Unit
				Min	Typ	
P/E	C	Number of program/erase cycles per block for 16 KB blocks over the operating temperature range (T_J)	—	100000	—	cycles
P/E	C	Number of program/erase cycles per block for 32 KB blocks over the operating temperature range (T_J)	—	10000	100000	cycles
P/E	C	Number of program/erase cycles per block for 128 KB blocks over the operating temperature range (T_J)	—	1000	100000	cycles
Retention	C	Minimum data retention at 85 °C average ambient temperature ⁽¹⁾	Blocks with 0–1000 P/E cycles	20	—	years
			Blocks with 10000 P/E cycles	10	—	years
			Blocks with 100000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

Table 35. Flash memory read access timing

Symbol	C	Parameter	Conditions ⁽¹⁾	Max value	Unit
f_{\max}	C	Maximum working frequency at given number of wait states in worst conditions	2 wait states	66	MHz
			0 wait states	18	

1. $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$, $T_A = -40$ to 125 °C , unless otherwise specified

3.16 AC specifications

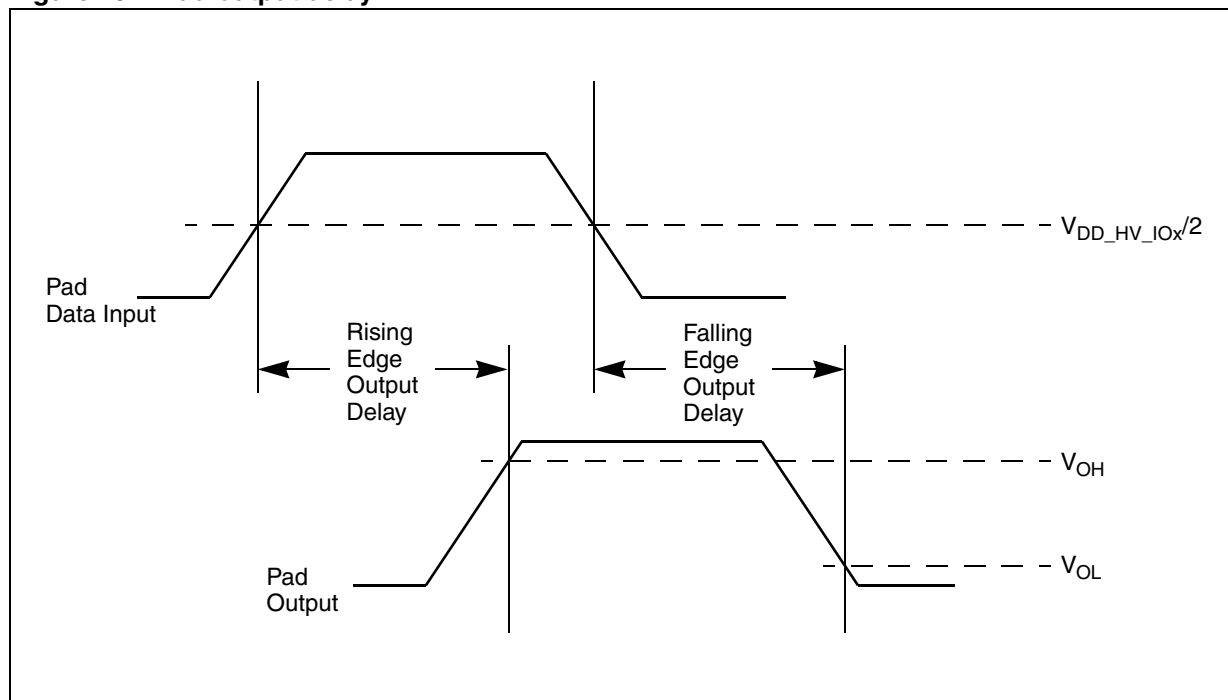
3.16.1 Pad AC specifications

Table 36. Output pin transition times

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit	
				Min	Typ	Max		
t _{tr}	CC	Output transition time output pin ⁽²⁾ SLOW configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
			C _L = 50 pF		—	—	100	
			C _L = 100 pF		—	—	125	
			C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	40	
			C _L = 50 pF		—	—	50	
			C _L = 100 pF		—	—	75	
t _{tr}	CC	Output transition time output pin ⁽²⁾ MEDIUM configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
			C _L = 50 pF		—	—	20	
			C _L = 100 pF		—	—	40	
			C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
			C _L = 50 pF		—	—	25	
			C _L = 100 pF		—	—	40	
t _{tr}	CC	Output transition time output pin ⁽²⁾ FAST configuration	C _L = 25 pF	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	4	ns
			C _L = 50 pF		—	—	6	
			C _L = 100 pF		—	—	12	
			C _L = 25 pF	V _{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	4	
			C _L = 50 pF		—	—	7	
			C _L = 100 pF		—	—	12	
t _{SYM} ⁽³⁾	CC	Symmetric transition time, same drive strength between N and P transistor	V _{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns	
			V _{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5		

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = -40 °C to T_A MAX, unless otherwise specified
2. C_L includes device and package capacitances (C_{PKG} < 5 pF).
3. Transition timing of both positive and negative slopes will differ maximum 50%

Figure 19. Pad output delay



3.17 AC timing characteristics

3.17.1 $\overline{\text{RESET}}$ pin characteristics

The SPC560P44Lx, SPC560P50Lx implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

Figure 20. Start-up reset requirements

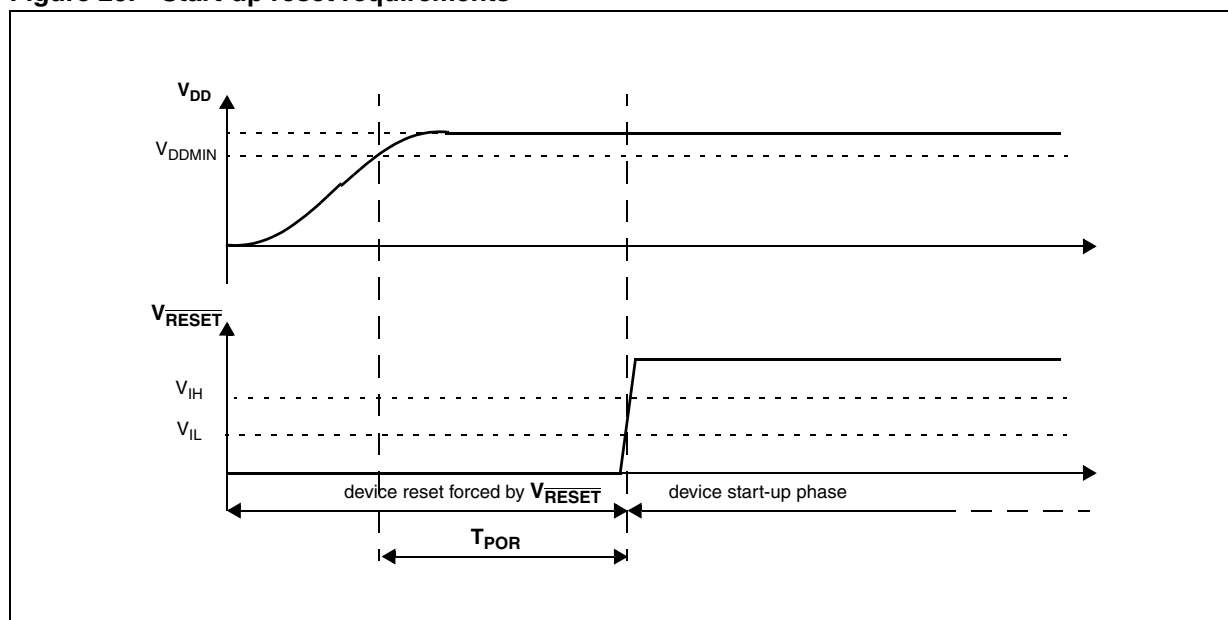


Figure 21. Noise filtering on reset signal

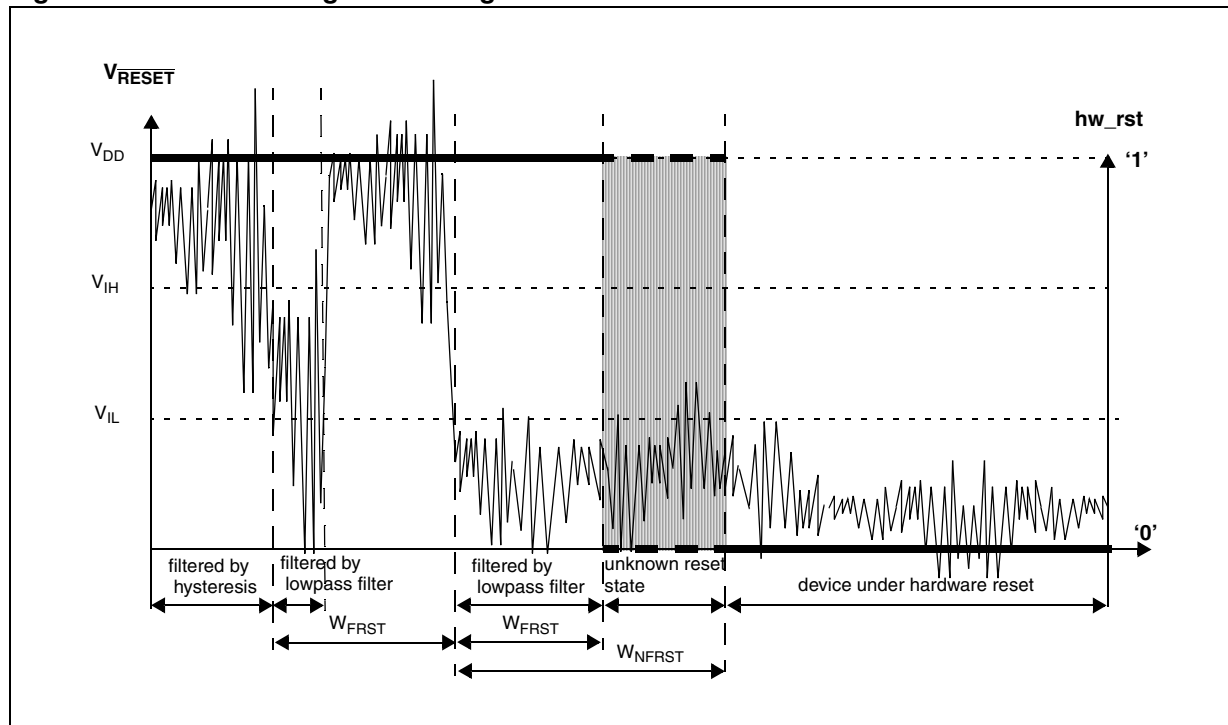


Table 37. $\overline{\text{RESET}}$ electrical characteristics

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit	
				Min	Typ	Max		
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	$0.65V_{DD}$	—	$V_{DD}+0.4$	V	
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	-0.4	—	$0.35V_{DD}$	V	
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	$0.1V_{DD}$	—	—	V	
V_{OL}	CC	P	Output low level	Push Pull, $I_{OL} = 2\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $PAD3V5V = 0$ (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, $I_{OL} = 1\text{mA}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $PAD3V5V = 1^{(2)}$	—	—	$0.1V_{DD}$	
				Push Pull, $I_{OL} = 1\text{mA}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, $PAD3V5V = 1$ (recommended)	—	—	0.5	

Table 37. $\overline{\text{RESET}}$ electrical characteristics (continued)

Symbol	C	Parameter	Conditions ⁽¹⁾	Value			Unit	
				Min	Typ	Max		
t_{tr}	CC	D	Output transition time output pin ⁽³⁾ MEDIUM configuration	$C_L = 25\text{pF}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $\text{PAD3V5V} = 0$	—	—	10	ns
				$C_L = 50\text{pF}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $\text{PAD3V5V} = 0$	—	—	20	
				$C_L = 100\text{pF}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $\text{PAD3V5V} = 0$	—	—	40	
				$C_L = 25\text{pF}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, $\text{PAD3V5V} = 1$	—	—	12	
				$C_L = 50\text{pF}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, $\text{PAD3V5V} = 1$	—	—	25	
				$C_L = 100\text{pF}$, $V_{DD} = 3.3\text{ V} \pm 10\%$, $\text{PAD3V5V} = 1$	—	—	40	
W_{FRST}	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	40	ns	
W_{NFRST}	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	500	—	ns	
t_{POR}	CC	D	Maximum delay before internal reset is released after all V_{DD_HV} reach nominal supply	Monotonic V_{DD_HV} supply ramp	—	—	1	ms
I_{WPU}	CC	P	Weak pull-up current absolute value	$V_{DD} = 3.3\text{ V} \pm 10\%$, $\text{PAD3V5V} = 1$	10	—	150	μA
				$V_{DD} = 5.0\text{ V} \pm 10\%$, $\text{PAD3V5V} = 0$	10	—	150	
				$V_{DD} = 5.0\text{ V} \pm 10\%$, $\text{PAD3V5V} = 1^{(4)}$	10	—	250	

1. $V_{DD} = 3.3\text{ V} \pm 10\%$ / $5.0\text{ V} \pm 10\%$, $T_A = -40\text{ }^\circ\text{C}$ to T_{A_MAX} , unless otherwise specified

2. This is a transient configuration during power-up, up to the end of reset PHASE2 (refer to RGM module section of device reference manual).

3. C_L includes device and package capacitance ($C_{PKG} < 5\text{ pF}$).

4. The configuration $\text{PAD3V5} = 1$ when $V_{DD} = 5\text{ V}$ is only transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics

No.	Symbol	C	Parameter	Conditions	Value		Unit	
					Min	Max		
1	t_{JCYC}	CC	D	TCK cycle time	—	100	—	ns
2	t_{JDC}	CC	D	TCK clock pulse width (measured at $V_{DD_HV_IOx}/2$)	—	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40% – 70%)	—	—	3	ns
4	t_{TMSS} , t_{TDIS}	CC	D	TMS, TDI data setup time	—	5	—	ns

Table 38. JTAG pin AC electrical characteristics (continued)

No.	Symbol	C	Parameter	Conditions	Value		Unit	
					Min	Max		
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	40	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

Figure 22. JTAG test clock input timing

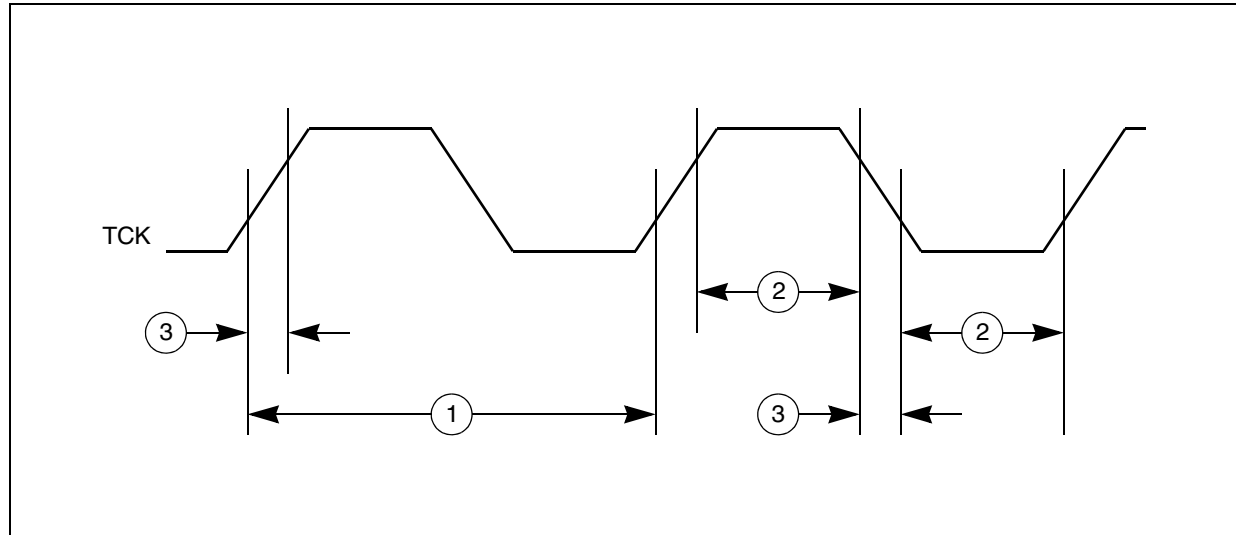


Figure 23. JTAG test access port timing

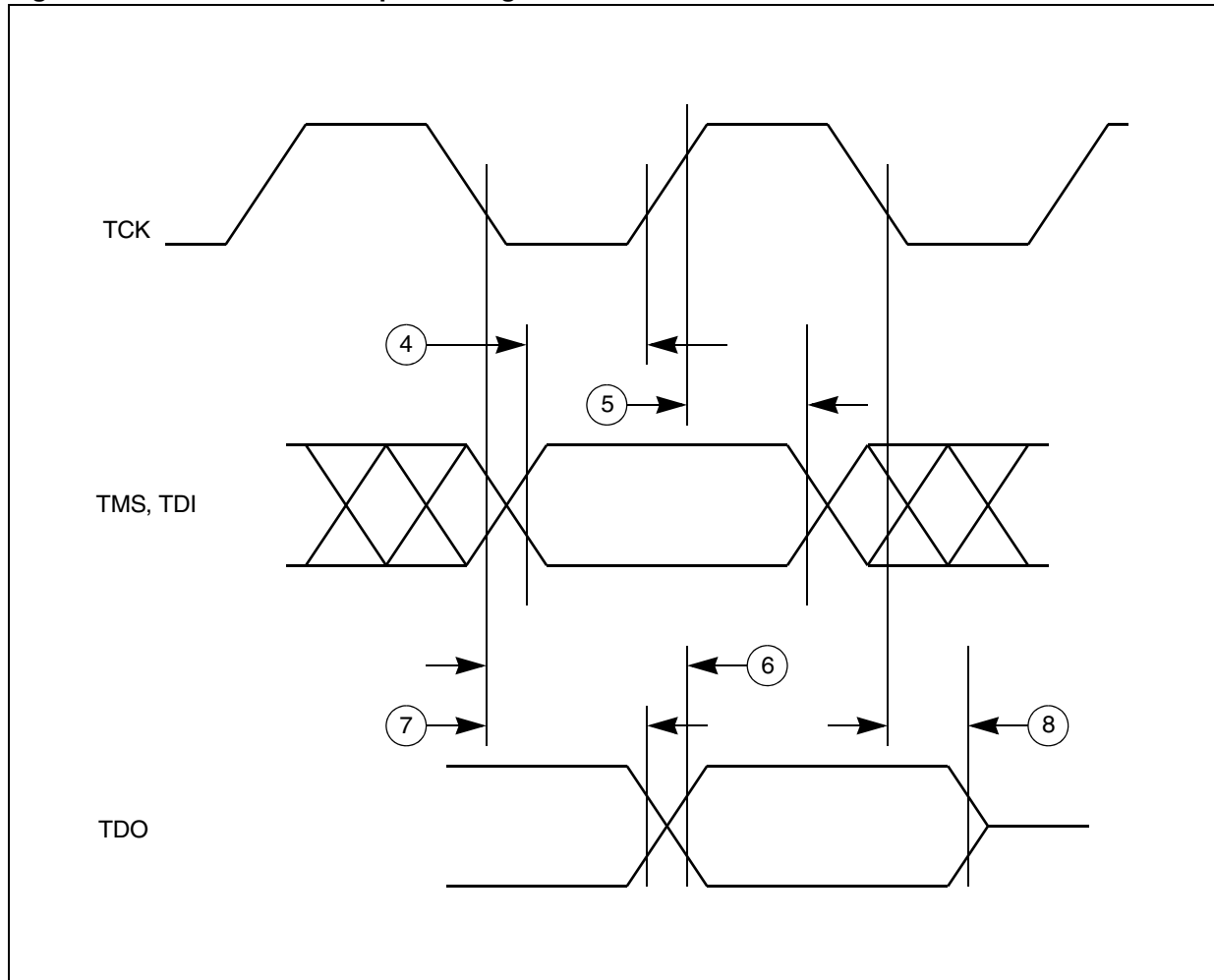
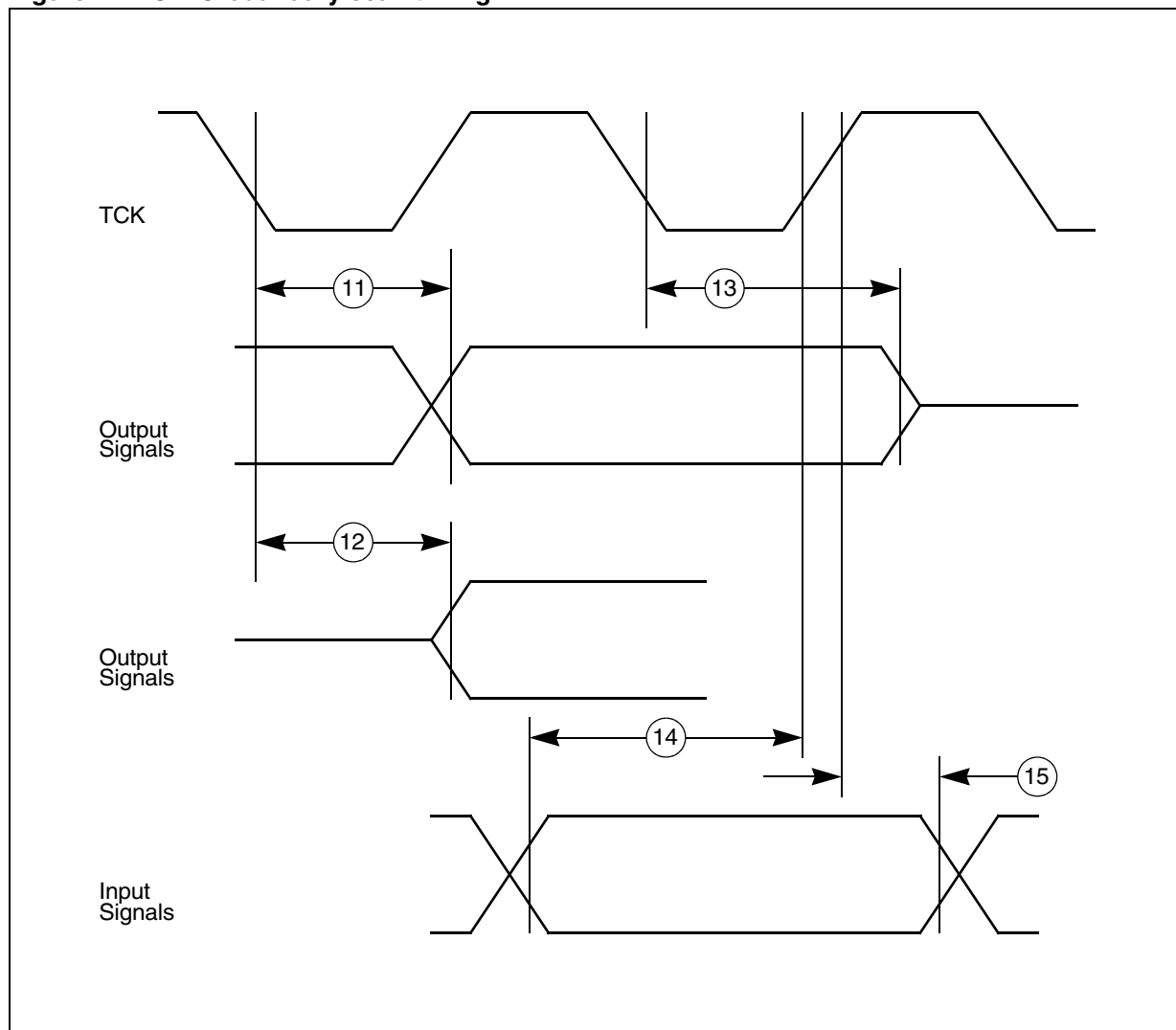


Figure 24. JTAG boundary scan timing



3.17.3 Nexus timing

Table 39. Nexus debug port timing⁽¹⁾

No.	Symbol	C	Parameter	Value			Unit	
				Min	Typ	Max		
1	t_{MCCY}	CC	D	MCKO cycle time	32	—	—	ns
2	t_{MDOV}	CC	D	MCKO low to MDO data valid ⁽²⁾	—	—	6	ns
3	t_{MSEOV}	CC	D	MCKO low to \overline{MSEO} data valid ⁽²⁾	—	—	6	ns
4	$t_{EVT OV}$	CC	D	MCKO low to $\overline{EVT O}$ data valid ⁽²⁾	—	—	6	ns
5	t_{TCYC}	CC	D	TCK cycle time	64 ⁽³⁾	—	—	ns
6	t_{NTDIS}	CC	D	TDI data setup time	6	—	—	ns
	t_{NTMSS}	CC	D	TMS data setup time	6	—	—	ns

Table 39. Nexus debug port timing⁽¹⁾ (continued)

No.	Symbol	C	Parameter	Value			Unit	
				Min	Typ	Max		
7	t_{NTDIH}	CC	D	TDI data hold time	10	—	—	ns
	t_{NTMSH}	CC	D	TMS data hold time	10	—	—	ns
8	t_{TDOV}	CC	D	TCK low to TDO data valid	—	—	35	ns
9	t_{TDOI}	CC	D	TCK low to TDO data invalid	6	—	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. MDO, \overline{MSEO} , and \overline{EVTO} data is held valid until next MCKO low cycle.
3. Lower frequency is required to be fully compliant to standard.

Figure 25. Nexus output timing

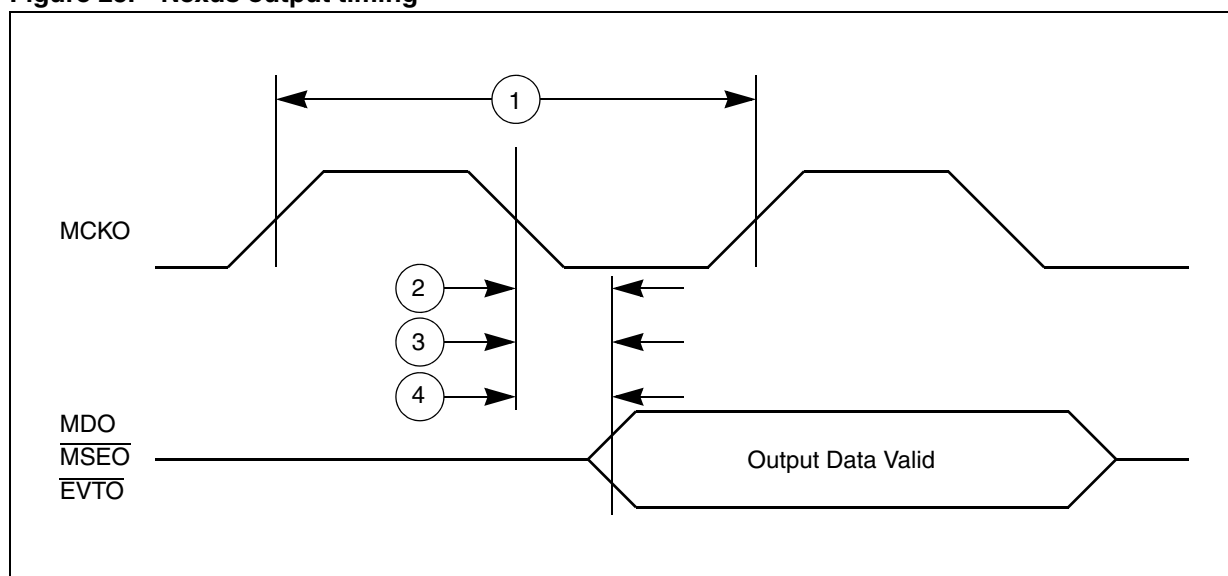


Figure 26. Nexus event trigger and test clock timings

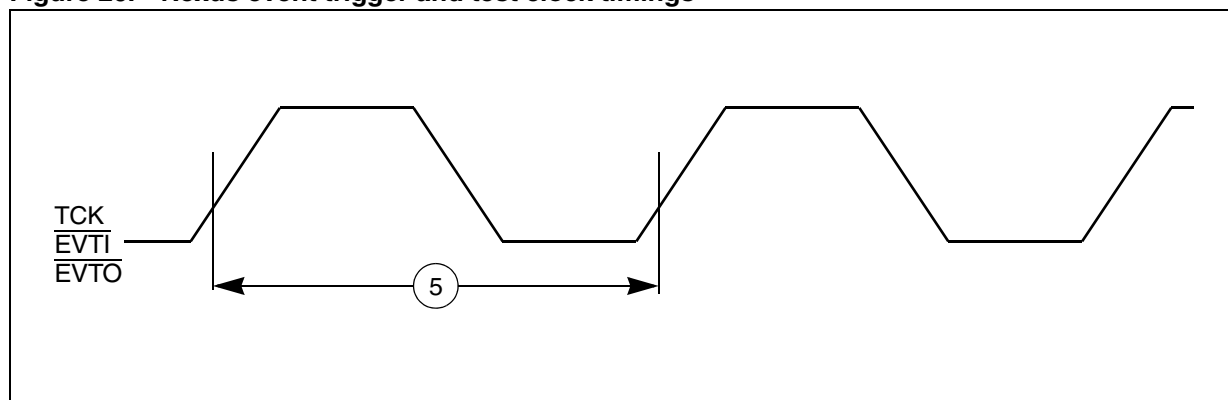
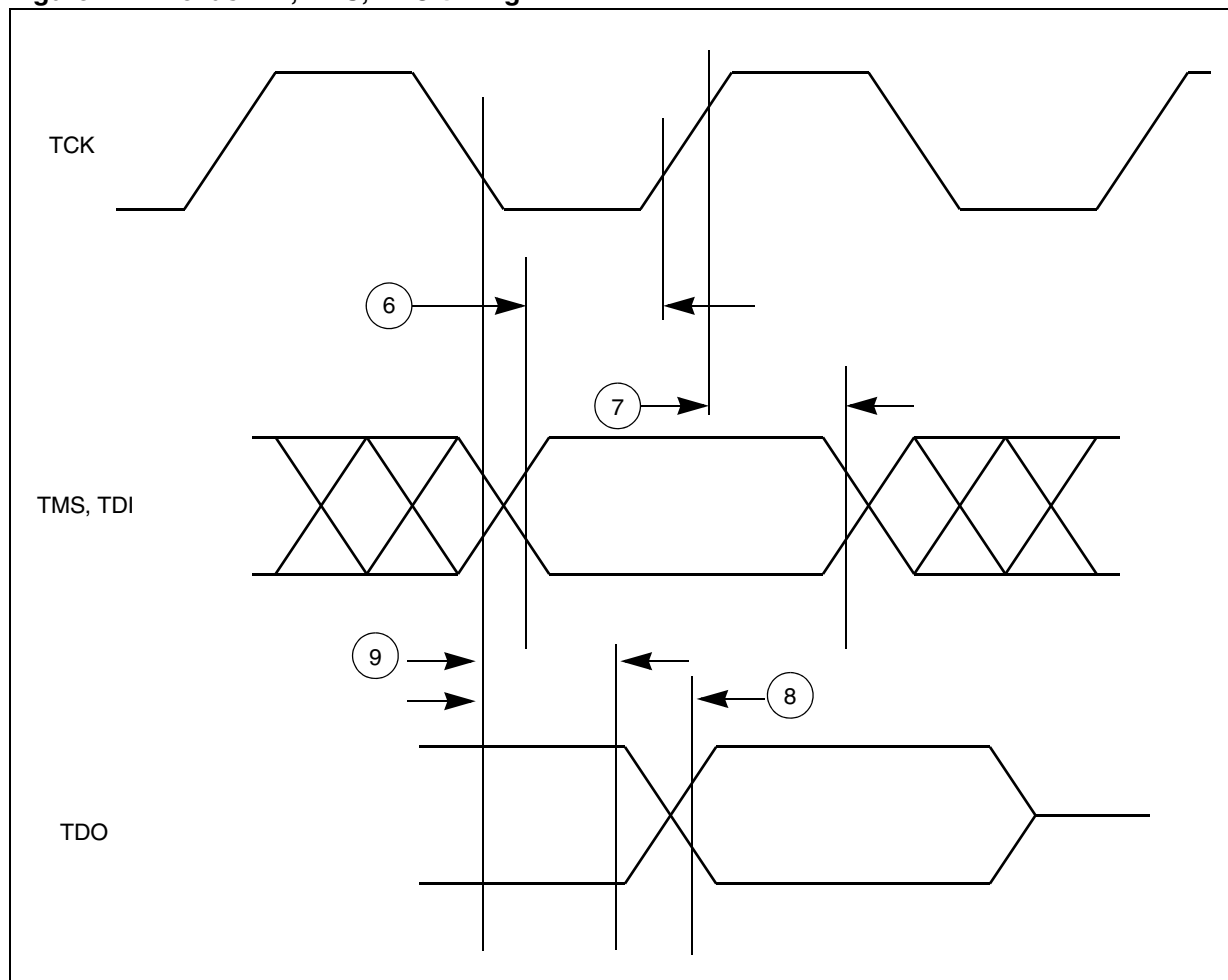


Figure 27. Nexus TDI, TMS, TDO timing



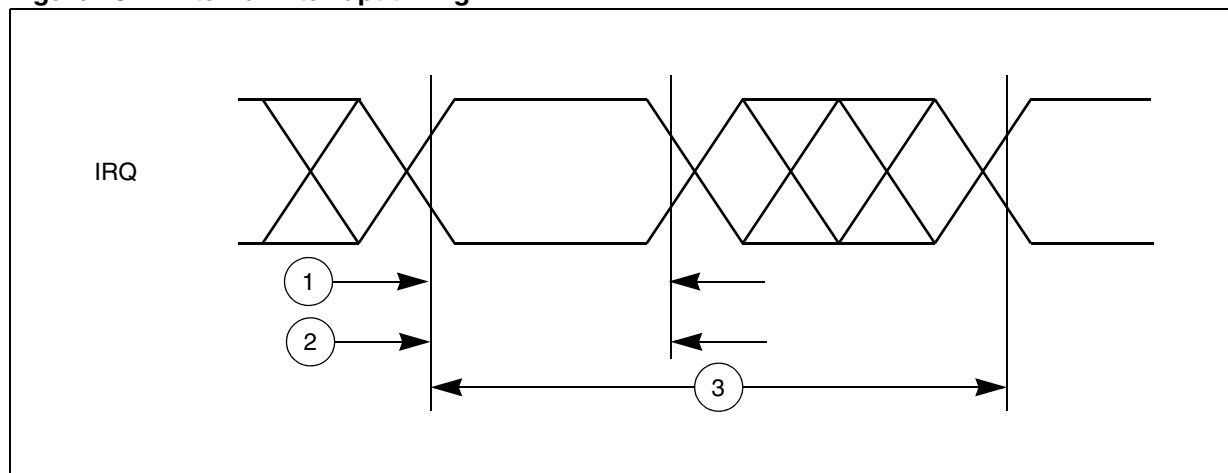
3.17.4 External interrupt timing (IRQ pin)

Table 40. External interrupt timing⁽¹⁾

No.	Symbol	C	Parameter	Conditions	Value		Unit	
					Min	Max		
1	t_{IPWL}	CC	D	IRQ pulse width low	—	4	—	t_{CYC}
2	t_{IPWH}	CC	D	IRQ pulse width high	—	4	—	t_{CYC}
3	t_{ICYC}	CC	D	IRQ edge to edge time ⁽²⁾	—	$4 + N^{(3)}$	—	t_{CYC}

1. IRQ timing specified at $f_{SYS} = 64$ MHz and $V_{DD_HV_IOx} = 3.0$ V to 5.5 V, $T_A = T_L$ to T_H , and $C_L = 200$ pF with $SRC = 0b00$.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.
3. $N =$ ISR time to clear the flag

Figure 28. External interrupt timing



3.17.5 DSPI timing

Table 41. DSPI timing⁽¹⁾

No.	Symbol	C	Parameter	Conditions	Value		Unit	
					Min	Max		
1	t _{SCK}	CC	D	DSPI cycle time	Master (MTFE = 0)	60	—	ns
					Slave (MTFE = 0)	60	—	
2	t _{CSC}	CC	D	CS to SCK delay	—	16	—	ns
3	t _{ASC}	CC	D	After SCK delay	—	26	—	ns
4	t _{SDC}	CC	D	SCK duty cycle	—	0.4 * t _{SCK}	0.6 * t _{SCK}	ns
5	t _A	CC	D	Slave access time	\overline{SS} active to SOUT valid	—	30	ns
6	t _{DIS}	CC	D	Slave SOUT disable time	\overline{SS} inactive to SOUT high impedance or invalid	—	16	ns
7	t _{PCSC}	CC	D	PCSx to \overline{PCSS} time	—	13	—	ns
8	t _{PASC}	CC	D	\overline{PCSS} to PCSx time	—	13	—	ns
9	t _{SUI}	CC	D	Data setup time for inputs	Master (MTFE = 0)	35	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	35	—	
					Master (MTFE = 1, CPHA = 1)	35	—	
10	t _{HI}	CC	D	Data hold time for inputs	Master (MTFE = 0)	-5	—	ns
					Slave	4	—	
					Master (MTFE = 1, CPHA = 0)	11	—	
					Master (MTFE = 1, CPHA = 1)	-5	—	

Table 41. DSPI timing⁽¹⁾ (continued)

No.	Symbol	C	Parameter	Conditions	Value		Unit	
					Min	Max		
11	t _{SUO}	CC	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	12	ns
					Slave	—	36	
					Master (MTFE = 1, CPHA = 0)	—	12	
					Master (MTFE = 1, CPHA = 1)	—	12	
12	t _{HO}	CC	D	Data hold time for outputs	Master (MTFE = 0)	-2	—	ns
					Slave	6	—	
					Master (MTFE = 1, CPHA = 0)	6	—	
					Master (MTFE = 1, CPHA = 1)	-2	—	

1. All timing is provided with 50 pF capacitance on output, 1 ns transition time on input signal.

Figure 29. DSPI classic SPI timing – Master, CPHA = 0

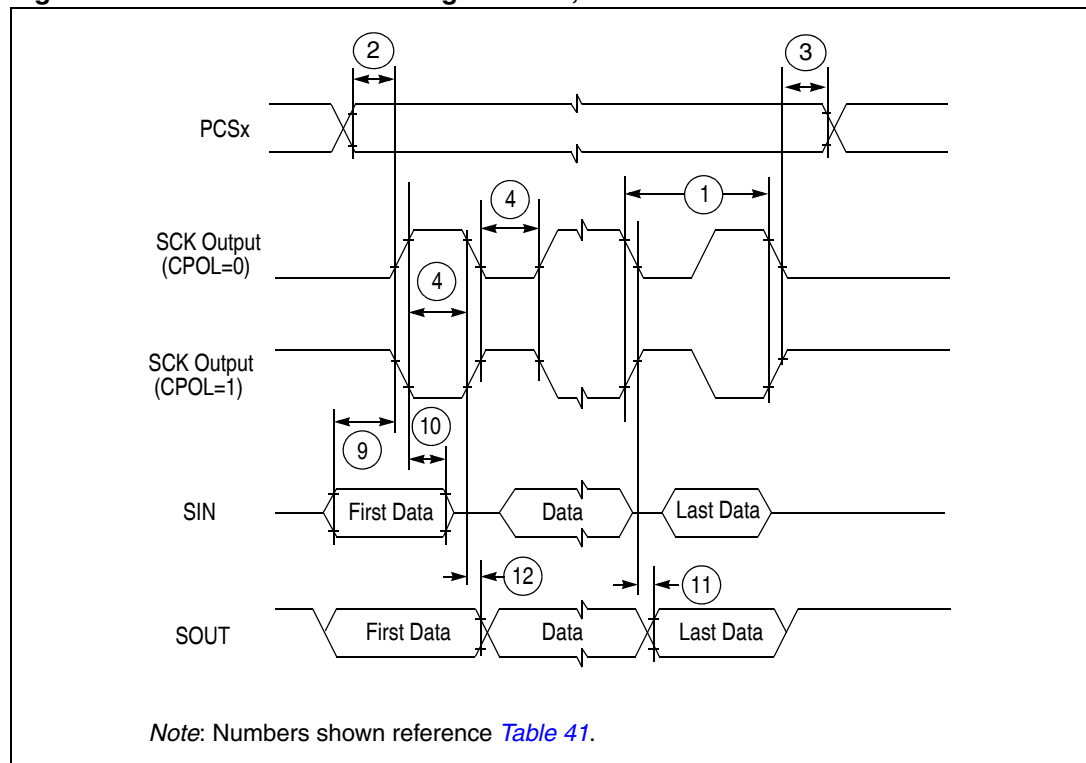


Figure 30. DSPI classic SPI timing – Master, CPHA = 1

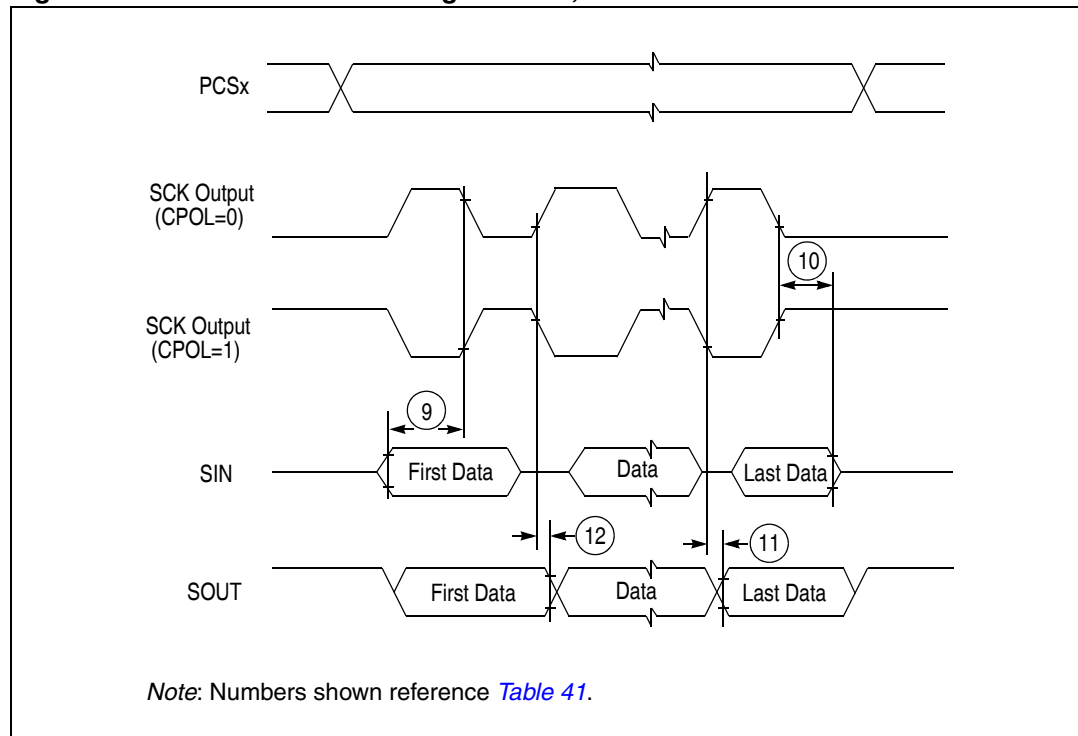


Figure 31. DSPI classic SPI timing – Slave, CPHA = 0

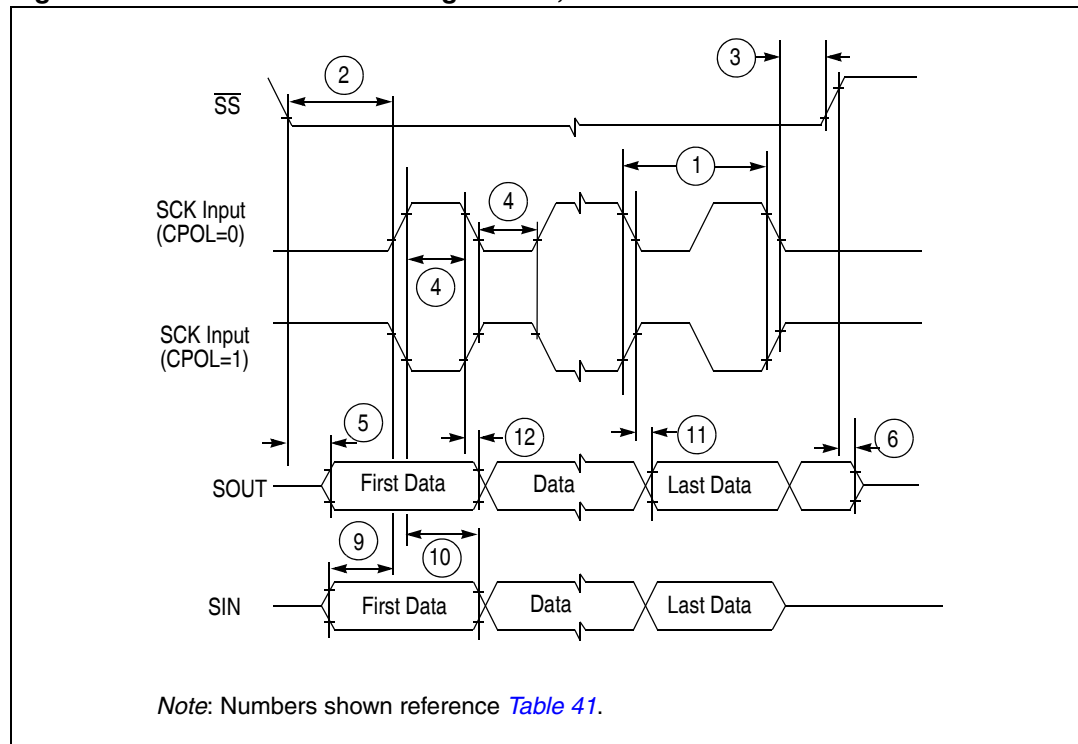


Figure 32. DSPI classic SPI timing – Slave, CPHA = 1

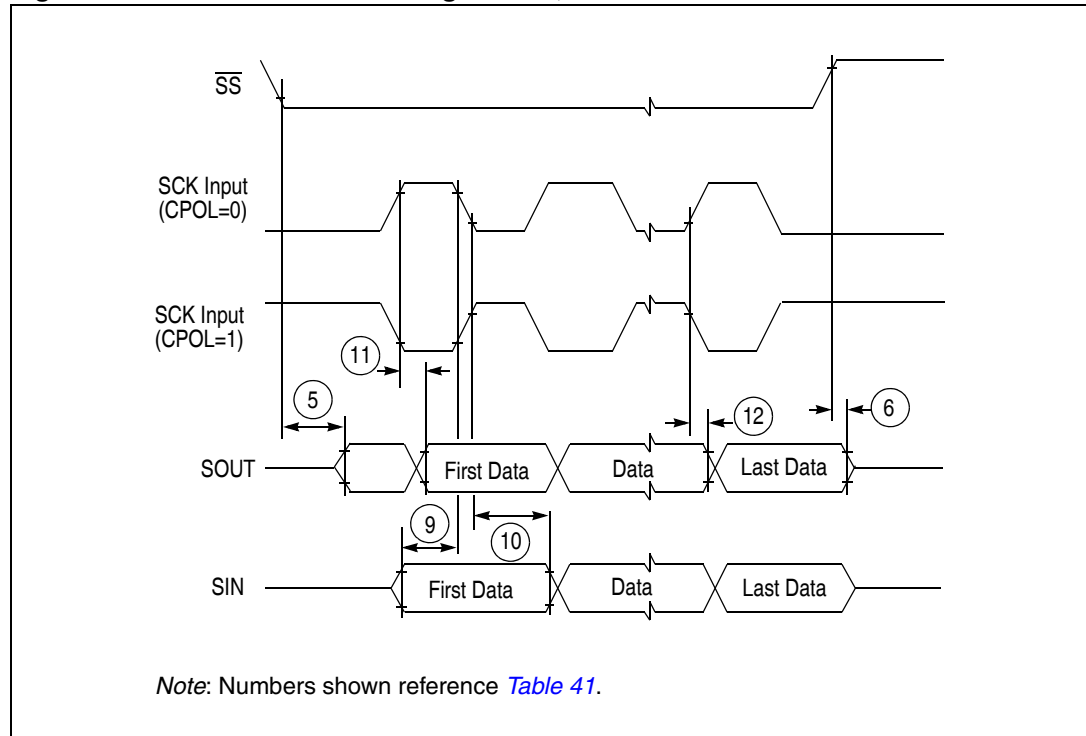


Figure 33. DSPI modified transfer format timing – Master, CPHA = 0

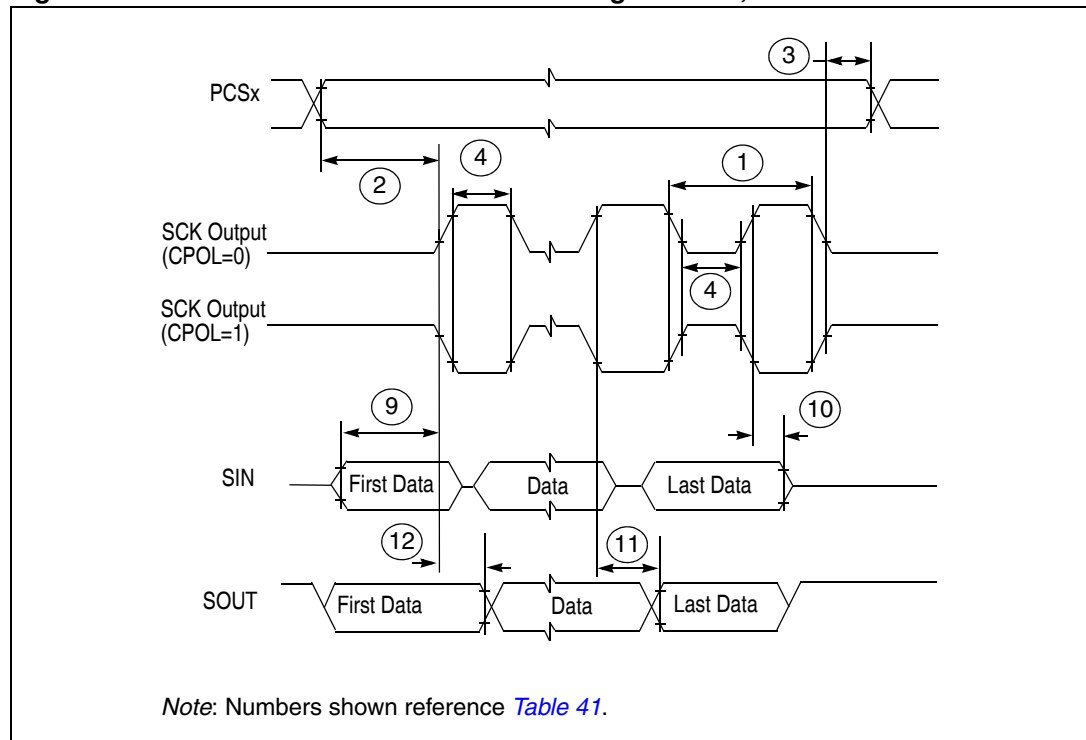


Figure 34. DSPI modified transfer format timing – Master, CPHA = 1

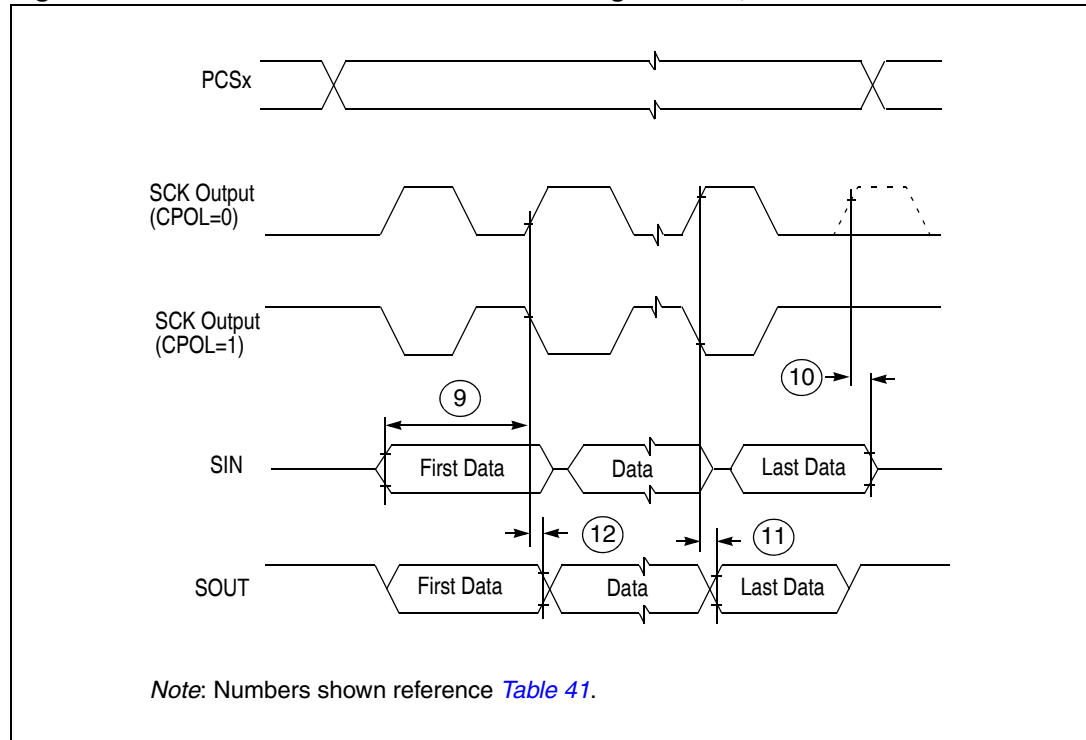


Figure 35. DSPI modified transfer format timing – Slave, CPHA = 0

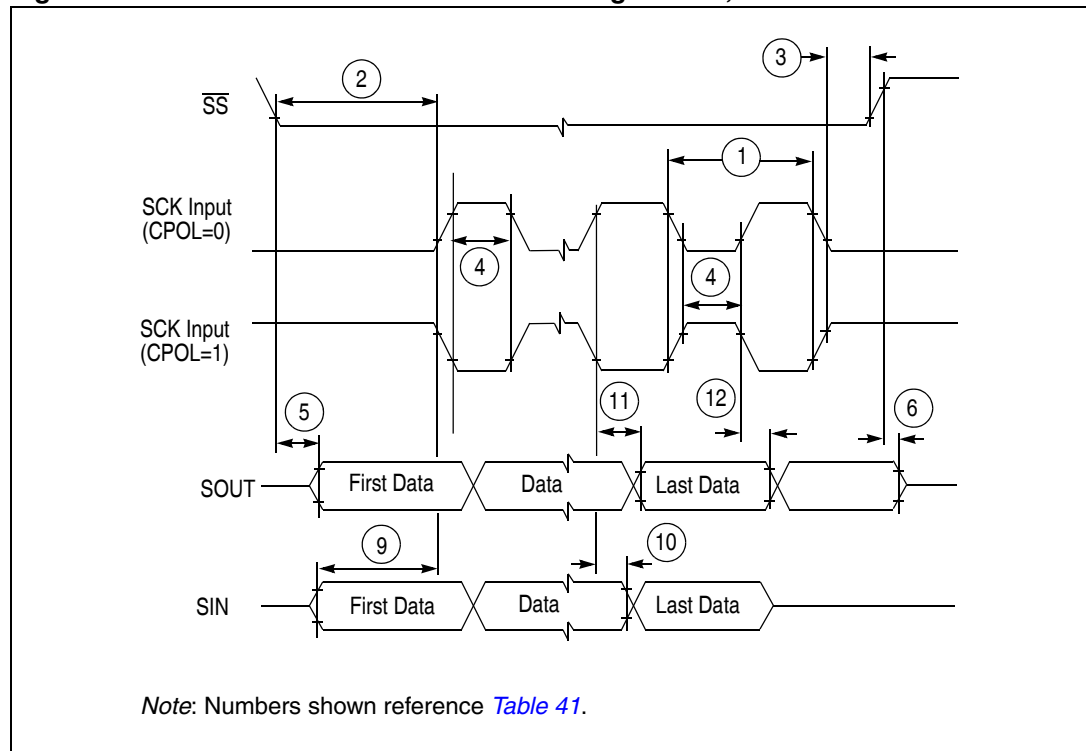


Figure 36. DSPI modified transfer format timing – Slave, CPHA = 1

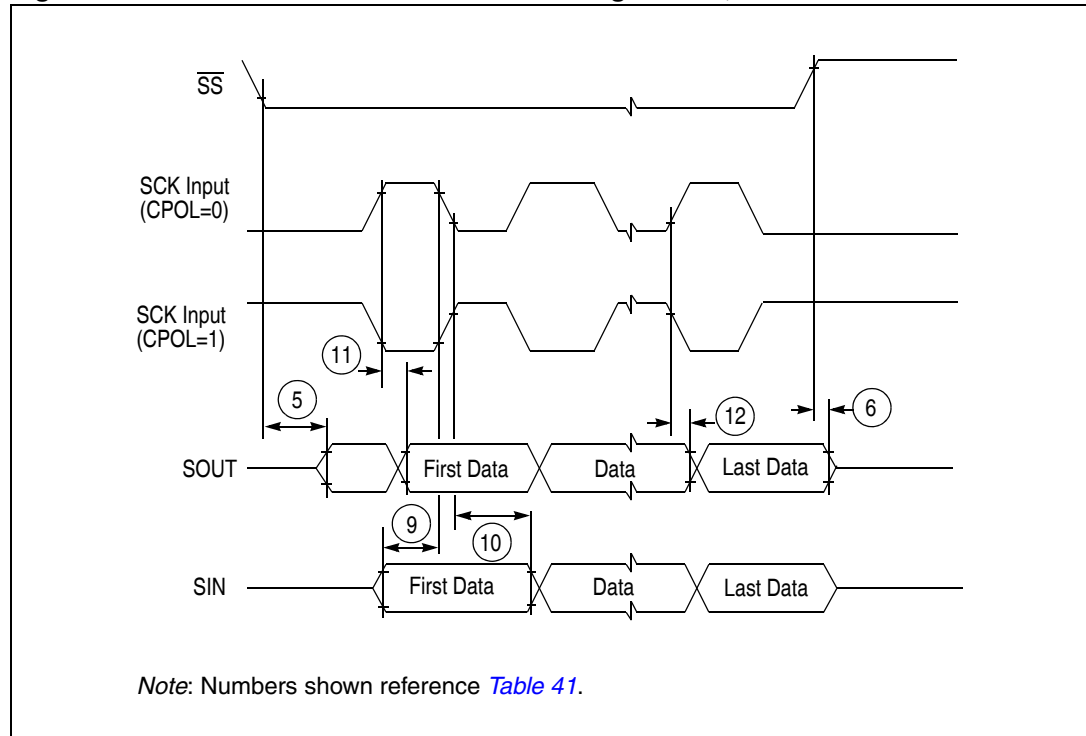
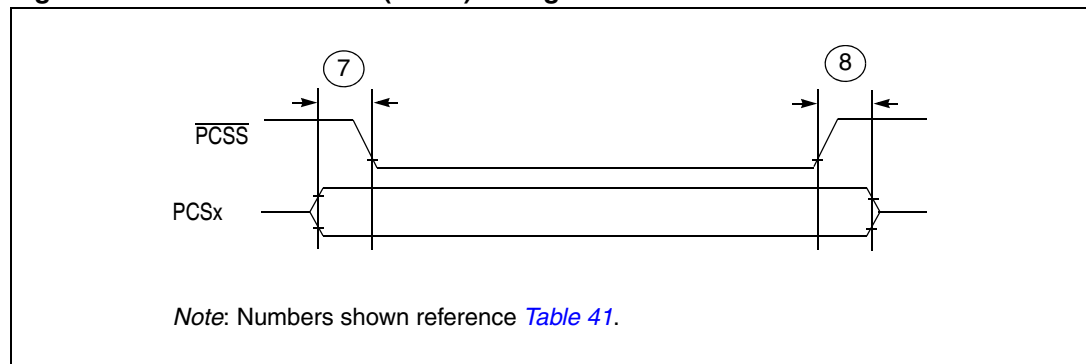


Figure 37. DSPI PCS strobe (\overline{PCSS}) timing



4 Package characteristics

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.2 Package mechanical data

4.2.1 LQFP144 mechanical outline drawing

Figure 38. LQFP144 package mechanical drawing

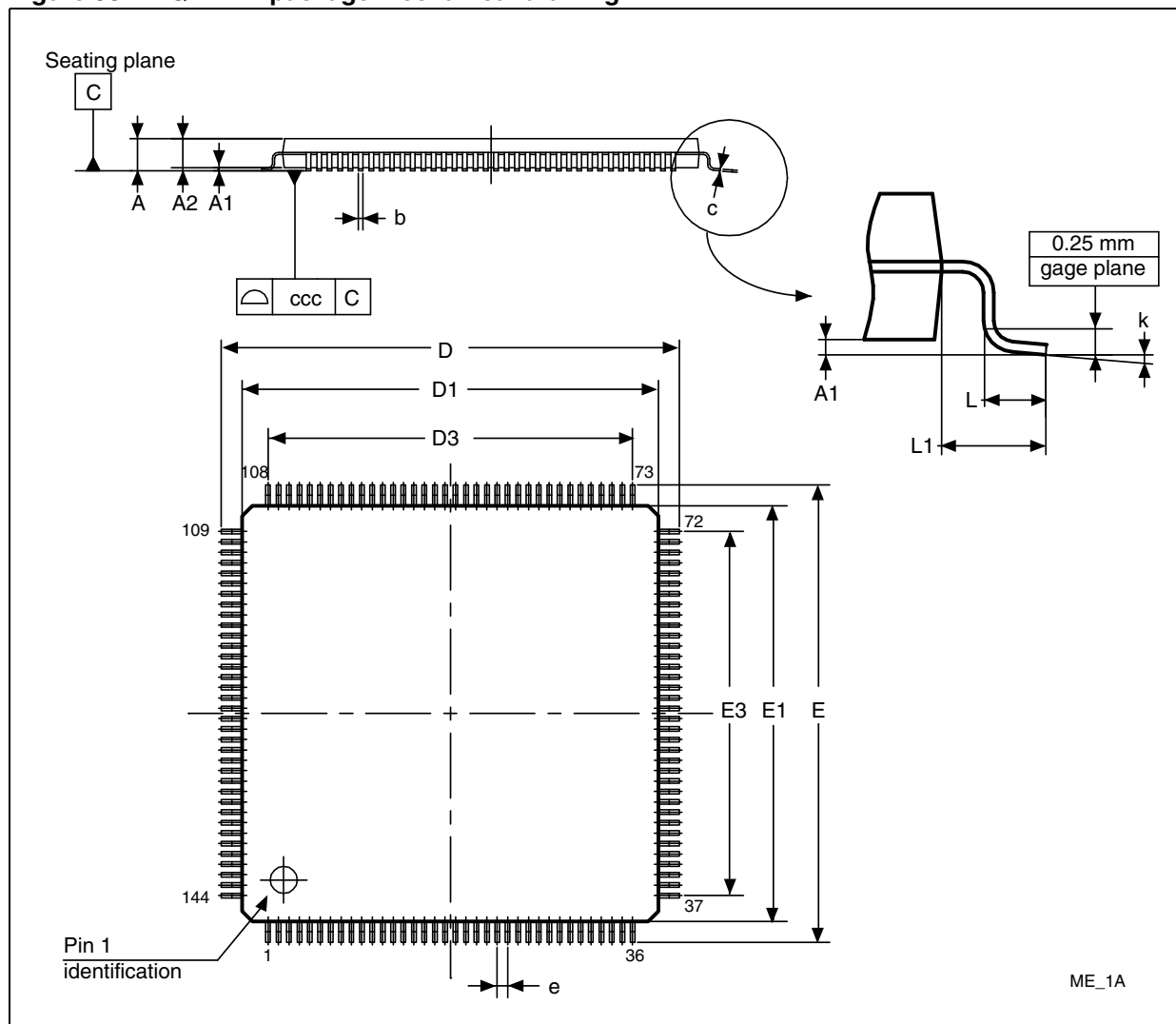


Table 42. LQFP144 mechanical data

Symbol	Dimensions					
	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	—	17.500	—	—	0.6890	—
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	—	17.500	—	—	0.6890	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	3.5°	0.0°	7.0°
ccc ⁽²⁾	0.080			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

2. Tolerance

4.2.2 LQFP100 mechanical outline drawing

Figure 39. LQFP100 package mechanical drawing

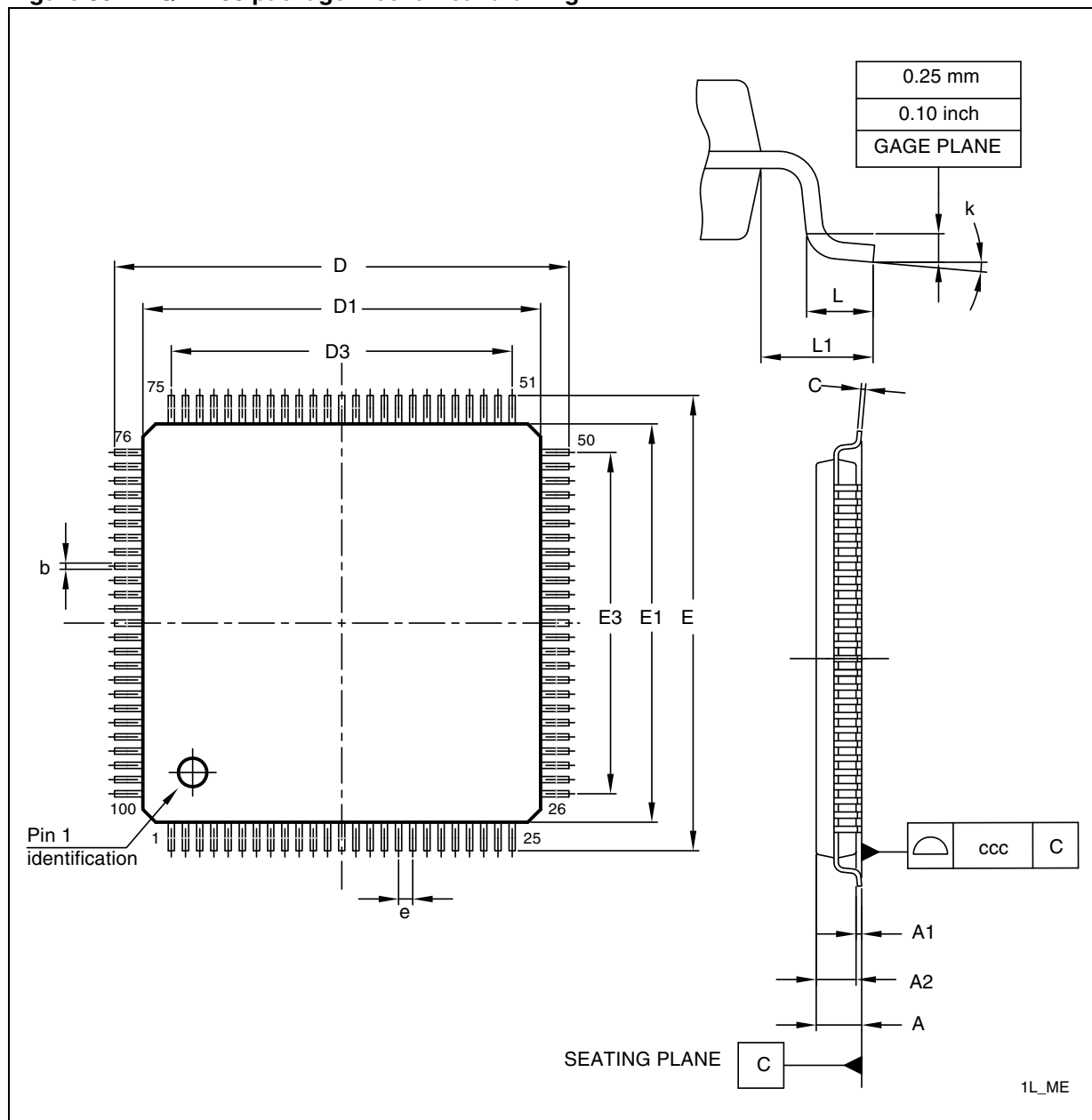


Table 43. LQFP100 package mechanical data

Symbol	Dimensions					
	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	—	—	1.600	—	—	0.0630
A1	0.050	—	0.150	0.0020	—	0.0059

Table 43. LQFP100 package mechanical data (continued)

Symbol	Dimensions					
	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	—	0.200	0.0035	—	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	—	12.000	—	—	0.4724	—
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	—	12.000	—	—	0.4724	—
e	—	0.500	—	—	0.0197	—
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	—	1.000	—	—	0.0394	—
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc ⁽²⁾	0.08			0.0031		

1. Values in inches are converted from millimeters (mm) and rounded to four decimal digits.

2. Tolerance

5 Ordering information

Table 44 shows the orderable part numbers for the SPC560P44Lx, SPC560P50Lx series.

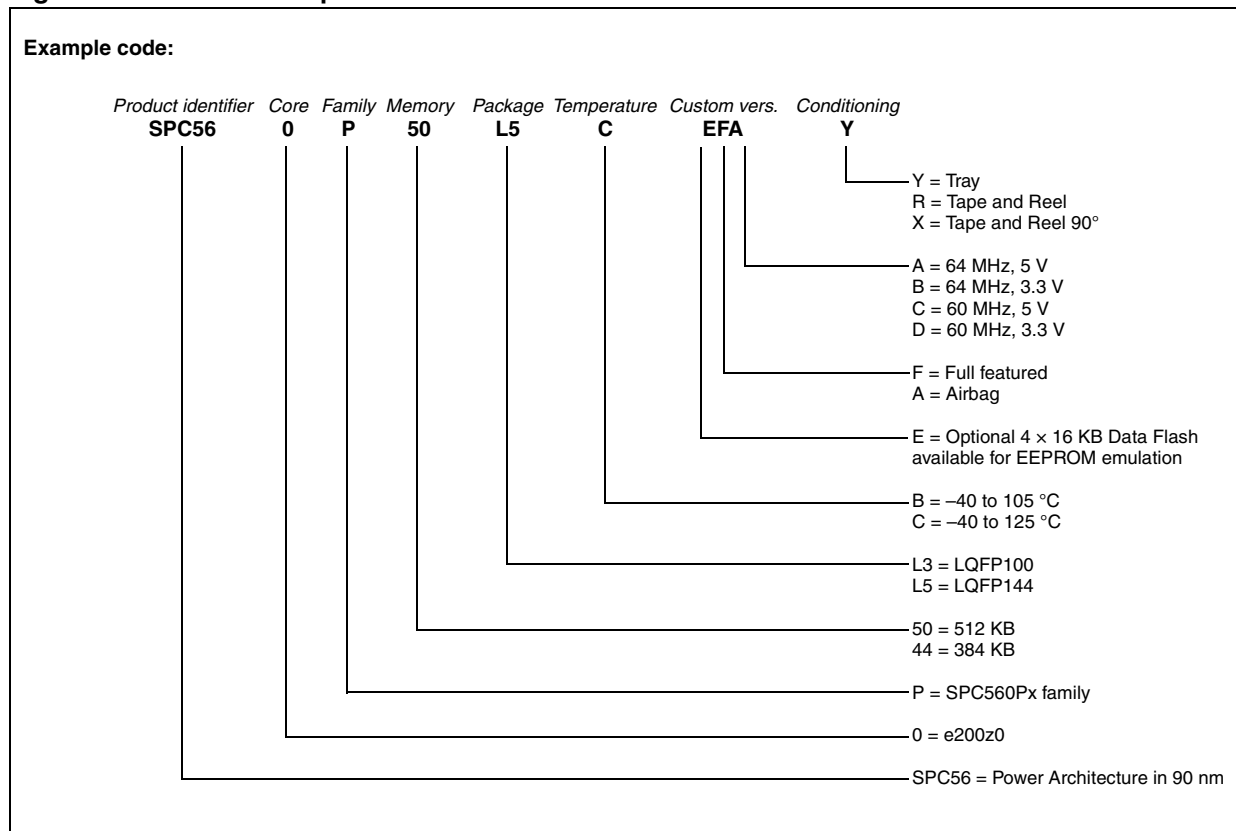
Table 44. Order codes

Order code	Flash memory		SRAM (KB)	Package	Characteristics
	Code	Data			
SPC560P44L3CEFAY	384 KB	4 × 16 KB	36	LQFP100	125 °C, Full featured, 5 V, 64 MHz
SPC560P44L3CEFAR					
SPC560P44L3CEFBY	384 KB	4 × 16 KB	36	LQFP100	125 °C, Full featured, 3.3 V, 64 MHz
SPC560P44L3CEFBR					
SPC560P44L3BEAAY	384 KB	4 × 16 KB	36	LQFP100	105 °C, Airbag, 5 V, 64 MHz
SPC560P44L3BEAAR					
SPC560P44L3BEABY	384 KB	4 × 16 KB	36	LQFP100	105 °C, Airbag, 3.3 V, 64 MHz
SPC560P44L3BEABR					
SPC560P44L5CEFAY	384 KB	4 × 16 KB	36	LQFP144	125 °C, Full featured, 5 V, 64 MHz
SPC560P44L5CEFAR					
SPC560P44L5CEFBY	384 KB	4 × 16 KB	36	LQFP144	125 °C, Full featured, 3.3 V, 64 MHz
SPC560P44L5CEFBR					
SPC560P44L5BEAAY	384 KB	4 × 16 KB	36	LQFP144	105 °C, Airbag, 5 V, 64 MHz
SPC560P44L5BEAAR					
SPC560P44L5BEABY	384 KB	4 × 16 KB	36	LQFP144	105 °C, Airbag, 3.3 V, 64 MHz
SPC560P44L5BEABR					
SPC560P50L3CEFAY	512 KB	4 × 16 KB	40	LQFP100	125 °C, Full featured, 5 V, 64 MHz
SPC560P50L3CEFAR					
SPC560P50L3CEFBY	512 KB	4 × 16 KB	40	LQFP100	125 °C, Full featured, 3.3 V, 64 MHz
SPC560P50L3CEFBR					
SPC560P50L3BEAAY	512 KB	4 × 16 KB	40	LQFP100	105 °C, Airbag, 5 V, 64 MHz
SPC560P50L3BEAAR					
SPC560P50L3BEABY	512 KB	4 × 16 KB	40	LQFP100	105 °C, Airbag, 3.3 V, 64 MHz
SPC560P50L3BEABR					
SPC560P50L3BEFBY	512 KB	4 × 16 KB	40	LQFP100	105 °C, Full featured, 3.3 V, 64 MHz
SPC560P50L3BEFBR					
SPC560P50L5CEFAY	512 KB	4 × 16 KB	40	LQFP144	125 °C, Full featured, 5 V, 64 MHz
SPC560P50L5CEFAR					
SPC560P50L5CEFBY	512 KB	4 × 16 KB	40	LQFP144	125 °C, Full featured, 3.3 V, 64 MHz
SPC560P50L5CEFBR					

Table 44. Order codes (continued)

Order code	Flash memory		SRAM (KB)	Package	Characteristics
	Code	Data			
SPC560P50L5BEAAY	512 KB	4 × 16 KB	40	LQFP144	105 °C, Airbag, 5 V, 64 MHz
SPC560P50L5BEAAR					
SPC560P50L5BEABY	512 KB	4 × 16 KB	40	LQFP144	105 °C, Airbag, 3.3 V, 64 MHz
SPC560P50L5BEABR					
SPC560P50L5BEFBY	512 KB	4 × 16 KB	40	LQFP144	105 °C, Full featured, 3.3 V, 64 MHz
SPC560P50L5BEFBR					

Figure 40. Commercial product code structure



Appendix A Abbreviations

Table 45 lists abbreviations used in this document.

Table 45. Abbreviations

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DUT	Device under test
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input/output
MC	Modulus counter
MCKO	Message clock out
MCU	Microcontroller unit
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NPN	Negative-positive-negative
NVUSRO	Non-volatile user options register
PTF	Post trimming frequency
PWM	Pulse width modulation
RBW	Resolution bandwidth
SCK	Serial communications clock
SOUT	Serial data out
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

Revision history

[Table 46](#) summarizes revisions to this document.

Table 46. Revision history

Date	Revision	Substantive changes
28-Aug-2008	1	Initial release
25-Nov-2008	2	<p>Table 7: TDO and TDI pins (Port pins B[4:5] are single function pins.</p> <p>Table 12, Table 13: Thermal characteristics added.</p> <p>Table 11, Table 12: EMI testing specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision.</p> <p>Table 16, Table 17, Table 19, Table 20: Supply current specifications split into separate tables for Normal mode and Airbag mode; data to be added in a later revision.</p> <p>Table 23:</p> <ul style="list-style-type: none"> ● Values for I_{OL} and I_{OH} (in Conditions column) changed. ● Max values for V_{OH_S}, V_{OH_M}, V_{OH_F} and V_{OH_SYM} deleted. ● V_{ILR} max value changed. ● I_{PUR} min and max values changed. <p>Table 27: Sensitivity value changed.</p> <p>Table 30: Most values in table changed.</p>
05-Mar-2009	3	<ul style="list-style-type: none"> ● Description of system requirements, controller characteristics and how controller characteristics are guaranteed updated. ● Electrical parameters updated. ● EMI characteristics are now in one table; values have been updated. ● ESD characteristics are now in one table. ● Electrical parameters are identified as either system requirements or controller characteristics. Method used to guarantee each controller characteristic is noted in table. ● AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections deleted

Table 46. Revision history (continued)

Date	Revision	Substantive changes
07-Jul-2009	4	<p>Through all document:</p> <ul style="list-style-type: none"> – Replaced all “RESET_B” occurrences with “$\overline{\text{RESET}}$” through all document. – AC Timings: 1149.1 (JTAG) Timing, Nexus Timing, External Interrupt Timing, and DSPI Timing sections inserted again. – Electrical parameters updated. <p><i>Section , Features:</i></p> <ul style="list-style-type: none"> – Specified LIN 2.1 in communications interfaces feature. <p><i>Table 2</i></p> <ul style="list-style-type: none"> – Added row for Data Flash. <p><i>Table 4</i></p> <ul style="list-style-type: none"> – Added a footnote regarding the decoupling capacitors. <p><i>Table 6</i></p> <ul style="list-style-type: none"> – Removed the “other function“ column. – Rearranged the contents. <p><i>Table 14</i></p> <ul style="list-style-type: none"> – Updated definition of Condition column. <p><i>Table 19</i></p> <ul style="list-style-type: none"> – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". <p><i>Table 21</i></p> <ul style="list-style-type: none"> – merged in an unique Table the power consumption data related to "Maximum mode" and "Airbag mode". <p><i>Table 29</i></p> <ul style="list-style-type: none"> – Updated the parameter definition of ΔRCMVAR. – Removed the condition definition of ΔRCMVAR. <p><i>Table 29</i></p> <ul style="list-style-type: none"> – Added $t_{\text{ADC_C}}$ and TUE rows. <p><i>Table 30</i></p> <ul style="list-style-type: none"> – Added $t_{\text{ADC_C}}$ and TUE rows. – Removed R_{sw2}. <p><i>Table 33</i></p> <ul style="list-style-type: none"> – Added. <p><i>Table 29</i></p> <ul style="list-style-type: none"> – Updated and added footnotes. <p><i>Section 3.16.1 RESET Pin Characteristics</i></p> <ul style="list-style-type: none"> – Replaces whole section. <p><i>Table 38</i></p> <ul style="list-style-type: none"> – Renamed the “Flash (KB)“ heading column in “Code Flash / Data Flash (EE) (KB)“ – Replaced the value of RAM from 32 to 36KB in the last four rows.

Table 46. Revision history (continued)

Date	Revision	Substantive changes
27-Oct-2009	5	<ul style="list-style-type: none"> - Added "Full Feature" and "Airbag" customization. - Removed B[4] and B[5] rows from "Pin muxing" table and inserted them on "System pins" table. - Updated package pinout. - Rewrote entirely section "Power Up/dpwn Sequencing" section. - Renamend "V_{DD_LV_PLL}" and "V_{SS_LV_PLL}" supply pins with respectively "V_{DD_LV_COR3}" and "V_{SS_LV_COR3}". - Added explicative figures on "Electrical characteristics" section. - Updated "Thermal characteristics" for 100-pin. - Proposed two different configuration of "voltage regulator. - Inserted Power Up/Down sequence. - Added explicative figures on "DC Electrical characteristics". - Added "I/O pad current specification" section. - Renamed the "Airbag mode" with "Typical mode"and updated the values on "supply current" tables. - Added more order code.
06-Apr-2010	6	<p>Inserted label of Y-axis in the "Independent ADC supply" figure. "Recommended Operating Conditions" tables: Moved the T_J row to "Absolute Maximum Ratings" table. Rewrite note 1 and 3</p> <p>Inserted Min a Typ value of C_{DEC2} on "Voltage Regulator Electrical Characteristics" table. Removed an useless duplicate of "Voltage Regulator Electrical Characteristics" table. Inserted the name of C_S into "Input Equivalent Circuit" figure. Removed leakage I_{vpp} from datasheet. Updated "Supply Current" tables. Added note on "Output pin transition times" table. Updated "Temperature Sensor Electrical Characteristics" table. Updated "16 MHz RC Oscillator Electrical Characteristics" table. Removed the note about the condition from "Flash read access timing" table. Removed the notes that assert the values need to be confirmed before validation.</p>
07-Apr-2011	7	<p>Formatting and editorial changes throughout Removed all content referencing Junction Temperature Sensor Cover page Features:</p> <ul style="list-style-type: none"> - CPU core—specified 64 MHz frequency - updated memory features - eTimer units: changed "up/down capabilities" to "up/down count capabilities" - ADC—changed "2 × 13 input channels" to "2 × 11 input channels, + 4 shared channels" - replaced "On-chip CAN/UART/FlexRay bootstrap loader" with "On-chip CAN/UART bootstrap loader" <p><i>Section 1: Introduction</i>: changed title (was: Overview); reorganized contents SPC560P44Lx, SPC560P50Lx device comparison:</p> <ul style="list-style-type: none"> - ADC feature: changed "16 channels" to "15-channel"; added footnote to to indicate that four channels are shared between the two ADCs - removed SPC560P40 column - changed "dual channel" to "selectable single or dual channel support" in FlexRay footnote - updated "eTimer" feature - updated footnote relative to "Digital power supply" feature

Table 46. Revision history (continued)

Date	Revision	Substantive changes
07-Apr-2011	7 (cont'd)	<p>SPC560P44Lx, SPC560P50Lx device configuration differences: Removed “temperature” row (temperature information is provided in Order codes)</p> <p>Updated SPC560P44Lx, SPC560P50Lx block diagram</p> <p>Added SPC560P44Lx, SPC560P50Lx series block summary</p> <p>Added Section 1.5 Feature details</p> <p>Section 2.1 Package pinouts: removed alternate functions from pinout diagrams</p> <p>Supply pins: updated descriptions of power supply pins (1.2 V)</p> <p>System pins: updated table</p> <p>Pin muxing: added rows “B[4]” and “B[5]”</p> <p>Section 3.3 Absolute maximum ratings: added voltage specifications to titles of Figure 5 and Figure 6; in Table 9, changed row “V_{SS_HV} / Digital Ground” to “V_{SS} / Device Ground”; updated symbols</p> <p>Section 3.4 Recommended operating conditions: added voltage specifications to titles of Figure 7 and Figure 8</p> <p>Recommended operating conditions (5.0 V), and Recommended operating conditions (3.3 V): changed row “V_{SS_HV} / Digital Ground” to “V_{SS} / Device Ground”; updated symbols</p> <p>Updated Section 3.5.1 Package thermal characteristics</p> <p>Updated Section 3.6 Electromagnetic interference (EMI) characteristics</p> <p>Section 3.8.1 Voltage regulator electrical characteristics: amended titles of Table 16 and Table 18</p> <p>Voltage regulator electrical characteristics (configuration without resistor on base) and Voltage regulator electrical characteristics (configuration with resistor on base): updated symbol and values for V_{DD_LV_REGCOR}</p> <p>Low voltage monitor electrical characteristics: Updated V_{MLVDDOK_H} max value—was 1.15 V; is 1.145 V</p> <p>Section 3.10 DC electrical characteristics: reorganized contents</p> <p>Updated Section 3.10.1 NVUSRO register (includes adding Section NVUSRO[OSCILLATOR_MARGIN] field description)</p> <p>Supply current (5.0 V, NVUSRO[PAD3V5V] = 0): updated symbols</p> <p>Corrected parameter descriptions in DC electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1):</p> <ul style="list-style-type: none"> – V_{OL_F}—was “Fast, high level output voltage”; is “Fast, low level output voltage” – V_{OL_SYM}—was “Symmetric, high level output voltage”; is “Symmetric, low level output voltage” <p>Supply current (3.3 V, NVUSRO[PAD3V5V] = 1): updated symbols</p> <p>Main oscillator output electrical characteristics (5.0 V, NVUSRO[PAD3V5V] = 0): replaced instances of EXTAL with XTAL</p> <p>Main oscillator output electrical characteristics (3.3 V, NVUSRO[PAD3V5V] = 1): replaced instances of EXTAL with XTAL</p> <p>FMPLL electrical characteristics: replaced “PLLMRFM” with “FMPLL” in table title; updated conditions; removed f_{sys} row; updated f_{FMPLLOUT} min value</p> <p>ADC conversion characteristics: updated symbols; added row t_{ADC_PU}</p> <p>Flash memory read access timing: added footnote to “Conditions” column</p> <p>Section 3.16.1 Pad AC specifications: added Pad output delay diagram</p> <p>In the range of figures “DSPI Classic SPI Timing — Master, CPHA = 0” to “DSPI PCS Strobe (PCSS) Timing”: added note</p> <p>Updated Order codes</p> <p>Updated “Commercial product code structure” figure</p> <p>Table 45: Added abbreviations “DUT”, “NPN”, and “RBW”</p>

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