



## SPZB32W1x2.1

### ZigBee™ PRO modules based on the STM32W chipset

#### Features

- 2.4 GHz IEEE 802.15.4-compliant SMD modules based on the ST single chip STM32W108CB featuring:
  - Integrated 2.4 GHz transceiver
  - PHY and MAC IEEE 802.15.4 features
  - Integrated ARM® Cortex-M3 core
  - Integrated 128 kB embedded Flash and 8 kB embedded RAM
  - Integrated encryption (AES-128) accelerator
  - +3 dBm output power (+8 dBm in boost mode)
  - -99 dBm receiver sensitivity
- Robust Wi-Fi and Bluetooth® coexistence
- 16 channels (IEEE 802.15.4 channel 11 to 26)
- 24 general purpose I/O lines including analogue inputs (all GPIOs of the STM32W108CB are accessible)
- Industry standard JTAG programming
- Deep sleep current of sub 1  $\mu$ A
- Onboard 24 MHz and 32.768 kHz stable Xtal
- Selectable chip integrated RC oscillator
- Multiple antenna options: integrated antenna (SPZB32W1A2.1) or integrated UFL connector (SPZB32W1C2.1)
- Single voltage supply (2.1 to 3.6 V)
- FCC and CE compliant qualified
- Small form factor: 16.4 x 26.5 mm
- Operating temperature range: -40 °C to +85 °C



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# 1 Description

SPZB32W1A2.1 and SPZB32W1C2.1 are ready-to-use ZigBee® modules optimized for embedded applications that require low data rate communications. The modules are very compact and enable OEMs to easily add wireless capabilities to electronic devices by optimizing time-to-market, cost, size, and consumption of their target applications. No RF experience or expertise is required to add this powerful wireless networking capability to the final product.

The modules are based on the ST STM32W108CB single chip which integrates a 2.4 GHz, IEEE 802.15.4-compliant transceiver together with an ARM® Cortex-M3 embedded processor.

24 MHz high stability Xtal is available aboard the modules to perform the timing requirements as per ZigBee specifications; additionally, a 32.768 kHz Xtal is also provided onboard for low power operation.

A single supply voltage is requested to power the modules. The supply is in the range of 2.8 to 3.6 V.

An innovative 2.5 GHz RF design and the relevant internal RF amplifier onboard ensure the optimal exploitation of the link budget, an excellent sensitivity and low power consumption for battery powered operation.

The voltage supply also determines the I/O port level, allowing an easy interface with additional peripherals.

To support user defined applications, a number of peripherals such as GPIO, UART, I<sup>2</sup>C, ADC, and general purpose timers are available through the 24 configurable general purpose I/O lines.

The modules can run the ZigBee PRO EmberZNet firmware packages (ZigBee PRO stack) which are accessible on the ST website.

Modules are available with two different antenna options:

- SPZB32W1A2.1, with an onboard integrated ceramic antenna
- SPZB32W1C2.1, with UFL RF connector for the connection of an external antenna.

*Note:* For details regarding STM32W108CB refer to the related datasheet available on the ST website.

## 2 RoHS compliance

ST modules are RoHS compliant and comply with ECOPACK<sup>®</sup> norms.

## 3 Application

- Smart energy applications
- Machine2Machine industrial control
- Wireless sensor networks
- Home/building automation
- Smart appliances
- Wireless alarms and security systems
- Lighting control
- Remote monitoring

# 4 Block diagram

Figure 1. SPZB32W1A2.1 block diagram

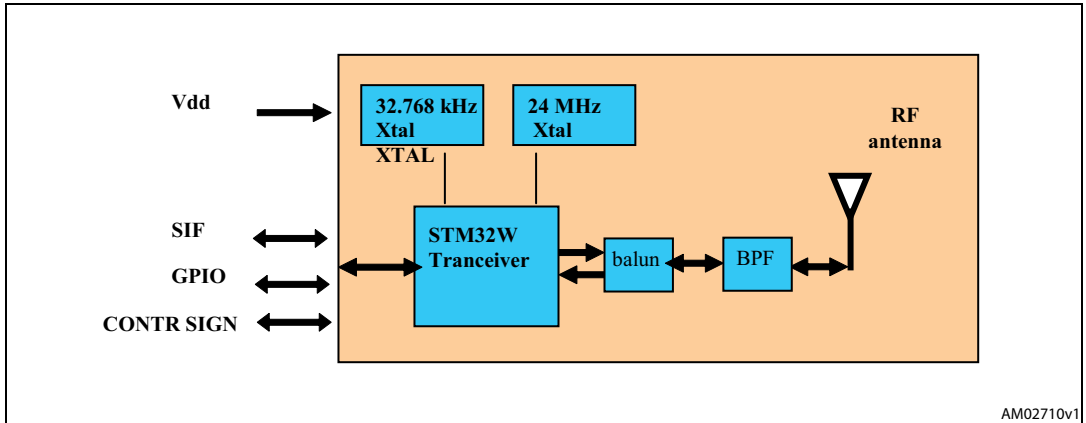
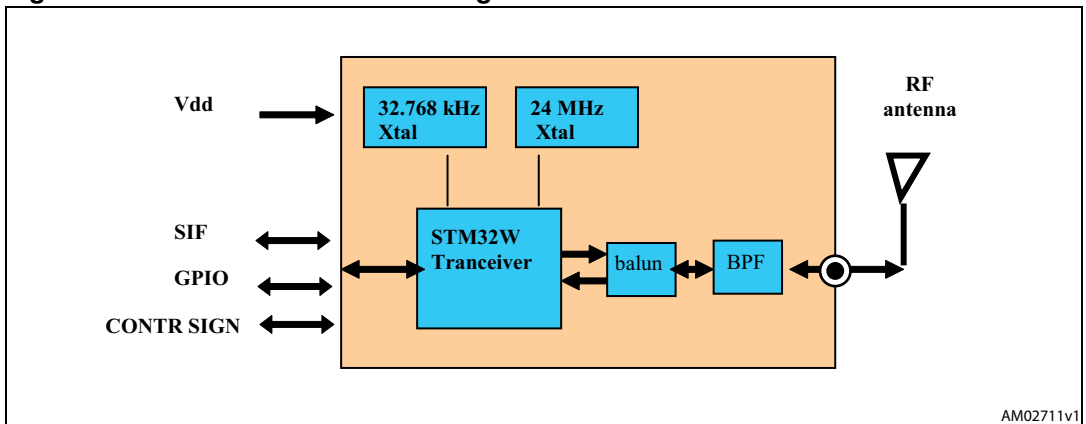


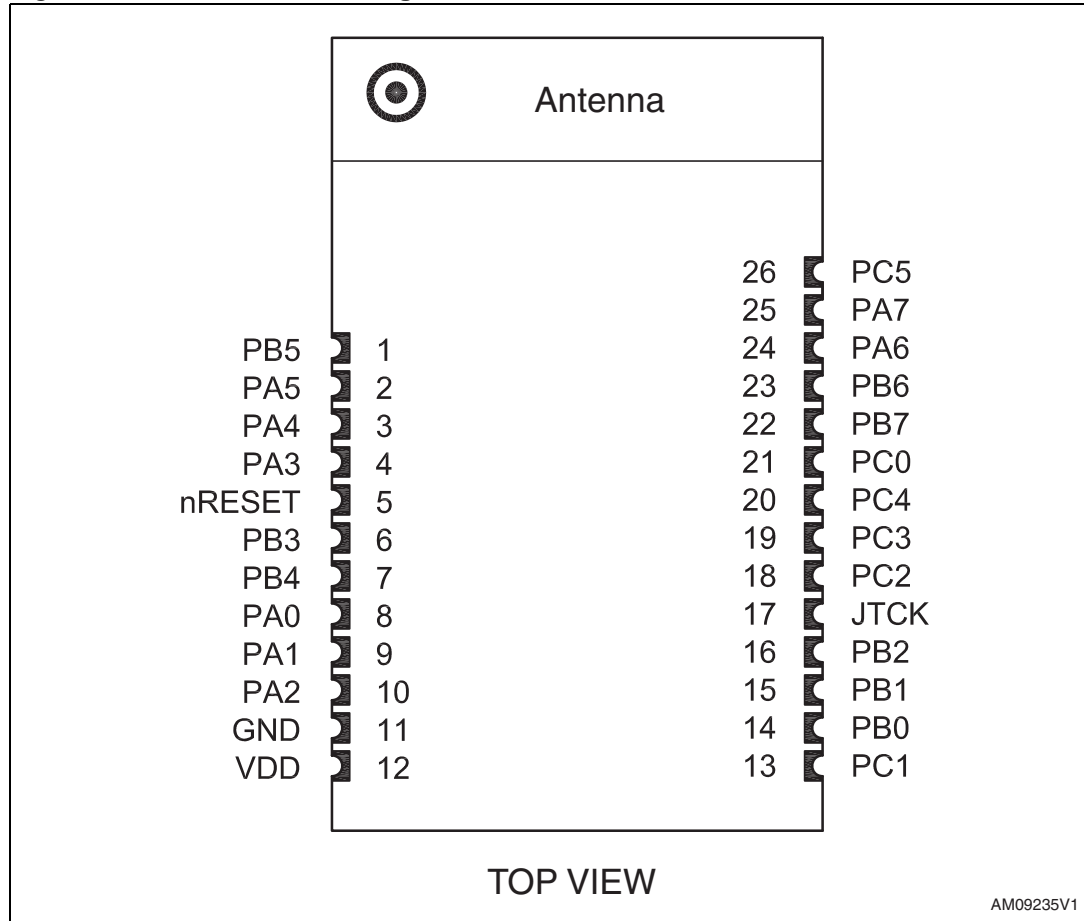
Figure 2. SPZB32W1C2.1 block diagram



## 5 Pin settings

### 5.1 Pin connections

Figure 3. Pin connection diagram





## 5.2 Pin description

Table 1. Pin description

Module pin n°	Pin name	Direction	STM32W pin	Description
1	PB5	I/O	43	Digital I/O
	ADC0	Analog	43	ADC input 0
	TIM2CLK	I	43	Timer 2 external clock input
	TIM1MSK	I	43	Timer 1 external clock mask input
2	PA5	I/O	27	Digital I/O
	ADC5	Analog	27	ADC input 1
	PTI_DATA	O	27	Frame signal of PTI (packet trace interface)
	nBOOTMODE	I	27	Embedded serial bootloader activation out of reset
	TRACEDATA3	O	27	Synchronous CPU trace data bit 3
3	PA4	I/O	26	Digital I/O
	ADC4	Analog	26	ADC input 0
	PTI_EN	O	26	Frame signal of PTI (packet trace interface)
	TRACEDATA2	O	26	Synchronous CPU trace data bit 2
4	PA3	I/O	25	Digital I/O
	SC2nSSEL	I	25	SPI slave select of serial controller 2
	TIM2_CH2	I/O	25	Timer 2 channel 2 output (or input - disable remap with TIM2_OR[5])
	TRACECLK	O	25	Synchronous CPU trace clock
5	nRESET	I	12	Active low reset (an internal pull-up of 30 kΩ typ. is provided)
6	PB3	I/O	19	Digital I/O
	UART_CTS	I	19	UART CTS handshake of serial controller 1
	SC1SCLK	I/O	19	SPI slave clock of serial controller SC1 / SPI master clock of serial controller SC1
	TIM2_CH3	I/O	19	Timer 2 channel 3 input / timer 2 channel 3 output

**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
7	PB4	I/O	20	Digital I/O
	UART_RTS	O	20	UART RTS handshake of serial controller 1
	TIM2_CH4	I/O	20	Timer 2 channel 4 input / timer 2 channel 4 output
	SC1nSSEL	I	20	SPI slave select of serial controller 1
8	PA0	I/O	21	Digital I/O
	SC2MOSI	O	21	SPI master data out of serial controller 2
	SC2MOSI	I	21	SPI slave data in of serial controller 2
	TIM2_CH1	I/O	21	Timer 2 channel 1 input / timer 2 channel 1 output
9	PA1	I/O	22	Digital I/O
	SC2MISO	I	22	SPI master data in of serial controller 2
	SC2MISO	O	22	SPI slave data out of serial controller 2
	SC2SDA	I/O	22	TWI (I <sup>2</sup> C) data of serial controller 2
	TIM2_CH3	I/O	22	Timer 2 channel 3 input / timer 2 channel 3 output
10	PA2	I/O	24	Digital I/O
	SC2SCLK	O	24	SPI master clock of serial controller 2
	SC2SCLK	I	24	SPI slave clock of serial controller 2
	SC2SCL	I/O	24	TWI (I <sup>2</sup> C) clock of serial controller 2
	TIM2_CH4	I/O	24	Timer 2 channel 4 input / timer 2 channel 4 output
11	GND	--	49	Ground
12	VDD	Power	16,23,28,37	Input power supply
13	PC1	I/O	38	Digital I/O
	ADC3	Analog	38	ADC input 3
	SWO	O	38	Serial wire output synchronous trace output to debugger
	TRACEDATA0	O	38	Synchronous CPU trace data bit 0



**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
14	PB0	I/O	36	Digital I/O
	VREF (O/I)	Analog	36	ADC reference output / ADC reference input
	TIM1CLK	I	36	Timer 1 external clock input
	TIM2MSK	I	36	Timer 2 external clock mask input
	IRQA	I	36	External interrupt source A
	TRACECLK	O	36	Synchronous CPU trace clock
15	PB1	I/O	30	Digital I/O
	SC1TXD	O	30	UART transmit data of serial controller 1
	SC1MOSI / SC1MISO	O	30	SPI master data out of serial controller 1 / SPI slave data out of serial controller 1
	SC1SDA	I/O	30	TWI (I2C) data of serial controller 1
	TIM2_CH1	I/O	30	Timer 2 channel 1 input / timer 2 channel 1 output
16	PB2	I/O	31	Digital I/O
	SC1RXD	I	31	UART receive data of serial controller 1
	SC1MISO / SC1MOSI	I	31	SPI master data in of serial controller SC1 / SPI slave data in of serial controller 1
	SC1SCL	I/O	31	TWI (I2C) clock of serial controller 1
	TIM2_CH2	I/O	31	Timer 2 channel 2 input / timer 2 channel 2 output
17	JTCK	I	32	JTAG clock input from debugger
	SWCLK	I/O	32	Serial wire clock input/output with debugger
18	PC2	I/O	33	Digital I/O
	JTDO	O	33	JTAG data out to debugger
	SWO	O	33	Serial wire output synchronous trace output to debugger
19	PC3	I/O	34	Digital I/O
	JTDI	I	34	JTAG data in from debugger
20	PC4	I/O	35	Digital I/O
	JTMS	I	35	JTAG mode select from debugger
	SWDIO	I/O	35	Serial wire bidirectional data to/from debugger

**Table 1. Pin description (continued)**

Module pin n°	Pin name	Direction	STM32W pin	Description
21	PC0	I/O	40	Digital I/O (high current)
	JRST	I	40	JTAG reset input from debugger
	TRACEDATA1	O	40	Synchronous CPU trace data bit 1
	IRQD	I	40	External interrupt source D
22	PB7	I/O	41	Digital I/O
	TIM1_CH2	O	41	Timer 1 channel 2 output
	TIM1_CH2	I	41	Timer 1 channel 2 input
	IRQC	I	41	External interrupt source C
	ADC2	I	41	ADC input 2
23	PB6	I/O	42	Digital I/O
	TIM1_CH1	O	42	Timer 1 channel 1 output
	TIM1_CH1	I	42	Timer 1 channel 1 input
	IRQB	I	42	External interrupt source B
	ADC1	Analog	42	ADC input 1
24	PA6	I/O	29	Digital I/O
	TIM1_CH3	O	29	Timer 1 channel 3 output
	TIM1_CH3	I	29	Timer 1 channel 3 input
25	PA7	I/O	18	Digital I/O
	TIM1_CH4	O	18	Timer 1 channel 4 output
	TIM1_CH4	I	18	Timer 1 channel 4 input
	REG_EN	O	18	External regulator open drain output (enabled after reset)
26	PC5	I/O	11	Digital I/O
	TX_ACTIVE	O	11	Logic level control for external Rx/Tx switch

## 6 Electrical characteristics

### 6.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V <sub>DD</sub>	Module supply voltage	- 0.3	3.6	V
V <sub>in</sub>	Input voltage on any digital pin	- 0.3	V <sub>DD</sub> + 0.3	V
T <sub>stg</sub>	Storage temperature	-40	+85	°C
T <sub>sold</sub>	Soldering temperature < 10s		250	°C

### 6.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Module supply voltage	-40 °C < T < +85 °C	2.8	3.3	3.6	V
T <sub>stg</sub>	Operating ambient temperature		-40		+85	°C

### 6.3 DC electrical characteristics

Table 4. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IRX	RX current	V <sub>DD</sub> = 3.3 V, T = 25 °C	-	28	-	mA
ITX	TX current	P <sub>o</sub> = 3 dBm, V <sub>DD</sub> = 3.3 V, T = 25 °C, F = 2450MHz	-	32	-	mA
IDS	Deep sleep current (32.768 kHz oscillator)	V <sub>DD</sub> = 3.3 V, T = 25 °C	-	1.3	-	μA

## 6.4 Digital I/O specifications

Table 5. Digital I/O specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Low level input voltage	$2.1 < V_{dd} < 3.6 \text{ V}$	0		$0.5 \times V_{dd}$	V
$V_{IH}$	High level input voltage	$2.1 < V_{dd} < 3.6 \text{ V}$	$0.62 \times V_{dd}$		$V_{dd}$	V
$I_{il}$	Input current for logic 0	$2.1 < V_{dd} < 3.6 \text{ V}$			-0.5	mA
$I_{ih}$	Input current for logic 1	$2.1 < V_{dd} < 3.6 \text{ V}$			0.5	mA
$R_{ipu}$	Input pull-up resistor			30		k $\Omega$
$R_{ipd}$	Input pull-down resistor			30		k $\Omega$
$V_{OL}$	Low level output voltage		0		$0.18 \times V_{dd}$	V
$V_{OH}$	High level output voltage		$0.82 \times V_{dd}$		$V_{dd}$	V
$I_{OHS}$	Output source current (standard)				4	mA
$I_{OLS}$	Output sink current (standard)				4	mA
$I_{OHH}$	Output source current (high current)				8	mA
$I_{OLH}$	Output sink current (high current)				8	mA
$I_{OTot}$	Total output current for I/O				40	mA

## 6.5 RF electrical characteristics

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Frequency range	$V_{dd} = 3.3 \text{ V}$ , $T = 25 \text{ }^\circ\text{C}$	2405		2480	MHz
TX	Output power	$V_{dd} = 3.3 \text{ V}$ , $T = 25 \text{ }^\circ\text{C}$		3	6	dBm
RX	Sensitivity	$V_{dd} = 3.3 \text{ V}$ , 1 % PER		-95	-97	dBm
	Adjacent channel rejection	$\pm 5 \text{ MHz}$ $\pm 10 \text{ MHz}$		35 40		dBm

# 7 Mechanical dimensions

Figure 4. Mechanical dimensions

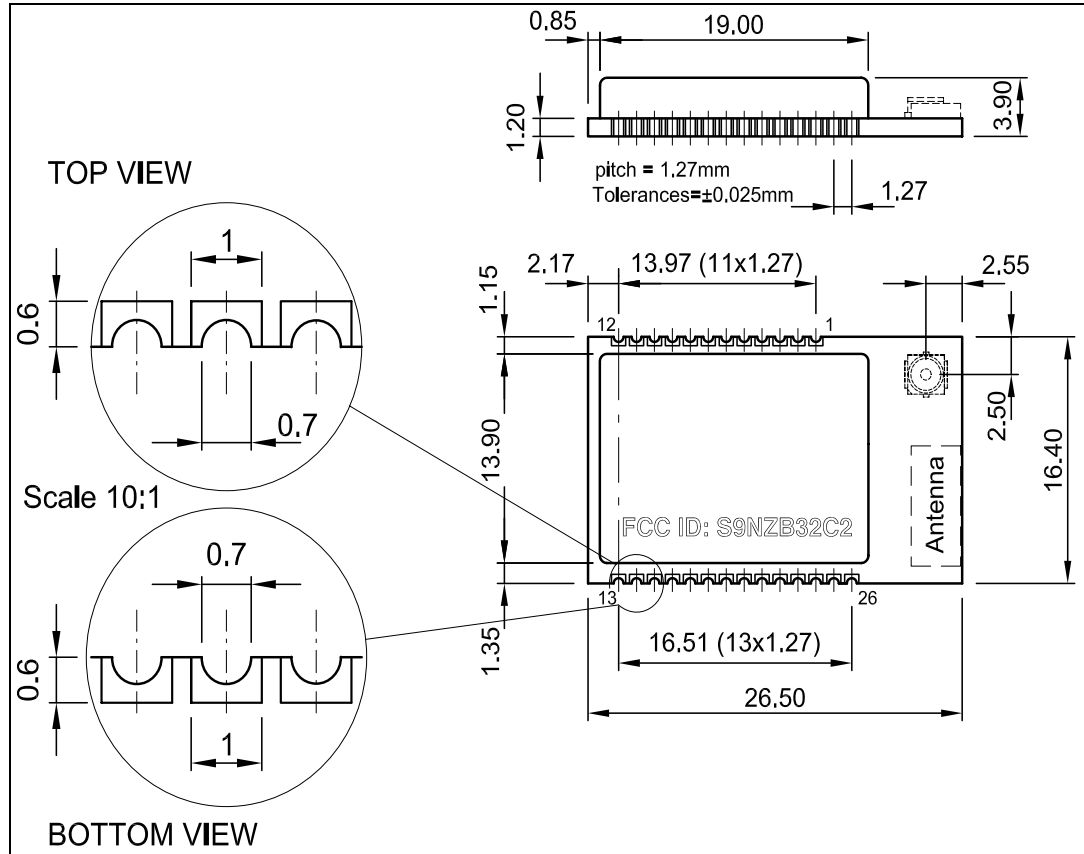
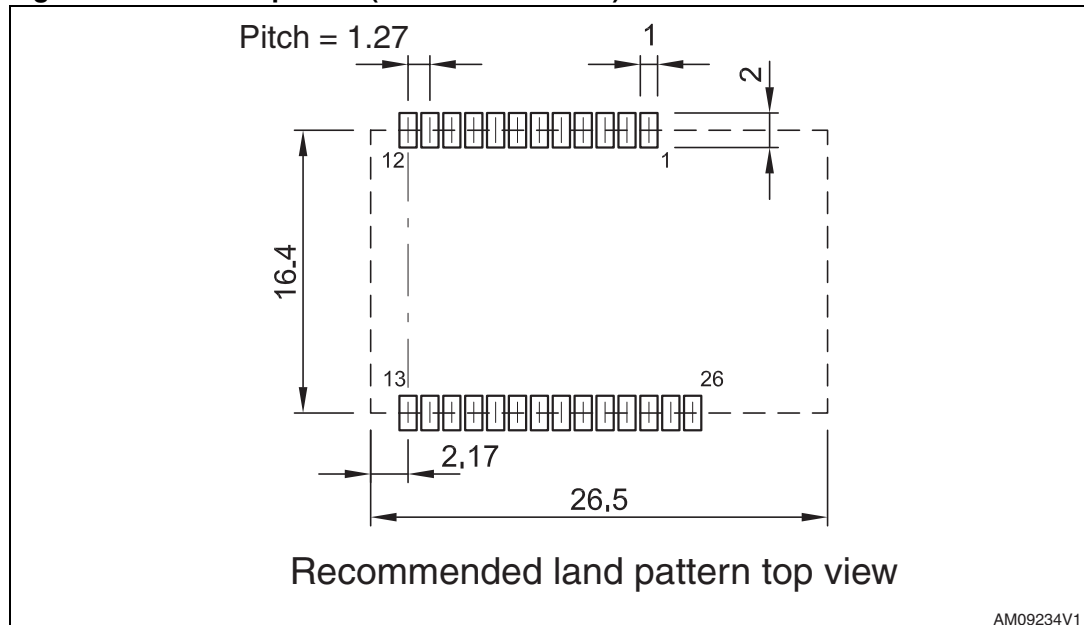


Figure 5. Pin land pattern (dimensions in mm)



AM09234V1



## 9 Product approvals

These modules have been designed to meet national regulations for world wide use. In particular the following certifications have been obtained

### 9.1 FCC approvals

The SPZB32W1A2.1 device, with integrated antenna, as well as the SPZB32W1C2.1, with the antenna specified in [Table 8](#), have been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate, radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference can not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment to an outlet on a circuit different from that to which the receiver is connected

Consult the dealer or an experienced radio/TV technician for help.

Module type: ZigBee<sup>®</sup> module, *SPZB32W1A2.1* / *SPZB32W1C2.1*

FCC-ID: S9NZB32C2

Modular type: single modular

**Table 8. FCC approvals**

ITEM	Part No.	Manufacturer
1	2010B4844-01 (Titanis Antenna)	Antenova

Any changes or modifications not expressly approved by the part responsible for compliance may cause the module to cease to comply with FCC rules part 15, and therefore render void the user's authority to operate the equipment.

While the applicant for a device into which the SPZB32W1A2.1 or the SPZB32W1C2.1 with the antenna specified in [Table 8](#) installed is not required to obtain new authorization for the module, this does not preclude the possibility that some other form of authorization or testing may be required for the end product.

### FCC labelling requirements

When integrating the SPZB32W1A2.1 / SPZB32W1C2.1 into the final product, it must be ensured that the FCC labelling requirements, as specified below, are satisfied.

Based on the Public Notice from FCC, the product into which the ST transmitter module is installed must display a label referring to the enclosed module.

The label should use wording such as “Contains Transmitter module FCC ID: S9NZB32C2 or “Contains FCC ID: S9NZB32C2, any similar wording that expressed the same meaning may be used.

An example is:

**Contains FCC ID: S9NZB32C2**

## 9.2 European certification

The SPZB32W1A2.1 and the SPZB32W1C2.1 devices are CE certified:



Expert opinion N. 0365-ARAKO0071 released by IMQ refers to the following normatives:

- Radio: EN300 328: V1.7.1: 2006-10
- EMS: EN301 489-17 v 2.1.1: 2009
- Safety: EN60950-1:2006 + A11:2009



# 10 Ordering information scheme

**Table 9. Ordering information scheme**

	SPZB	32W1	A	2	.1
ZigBee modules					
Based on STM32W108CB					
A: Integrated antenna					
C: Integrated UFL connector					
2: Normal TX range					
1: Long TX range					
ZigBee PRO (EmberZnet)					

## 11 Revision history

Table 10. Document revision history

Date	Revision	Changes
22-Jun-2011	1	Initial release.
25-Jul-2011	2	Updated single voltage supply in features on cover page. Updated <a href="#">Table 4: DC electrical characteristics</a> . Updated test conditions in <a href="#">Table 5: Digital I/O specifications</a> . Removed CFE parameter in <a href="#">Table 5: Digital I/O specifications</a> . Updated description of letter C in <a href="#">Table 9: Ordering information scheme</a> . Minor text changes.

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