



ST72321BLJ6-Auto

3.3V range 8-bit MCU for automotive with 32 Kbyte Flash,
10-bit ADC, 5 timers, SPI, SCI, I²C interface

Features

Memories

- 32 Kbyte dual voltage high density Flash (HDFlash) with readout protection capability (in-application programming and in-circuit programming for HDFlash devices)
- 512 bytes to 1 Kbyte RAM
- HDFlash endurance: 100 cycles, data retention 20 years

Clock, reset and supply management

- Clock sources: Crystal/ceramic resonator oscillators, internal RC oscillator and bypass for external clock
- PLL for 2x frequency multiplication
- 4 power saving modes: Halt, active halt, wait and slow

Interrupt management

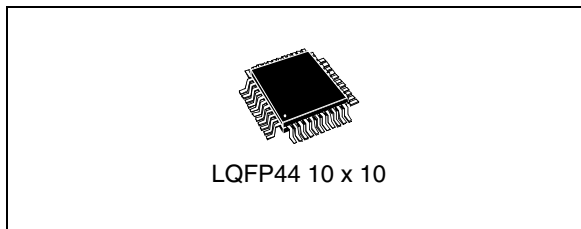
- Nested interrupt controller
- 10 interrupt vectors plus TRAP and reset
- 9/6 external interrupt lines (on 4 vectors)

Up to 32 I/O ports

- 32/24 multifunctional bidirectional I/O lines
- 22/17 alternate function lines
- 12/10 high sink outputs

5 timers

- Main clock controller with real-time base, beep and clock-out capabilities
- Configurable watchdog timer



- 16-bit timer A with 1 input capture, 1 output compare, external clock input, PWM and pulse generator modes
- 16-bit timer B with 2 input captures, 2 output compares, PWM and pulse generator modes
- 8-bit PWM auto-reload timer with 2 input captures, 4 PWM outputs, output compare and time base interrupt, external clock with event detector

3 communication interfaces

- SPI synchronous serial interface
- SCI asynchronous serial interface
- I²C multimaster interface

1 analog peripheral (low current coupling)

- 10-bit ADC with up to 12 robust input ports

Instruction set

- 8-bit data manipulation
- 63 basic instructions
- 17 main addressing modes
- 8 x 8 unsigned multiply instruction

Development tools

- Full HW/SW development package
- In-circuit testing capability

Table 1. Device summary

Device	Program memory	RAM (stack)	Oper. voltage	Temp. range	Package
ST72321BLJ6-Auto	Flash 32 Kbytes	1024 (256) bytes	3.0 to 3.6V	-40 to +85°C	LQFP44 10x10

Contents

1	Description	14
2	Package pinout and pin description	15
3	Register and memory map	18
4	Flash program memory	22
4.1	Introduction	22
4.2	Main features	22
4.3	Structure	22
4.3.1	Readout protection	23
4.4	ICC interface	23
4.5	In-circuit programming (ICP)	24
4.6	In-application programming (IAP)	25
4.7	Related documentation	25
4.7.1	Register description	25
5	Central processing unit	26
5.1	Introduction	26
5.2	Main features	26
5.3	CPU registers	26
6	Supply, reset and clock management	31
6.1	Introduction	31
6.2	Main features	31
6.3	Phase locked loop	31
6.4	Multi-oscillator (MO)	32
6.4.1	External clock source	32
6.4.2	Crystal/ceramic oscillators	32
6.4.3	Internal RC oscillator	32
6.5	Reset sequence manager (RSM)	33
6.5.1	Introduction	33
6.5.2	Asynchronous external $\overline{\text{RESET}}$ pin	34

6.5.3	External power-on reset	35
6.5.4	Internal watchdog reset	35
7	Interrupts	36
7.1	Introduction	36
7.2	Masking and processing flow	36
7.2.1	Servicing pending interrupts	38
7.2.2	Different interrupt vector sources	38
7.2.3	Non-maskable sources	39
7.2.4	Maskable sources	39
7.3	Interrupts and low power modes	40
7.4	Concurrent and nested management	40
7.5	Interrupt registers	41
7.6	Interrupt related instructions	43
7.7	External interrupts	43
7.7.1	I/O port interrupt sensitivity	43
7.8	External interrupt control register (EICR)	45
7.9	Nested interrupts register map and reset value	47
7.10	Interrupt mapping	47
8	Power saving modes	48
8.1	Introduction	48
8.2	Slow mode	48
8.3	Wait mode	49
8.4	Active halt and halt modes	50
8.4.1	Active halt mode	51
8.4.2	Halt mode	52
9	I/O ports	56
9.1	Introduction	56
9.2	Functional description	56
9.2.1	Input modes	56
9.2.2	Output modes	57
9.2.3	Alternate functions	57
9.3	I/O port implementation	60

9.4	Low power modes	61
9.5	Interrupts	61
10	On-chip peripherals	63
10.1	Watchdog timer (WDG)	63
10.1.1	Introduction	63
10.1.2	Main features	63
10.1.3	Functional description	63
10.1.4	How to program the watchdog timeout	64
10.1.5	Low power modes	66
10.1.6	Hardware watchdog option	66
10.1.7	Using halt mode with the WDG (WDGHALT option)	66
10.1.8	Interrupts	66
10.1.9	Control register (WDGCR)	67
10.1.10	Watchdog timer register map and reset values	67
10.2	Main clock controller with real-time clock and beeper (MCC/RTC)	67
10.2.1	Programmable CPU clock prescaler	67
10.2.2	Clock-out capability	68
10.2.3	Real-time clock timer (RTC)	68
10.2.4	Beeper	68
10.2.5	Low power modes	69
10.2.6	Interrupts	69
10.2.7	MCC/RTC registers	70
10.2.8	MCC register map and reset values	72
10.3	PWM auto-reload timer (ART)	72
10.3.1	Introduction	72
10.3.2	Functional description	73
10.3.3	ART registers	78
10.4	16-bit timer	83
10.4.1	Introduction	83
10.4.2	Main features	83
10.4.3	Functional description	84
10.4.4	Low power modes	97
10.4.5	Interrupts	97
10.4.6	Summary of timer modes	98
10.4.7	16-bit timer registers	98

10.5	Serial peripheral interface (SPI)	106
10.5.1	Introduction	106
10.5.2	Main features	106
10.5.3	General description	106
10.5.4	Clock phase and clock polarity	111
10.5.5	Error flags	113
10.5.6	Low power modes	115
10.5.7	Interrupts	116
10.5.8	SPI registers	116
10.6	Serial communications interface (SCI)	120
10.6.1	Introduction	120
10.6.2	Main features	120
10.6.3	General description	121
10.6.4	Functional description	123
10.6.5	Low power modes	133
10.6.6	Interrupts	133
10.6.7	SCI registers	134
10.7	I ² C bus interface (I ² C)	142
10.7.1	Introduction	142
10.7.2	Main features	142
10.7.3	General description	142
10.7.4	Functional description	145
10.7.5	Low power modes	150
10.7.6	Interrupts	150
10.7.7	Register description	151
10.8	10-bit A/D converter (ADC)	159
10.8.1	Introduction	159
10.8.2	Main features	159
10.8.3	Functional description	160
10.8.4	Low power modes	161
10.8.5	Interrupts	161
10.8.6	10-bit ADC registers	161
11	Instruction set	164
11.1	CPU addressing modes	164
11.1.1	Inherent instructions	166
11.1.2	Immediate instructions	166

11.1.3	Direct instructions	167
11.1.4	Indexed instructions (no offset, short, long)	167
11.1.5	Indirect instructions (short, long)	167
11.1.6	Indirect indexed instructions (short, long)	168
11.1.7	Relative mode instructions (direct, indirect)	169
11.2	Instruction groups	169
11.3	Using a prebyte	170
12	Electrical characteristics	173
12.1	Parameter conditions	173
12.1.1	Minimum and maximum values	173
12.1.2	Typical values	173
12.1.3	Typical curves	173
12.1.4	Loading capacitor	173
12.1.5	Pin input voltage	174
12.2	Absolute maximum ratings	174
12.2.1	Voltage characteristics	174
12.2.2	Current characteristics	175
12.2.3	Thermal characteristics	175
12.3	Operating conditions	176
12.4	Supply current characteristics	177
12.4.1	Current consumption	177
12.4.2	Supply and clock managers	180
12.4.3	On-chip peripherals	180
12.5	Clock and timing characteristics	181
12.5.1	General timings	181
12.5.2	External clock source	181
12.5.3	Crystal and ceramic resonator oscillators	182
12.5.4	RC oscillators	183
12.5.5	PLL characteristics	183
12.6	Memory characteristics	185
12.6.1	RAM and hardware registers	185
12.6.2	Flash memory	185
12.7	Electromagnetic compatibility (EMC) characteristics	186
12.7.1	Functional electromagnetic susceptibility (EMS)	186
12.7.2	Electromagnetic interference (EMI)	187

12.7.3	Absolute maximum ratings (electrical sensitivity)	188
12.8	I/O port pin characteristics	189
12.8.1	General characteristics	189
12.8.2	Output driving current	191
12.9	Control pin characteristics	194
12.9.1	Asynchronous $\overline{\text{RESET}}$ pin	194
12.9.2	ICCSEL/V _{PP} pin	195
12.10	Timer peripheral characteristics	195
12.10.1	16-bit timer	195
12.11	Communication interface characteristics	196
12.11.1	Serial peripheral interface (SPI)	196
12.11.2	I ² C - inter IC control interface	199
12.12	10-bit ADC characteristics	201
12.12.1	Analog power supply and reference pins	202
12.12.2	General PCB design guidelines	203
12.12.3	ADC accuracy	204
13	Package characteristics	205
13.1	Package mechanical data	205
13.2	Thermal characteristics	206
13.3	Soldering information	206
14	Device configuration and ordering information	207
14.1	Introduction	207
14.2	Flash devices	207
14.2.1	Flash configuration	207
14.2.2	Flash ordering information	209
14.3	FASTROM device ordering information and transfer of customer code	209
14.4	Development tools	212
14.4.1	Introduction	212
14.4.2	Evaluation tools and starter kits	212
14.4.3	Development and debugging tools	212
14.4.4	Programming tools	212
14.4.5	Socket and emulator adapter information	213
14.5	ST7 application notes	213

15	Known limitations	214
15.1	All Flash devices	214
15.1.1	Safe connection of OSC1/OSC2 pins	214
15.1.2	External interrupt missed	214
15.1.3	Unexpected reset fetch	216
15.1.4	Clearing active interrupts outside interrupt routine	216
15.1.5	16-bit timer PWM mode	217
15.1.6	TIMD set simultaneously with OC interrupt	217
15.1.7	SCI wrong break duration	218
15.1.8	I ² C multimaster	218
15.1.9	I ² C exit from halt/active halt	218
16	Revision history	219

List of tables

Table 1.	Device summary	1
Table 2.	Device pin description (LQFP44)	16
Table 3.	Hardware register map	19
Table 4.	Sectors available in Flash devices	22
Table 5.	Flash control/status register address and reset value	25
Table 6.	CC register description	28
Table 7.	ST7 clock source	33
Table 8.	Interrupt software priority levels	37
Table 9.	CPU CC register description.	41
Table 10.	ISPRx interrupt vector correspondence	42
Table 11.	Dedicated interrupt instruction set	43
Table 12.	EICR register description	45
Table 13.	Nested interrupts register map and reset values	47
Table 14.	Interrupt mapping	47
Table 15.	Active halt and halt power saving modes	50
Table 16.	DR register value and output pin status	57
Table 17.	I/O port mode options	58
Table 18.	I/O port configurations	59
Table 19.	Port register configurations.	61
Table 20.	Effect of low power modes on I/O ports	61
Table 21.	I/O interrupt control/wake-up capability	61
Table 22.	I/O port register map and reset values	62
Table 23.	Effect of low power modes on watchdog timer	66
Table 24.	WDGCR register description	67
Table 25.	Watchdog timer register map and reset values	67
Table 26.	Effect of low power modes on MCC/RTC	69
Table 27.	MCC/RTC interrupt control/wake-up capability.	69
Table 28.	MCCSR register description	70
Table 29.	MCCBCR register description.	71
Table 30.	Main clock controller register map and reset values.	72
Table 31.	ARTCSR register description	78
Table 32.	Prescaler selection for ART	79
Table 33.	ARTCAR register description	79
Table 34.	ARTAAR register description	79
Table 35.	PWM frequency versus resolution	80
Table 36.	PWMCR register description	80
Table 37.	PWM output signal polarity selection	80
Table 38.	PWMDCRx register description	81
Table 39.	ARTICCSR register description	81
Table 40.	ARTICRx register description	82
Table 41.	PWM auto-reload timer register map and reset values.	82
Table 42.	Effect of low power modes on 16-bit timer	97
Table 43.	16-bit timer interrupt control/wake-up capability	97
Table 44.	Summary of timer modes	98
Table 45.	CR1 register description	98
Table 46.	CR2 register description	100
Table 47.	CSR register description.	101
Table 48.	16-bit timer register map and reset values	105

Table 49.	Effect of low power modes on SPI	115
Table 50.	SPI interrupt control/wake-up capability	116
Table 51.	SPICR register description	116
Table 52.	SPICSR register description	118
Table 53.	SPI register map and reset values	120
Table 54.	Frame formats	131
Table 55.	Effect of low power modes on SCI	133
Table 56.	SCI interrupt control/wake-up capability	133
Table 57.	SCISR register description	134
Table 58.	SCICR1 register description	136
Table 59.	SCICR2 register description	137
Table 60.	SCIBRR register description	139
Table 61.	SCIERP register description	140
Table 62.	SCIETPR register description	140
Table 63.	Baud rate selection	141
Table 64.	SCI register map and reset values	141
Table 65.	Effect of low power modes on I2C	150
Table 66.	I2C interrupt control/wake-up capability	150
Table 67.	CR register description	151
Table 68.	SR1 register description	152
Table 69.	SR2 register description	154
Table 70.	CCR register description	156
Table 71.	DR register description	156
Table 72.	OAR1 register description	157
Table 73.	OAR2 register description	158
Table 74.	I2C register map and reset values	158
Table 75.	Effect of low power modes on 10-bit ADC	161
Table 76.	ADCCSR register description	161
Table 77.	ADCDRH register description	162
Table 78.	ADCDRL register description	163
Table 79.	ADC register map and reset values	163
Table 80.	CPU addressing mode groups	164
Table 81.	CPU addressing mode overview	165
Table 82.	Inherent instructions	166
Table 83.	Immediate instructions	166
Table 84.	Instructions supporting direct, indexed, indirect and indirect indexed addressing modes	168
Table 85.	Short instructions and functions	168
Table 86.	Relative mode instructions (direct and indirect)	169
Table 87.	Instruction groups	169
Table 88.	Instruction set overview	171
Table 89.	Voltage characteristics	174
Table 90.	Current characteristics	175
Table 91.	Thermal characteristics	175
Table 92.	General operating conditions	176
Table 93.	Current consumption	177
Table 94.	Oscillators, PLL and LVD current consumption	180
Table 95.	On-chip peripherals	180
Table 96.	General timings	181
Table 97.	External clock source	181
Table 98.	Oscillator parameters	182
Table 99.	Examples of typical resonators	183
Table 100.	RC oscillators	183

Table 101.	PLL characteristics	183
Table 102.	RAM and hardware registers	185
Table 103.	Characteristics of dual voltage HDFlash memory	185
Table 104.	Electromagnetic test results	186
Table 105.	EMI emissions	187
Table 106.	ESD absolute maximum ratings	188
Table 107.	Latch-up results	188
Table 108.	I/O general port pin characteristics	189
Table 109.	Output driving current	191
Table 110.	Asynchronous RESET pin	194
Table 111.	ICCSEL/VPP pin characteristics	195
Table 112.	16-bit timer	195
Table 113.	SPI characteristics	196
Table 114.	I ² C control interface characteristics	199
Table 115.	SCL frequency table	200
Table 116.	10-bit ADC characteristics	201
Table 117.	ADC accuracy with V _{DD} = 3.3V	204
Table 118.	44-pin low profile quad flat package mechanical data	205
Table 119.	Thermal characteristics	206
Table 120.	Soldering compatibility (wave and reflow soldering process)	206
Table 121.	Flash option bytes	207
Table 122.	Option byte 0 description	207
Table 123.	Option byte 1 description	208
Table 124.	Flash user programmable device types	209
Table 125.	FASTROM factory coded device types	210
Table 126.	Development tool order codes for the ST72321BL family	213
Table 127.	Suggested list of socket types	213
Table 128.	Document revision history	219

List of figures

Figure 1.	Device block diagram	14
Figure 2.	44-pin LQFP 10x10 package pinout	15
Figure 3.	Memory map	18
Figure 4.	Memory map and sector address	23
Figure 5.	Typical ICC interface	24
Figure 6.	CPU registers	26
Figure 7.	Stack manipulation example	30
Figure 8.	Clock, reset and supply block diagram	31
Figure 9.	Reset sequence phases	34
Figure 10.	Reset block diagram	34
Figure 11.	Reset sequences	35
Figure 12.	Interrupt processing flowchart	37
Figure 13.	Priority decision process	38
Figure 14.	Concurrent interrupt management	40
Figure 15.	Nested interrupt management	41
Figure 16.	External interrupt control bits	44
Figure 17.	Power saving mode transitions	48
Figure 18.	Slow mode clock transitions	49
Figure 19.	Wait mode flowchart	50
Figure 20.	Active halt timing overview	51
Figure 21.	Active halt mode flowchart	52
Figure 22.	Halt timing overview	53
Figure 23.	Halt mode flowchart	54
Figure 24.	I/O port general block diagram	58
Figure 25.	Interrupt I/O port state transitions	60
Figure 26.	Watchdog block diagram	64
Figure 27.	Approximate timeout duration	64
Figure 28.	Exact timeout duration (t_{min} and t_{max})	65
Figure 29.	Main clock controller (MCC/RTC) block diagram	68
Figure 30.	PWM auto-reload timer block diagram	73
Figure 31.	Output compare control	74
Figure 32.	PWM auto-reload timer function	75
Figure 33.	PWM signal from 0% to 100% duty cycle	76
Figure 34.	External event detector example (3 counts)	76
Figure 35.	Input capture timing diagram	77
Figure 36.	Timer block diagram	85
Figure 37.	16-bit read sequence	86
Figure 38.	Counter timing diagram, internal clock divided by 2	87
Figure 39.	Counter timing diagram, internal clock divided by 4	87
Figure 40.	Counter timing diagram, internal clock divided by 8	87
Figure 41.	Input capture block diagram	89
Figure 42.	Input capture timing diagram ⁽¹⁾	89
Figure 43.	Output compare block diagram	92
Figure 44.	Output compare timing diagram, $f_{TIMER} = f_{CPU}/2$	92
Figure 45.	Output compare timing diagram, $f_{TIMER} = f_{CPU}/4$	92
Figure 46.	One pulse mode sequence	93
Figure 47.	One pulse mode timing example ⁽¹⁾	94
Figure 48.	Pulse width modulation mode timing example with 2 output compare functions ⁽¹⁾	95

Figure 49.	Pulse width modulation cycle	96
Figure 50.	Serial peripheral interface block diagram	107
Figure 51.	Single master/single slave application	108
Figure 52.	Generic \overline{SS} timing diagram	109
Figure 53.	Hardware/software slave select management	109
Figure 54.	Data clock timing diagram	112
Figure 55.	Clearing the WCOL bit (write collision flag) software sequence	114
Figure 56.	Single master/multiple slave configuration	115
Figure 57.	SCI block diagram	122
Figure 58.	Word length programming	124
Figure 59.	SCI baud rate and extended prescaler block diagram	128
Figure 60.	Bit sampling in reception mode	133
Figure 61.	I ² C bus protocol	143
Figure 62.	I ² C interface block diagram	144
Figure 63.	Transfer sequencing	149
Figure 64.	Interrupt control logic diagram	150
Figure 65.	ADC block diagram	159
Figure 66.	Pin loading conditions	173
Figure 67.	Pin input voltage	174
Figure 68.	f_{CPU} max versus V_{DD}	176
Figure 69.	Typical I_{DD} in run mode	178
Figure 70.	Typical I_{DD} in slow mode	178
Figure 71.	Typical I_{DD} in wait mode	179
Figure 72.	Typical I_{DD} in slow wait mode	179
Figure 73.	Typical application with an external clock source	181
Figure 74.	Typical application with a crystal or ceramic resonator	182
Figure 75.	Integrated PLL jitter vs signal frequency	184
Figure 76.	Unused I/O pins configured as input	190
Figure 77.	Typical I_{PU} versus V_{DD} with $V_{IN} = V_{SS}$	190
Figure 78.	Typical V_{OL} versus I_{IO} at $V_{DD} = 3.3V$ (standard ports)	191
Figure 79.	Typical V_{OL} versus I_{IO} at $V_{DD} = 3.3V$ (high-sink ports)	192
Figure 80.	Typical V_{OH} versus I_{IO} at $V_{DD} = 3.3V$	192
Figure 81.	Typical V_{OL} versus V_{DD} at $I_{IO} = 2mA$	192
Figure 82.	Typical V_{OL} versus V_{DD} at $I_{IO} = 8mA$ (high-sink ports)	193
Figure 83.	Typical V_{OH} versus V_{DD} at $I_{IO} = -2mA$	193
Figure 84.	RESET pin protection	194
Figure 85.	Two typical applications with ICCSEL/ V_{PP} pin	195
Figure 86.	SPI slave timing diagram with CPHA = 0	197
Figure 87.	SPI slave timing diagram with CPHA = 1	197
Figure 88.	SPI master timing diagram	198
Figure 89.	Typical application with I ² C bus and timing diagram(1)	200
Figure 90.	R_{AIN} maximum versus f_{ADC} with $C_{AIN} = 0pF$	201
Figure 91.	Recommended C_{AIN} and R_{AIN} values	201
Figure 92.	Typical A/D converter application	202
Figure 93.	Power supply filtering	203
Figure 94.	ADC accuracy characteristics	204
Figure 95.	44-pin low profile quad flat package outline	205
Figure 96.	Flash commercial product code structure	209
Figure 97.	FASTROM commercial product code structure	210

1 Description

The ST72321BLJ6-Auto device is a member of the ST7 microcontroller family designed for mid-range automotive applications running at 3.3V.

All devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set and are available with Flash memory. The ST7 family architecture offers both power and flexibility to software developers, enabling the design of highly efficient and compact application code.

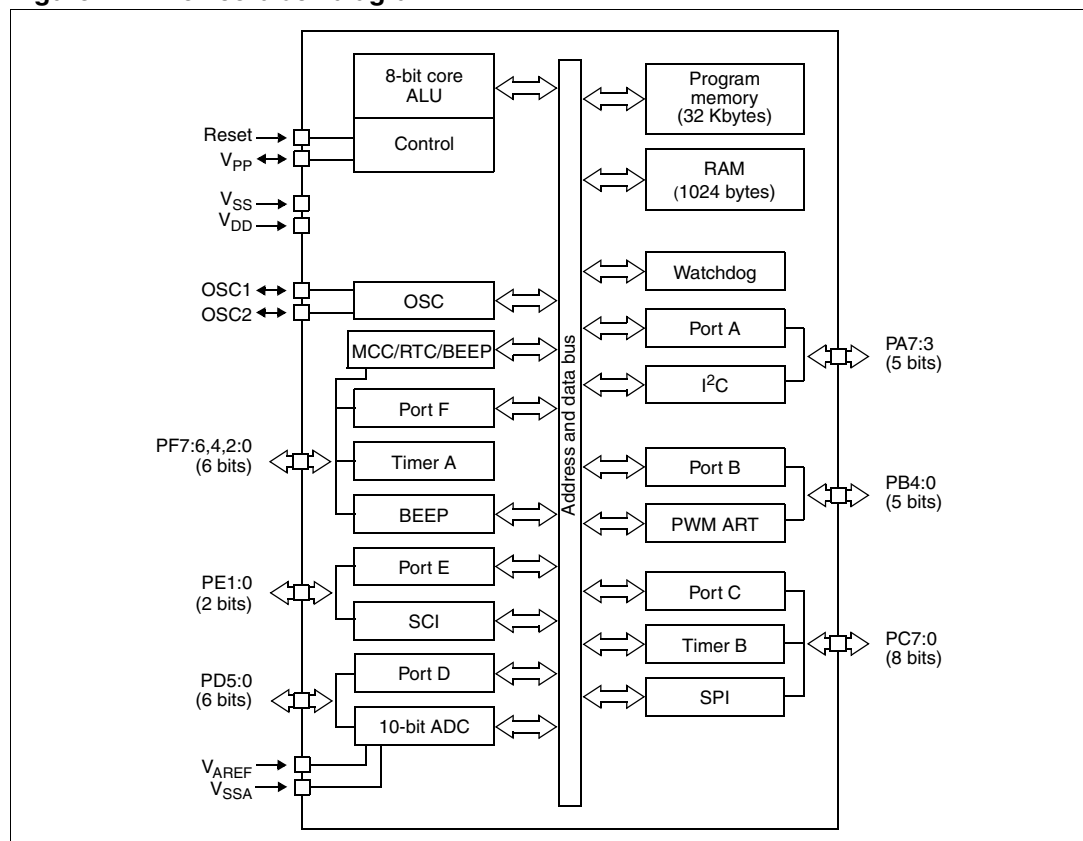
The on-chip peripherals include an A/D converter, a PWM autoreload timer, two general purpose timers, SPI, SCI and I²C interface.

For power economy, the microcontroller can switch dynamically into wait, slow, active halt or halt mode when the application is in idle or standby state.

Typical applications include:

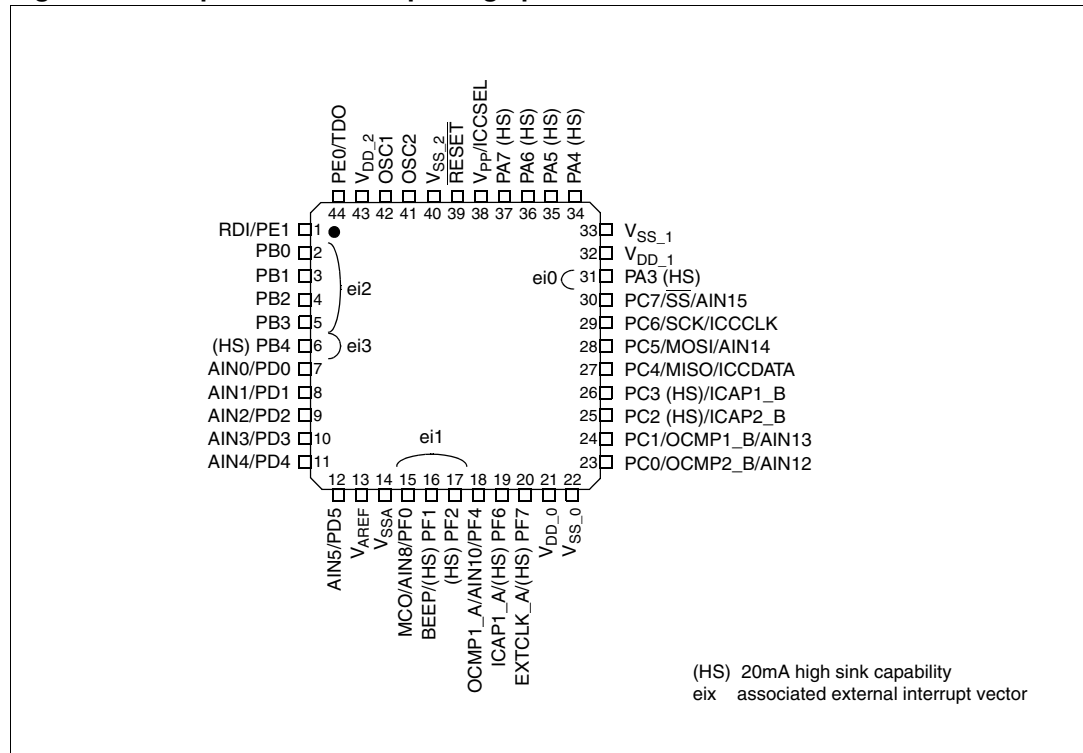
- All types of car body applications such as window lift, DC motor control and rain sensors
- Safety microcontrollers in airbag and engine management applications
- Auxiliary functions in car radios

Figure 1. Device block diagram



2 Package pinout and pin description

Figure 2. 44-pin LQFP 10x10 package pinout



For external pin connection guidelines refer to [Section 12: Electrical characteristics on page 173](#).

In [Table 2](#) below, refer to [Section 9: I/O ports on page 56](#) for more details on the software configuration of the I/O ports. The **RESET** configuration of each pin is shown in bold. This configuration is valid as long as the device is in reset state.

Table 2. Device pin description (LQFP44)⁽¹⁾

Pin		Type	Level		Port						Main function (after reset)	Alternate function	
No	Name		Input	Output	float	wpu	int ⁽²⁾	ana	OD ⁽³⁾	PP			
1	RDI/PE1	I/O	C _T		X	X			X	X	Port E1	SCI receive data in	
2	PB0	I/O	C _T		X	ei2			X	X	Port B0		
3	PB1	I/O	C _T		X	ei2			X	X	Port B1		
4	PB2	I/O	C _T		X	ei2			X	X	Port B2		
5	PB3	I/O	C _T		X		ei2		X	X	Port B3		
6	(HS) PB4	I/O	C _T	HS	X	ei3			X	X	Port B4		
7	AIN0/PD0	I/O	C _T		X	X		X	X	X	Port D0	ADC analog input 0	
8	AIN1/PD1	I/O	C _T		X	X		X	X	X	Port D1	ADC analog input 1	
9	AIN2/PD2	I/O	C _T		X	X		X	X	X	Port D2	ADC analog Input 2	
10	AIN3/PD3	I/O	C _T		X	X		X	X	X	Port D3	ADC analog Input 3	
11	AIN4/PD4	I/O	C _T		X	X		X	X	X	Port D4	ADC analog Input 4	
12	AIN5/PD5	I/O	C _T		X	X		X	X	X	Port D5	ADC analog Input 5	
13	V _{AREF} ⁽⁴⁾	S									Analog reference voltage for ADC		
14	V _{SSA} ⁽⁴⁾	S									Analog ground voltage		
15	MCO/AIN8/PF0	I/O	C _T		X	ei1		X	X	X	Port F0	Main clock out (f _{CPU})	ADC analog input 8
16	BEEP/(HS) PF1	I/O	C _T	HS	X	ei1			X	X	Port F1	Beep signal output	
17	(HS) PF2	I/O	C _T	HS	X		ei1		X	X	Port F2		
18	OCMP1_A/AIN10/PF4	I/O	C _T		X	X		X	X	X	Port F4	Timer A output compare 1	ADC analog input 10
19	ICAP1_A/(HS) PF6	I/O	C _T	HS	X	X			X	X	Port F6	Timer A input capture 1	
20	EXTCLK_A/(HS) PF7	I/O	C _T	HS	X	X			X	X	Port F7	Timer A external clock source	
21	V _{DD_0} ⁽⁴⁾	S									Digital main supply voltage		
22	V _{SS_0} ⁽⁴⁾	S									Digital ground voltage		
23	PC0/OCMP2_B/ AIN12	I/O	C _T		X	X		X	X	X	Port C0	Timer B output compare 2	ADC analog input 12
24	PC1/OCMP1_B/ AIN13	I/O	C _T		X	X		X	X	X	Port C1	Timer B output compare 1	ADC analog input 13
25	PC2 (HS)/ICAP2_B	I/O	C _T	HS	X	X			X	X	Port C2	Timer B input capture 2	
26	PC3 (HS)/ICAP1_B	I/O	C _T	HS	X	X			X	X	Port C3	Timer B input capture 1	
27	PC4/MISO/ICCDATA	I/O	C _T		X	X			X	X	Port C4	SPI master in/ slave out data	ICC data input

Table 2. Device pin description (LQFP44)⁽¹⁾ (continued)

Pin		Type	Level		Port						Main function (after reset)	Alternate function	
					Input				Output				
No	Name		Input	Output	float	wpu	int ⁽²⁾	ana	OD ⁽³⁾	PP			
28	PC5/MOSI/AIN14	I/O	C _T		X	X		X	X	X	Port C5	SPI master out /slave in data	ADC analog input 14
29	PC6/SCK/ICCCLK	I/O	C _T		X	X			X	X	Port C6	SPI serial clock	ICC clock output
30	PC7/ \overline{SS} /AIN15	I/O	C _T		X	X		X	X	X	Port C7	SPI slave select (active low)	ADC analog input 15
31	PA3 (HS)	I/O	C _T	HS	X		ei0		X	X	Port A3		
32	V _{DD_1} ⁽⁴⁾	S									Digital main supply voltage		
33	V _{SS_1} ⁽⁴⁾	S									Digital ground voltage		
34	PA4 (HS)	I/O	C _T	HS	X	X			X	X	Port A4		
35	PA5 (HS)	I/O	C _T	HS	X	X			X	X	Port A5		
36	PA6 (HS)	I/O	C _T	HS	X				T		Port A6		
37	PA7 (HS)	I/O	C _T	HS	X				T		Port A7		
38	V _{PP} /ICCSEL	I									Must be tied low. In the Flash programming mode, this pin acts as the programming voltage input V _{PP} . See Section 12.9.2: ICCSEL/VPP pin on page 195 for more details.		
39	\overline{RESET}	I/O	C _T								Top priority non-maskable interrupt		
40	V _{SS_2} ⁽⁴⁾	S									Digital ground voltage		
41	OSC2 ⁽⁵⁾	O									Resonator oscillator inverter output		
42	OSC1 ⁽⁵⁾	I									External clock input or resonator oscillator inverter input		
43	V _{DD_2} ⁽⁴⁾	S									Digital main supply voltage		
44	PE0/TDO	I/O	C _T		X	X			X	X	Port E0	SCI transmit data out	

1. Legend/abbreviations for [Table 2](#):

Type: I = input, O = output, S = supply

Input level: C_T = CMOS 0.3V_{DD}/0.7V_{DD} with input trigger

Output level: HS = 20mA high sink (on N-buffer only)

Port and control configuration inputs: float = floating, wpu = weak pull-up, int = interrupt, ana = analog ports

Port and control configuration outputs: OD = open drain, PP = push-pull

- 'eiX' defines the associated external interrupt vector. If the weak pull-up column (wpu) is merged with the interrupt column (int), then the I/O configuration is pull-up interrupt input; otherwise the configuration is floating interrupt input
- 'T' defines a true open drain I/O (P-buffer and protection diode to V_{DD} are not implemented). See [Section 9: I/O ports on page 56](#) and [Section 12.8: I/O port pin characteristics on page 189](#) for more details
- It is mandatory to connect all available V_{DD} and V_{AREF} pins to the supply voltage and all V_{SS} and V_{SSA} pins to ground.
- OSC1 and OSC2 pins connect a crystal/ceramic resonator, or an external source to the on-chip oscillator; see [Section 1: Description on page 14](#) and [Section 12.5: Clock and timing characteristics on page 181](#) for more details

3 Register and memory map

As shown in [Figure 3](#), the MCU is capable of addressing 64 Kbytes of memories and I/O registers.

The available memory locations consist of 128 bytes of register locations, up to 1024 bytes of RAM and up to 32 Kbytes of user program memory. The RAM space includes up to 256 bytes for the stack from 0100h to 01FFh.

The highest address bytes contain the user reset and interrupt vectors.

Important: Memory locations marked as ‘reserved’ must never be accessed. Accessing a reserved area can have unpredictable effects on the device.

Figure 3. Memory map

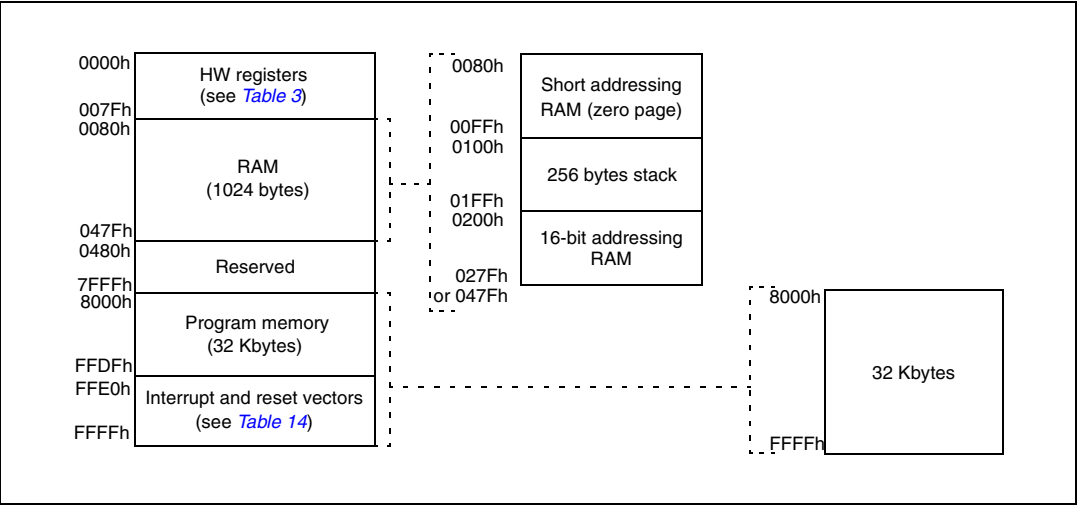


Table 3. Hardware register map⁽¹⁾

Address	Block	Register label	Register name	Reset status	Remarks
0000h 0001h 0002h	Port A ⁽²⁾	PADR	Port A data register	00h ⁽³⁾	R/W
		PADDR	Port A data direction register	00h	R/W
		PAOR	Port A option register	00h	R/W
0003h 0004h 0005h	Port B ⁽²⁾	PBDR	Port B data register	00h ⁽³⁾	R/W
		PBDDR	Port B data direction register	00h	R/W
		PBOR	Port B option register	00h	R/W
0006h 0007h 0008h	Port C	PCDR	Port C data register	00h ⁽³⁾	R/W
		PCDDR	Port C data direction register	00h	R/W
		PCOR	Port C option register	00h	R/W
0009h 000Ah 000Bh	Port D ⁽²⁾	PDADR	Port D data register	00h ⁽³⁾	R/W
		PDDDR	Port D data direction register	00h	R/W
		PDOR	Port D option register	00h	R/W
000Ch 000Dh 000Eh	Port E ⁽²⁾	PEDR	Port E data register	00h ⁽³⁾	R/W
		PEDDR	Port E data direction register	00h	R/W ⁽²⁾
		PEOR	Port E option register	00h	R/W ⁽²⁾
000Fh 0010h 0011h	Port F ⁽²⁾	PFDR	Port F data register	00h ⁽³⁾	R/W
		PFDDR	Port F data direction register	00h	R/W
		PFOR	Port F option register	00h	R/W
0012h to 0017h	Reserved area (6 bytes)				
0018h 0019h 001Ah 001Bh 001Ch 001Dh 001Eh	I ² C	I ² CCR	I ² C control register	00h	R/W
		I ² CSR1	I ² C status register 1	00h	Read only
		I ² CSR2	I ² C status register 2	00h	Read only
		I ² CCCR	I ² C clock control register	00h	R/W
		I ² COAR1	I ² C own address register 1	00h	R/W
		I ² COAR2	I ² C own address register2	00h	R/W
		I ² CDR	I ² C data register	00h	R/W
001Fh to 0020h	Reserved area (2 bytes)				
0021h 0022h 0023h	SPI	SPIDR	SPI data I/O register	xxh	R/W
		SPICR	SPI control register	0xh	R/W
		SPICSR	SPI control/status register	00h	R/W
0024h 0025h 0026h 0027h	ITC	ISPR0	Interrupt software priority register 0	FFh	R/W
		ISPR1	Interrupt software priority register 1	FFh	R/W
		ISPR2	Interrupt software priority register 2	FFh	R/W
		ISPR3	Interrupt software priority register 3	FFh	R/W
0028h		EICR	External interrupt control register	00h	R/W
0029h	Flash	FCSR	Flash control/status register	00h	R/W
002Ah	Watchdog	WDGCR	Watchdog control register	7Fh	R/W
002Bh	Reserved area (1 byte)				
002Ch 002Dh	MCC	MCCSR	Main clock control/status register	00h	R/W
		MCCBCR	Main clock controller: beep control register	00h	R/W
002Eh to 0030h	Reserved area (3 bytes)				

Table 3. Hardware register map⁽¹⁾ (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0031h	Timer A	TACR2	Timer A control register 2	00h	R/W
0032h		TACR1	Timer A control register 1	00h	R/W
0033h		TACSR	Timer A control/status register	xxxx x0xxb	R/W
0034h		TAIC1HR	Timer A input capture 1 high register	xxh	Read only
0035h		TAIC1LR	Timer A input capture 1 low register	xxh	Read only
0036h		TAOC1HR	Timer A output compare 1 high register	80h	R/W
0037h		TAOC1LR	Timer A output compare 1 low register	00h	R/W
0038h		TACHR	Timer A counter high register	FFh	Read only
0039h		TACLRL	Timer A counter low register	FCh	Read only
003Ah		TAACHR	Timer A alternate counter high register	FFh	Read only
003Bh		TAACLRL	Timer A alternate counter low register	FCh	Read only
003Ch		TAIC2HR	Timer A input capture 2 high register	xxh	Read only
003Dh		TAIC2LR	Timer A input capture 2 low register	xxh	Read only
003Eh		TAOC2HR	Timer A output compare 2 high register	80h	R/W
003Fh		TAOC2LR	Timer A output compare 2 low register	00h	R/W
0040h	Reserved area (1 byte)				
0041h	Timer B	TBCR2	Timer B control register 2	00h	R/W
0042h		TBCR1	Timer B control register 1	00h	R/W
0043h		TBCSR	Timer B control/status register	xxxx x0xxb	R/W
0044h		TBIC1HR	Timer B input capture 1 high register	xxh	Read only
0045h		TBIC1LR	Timer B input capture 1 low register	xxh	Read only
0046h		TBOC1HR	Timer B output compare 1 high register	80h	R/W
0047h		TBOC1LR	Timer B output compare 1 low register	00h	R/W
0048h		TBCHR	Timer B counter high register	FFh	Read only
0049h		TBCLRL	Timer B counter low register	FCh	Read only
004Ah		TBACHR	Timer B alternate counter high register	FFh	Read only
004Bh		TBACLRL	Timer B alternate counter low register	FCh	Read only
004Ch		TBIC2HR	Timer B input capture 2 high register	xxh	Read only
004Dh		TBIC2LR	Timer B input capture 2 low register	xxh	Read only
004Eh		TBOC2HR	Timer B output compare 2 high register	80h	R/W
004Fh		TBOC2LR	Timer B output compare 2 low register	00h	R/W
0050h	SCI	SCISR	SCI status register	C0h	Read only
0051h		SCIDR	SCI data register	xxh	R/W
0052h		SCIBRR	SCI baud rate register	00h	R/W
0053h		SCICR1	SCI control register 1	x000 0000b	R/W
0054h		SCICR2	SCI control register 2	00h	R/W
0055h		SCIERPR	SCI extended receive prescaler register	00h	R/W
0056h			Reserved area	---	
0057h		SCIETPR	SCI extended transmit prescaler register	00h	R/W
0058h to 006Fh	Reserved area (24 bytes)				
0070h	ADC	ADCCSR	Control/status register	00h	R/W
0071h		ADCDRL	Data high register	00h	Read only
0072h		ADCDRL	Data low register	00h	Read only

Table 3. Hardware register map⁽¹⁾ (continued)

Address	Block	Register label	Register name	Reset status	Remarks
0073h	PWM ART	PWMDCR3	PWM AR Timer Duty Cycle Register 3	00h	R/W
0074h		PWMDCR2	PWM AR Timer Duty Cycle Register 2	00h	R/W
0075h		PWMDCR1	PWM AR Timer Duty Cycle Register 1	00h	R/W
0076h		PWMDCR0	PWM AR Timer Duty Cycle Register 0	00h	R/W
0077h		PWMCR	PWM AR Timer Control Register	00h	R/W
0078h		ARTCSR	Auto-Reload Timer Control/Status Register	00h	R/W
0079h		ARTCAR	Auto-Reload Timer Counter Access Register	00h	R/W
007Ah		ARTARR	Auto-Reload Timer Auto-Reload Register	00h	R/W
007Bh		ARTICCSR	AR Timer Input Capture Control/Status Reg.	00h	R/W
007Ch		ARTICR1	AR Timer Input Capture Register 1	00h	Read only
007Dh		ARTICR2	AR Timer Input Capture Register 1	00h	Read only
007Eh 007Fh	Reserved area (2 bytes)				

1. Legend: X = undefined; R/W = read/write
2. The bits associated with unavailable pins must always keep their reset value.
3. The contents of the I/O port DR registers are readable only in output configuration. In input configuration, the values of the I/O pins are returned instead of the DR register contents.

4 Flash program memory

4.1 Introduction

The ST7 dual voltage high density Flash (HDFlash) is a non-volatile memory that can be electrically erased as a single block or by individual sectors and programmed on a byte-by-byte basis using an external V_{PP} supply.

The HDFlash devices can be programmed and erased off-board (plugged in a programming tool) or on-board using ICP (in-circuit programming) or IAP (in-application programming).

The array matrix organization means that each sector can be erased and reprogrammed without affecting other sectors.

4.2 Main features

- 3 Flash programming modes:
 - Insertion in a programming tool: In this mode, all sectors including option bytes can be programmed or erased.
 - ICP (in-circuit programming): In this mode, all sectors including option bytes can be programmed or erased without removing the device from the application board.
 - IAP (in-application programming): In this mode, all sectors except sector 0, can be programmed or erased without removing the device from the application board and while the application is running.
- ICT (in-circuit testing) for downloading and executing user application test patterns in RAM
- Readout protection
- Register access security system (RASS) to prevent accidental programming or erasing

4.3 Structure

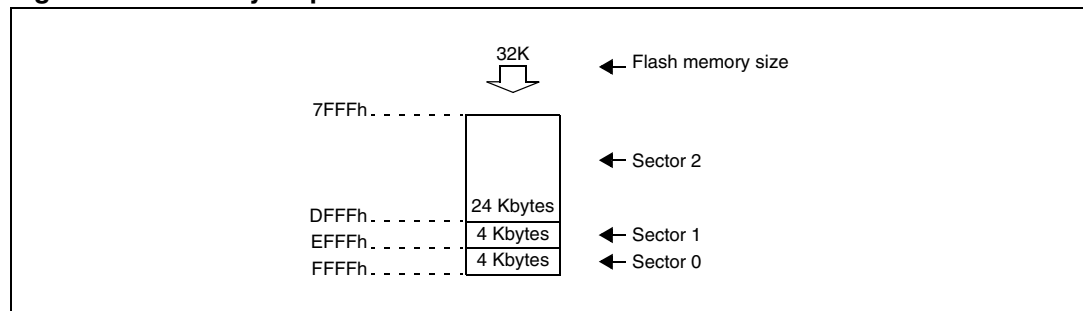
The Flash memory is organized in sectors and can be used for both code and data storage.

Depending on the overall Flash memory size in the microcontroller device, there are up to three user sectors (see [Table 4](#)). Each of these sectors can be erased independently to avoid unnecessary erasing of the whole Flash memory when only a partial erasing is required.

The first two sectors have a fixed size of 4 Kbytes (see [Figure 4: Memory map and sector address on page 23](#)). They are mapped in the upper part of the ST7 addressing space so the reset and interrupt vectors are located in sector 0 (F000h-FFFFh).

Table 4. Sectors available in Flash devices

Flash size (bytes)	Available sectors
32K	Sectors 0, 1, 2

Figure 4. Memory map and sector address

4.3.1 Readout protection

Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Even if no protection can be considered as totally unbreakable, the feature provides a very high level of protection for a general purpose microcontroller.

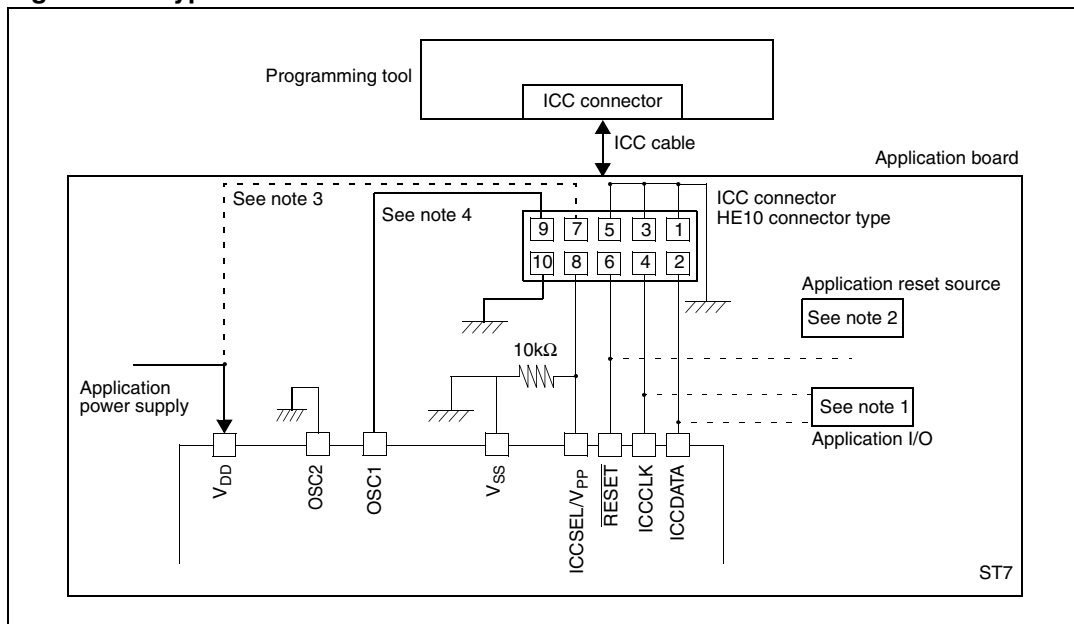
In Flash devices, this protection is removed by reprogramming the option. In this case, the entire program memory is first automatically erased.

Readout protection selection in Flash devices is enabled and removed through the FMP_R bit in the option byte.

4.4 ICC interface

ICC needs a minimum of four and up to six pins to be connected to the programming tool (see [Figure 5: Typical ICC interface on page 24](#)). These pins are:

$\overline{\text{RESET}}$:	Device reset
V_{SS} :	Device power supply ground
ICCCLK:	ICC output serial clock pin
ICCDATA:	ICC input/output serial data pin
ICCSEL/ V_{PP} :	Programming voltage
OSC1(or OSCIN):	Main clock input for external source (optional)
V_{DD} :	Application board power supply (optional, see Figure 5: Typical ICC interface on page 24, Note 3)

Figure 5. Typical ICC interface

1. If the ICCCLK or ICCDATA pins are only used as outputs in the application, no signal isolation is necessary. As soon as the programming tool is plugged to the board, even if an ICC session is not in progress, the ICCCLK and ICCDATA pins are not available for the application. If they are used as inputs by the application, isolation such as a serial resistor has to be implemented in case another device forces the signal. Refer to the programming tool documentation for recommended resistor values.
2. During the ICC session, the programming tool must control the RESET pin. This can lead to conflicts between the programming tool and the application reset circuit if it drives more than 5mA at high level (push pull output or pull-up resistor <1K). A Schottky diode can be used to isolate the application reset circuit in this case. When using a classical RC network with $R > 1K$ or a reset management IC with open drain output and pull-up resistor $> 1K$, no additional components are needed. In all cases the user must ensure that no external reset is generated by the application during the ICC session.
3. The use of pin 7 of the ICC connector depends on the programming tool architecture. This pin must be connected when using most ST programming tools (it is used to monitor the application power supply). Please refer to the programming tool manual.
4. Pin 9 must be connected to the OSC1 or OSCIN pin of the ST7 when the clock is not available in the application or if the selected clock option is not programmed in the option byte. ST7 devices with multi-oscillator capability must have OSC2 grounded in this case.

4.5 In-circuit programming (ICP)

To perform ICP the microcontroller must be switched to ICC (in-circuit communication) mode by an external controller or programming tool.

Depending on the ICP code downloaded in RAM, Flash memory programming can be fully customized (number of bytes to program, program locations, or selection serial communication interface for downloading).

When using an STMicroelectronics or third-party programming tool that supports ICP and the specific microcontroller device, the user needs only to implement the ICP hardware interface on the application board (see [Figure 5](#)). For more details on the pin locations, refer to [Section 2: Package pinout and pin description on page 15](#).

4.6 In-application programming (IAP)

This mode uses a BootLoader program previously stored in sector 0 by the user (in ICP mode or by plugging the device in a programming tool).

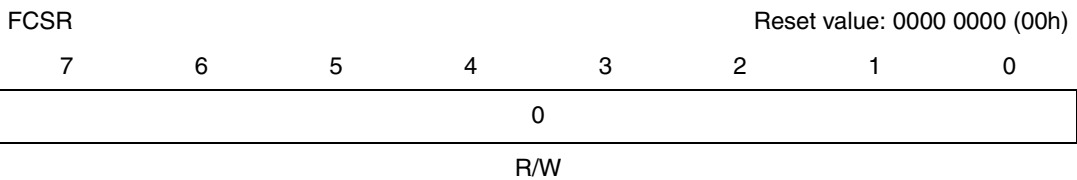
This mode is fully controlled by user software, which means it can be adapted to the user application (such as user-defined strategy for entering programming mode, choice of communications protocol used to fetch the data to be stored). For example, it is possible to download code from the SPI, SCI, USB or CAN interfaces and program it in the Flash. IAP mode can be used to program any of the Flash sectors except sector 0, which is write/erase protected to allow recovery in case errors occur during the programming operation.

4.7 Related documentation

For details on Flash programming and ICC protocol, refer to the *ST7 Flash programming reference manual* and to the *ST7 ICC protocol reference manual*.

4.7.1 Register description

Flash control/status register (FCSR)



This register is reserved for use by programming tool software. It controls the Flash programming and erasing operations.

Table 5. Flash control/status register address and reset value

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0029h	FCSR Reset value	0	0	0	0	0	0	0	0

5 Central processing unit

5.1 Introduction

This CPU has a full 8-bit architecture and contains six internal registers allowing efficient 8-bit data manipulation.

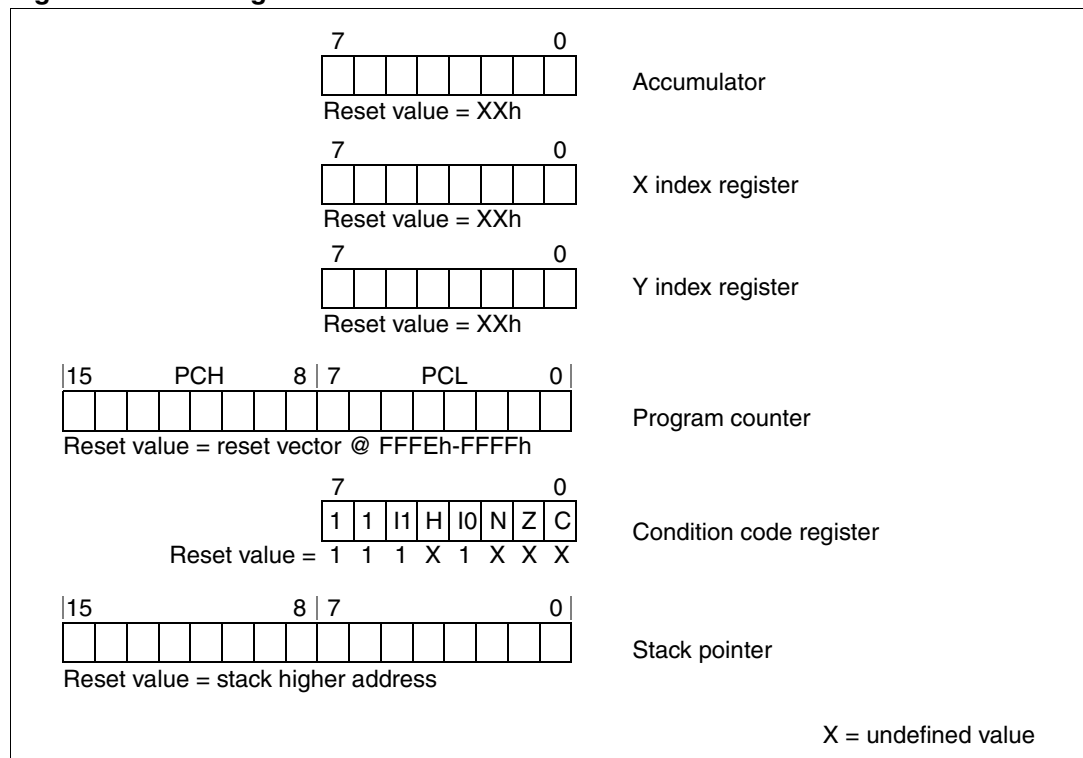
5.2 Main features

- Enables execution of 63 basic instructions
- Fast 8-bit by 8-bit multiply
- 17 main addressing modes (with indirect addressing mode)
- Two 8-bit index registers
- 16-bit stack pointer
- Low power halt and wait modes
- Priority maskable hardware interrupts
- Non-maskable software/hardware interrupts

5.3 CPU registers

The six CPU registers shown in [Figure 6](#) are not present in the memory mapping and are accessed by specific instructions.

Figure 6. CPU registers



Accumulator (A)

The accumulator is an 8-bit general purpose register used for holding operands and the results of the arithmetic and logic calculations as well as the results of data manipulations.

Index registers (X and Y)

These 8-bit registers are used to create effective addresses or as temporary storage areas for data manipulation (the cross-assembler generates a precede instruction (PRE) to indicate that the following instruction refers to the Y register).

The Y register is not affected by the interrupt automatic procedures.

Program counter (PC)

The program counter is a 16-bit register containing the address of the next instruction to be executed by the CPU. It is made of two 8-bit registers PCL (program counter low which is the LSB) and PCH (program counter high which is the MSB).

Condition code register (CC)

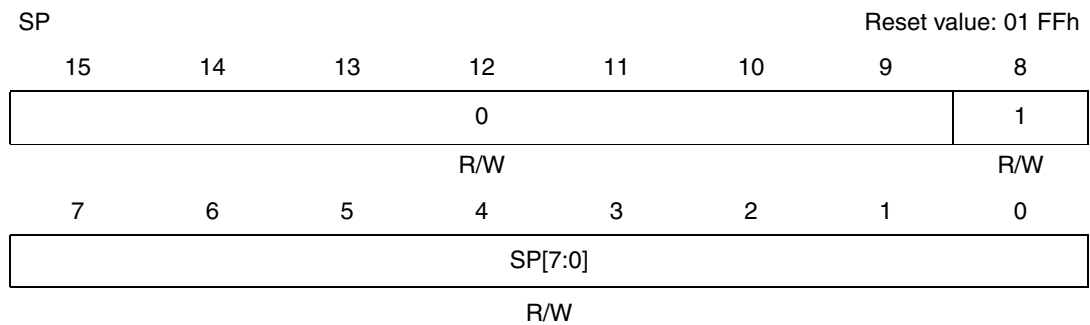
CC							Reset value: 111x 1xxx
7	6	5	4	3	2	1	0
1	I1	H	I0	N	Z	C	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The 8-bit condition code register contains the interrupt masks and four flags representative of the result of the instruction just executed. This register can also be handled by the PUSH and POP instructions.

These bits can be individually tested and/or controlled by specific instructions.

Table 6. CC register description

Bit	Bit name	Function
5,3	I1, I0	<p>Interrupt management bits - interrupt</p> <p>The combination of the I1 and I0 bits gives the current interrupt software priority:</p> <p>10: Interrupt software priority = level 0 (main)</p> <p>01: Interrupt software priority = level 1</p> <p>00: Interrupt software priority = level 2</p> <p>11: Interrupt software priority = level 3 (= interrupt disable)</p> <p>These two bits are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (ISPRx). They can also be set/cleared by software with the RIM, SIM, IRET, HALT, WFI and PUSH/POP instructions. See Section 7: Interrupts on page 36 for more details.</p>
4	H	<p>Arithmetic management bit - half carry</p> <p>This bit is set by hardware when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. It is reset by hardware during the same instruction.</p> <p>0: No half carry has occurred</p> <p>1: A half carry has occurred</p> <p>This bit is tested using the JRH or JRNH instruction. The H bit is useful in BCD arithmetic subroutines.</p>
2	N	<p>Arithmetic management bit - negative</p> <p>This bit is set and cleared by hardware. It is representative of the result sign of the last arithmetic, logical or data manipulation. It is a copy of the result 7th bit.</p> <p>0: The result of the last operation is positive or null</p> <p>1: The result of the last operation is negative (i.e. the most significant bit is a logic 1)</p> <p>This bit is accessed by the JRMI and JRPL instructions.</p>
1	Z	<p>Arithmetic management bit - zero</p> <p>This bit is set and cleared by hardware. This bit indicates that the result of the last arithmetic, logical or data manipulation is zero.</p> <p>0: The result of the last operation is different from zero</p> <p>1: The result of the last operation is zero</p> <p>This bit is accessed by the JREQ and JRNE test instructions.</p>
0	C	<p>Arithmetic management bit - carry/borrow</p> <p>This bit is set and cleared by hardware and software. It indicates an overflow or an underflow has occurred during the last arithmetic operation.</p> <p>0: No overflow or underflow has occurred</p> <p>1: An overflow or underflow has occurred</p> <p>This bit is driven by the SCF and RCF instructions and tested by the JRC and JRNC instructions. It is also affected by the 'bit test and branch', shift and rotate instructions.</p>

Stack pointer register (SP)

The stack pointer is a 16-bit register which is always pointing to the next free location in the stack. It is then decremented after data has been pushed onto the stack and incremented before data is popped from the stack (see [Figure 7: Stack manipulation example on page 30](#)).

Since the stack is 256 bytes deep, the 8 most significant bits are forced by hardware. Following an MCU reset, or after a reset stack pointer instruction (RSP), the stack pointer contains its reset value (the SP7 to SP0 bits are set) which is the stack higher address.

The least significant byte of the stack pointer (called S) can be directly accessed by an LD instruction.

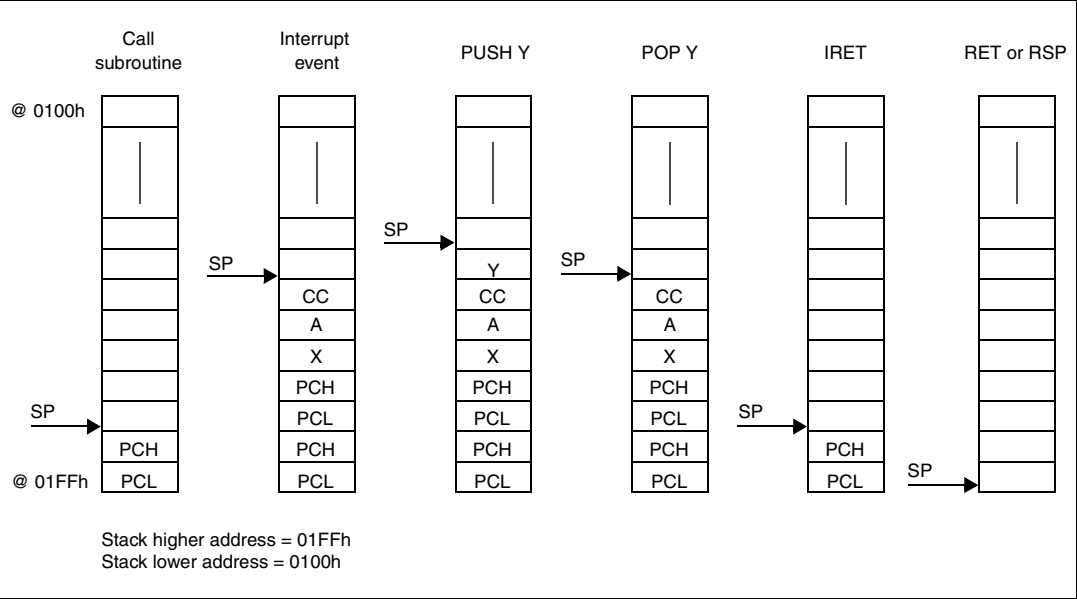
Note: *When the lower limit is exceeded, the stack pointer wraps around to the stack upper limit, without indicating the stack overflow. The previously stored information is then overwritten and therefore lost. The stack also wraps in case of an underflow.*

The stack is used to save the return address during a subroutine call and the CPU context during an interrupt. The user may also directly manipulate the stack by means of the PUSH and POP instructions. In the case of an interrupt, the PCL is stored at the first location pointed to by the SP. Then the other registers are stored in the next locations as shown in [Figure 7](#).

- When an interrupt is received, the SP is decremented and the context is pushed on the stack
- On return from interrupt, the SP is incremented and the context is popped from the stack

A subroutine call occupies two locations and an interrupt five locations in the stack area.

Figure 7. Stack manipulation example



6 Supply, reset and clock management

6.1 Introduction

The device includes a range of utility features for securing the application in critical situations (for example in case of a power brown-out), and reducing the number of external components. An overview is shown in [Figure 8](#).

6.2 Main features

- Optional PLL for multiplying the frequency by 2 (not to be used with the internal RC oscillator in order to respect the maximum operating frequency)
- Reset sequence manager (RSM)
- Multi-oscillator clock management (MO)
 - 5 crystal/ceramic resonator oscillators
 - 1 internal RC oscillator

6.3 Phase locked loop

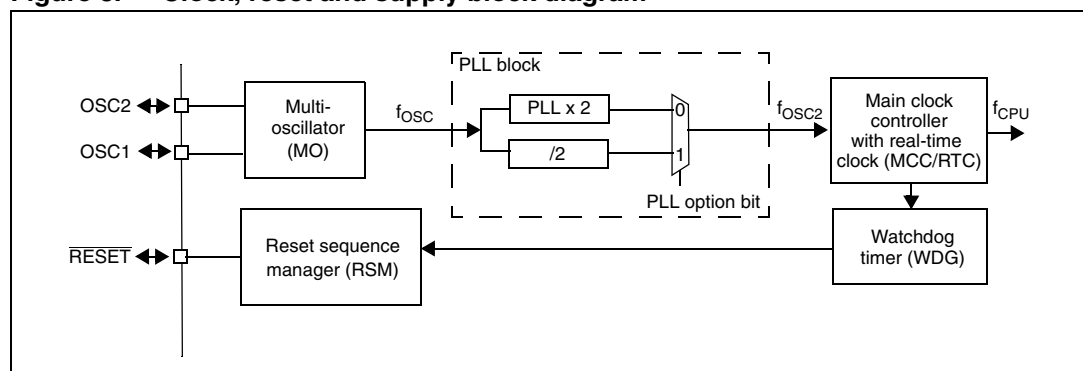
If the clock frequency input to the PLL is in the range 2 to 4 MHz, the PLL can be used to multiply the frequency by two to obtain an f_{OSC2} of 4 to 8 MHz. The PLL is enabled by option byte 1, bit opt0 (see [Table 123: Option byte 1 description on page 208](#)). If the PLL is disabled, then $f_{OSC2} = f_{OSC}/2$.

Caution: The PLL is not recommended for applications where timing accuracy is required.

Caution: The PLL must not be used with the internal RC oscillator.

Caution: When the PLL is used with an external clock signal, the clock signal must be available on the OSCIN pin before the reset signal is released.

Figure 8. Clock, reset and supply block diagram



6.4 Multi-oscillator (MO)

The main clock of the ST7 can be generated by three different source types coming from the multi-oscillator block:

- An external source
- 4 crystal or ceramic resonator oscillators
- An internal high frequency RC oscillator

Each oscillator is optimized for a given frequency range in terms of consumption and is selectable through the option byte. The associated hardware configurations are shown in [Table 7: ST7 clock source on page 33](#). Refer to the electrical characteristics section for more details.

Caution: The OSC1 and/or OSC2 pins must not be left unconnected. For the purposes of failure mode and effect analysis, it should be noted that if the OSC1 and/or OSC2 pins are left unconnected, the ST7 main oscillator may start and, in this configuration, could generate an f_{OSC} clock frequency in excess of the allowed maximum (> 16 MHz), putting the ST7 in an unsafe/undefined state. The product behavior must therefore be considered undefined when the OSC pins are left unconnected.

6.4.1 External clock source

In this external clock mode, a clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC1 pin while the OSC2 pin is tied to ground.

6.4.2 Crystal/ceramic oscillators

This family of oscillators has the advantage of producing a very accurate rate on the main clock of the ST7. The selection within a list of four oscillators with different frequency ranges has to be made by option byte in order to reduce consumption (refer to [Section 14.2.1: Flash configuration on page 207](#) for more details on the frequency ranges). In this mode of the multi-oscillator, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

These oscillators are not stopped during the reset phase to avoid losing time in the oscillator start-up phase.

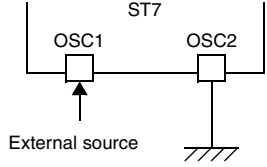
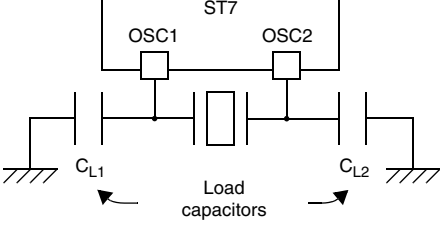
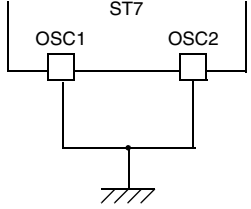
6.4.3 Internal RC oscillator

This oscillator provides a low cost solution for the main clock of the ST7 using only an internal resistor and capacitor. Internal RC oscillator mode has the drawback of a lower frequency accuracy and should not be used in applications that require accurate timing.

In this mode, the two oscillator pins have to be tied to ground.

In order not to exceed the maximum operating frequency, the internal RC oscillator must not be used with the PLL.

Table 7. ST7 clock source

	Hardware configuration
External clock	
Crystal/ceramic resonators	
Internal RC oscillator	

6.5 Reset sequence manager (RSM)

6.5.1 Introduction

The reset sequence manager includes three reset sources as shown in [Figure 10: Reset block diagram on page 34](#):

- External $\overline{\text{RESET}}$ source pulse
- Internal watchdog reset

These sources act on the $\overline{\text{RESET}}$ pin which is always kept low during the delay phase. The reset service routine vector is fixed at addresses FFFEh-FFFFh in the ST7 memory map.

The basic reset sequence consists of three phases as shown in [Figure 9: Reset sequence phases on page 34](#):

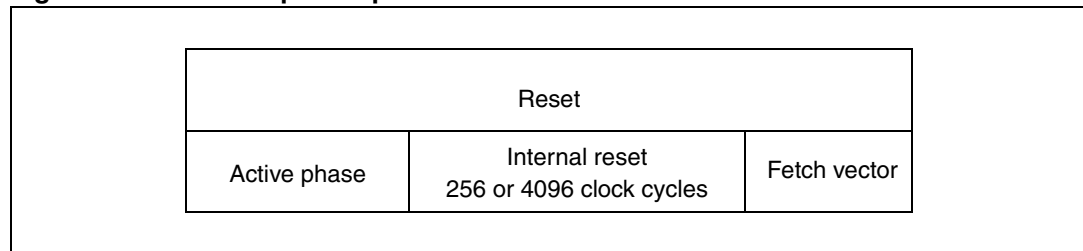
- Active phase depending on the reset source
- 256 or 4096 CPU clock cycle delay (selected by option byte)
- Reset vector fetch

Caution: When the ST7 is unprogrammed or fully erased, the Flash is blank and the reset vector is not programmed. For this reason, it is recommended to keep the $\overline{\text{RESET}}$ pin in low state until programming mode is entered, in order to avoid unwanted behavior.

The 256 or 4096 CPU clock cycle delay allows the oscillator to stabilize and ensures that recovery has taken place from the reset state. The shorter or longer clock cycle delay should be selected by option byte to correspond to the stabilization time of the external oscillator used in the application.

The reset vector fetch phase duration is two clock cycles.

Figure 9. Reset sequence phases

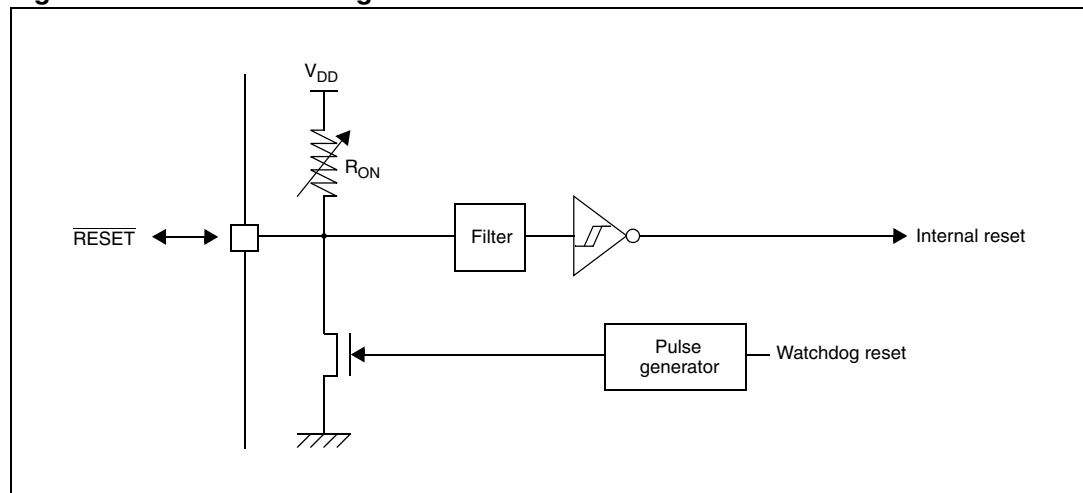


6.5.2 Asynchronous external $\overline{\text{RESET}}$ pin

The $\overline{\text{RESET}}$ pin is both an input and an open-drain output with integrated R_{ON} weak pull-up resistor. This pull-up has no fixed value but varies according to the input voltage. It can be pulled low by external circuitry to reset the device. See [Section 12: Electrical characteristics on page 173](#).

A reset signal originating from an external source must have a duration of at least $t_{\text{h(RSTL)in}}$ in order to be recognized (see [Figure 11: Reset sequences on page 35](#)). This detection is asynchronous and therefore the MCU can enter reset state even in halt mode.

Figure 10. Reset block diagram



The $\overline{\text{RESET}}$ pin is an asynchronous signal which plays a major role in EMS performance. In a noisy environment, it is recommended to follow the guidelines mentioned in the electrical characteristics section.

6.5.3 External power-on reset

To start the microcontroller correctly, the user must ensure by means of an external reset circuit that the reset signal is held low until V_{DD} is over the minimum level specified for the selected f_{OSC} frequency.

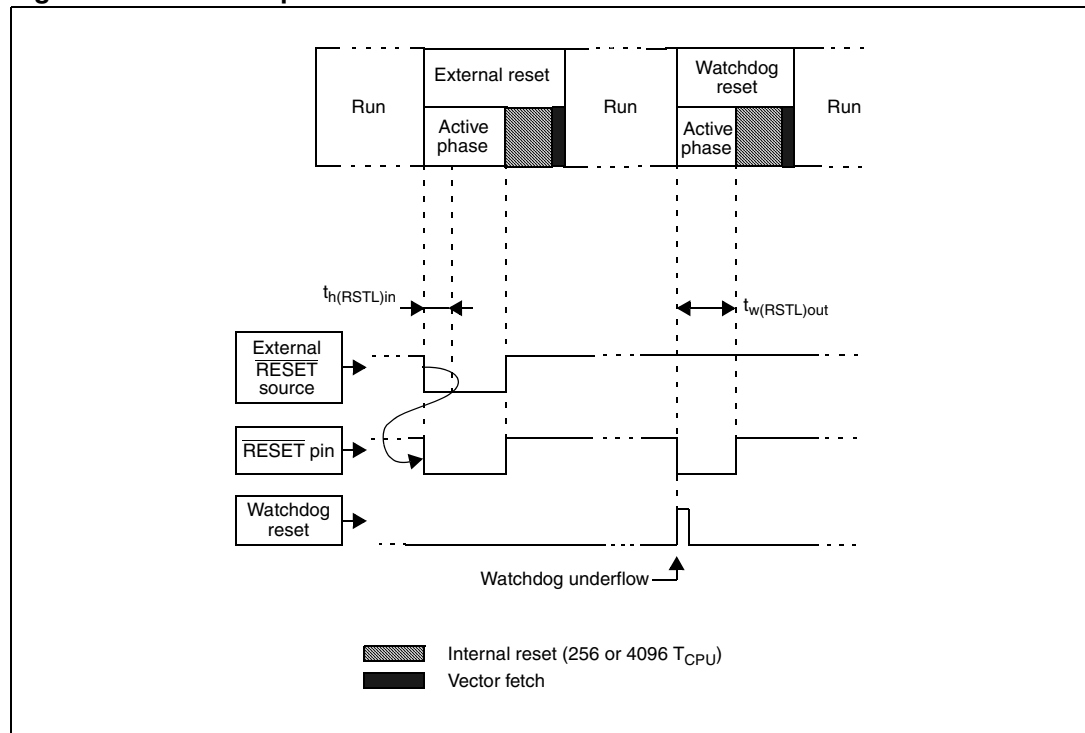
A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the \overline{RESET} pin.

6.5.4 Internal watchdog reset

The reset sequence generated by an internal watchdog counter overflow is shown in [Figure 11](#).

Starting from the watchdog counter underflow, the device \overline{RESET} pin acts as an output that is pulled low during at least $t_{w(RSTL)out}$.

Figure 11. Reset sequences



7 Interrupts

7.1 Introduction

The ST7 enhanced interrupt management provides the following features:

- Hardware interrupts
- Software interrupt (TRAP)
- Nested or concurrent interrupt management with flexible interrupt priority and level management:
 - Up to 4 software programmable nesting levels
 - Up to 16 interrupt vectors fixed by hardware
 - 2 non maskable events: reset, TRAP

This interrupt management is based on:

- Bit 5 and bit 3 of the CPU CC register (I1:0)
- Interrupt software priority registers (ISPRx)
- Fixed interrupt vector addresses located at the high addresses of the memory map (FFE0h to FFFFh) sorted by hardware priority order

This enhanced interrupt controller guarantees full upward compatibility with the standard (not nested) ST7 interrupt controller.

7.2 Masking and processing flow

The interrupt masking is managed by the I1 and I0 bits of the CC register and the ISPRx registers which give the interrupt software priority level of each interrupt vector (see [Table 8: Interrupt software priority levels on page 37](#)). The processing flow is shown in [Figure 12: Interrupt processing flowchart on page 37](#)

When an interrupt request has to be serviced:

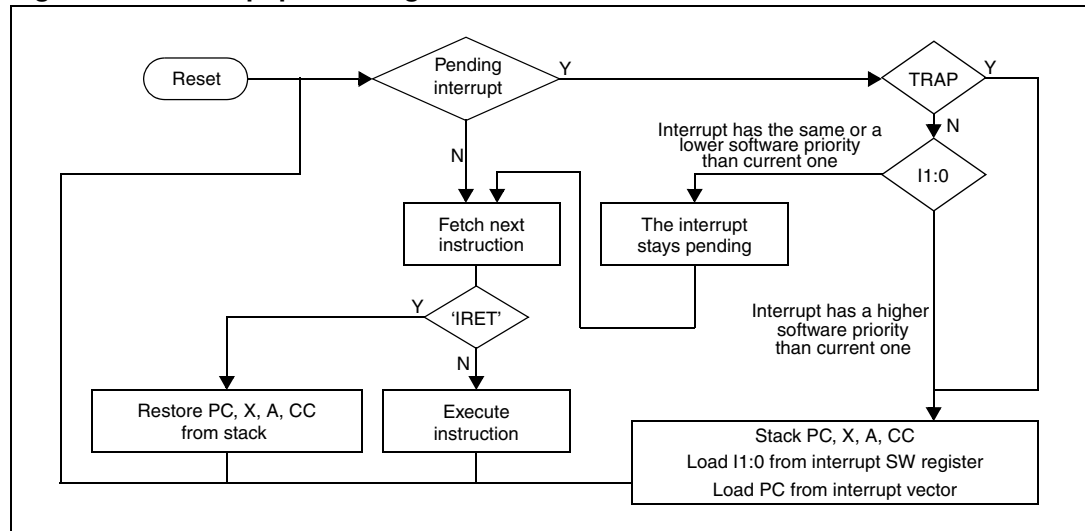
- Normal processing is suspended at the end of the current instruction execution
- The PC, X, A and CC registers are saved onto the stack
- I1 and I0 bits of CC register are set according to the corresponding values in the ISPRx registers of the serviced interrupt vector
- The PC is then loaded with the interrupt vector of the interrupt to service and the first instruction of the interrupt service routine is fetched (refer to [Table 14: Interrupt mapping on page 47](#) for vector addresses).

The interrupt service routine should end with the IRET instruction which causes the contents of the saved registers to be recovered from the stack.

Note: As a consequence of the IRET instruction, the I1 and I0 bits are restored from the stack and the program in the previous level resumes.

Table 8. Interrupt software priority levels

Interrupt software priority	Level	I1	I0
Level 0 (main)	Low ↓ High	1	0
Level 1		0	1
Level 2		0	0
Level 3 (= interrupt disable)		1	1

Figure 12. Interrupt processing flowchart

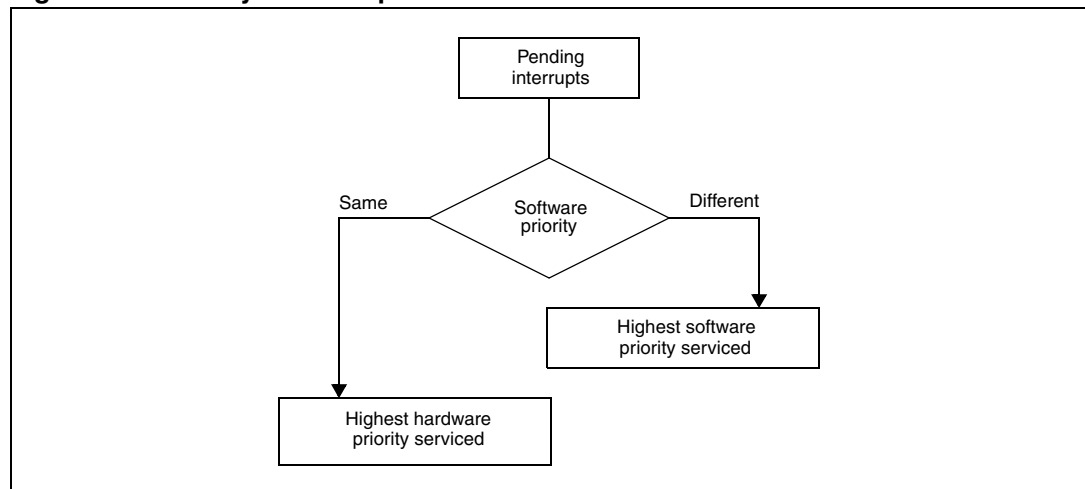
7.2.1 Servicing pending interrupts

As several interrupts can be pending at the same time, the interrupt to be taken into account is determined by the following two-step process:

- The highest software priority interrupt is serviced
- If several interrupts have the same software priority then the interrupt with the highest hardware priority is serviced first.

Figure 13 describes this decision process.

Figure 13. Priority decision process



When an interrupt request is not serviced immediately, it is latched and then processed when its software priority combined with the hardware priority becomes the highest one.

- Note:*
- 1 The hardware priority is exclusive while the software one is not. This allows the previous process to succeed with only one interrupt.
 - 2 Reset and TRAP can be considered as having the highest software priority in the decision process.

7.2.2 Different interrupt vector sources

Two interrupt source types are managed by the ST7 interrupt controller: the non-maskable type (reset, TRAP) and the maskable type (external or from internal peripherals).

7.2.3 Non-maskable sources

These sources are processed regardless of the state of the I1 and I0 bits of the CC register (see [Figure 12: Interrupt processing flowchart on page 37](#)). After stacking the PC, X, A and CC registers (except for reset), the corresponding vector is loaded in the PC register and the I1 and I0 bits of the CC are set to disable interrupts (level 3). These sources allow the processor to exit halt mode.

- TRAP (non maskable software interrupt)

This software interrupt is serviced when the TRAP instruction is executed. It will be serviced according to the flowchart in [Figure 12: Interrupt processing flowchart on page 37](#).

- Reset

The reset source has the highest priority in the ST7. This means that the first current routine has the highest software priority (level 3) and the highest hardware priority. See [Section 6.5: Reset sequence manager \(RSM\) on page 33](#).

7.2.4 Maskable sources

Maskable interrupt vector sources can be serviced if the corresponding interrupt is enabled and if its own interrupt software priority (in ISPRx registers) is higher than the one currently being serviced (I1 and I0 in CC register). If any of these two conditions is false, the interrupt is latched and thus remains pending.

- External interrupts

External interrupts allow the processor to exit from halt low power mode. External interrupt sensitivity is software selectable through the external interrupt control register (EICR). An external interrupt triggered on edge is latched and the interrupt request automatically cleared upon entering the interrupt service routine. If several input pins of a group connected to the same interrupt line are selected simultaneously, these are logically ORed.

- Peripheral interrupts

Usually the peripheral interrupts cause the MCU to exit from halt mode except those mentioned in [Table 14: Interrupt mapping on page 47](#). A peripheral interrupt occurs when a specific flag is set in the peripheral status registers and if the corresponding enable bit is set in the peripheral control register. The general sequence for clearing an interrupt is based on an access to the status register followed by a read or write to an associated register.

Note: The clearing sequence resets the internal latch. A pending interrupt (that is, waiting to be serviced) is therefore lost if the clear sequence is executed.

7.3 Interrupts and low power modes

All interrupts allow the processor to exit the wait low power mode. On the contrary, only external and other specified interrupts allow the processor to exit from the halt modes (see column ‘exit from halt’ in [Table 14: Interrupt mapping on page 47](#). When several pending interrupts are present while exiting halt mode, the first one serviced can only be an interrupt with exit from halt mode capability and it is selected through the same decision process shown in [Figure 13: Priority decision process on page 38](#).

Note: If an interrupt, that is not able to exit from halt mode, is pending with the highest priority when exiting halt mode, this interrupt is serviced after the first one serviced.

7.4 Concurrent and nested management

[Figure 14](#) and [Figure 15: Nested interrupt management on page 41](#) show two different interrupt management modes. The first is called concurrent mode and does not allow an interrupt to be interrupted, unlike the nested mode in [Figure 15](#). The interrupt hardware priority is given in this order from the lowest to the highest: MAIN, IT4, IT3, IT2, IT1, IT0. The software priority is given for each interrupt.

Warning: A stack overflow may occur without notifying the software of the failure.

Figure 14. Concurrent interrupt management

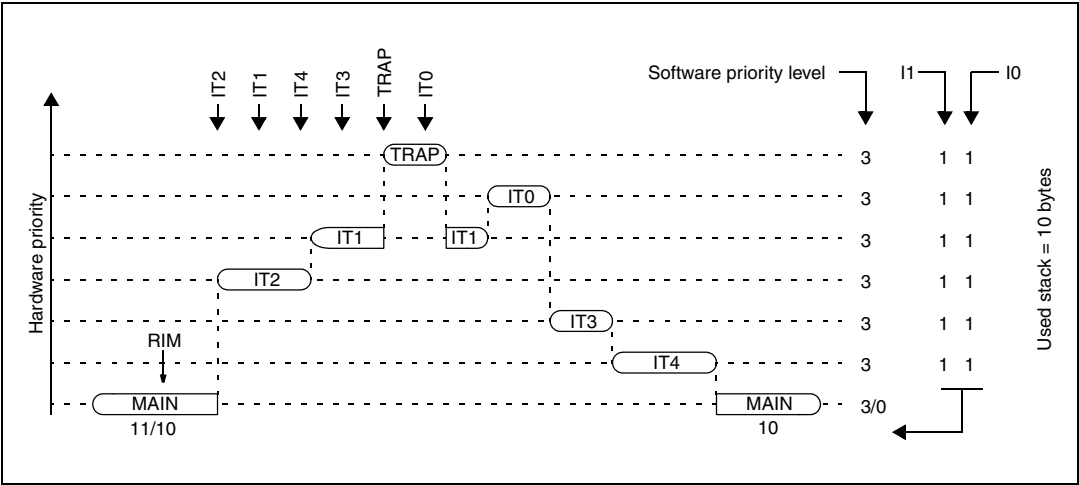
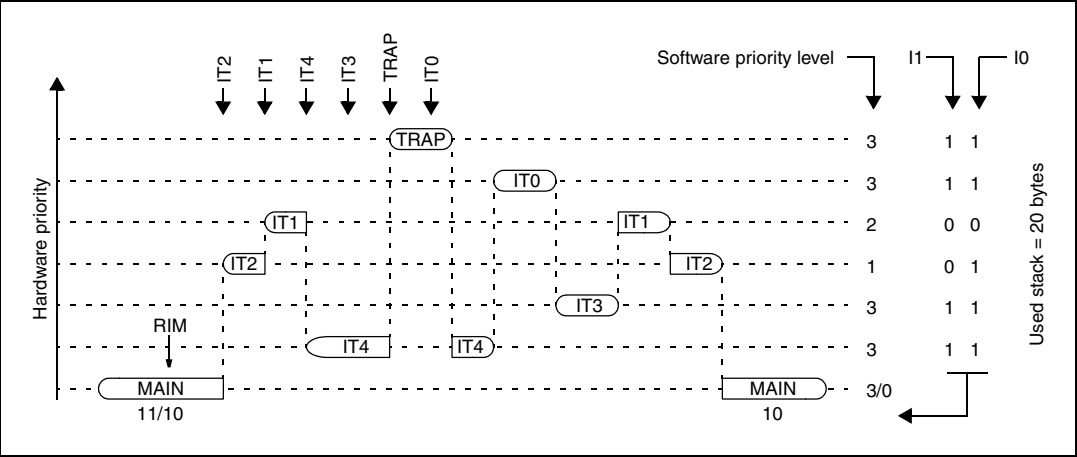


Figure 15. Nested interrupt management



7.5 Interrupt registers

CPU CC register interrupt bits

CPU CC							Reset value: 111x 1010 (xAh)
7	6	5	4	3	2	1	0
1	I1	H	I0	N	Z	C	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 9. CPU CC register description

Bit	Bit name	Function
5, 3	I1, I0	<p>Software interrupt priority</p> <p>These two bits indicate the current interrupt software priority:</p> <ul style="list-style-type: none">10: Interrupt software priority = level 0 (main)01: Interrupt software priority = level 100: Interrupt software priority = level 211: Interrupt software priority = level 3 (= interrupt disable⁽¹⁾) <p>These two bits are set/cleared by hardware when entering in interrupt. The loaded value is given by the corresponding bits in the interrupt software priority registers (ISPRx). They can also be set/cleared by software with the RIM, SIM, HALT, WFI, IRET and PUSH/POP instructions (see Table 11: Dedicated interrupt instruction set on page 43).</p>

1. TRAP and reset events can interrupt a level 3 program.

Interrupt software priority registers (ISPRX)

ISPR0				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
I1_3	I0_3	I1_2	I0_2	I1_1	I0_1	I1_0	I0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ISPR1				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
I1_7	I0_7	I1_6	I0_6	I1_5	I0_5	I1_4	I0_4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ISPR2				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
I1_11	I0_11	I1_10	I0_10	I1_9	I0_9	I1_8	I0_8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ISPR3				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
1	1	1	1	I1_13	I0_13	I1_12	I0_12
RO	RO	RO	RO	R/W	R/W	R/W	R/W

These four registers contain the interrupt software priority of each interrupt vector.

- Each interrupt vector (except reset and TRAP) has corresponding bits in the ISPRx registers where its own software priority is stored. This correspondence is shown in [Table 10](#).
- Each I1_x and I0_x bit value in the ISPRx registers has the same meaning as the I1 and I0 bits in the CC register.
- Level 0 cannot be written (I1_x = 1, I0_x = 0). In this case, the previously stored value is kept (example, previous = CFh, write = 64h, result = 44h).

Table 10. ISPRx interrupt vector correspondence

Vector address	ISPRx bits
FFFBh-FFFAh	I1_0 and I0_0 bits*
FFF9h-FFF8h	I1_1 and I0_1 bits
-	-
FFE1h-FFE0h	I1_13 and I0_13 bits

The reset, and TRAP vectors have no software priorities. When one is serviced, the I1 and I0 bits of the CC register are both set.

Caution: If the I1_x and I0_x bits are modified while the interrupt x is executed the following behavior has to be considered: If the interrupt x is still pending (new interrupt or flag not cleared) and the new software priority is higher than the previous one, the interrupt x is re-entered. Otherwise, the software priority stays unchanged up to the next interrupt request (after the IRET of the interrupt x).

7.6 Interrupt related instructions

Table 11. Dedicated interrupt instruction set⁽¹⁾

Instruction	New description	Function/example	I1	H	I0	N	Z	C
HALT	Entering halt mode		1		0			
IRET	Interrupt routine return	Pop CC, A, X, PC	I1	H	I0	N	Z	C
JRM	Jump if I1:0 = 11 (level 3)	I1:0 = 11 ?						
JRNM	Jump if I1:0 <> 11	I1:0 <> 11 ?						
POP CC	Pop CC from the stack	Mem => CC	I1	H	I0	N	Z	C
RIM	Enable interrupt (level 0 set)	Load 10 in I1:0 of CC	1		0			
SIM	Disable interrupt (level 3 set)	Load 11 in I1:0 of CC	1		1			
TRAP	Software trap	Software NMI	1		1			
WFI	Wait for interrupt		1		0			

1. During the execution of an interrupt routine, the HALT, POP CC, RIM, SIM and WFI instructions change the current software priority up to the next IRET instruction or one of the previously mentioned instructions.

7.7 External interrupts

7.7.1 I/O port interrupt sensitivity

The external interrupt sensitivity is controlled by the IPA, IPB and ISxx bits of the EICR register ([Figure 16: External interrupt control bits on page 44](#)). This control allows up to four fully independent external interrupt source sensitivities.

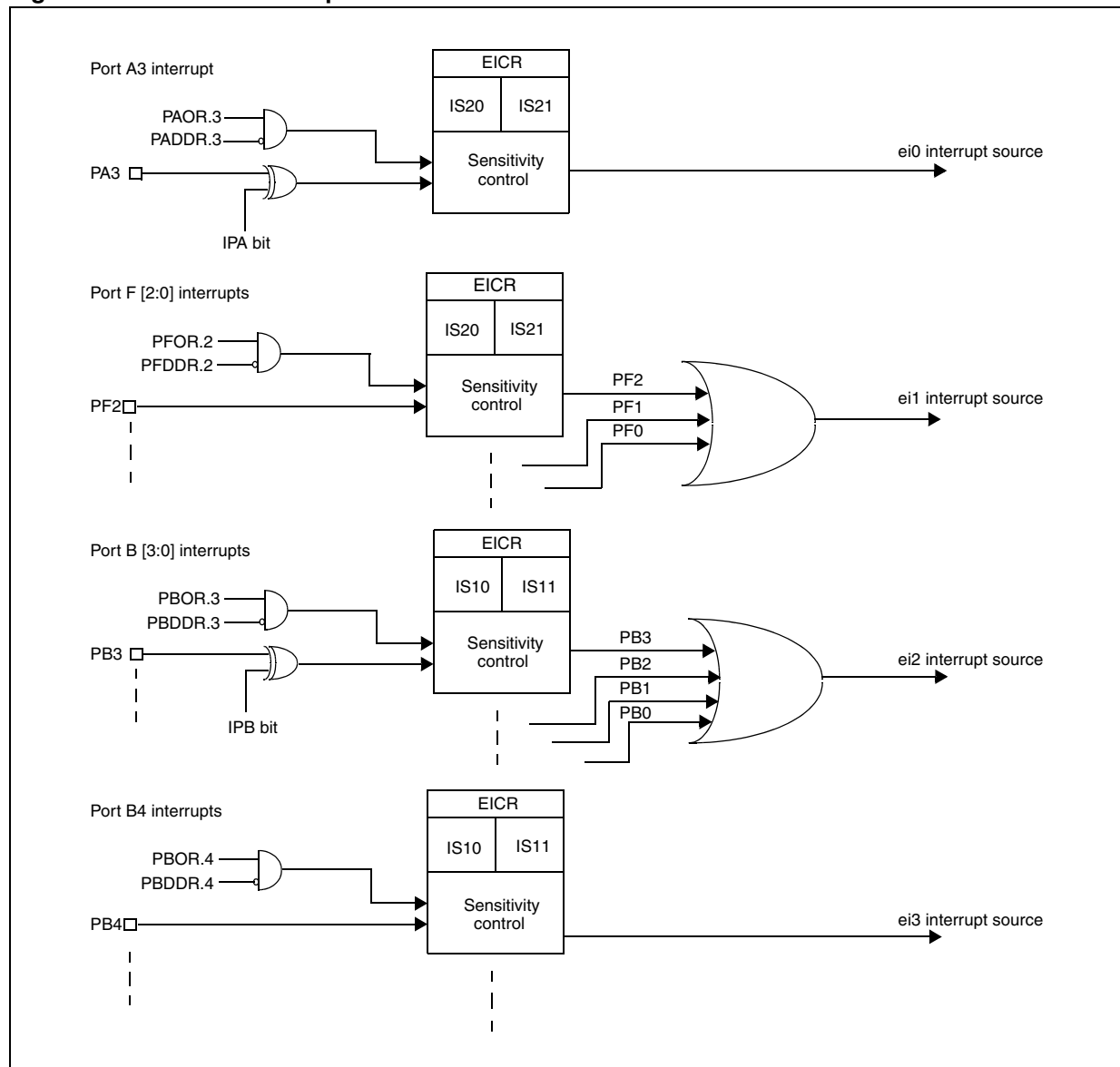
Each external interrupt source can be generated on four (or five) different events on the pin:

- Falling edge
- Rising edge
- Falling and rising edge
- Falling edge and low level
- Rising edge and high level (only for ei0 and ei2)

To guarantee correct functionality, the sensitivity bits in the EICR register can be modified only when the I1 and I0 bits of the CC register are both set to 1 (level 3). This means that interrupts must be disabled before changing sensitivity.

The pending interrupts are cleared by writing a different value in the ISx[1:0], IPA or IPB bits of the EICR.

Figure 16. External interrupt control bits



7.8 External interrupt control register (EICR)

EICR					Reset value: 0000 0000 (00h)		
7	6	5	4	3	2	1	0
IS1[1:0]		IPB	IS2[1:0]		IPA	Reserved	
R/W		R/W	R/W		R/W	-	

Table 12. EICR register description

Bit	Bit name	Function
7:6	IS1[1:0]	<p>Interrupt sensitivity (ei2 and ei3)</p> <p>The interrupt sensitivity, defined using the IS1[1:0] bits, is applied to the following external interrupts:</p> <p>External interrupt ei2 (port B[3:0]):</p> <p>00: External interrupt sensitivity = falling edge and low level (IPB bit = 0) and rising edge and high level (IPB bit = 1)</p> <p>01: External interrupt sensitivity = rising edge only (IPB bit = 0) and falling edge only (IPB bit = 1)</p> <p>10: External interrupt sensitivity = falling edge only (IPB bit = 0) and rising edge only (IPB bit = 1)</p> <p>11: External interrupt sensitivity = rising and falling edge (IPB bit = 0 and 1)</p> <p>External interrupt ei3 (port B[4]):</p> <p>00: external interrupt sensitivity = falling edge and low level</p> <p>01: external interrupt sensitivity = rising edge only</p> <p>10: external interrupt sensitivity = falling edge only</p> <p>11: external interrupt sensitivity = rising and falling edge</p> <p>These 2 bits can be written only when I1 and I0 of the CC register are both set to 1 (level 3).</p>
5	IPB	<p>Interrupt polarity for port B</p> <p>This bit is used to invert the sensitivity of the port B [3:0] external interrupts. It can be set and cleared by software only when I1 and I0 of the CC register are both set to 1 (level 3).</p> <p>0: No sensitivity inversion</p> <p>1: Sensitivity inversion</p>

Table 12. EICR register description (continued)

Bit	Bit name	Function
4:3	IS2[1:0]	<p>Interrupt sensitivity (ei0 and ei1)</p> <p>The interrupt sensitivity, defined using the IS2[1:0] bits, is applied to the following external interrupts:</p> <p>External interrupt ei0 (port A[3]):</p> <p>00: External interrupt sensitivity = falling edge and low level (IPA bit = 0) and rising edge and high level (IPA bit = 1)</p> <p>01: External interrupt sensitivity = rising edge only (IPA bit = 0) and falling edge only (IPA bit = 1)</p> <p>10: External interrupt sensitivity = falling edge only (IPA bit = 0) and rising edge only (IPA bit = 1)</p> <p>11: External interrupt sensitivity = rising and falling edge (IPA bit = 0 and 1)</p> <p>External interrupt ei1 port ([F2:0]):</p> <p>00: External interrupt sensitivity = falling edge and low level</p> <p>01: External interrupt sensitivity = rising edge only</p> <p>10: External interrupt sensitivity = falling edge only</p> <p>11: External interrupt sensitivity = rising and falling edge</p> <p>These 2 bits can be written only when I1 and I0 of the CC register are both set to 1 (level 3).</p>
2	IPA	<p>Interrupt polarity for port A</p> <p>This bit is used to invert the sensitivity of the port A[3] external interrupts. It can be set and cleared by software only when I1 and I0 of the CC register are both set to 1 (level 3).</p> <p>0: No sensitivity inversion</p> <p>1: Sensitivity inversion</p>
1:0	-	Reserved, must always be kept cleared

7.9 Nested interrupts register map and reset value

Table 13. Nested interrupts register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0024h	ISPR0 Reset value	ei1		ei0		MCC + SI			
		I1_3 1	I0_3 1	I1_2 1	I0_2 1	I1_1 1	I0_1 1	1	1
0025h	ISPR1 Reset value	SPI				ei3		ei2	
		I1_7 1	I0_7 1	I1_6 1	I0_6 1	I1_5 1	I0_5 1	I1_4 1	I0_4 1
0026h	ISPR2 Reset value	1	1	SCI		Timer B		Timer A	
				I1_10 1	I0_10 1	I1_9 1	I0_9 1	I1_8 1	I0_8 1
0027h	ISPR3 Reset value	1	1	1	1	I1_13 1	I0_13 1	I1_12 1	I0_12 1
0028h	EICR Reset value	IS11 0	IS10 0	IPB 0	IS21 0	IS20 0	IPA 0	0	0

7.10 Interrupt mapping

Table 14. Interrupt mapping

No.	Source block	Description	Register label	Priority order	Exit from halt	Exit from active halt	Address vector
	Reset	Reset	N/A	Higher priority	Yes	Yes	FFFEh-FFFFh
	TRAP	Software interrupt			No	No	FFFCCh-FFFDh
0	Not used			<div><div></div><div>↓</div><div>Lower priority</div></div>	-	-	FFFAh-FFFBh
1	MCC/RTC	Main clock controller time base interrupt	MCCSR		No	Yes	FFF8h-FFF9h
2	ei0	External interrupt port A[3:0]	N/A		Yes	Yes	FFF6h-FFF7h
3	ei1	External interrupt port F[2:0]			Yes	Yes	FFF4h-FFF5h
4	ei2	External interrupt port B[3:0]			Yes	Yes	FFF2h-FFF3h
5	ei3	External interrupt port B[7:4]			Yes	Yes	FFF0h-FFF1h
6	Not used				-	-	FFEEh-FFEFh
7	SPI	SPI peripheral interrupts	SPICSR		Yes	Yes	FFECCh-FFEDh
8	Timer A	Timer A peripheral interrupts	TASR		No	No	FFEAh-FFEBh
9	Timer B	Timer B peripheral interrupts	TBSR		No	No	FFE8h-FFE9h
10	SCI	SCI peripheral interrupts	SCISR	No	No	FFE6h-FFE7h	

8 Power saving modes

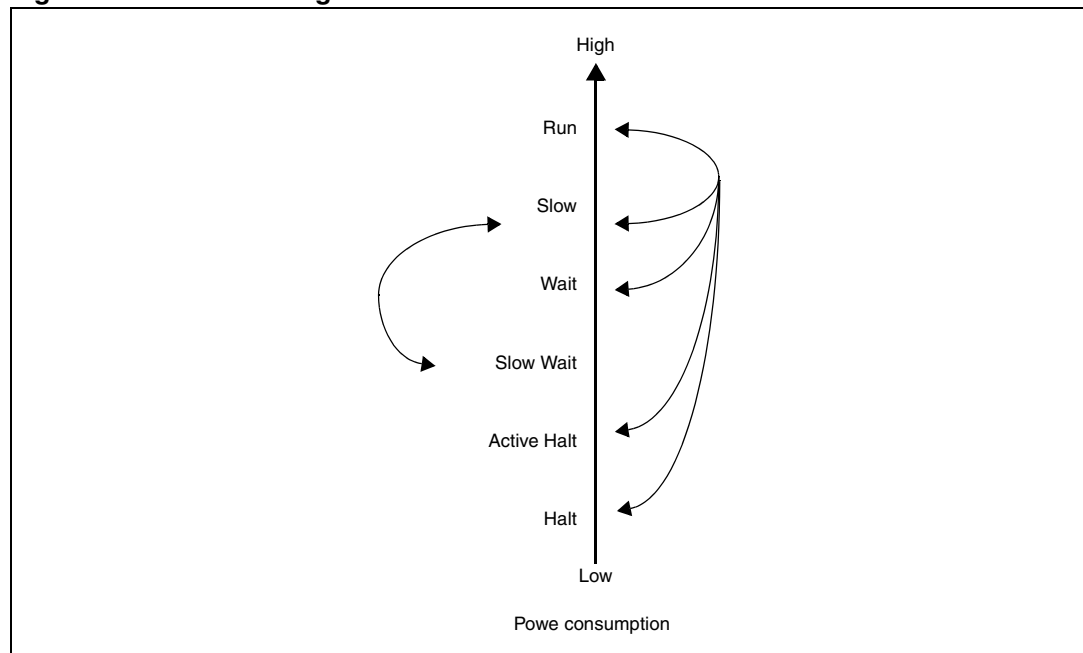
8.1 Introduction

To give a large measure of flexibility to the application in terms of power consumption, four main power saving modes are implemented in the ST7 (see [Figure 17](#)): Slow, wait (slow wait), active halt and halt.

After a reset the normal operating mode is selected by default (run mode). This mode drives the device (CPU and embedded peripherals) by means of a master clock which is based on the main oscillator frequency divided or multiplied by 2 (f_{OSC2}).

From run mode, the different power saving modes may be selected by setting the relevant register bits or by calling the specific ST7 software instruction whose action depends on the oscillator status.

Figure 17. Power saving mode transitions



8.2 Slow mode

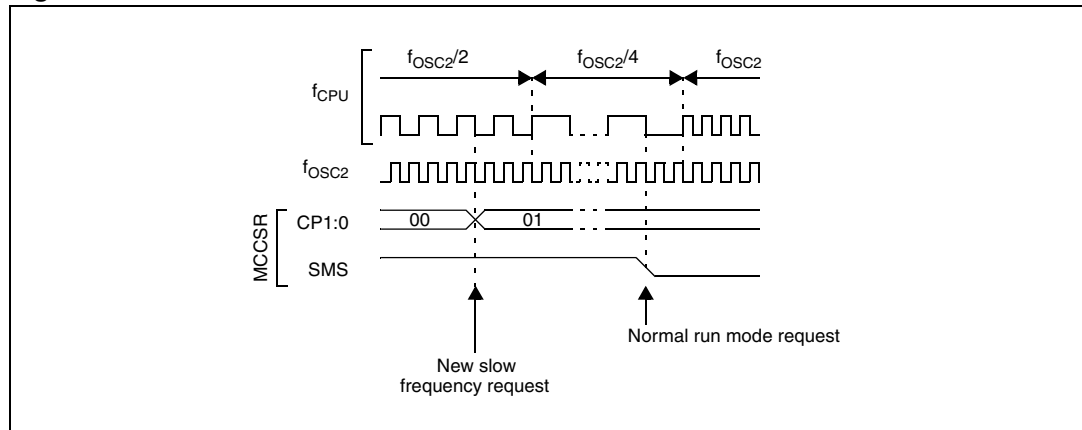
This mode has two targets:

- To reduce power consumption by decreasing the internal clock in the device
- To adapt the internal clock frequency (f_{CPU}) to the available supply voltage

Slow mode is controlled by three bits in the MCCSR register: The SMS bit which enables or disables slow mode and two CPx bits which select the internal slow frequency (f_{CPU}).

In this mode, the master clock frequency (f_{OSC2}) can be divided by 2, 4, 8 or 16. The CPU and peripherals are clocked at this lower frequency (f_{CPU}).

Note: Slow wait mode is activated when entering the wait mode while the device is already in slow mode.

Figure 18. Slow mode clock transitions

8.3 Wait mode

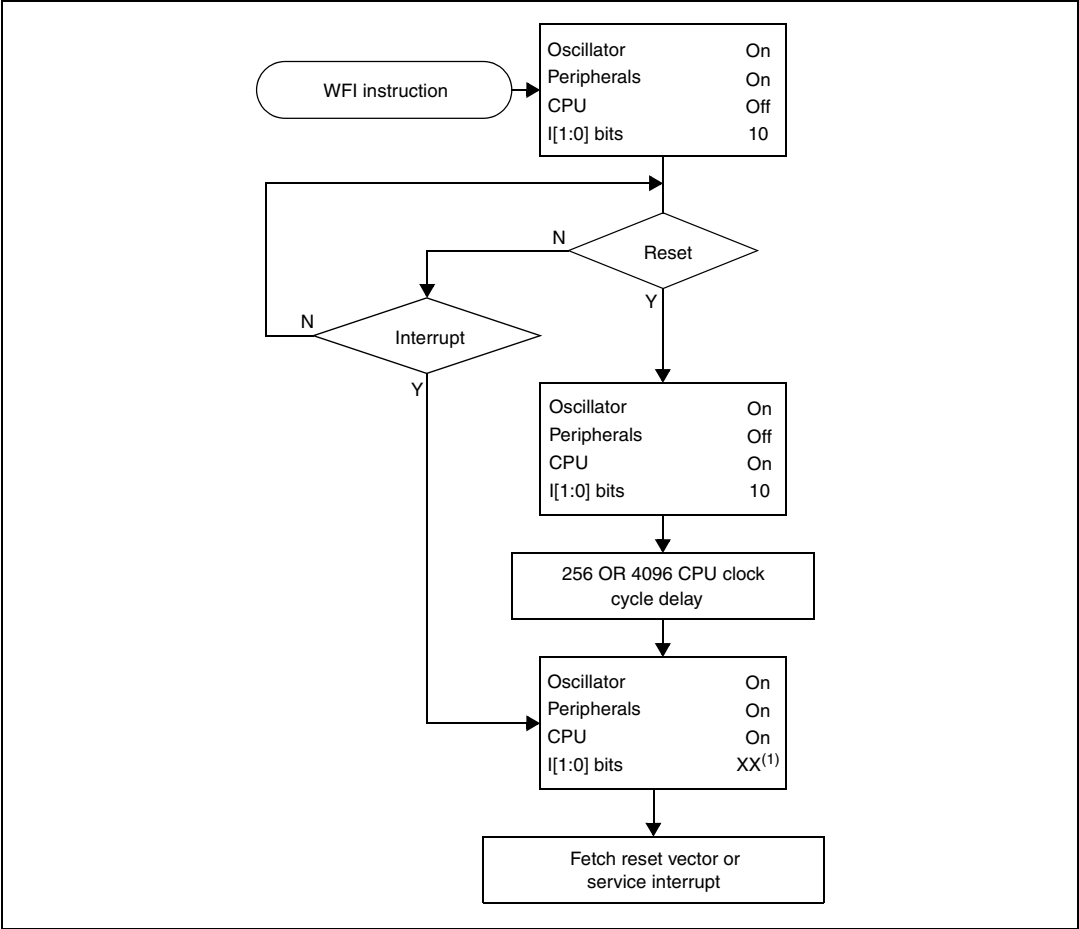
Wait mode places the MCU in a low power consumption mode by stopping the CPU.

This power saving mode is selected by calling the 'WFI' instruction.

All peripherals remain active. During wait mode, the I[1:0] bits of the CC register are forced to '10', to enable all interrupts. All other registers and memory remain unchanged. The MCU remains in wait mode until an interrupt or reset occurs, whereupon the program counter branches to the starting address of the interrupt or reset service routine. The MCU remains in Wait mode until a reset or an interrupt occurs, causing it to wake up.

Refer to [Figure 19: Wait mode flowchart on page 50](#).

Figure 19. Wait mode flowchart



1. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and recovered when the CC register is popped.

8.4 Active halt and halt modes

Active halt and halt modes are the two lowest power consumption modes of the MCU. They are both entered by executing the 'HALT' instruction. The decision to enter either in Active halt or halt mode is given by the MCC/RTC interrupt enable flag (OIE bit in MCCR register).

Table 15. Active halt and halt power saving modes

MCCR OIE bit	Power saving mode entered when HALT instruction is executed
0	Halt mode
1	Active halt mode

8.4.1 Active halt mode

Active halt mode is one of the lowest power consumption modes of the MCU with a real-time clock available. It is entered by executing the 'HALT' instruction when the OIE bit of the main clock controller status register (MCCSR) is set (see [Section 10.2: Main clock controller with real-time clock and beeper \(MCC/RTC\) on page 67](#) for more details on the MCCSR register).

The MCU can exit active halt mode on reception of either an MCC/RTC interrupt, a specific interrupt (see [Table 14: Interrupt mapping on page 47](#)) or a reset. When exiting active halt mode by means of an interrupt, no 256 or 4096 CPU cycle delay occurs. The CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see [Figure 21: Active halt mode flowchart on page 52](#)).

When entering active halt mode, the I[1:0] bits in the CC register are forced to '10b' to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

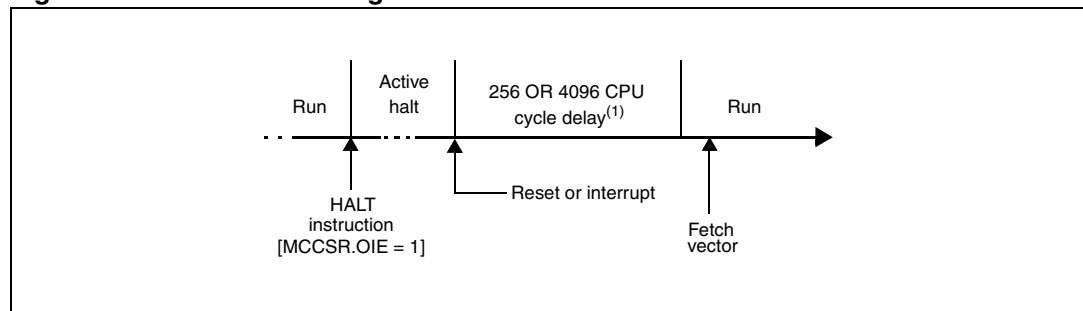
In active halt mode, only the main oscillator and its associated counter (MCC/RTC) are running to keep a wake up time base. All other peripherals are not clocked except those which get their clock supply from another clock generator (such as external or auxiliary oscillator).

The safeguard against staying locked in active halt mode is provided by the oscillator interrupt.

Note: As soon as the interrupt capability of one of the oscillators is selected (MCCSR.OIE bit set), entering active halt mode while the watchdog is active does not generate a reset. This means that the device cannot spend more than a defined delay in this power saving mode.

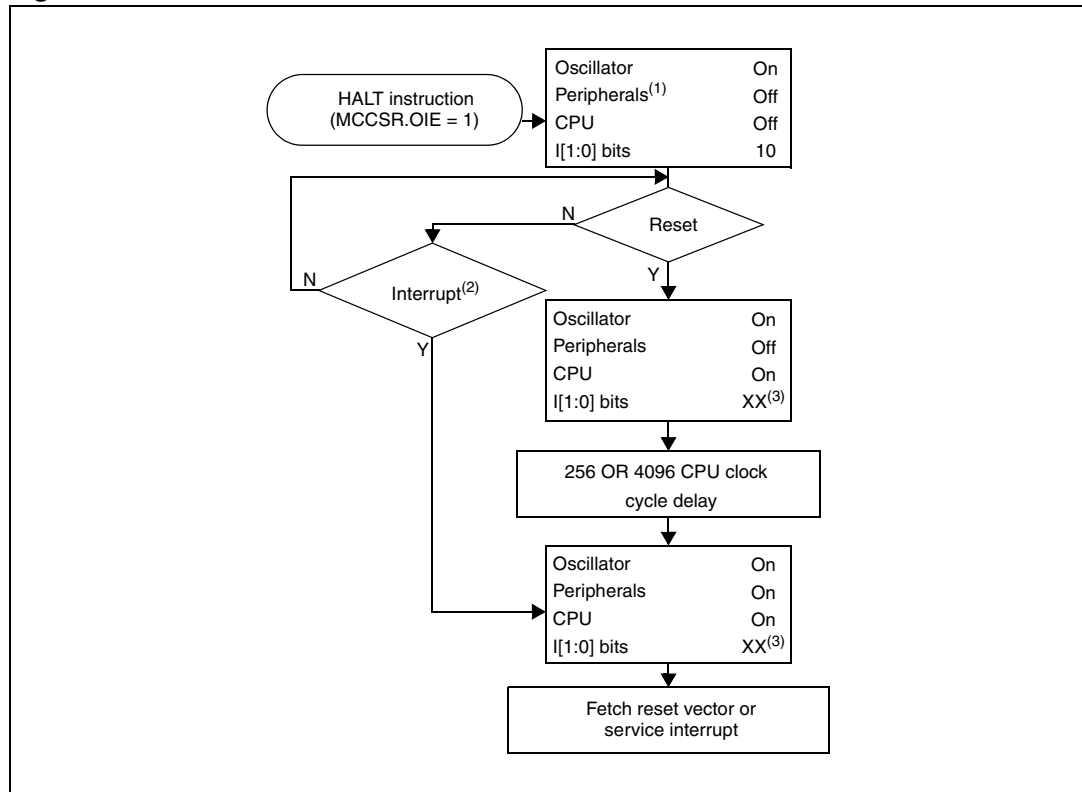
Caution: When exiting active halt mode following an interrupt, the OIE bit of MCCSR register must not be cleared before t_{DELAY} after the interrupt occurs ($t_{\text{DELAY}} = 256$ or $4096 t_{\text{CPU}}$ delay depending on option byte). Otherwise, the ST7 enters halt mode for the remaining t_{DELAY} period.

Figure 20. Active halt timing overview



1. This delay occurs only if the MCU exits active halt mode by means of a reset

Figure 21. Active halt mode flowchart



1. Peripheral clocked with an external clock source can still be active
2. Only the MCC/RTC interrupt and some specific interrupts can exit the MCU from active halt mode (such as external interrupt). Refer to [Table 14: Interrupt mapping on page 47](#) for more details.
3. Before servicing an interrupt, the CC register is pushed on the stack. The I[1:0] bits of the CC register are set to the current software priority level of the interrupt routine and restored when the CC register is popped.

8.4.2 Halt mode

The halt mode is the lowest power consumption modes of the MCU. It is entered by executing the 'HALT' instruction when the OIE bit of the main clock controller status register (MCCSR) is cleared (see [Section 10.2: Main clock controller with real-time clock and beeper \(MCC/RTC\) on page 67](#) for more details on the MCCSR register).

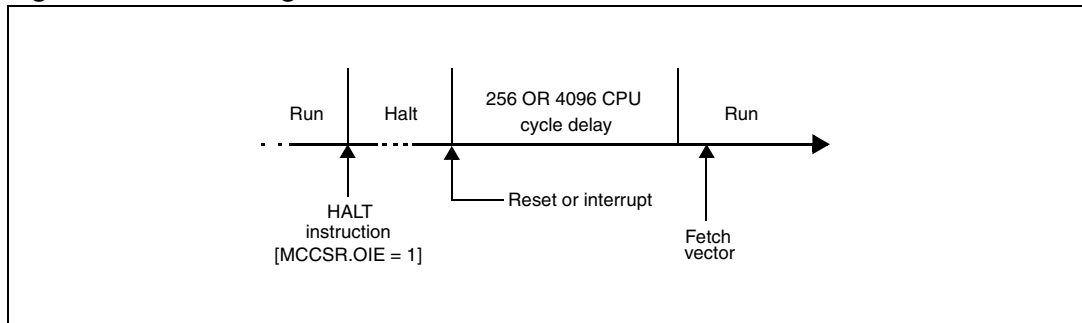
The MCU can exit halt mode on reception of either a specific interrupt (see [Table 14](#)) or a reset. When exiting halt mode by means of a reset or an interrupt, the oscillator is immediately turned on and the 256 or 4096 CPU cycle delay is used to stabilize the oscillator. After the start up delay, the CPU resumes operation by servicing the interrupt or by fetching the reset vector which woke it up (see [Figure 23: Halt mode flowchart on page 54](#)).

When entering halt mode, the I[1:0] bits in the CC register are forced to '10b' to enable interrupts. Therefore, if an interrupt is pending, the MCU wakes up immediately.

In halt mode, the main oscillator is turned off causing all internal processing to be stopped, including the operation of the on-chip peripherals. Peripherals are not clocked except those which get their clock supply from another clock generator (such as an external or auxiliary oscillator).

The compatibility of watchdog operation with halt mode is configured by the 'WDGHALT' option bit of the option byte. The HALT instruction when executed while the watchdog system is enabled, can generate a watchdog reset (see [Section 14.2.1: Flash configuration on page 207](#)) for more details.

Figure 22. Halt timing overview



Halt mode recommendations

- Make sure that an external event is available to wake up the microcontroller from halt mode
- When using an external interrupt to wake up the microcontroller, reinitialize the corresponding I/O as 'input pull-up with interrupt' before executing the HALT instruction. The main reason for this is that the I/O may be wrongly configured due to external interference or by an unforeseen logical condition.
- For the same reason, reinitialize the level sensitiveness of each external interrupt as a precautionary measure.
- The opcode for the HALT instruction is 0 x 8E. To avoid an unexpected HALT instruction due to a program counter failure, it is advised to clear all occurrences of the data value 0 x 8E from memory. For example, avoid defining a constant in ROM with the value 0 x 8E.
- As the HALT instruction clears the interrupt mask in the CC register to allow interrupts, the user may choose to clear all pending interrupt bits before executing the HALT instruction. This avoids entering other peripheral interrupt routines after executing the external interrupt routine corresponding to the wake up event (reset or external interrupt).

9 I/O ports

9.1 Introduction

The I/O ports offer different functional modes:

- Transfer of data through digital inputs and outputs

For specific pins they offer the following:

- External interrupt generation
- Alternate signal input/output for the on-chip peripherals

An I/O port contains up to 8 pins. Each pin can be programmed independently as digital input (with or without interrupt generation) or digital output.

9.2 Functional description

Each port has two main registers:

- Data register (DR)
- Data direction register (DDR)

Each port also has one optional register:

- Option register (OR)

Each I/O pin may be programmed using the corresponding register bits in the DDR and OR registers: bit X corresponding to pin X of the port. The same correspondence is used for the DR register.

The following description takes into account the OR register, (for specific ports which do not provide this register refer to [Section 9.3: I/O port implementation on page 60](#)). The generic I/O block diagram is shown in [Figure 24: I/O port general block diagram on page 58](#).

9.2.1 Input modes

The input configuration is selected by clearing the corresponding DDR register bit. In this case, reading the DR register returns the digital value applied to the external I/O pin. Different input modes can be selected by software through the OR register.

- Note:*
- 1 *Writing the DR register modifies the latch value but does not affect the pin status.*
 - 2 *When switching from input to output mode, the DR register has to be written first to drive the correct level on the pin as soon as the port is configured as an output.*
 - 3 *Do not use read/modify/write instructions (BSET or BRES) to modify the DR register as this might corrupt the DR content for I/Os configured as input.*

External interrupt function

When an I/O is configured as input with interrupt, an event on this I/O can generate an external interrupt request to the CPU.

Each pin can independently generate an interrupt request. The interrupt sensitivity is independently programmable using the sensitivity bits in the EICR register.

Each external interrupt vector is linked to a dedicated group of I/O port pins (see [Section 2: Package pinout and pin description on page 15](#) and [Section 7: Interrupts on page 36](#)). If several input pins are selected simultaneously as interrupt sources, these are first detected according to the sensitivity bits in the EICR register and then logically ORed.

The external interrupts are hardware interrupts, which means that the request latch (not accessible directly by the application) is automatically cleared when the corresponding interrupt vector is fetched. To clear an unwanted pending interrupt by software, the sensitivity bits in the EICR register must be modified.

9.2.2 Output modes

The output configuration is selected by setting the corresponding DDR register bit. In this case, writing the DR register applies this digital value to the I/O pin through the latch. Then reading the DR register returns the previously stored value.

Two different output modes can be selected by software through the OR register: Output push-pull and open-drain.

See [Table 16](#) for the DR register value and output pin status.

Table 16. DR register value and output pin status

DR	Push-pull	Open-drain
0	V _{SS}	V _{SS}
1	V _{DD}	Floating

9.2.3 Alternate functions

When an on-chip peripheral is configured to use a pin, the alternate function is automatically selected. This alternate function takes priority over the standard I/O programming.

When the signal is coming from an on-chip peripheral, the I/O pin is automatically configured in output mode (push-pull or open drain according to the peripheral).

When the signal is going to an on-chip peripheral, the I/O pin must be configured in input mode. In this case, the pin state is also digitally readable by addressing the DR register.

Note: Input pull-up configuration can cause unexpected value at the input of the alternate peripheral input. When an on-chip peripheral uses a pin as input and output, this pin has to be configured in input floating mode.

Figure 24. I/O port general block diagram

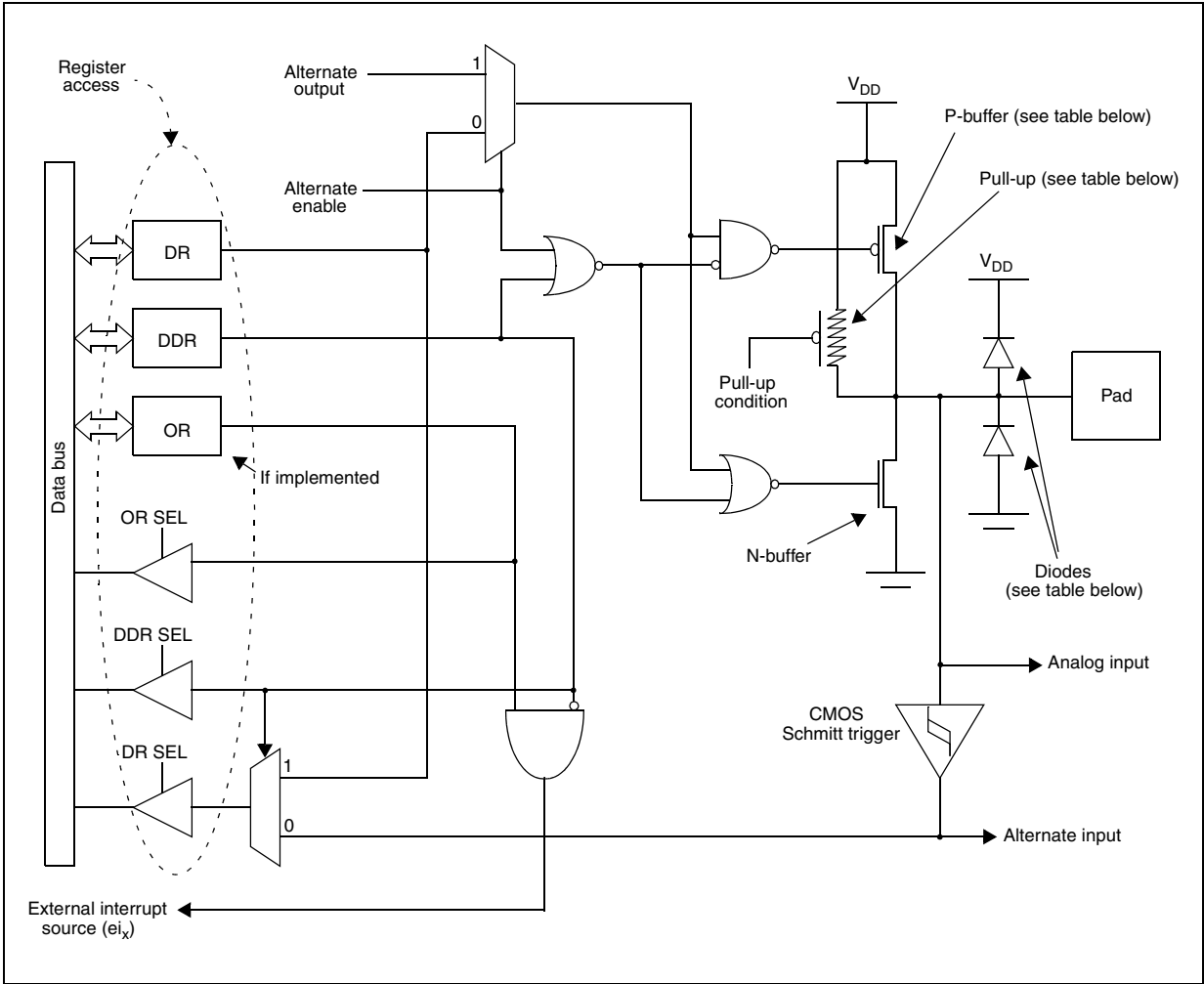


Table 17. I/O port mode options

Configuration mode		Pull-up	P-buffer	Diodes	
				to V _{DD}	to V _{SS}
Input	Floating with/without interrupt	Off ⁽¹⁾	Off ⁽¹⁾	On ⁽²⁾	On ⁽²⁾
	Pull-up with/without interrupt	On ⁽²⁾			
Output	Push-pull	Off ⁽¹⁾	On ⁽²⁾		
	Open drain (logic level)		Off ⁽¹⁾		
	True open drain	NI ⁽³⁾	NI ⁽³⁾	NI ⁽⁴⁾	

1. Implemented not activated

2. Implemented and activated

3. Not implemented

4. The diode to V_{DD} is not implemented in the true open drain pads. A local protection between the pad and V_{SS} is implemented to protect the device against positive stress.

Table 18. I/O port configurations

	Hardware configuration
Input ⁽¹⁾	<p>Not implemented in true open drain I/O ports</p> <p>Pad</p> <p>V_{DD}</p> <p>R_{PU}</p> <p>Pull-up condition</p> <p>DR register access</p> <p>DR register</p> <p>W</p> <p>R</p> <p>Data bus</p> <p>Alternate input</p> <p>Interrupt condition</p> <p>External interrupt source (ei_x)</p> <p>Analog input</p>
Open-drain output ⁽²⁾	<p>Not implemented in true open drain I/O ports</p> <p>Pad</p> <p>V_{DD}</p> <p>R_{PU}</p> <p>DR register access</p> <p>DR register</p> <p>R/W</p> <p>Data bus</p> <p>Alternate enable</p> <p>Alternate output</p>
Push-pull output ⁽²⁾	<p>Not implemented in true open drain I/O ports</p> <p>Pad</p> <p>V_{DD}</p> <p>R_{PU}</p> <p>DR register access</p> <p>DR register</p> <p>R/W</p> <p>Data bus</p> <p>Alternate enable</p> <p>Alternate output</p>

1. When the I/O port is in input configuration and the associated alternate function is enabled as an output, reading the DR register reads the alternate function output status.
2. When the I/O port is in output configuration and the associated alternate function is enabled as an input, the alternate function reads the pin status given by the DR register content.

Caution: The alternate function must not be activated as long as the pin is configured as input with interrupt, in order to avoid generating spurious interrupts.

Analog alternate function

When the pin is used as an ADC input, the I/O must be configured as floating input. The analog multiplexer (controlled by the ADC registers) switches the analog voltage present on the selected pin to the common analog rail which is connected to the ADC input.

It is recommended not to change the voltage level or loading on any port pin while conversion is in progress. Furthermore it is recommended not to have clocking pins located close to a selected analog pin.

Warning: The analog input voltage level must be within the limits stated in the absolute maximum ratings.

9.3 I/O port implementation

The hardware implementation on each I/O port depends on the settings in the DDR and OR registers and specific features of the I/O port such as ADC input or true open drain.

Switching these I/O ports from one state to another should be done in a sequence that prevents unwanted side effects. Recommended safe transitions are illustrated in [Figure 25](#). Other transitions are potentially risky and should be avoided, since they are likely to present unwanted side-effects such as spurious interrupt generation. The I/O port register configurations are summarized in [Table 19: Port register configurations on page 61](#).

Figure 25. Interrupt I/O port state transitions

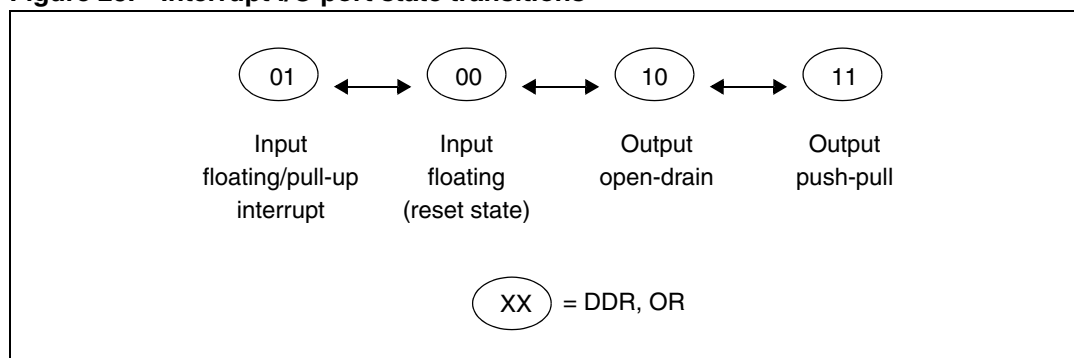


Table 19. Port register configurations

Port	Pin name	Input (DDR = 0)		Output (DDR = 1)		
		OR = 0	OR = 1	OR = 0	OR = 1	
Port A	PA[7:6]	Floating		True open-drain		
	PA[5:4]	Floating	Pull-up	Open drain	Push-pull	
	PA[3]		Floating interrupt			
Port B	PB[3]		Pull-up interrupt			
	PB[4] PB[2:0]					
Port C	PC[7:0]		Pull-up			
Port D	PD[5:0]					
Port E	PE[1:0]					
Port F	PF[7:6] PF[4]					Pull-up interrupt
	PF[2:0]					

9.4 Low power modes

Table 20. Effect of low power modes on I/O ports

Mode	Description
Wait	No effect on I/O ports. External interrupts cause the device to exit from wait mode.
Halt	No effect on I/O ports. External interrupts cause the device to exit from halt mode.

9.5 Interrupts

The external interrupt event generates an interrupt if the corresponding configuration is selected with DDR and OR registers and the interrupt mask in the CC register is not active (RIM instruction).

Table 21. I/O interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
External interrupt on selected external event	-	DDRx ORx	Yes	Yes

Table 22. I/O port register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
Reset value of all I/O port registers		0	0	0	0	0	0	0	0
0000h	PADR	MSB							LSB
0001h	PADDR								
0002h	PAOR								
0003h	PBDR	MSB							LSB
0004h	PBDDR								
0005h	PBOR								
0006h	PCDR	MSB							LSB
0007h	PCDDR								
0008h	PCOR								
0009h	PDDR	MSB							LSB
000Ah	PDDDR								
000Bh	PDOR								
000Ch	PEDR	MSB							LSB
000Dh	PEDDR								
000Eh	PEOR								
000Fh	PFDR	MSB							LSB
0010h	PFDDR								
0011h	PFOR								

10 On-chip peripherals

10.1 Watchdog timer (WDG)

10.1.1 Introduction

The watchdog timer is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The watchdog circuit generates an MCU reset on expiry of a programmed time period, unless the program refreshes the counter's contents before the T6 bit becomes cleared.

10.1.2 Main features

- Programmable free-running downcounter
- Programmable reset
- Reset (if watchdog activated) when the T6 bit reaches zero
- Optional reset on HALT instruction (configurable by option byte)
- Hardware watchdog selectable by option byte

10.1.3 Functional description

The counter value stored in the watchdog control register (WDGCR bits T[6:0]), is decremented every $16384 f_{OSC2}$ cycles (approx.), and the length of the timeout period can be programmed by the user in 64 increments.

If the watchdog is activated (the WDGA bit is set) and when the 7-bit timer (bits T[6:0]) rolls over from 40h to 3Fh (T6 is cleared), it initiates a reset cycle pulling the **RESET** pin low for typically 30µs.

The application program must write in the WDGCR register at regular intervals during normal operation to prevent an MCU reset. This downcounter is free-running: it counts down even if the watchdog is disabled. The value to be stored in the WDGCR register must be between FFh and C0h:

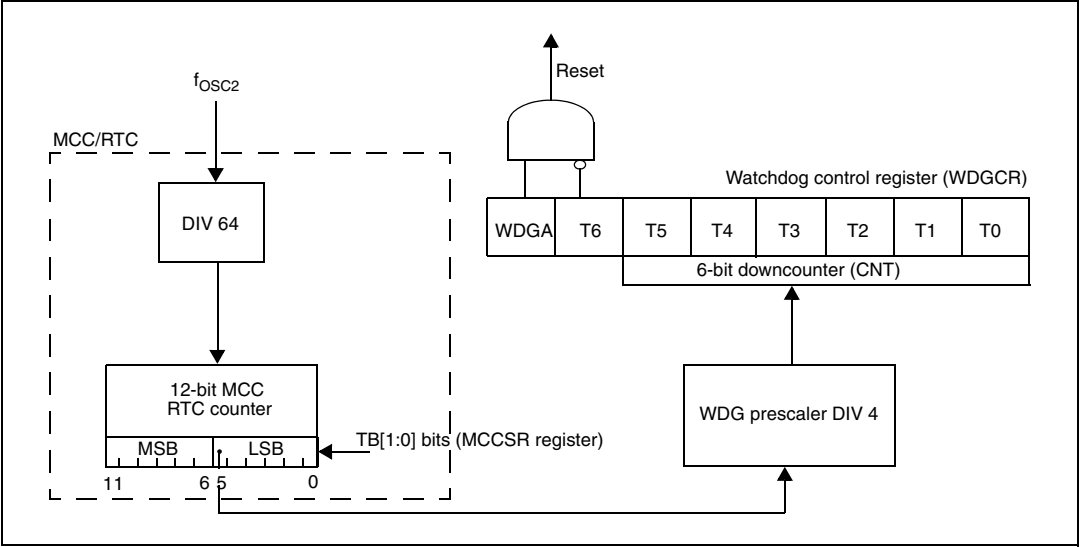
- The WDGA bit is set (watchdog enabled)
- The T6 bit is set to prevent generating an immediate reset
- The T[5:0] bits contain the number of increments which represents the time delay before the watchdog produces a reset (see [Figure 27: Approximate timeout duration on page 64](#)). The timing varies between a minimum and a maximum value due to the unknown status of the prescaler when writing to the WDGCR register (see [Figure 28: Exact timeout duration \(tmin and tmax\) on page 65](#)).

Following a reset, the watchdog is disabled. Once activated it cannot be disabled, except by a reset.

The T6 bit can be used to generate a software reset (the WDGA bit is set and the T6 bit is cleared).

If the watchdog is activated, the HALT instruction generates a reset.

Figure 26. Watchdog block diagram



10.1.4 How to program the watchdog timeout

Figure 27 shows the linear relationship between the 6-bit value to be loaded in the watchdog counter (CNT) and the resulting timeout duration in milliseconds. This can be used for a quick calculation without taking the timing variations into account. If more precision is needed, use the formulae in [Figure 28: Exact timeout duration \(\$t_{min}\$ and \$t_{max}\$ \) on page 65](#).

Caution: When writing to the WDGCR register, always write 1 in the T6 bit to avoid generating an immediate reset.

Figure 27. Approximate timeout duration

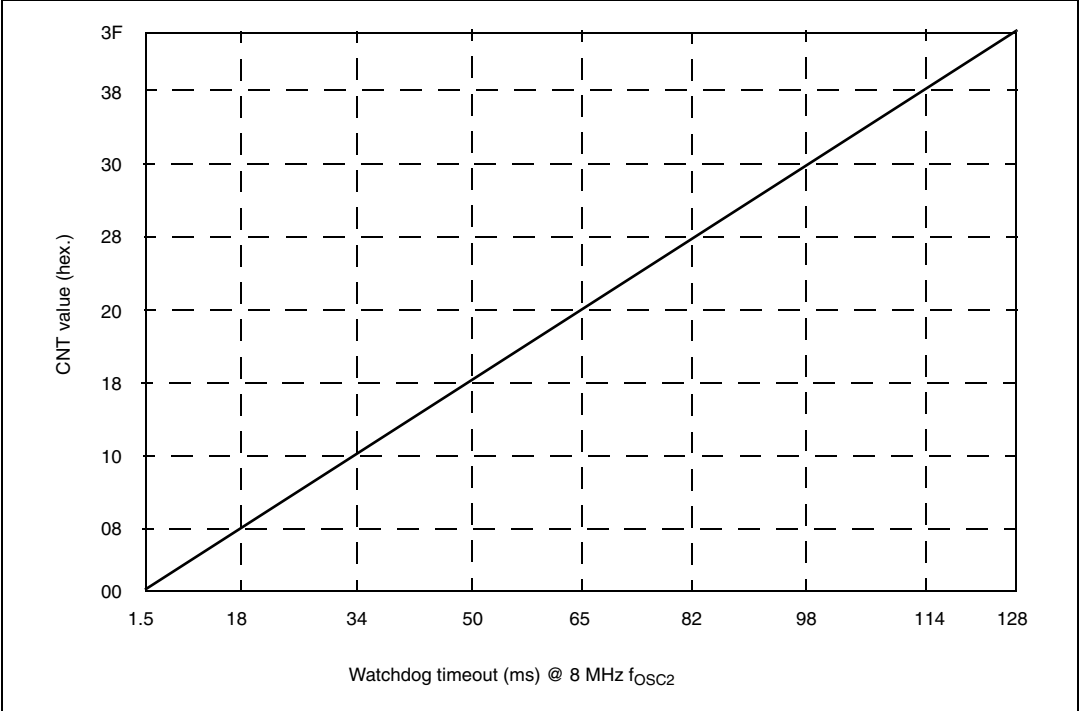


Figure 28. Exact timeout duration (t_{\min} and t_{\max})**Where:**

$$t_{\min 0} = (\text{LSB} + 128) \times 64 \times t_{\text{OSC2}}$$

$$t_{\max 0} = 16384 \times t_{\text{OSC2}}$$

$$t_{\text{OSC2}} = 125\text{ns if } f_{\text{OSC2}} = 8\text{ MHz}$$

CNT = value of T[5:0] bits in the WDGCR register (6 bits)

MSB and LSB are values from the table below depending on the timebase selected by the TB[1:0] bits in the MCCR register.

TB1 bit (MCCR reg.)	TB0 bit (MCCR reg.)	Selected MCCR timebase	MSB	LSB
0	0	2ms	4	59
0	1	4ms	8	53
1	0	10ms	20	35
1	1	25ms	49	54

To calculate the minimum watchdog timeout (t_{\min}):

$$\text{If } \text{CNT} < \left\lceil \frac{\text{MSB}}{4} \right\rceil \quad \text{Then } t_{\min} = t_{\min 0} + 16384 \times \text{CNT} \times t_{\text{osc2}}$$

$$\text{Else } t_{\min} = t_{\min 0} + \left[16384 \times \left(\text{CNT} - \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right) + (192 + \text{LSB}) \times 64 \times \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right] \times t_{\text{osc2}}$$

To calculate the maximum watchdog timeout (t_{\max}):

$$\text{If } \text{CNT} \leq \left\lceil \frac{\text{MSB}}{4} \right\rceil \quad \text{Then } t_{\max} = t_{\max 0} + 16384 \times \text{CNT} \times t_{\text{osc2}}$$

$$\text{Else } t_{\max} = t_{\max 0} + \left[16384 \times \left(\text{CNT} - \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right) + (192 + \text{LSB}) \times 64 \times \left\lceil \frac{4\text{CNT}}{\text{MSB}} \right\rceil \right] \times t_{\text{osc2}}$$

Note: In the above formulae, division results must be rounded down to the next integer value.

Example: with 2ms timeout selected in MCCR register

Value of T[5:0] bits in WDGCR register (Hex.)	Min. watchdog timeout (ms) t_{\min}	Max. watchdog timeout (ms) t_{\max}
00	1.496	2.048
3F	128	128.552

10.1.5 Low power modes

Table 23. Effect of low power modes on watchdog timer

Mode	Description		
Slow	No effect on watchdog		
Wait	No effect on watchdog		
Halt	OIE bit in MCCR register	WDGHALT bit in option byte	
	0	0	No watchdog reset is generated. The MCU enters halt mode. The watchdog counter is decremented once and then stops counting and is no longer able to generate a watchdog reset until the MCU receives an external interrupt or a reset. If an external interrupt is received, the watchdog restarts counting after 256 or 4096 CPU clocks. If a reset is generated, the watchdog is disabled (reset state) unless hardware watchdog is selected by option byte. For application recommendations see Section 10.1.7 below.
	0	1	A reset is generated.
	1	x	No reset is generated. The MCU enters active halt mode. The watchdog counter is not decremented. It stops counting. When the MCU receives an oscillator interrupt or external interrupt, the watchdog restarts counting immediately. When the MCU receives a reset the watchdog restarts counting after 256 or 4096 CPU clocks.

10.1.6 Hardware watchdog option

If hardware watchdog is selected by option byte, the watchdog is always active and the WDGA bit in the WDGCR is not used. Refer to [Section 14.2.1: Flash configuration on page 207](#).

10.1.7 Using halt mode with the WDG (WDGHALT option)

The following recommendation applies if halt mode is used when the watchdog is enabled:

Before executing the HALT instruction, refresh the WDG counter, to avoid an unexpected WDG reset immediately after waking up the microcontroller.

10.1.8 Interrupts

None

10.1.9 Control register (WDGCR)

WDGCR							Reset value: 0111 1111 (7Fh)	
7	6	5	4	3	2	1	0	
WDGA	T[6:0]							
R/W	R/W							

Table 24. WDGCR register description

Bit	Bit name	Function
7	WDGA	Activation bit ⁽¹⁾ This bit is set by software and only cleared by hardware after a reset. When WDGA = 1, the watchdog can generate a reset. 0: Watchdog disabled 1: Watchdog enabled
6:0	T[6:0]	7-bit counter (MSB to LSB) These bits contain the value of the watchdog counter. They are decremented every 16384 f _{OSC2} cycles (approx.). A reset is produced when it rolls over from 40h to 3Fh (T6 is cleared).

1. The WDGA bit is not used if the hardware watchdog option is enabled by option byte.

10.1.10 Watchdog timer register map and reset values

Table 25. Watchdog timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
002Ah	WDGCR	WDGA	T6	T5	T4	T3	T2	T1	T0
	Reset value	0	1	1	1	1	1	1	1

10.2 Main clock controller with real-time clock and beeper (MCC/RTC)

The main clock controller consists of three different functions:

- A programmable CPU clock prescaler
- A clock-out signal to supply external devices
- A real-time clock timer with interrupt capability

Each function can be used independently and simultaneously.

10.2.1 Programmable CPU clock prescaler

The programmable CPU clock prescaler supplies the clock for the ST7 CPU and its internal peripherals. It manages Slow power saving mode (see [Section 8.2: Slow mode on page 48](#) for more details).

The prescaler selects the f_{CPU} main clock frequency and is controlled by three bits in the MCCSR register: CP[1:0] and SMS.

10.2.2 Clock-out capability

The clock-out capability is an alternate function of an I/O port pin that outputs a f_{OSC2} clock to drive external devices. It is controlled by the MCO bit in the MCCSR register.

Caution: When selected, the clock out pin suspends the clock during active halt mode.

10.2.3 Real-time clock timer (RTC)

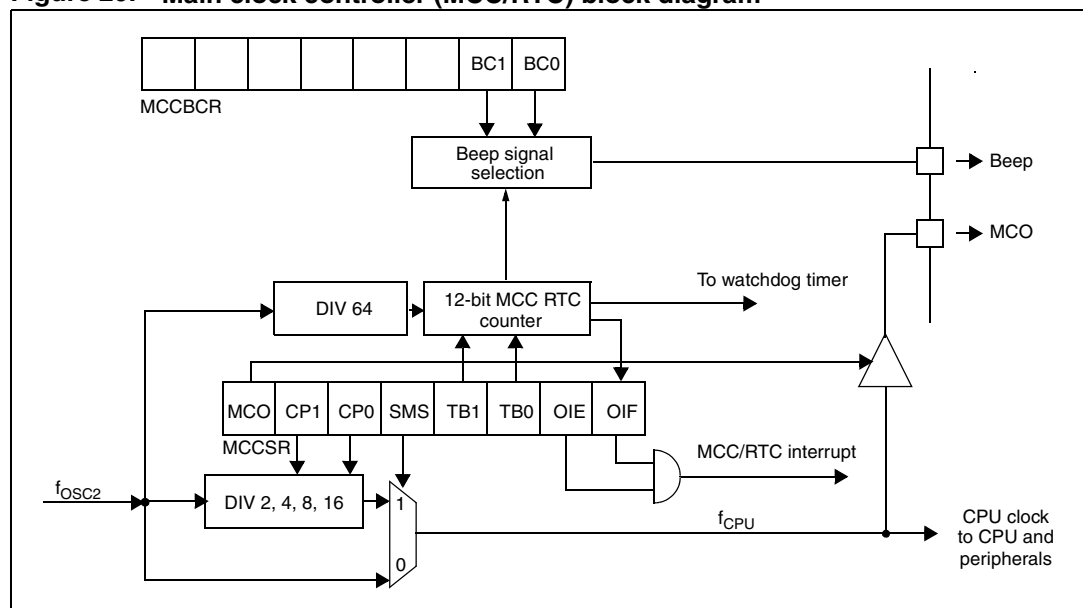
The counter of the real-time clock timer allows an interrupt to be generated based on an accurate real-time clock. Four different time bases depending directly on f_{OSC2} are available. The whole functionality is controlled by four bits of the MCCSR register: TB[1:0], OIE and OIF.

When the RTC interrupt is enabled (OIE bit set), the ST7 enters active halt mode when the HALT instruction is executed. See [Section 8.4: Active halt and halt modes on page 50](#) for more details.

10.2.4 Beeper

The beep function is controlled by the MCCBCR register. It can output three selectable frequencies on the BEEP pin (I/O port alternate function).

Figure 29. Main clock controller (MCC/RTC) block diagram



10.2.5 Low power modes

Table 26. Effect of low power modes on MCC/RTC

Mode	Description
Wait	No effect on MCC/RTC peripheral. MCC/RTC interrupt causes the device to exit from wait mode.
Active Halt	No effect on MCC/RTC counter (OIE bit is set), the registers are frozen. MCC/RTC interrupt causes the device to exit from active halt mode.
Halt	MCC/RTC counter and registers are frozen. MCC/RTC operation resumes when the MCU is woken up by an interrupt with 'exit from halt' capability.

10.2.6 Interrupts

The MCC/RTC interrupt event generates an interrupt if the OIE bit of the MCCSR register is set and the interrupt mask in the CC register is not active (RIM instruction).

Table 27. MCC/RTC interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
Time base overflow event	OIF	OIE	Yes	No ⁽¹⁾

1. The MCC/RTC interrupt wakes up the MCU from Active Halt mode, not from Halt mode

10.2.7 MCC/RTC registers

MCC control/status register (MCCSR)

MCCSR

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
MCO	CP[1:0]		SMS	TB[1:0]		OIE	OIF
R/W	R/W		R/W	R/W		R/W	R/W

Table 28. MCCSR register description

Bit	Bit name	Function
7	MCO	<p>Main clock out selection</p> <p>This bit enables the MCO alternate function on the PF0 I/O port. It is set and cleared by software.</p> <p>0: MCO alternate function disabled (I/O pin free for general-purpose I/O)</p> <p>1: MCO alternate function enabled (f_{CPU} on I/O port)</p> <p><i>Note: To reduce power consumption, the MCO function is not active in active halt mode.</i></p>
6:5	CP[1:0]	<p>CPU clock prescaler</p> <p>These bits select the CPU clock prescaler which is applied in the different slow modes. Their action is conditioned by the setting of the SMS bit. These two bits are set and cleared by software.</p> <p>00: f_{CPU} in slow mode = $f_{OSC2}/2$</p> <p>01: f_{CPU} in slow mode = $f_{OSC2}/4$</p> <p>10: f_{CPU} in slow mode = $f_{OSC2}/8$</p> <p>11: f_{CPU} in slow mode = $f_{OSC2}/16$</p>
4	SMS	<p>Slow mode select</p> <p>This bit is set and cleared by software.</p> <p>0: Normal mode, $f_{CPU} = f_{OSC2}$</p> <p>1: Slow mode, f_{CPU} is given by CP1, CP0; see Section 8.2: Slow mode on page 48 and Section 10.2: Main clock controller with real-time clock and beeper (MCC/RTC) on page 67 for more details.</p>
3:2	TB[1:0]	<p>Time base control</p> <p>These bits select the programmable divider time base. They are set and cleared by software:</p> <p>00: Time base (for counter prescaler 16000) = 4ms ($f_{OSC2} = 4$ MHz) and 2ms ($f_{OSC2} = 8$ MHz)</p> <p>01: Time base (for counter prescaler 32000) = 8ms ($f_{OSC2} = 4$ MHz) and 4ms ($f_{OSC2} = 8$ MHz)</p> <p>10: Time base (for counter prescaler 80000) = 20ms ($f_{OSC2} = 4$ MHz) and 10ms ($f_{OSC2} = 8$ MHz)</p> <p>11: Time base (for counter prescaler 200000) = 50ms ($f_{OSC2} = 4$ MHz) and 25ms ($f_{OSC2} = 8$ MHz)</p> <p>A modification of the time base is taken into account at the end of the current period (previously set) to avoid an unwanted time shift. This allows use of this time base as a real-time clock.</p>

Table 28. MCCR register description (continued)

Bit	Bit name	Function
1	OIE	Oscillator interrupt enable This bit set and cleared by software. 0: Oscillator interrupt disabled 1: Oscillator interrupt enabled This interrupt can be used to exit from active halt mode. When this bit is set, calling the ST7 software HALT instruction enters the active halt power saving mode.
0	OIF	Oscillator interrupt flag This bit is set by hardware and cleared by software reading the MCCR register. It indicates when set that the main oscillator has reached the selected elapsed time (TB1:0). 0: Timeout not reached 1: Timeout reached Caution: The BRES and BSET instructions must not be used on the MCCR register to avoid unintentionally clearing the OIF bit.

MCC beep control register (MCCBCR)

MCCBCR

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved						BC[1:0]	
-						R/W	

Table 29. MCCBCR register description

Bit	Bit name	Function
7:2	-	Reserved, must be kept cleared.
1:0	BC[1:0]	Beep control These 2 bits select the PF1 pin beep capability: 00: Beep mode (with $f_{OSC2} = 8\text{ MHz}$) = off 01: Beep mode (with $f_{OSC2} = 8\text{ MHz}$) = ~2 kHz (output beep signal ~ 50% duty cycle) 10: Beep mode (with $f_{OSC2} = 8\text{ MHz}$) = ~1 kHz (output beep signal ~ 50% duty cycle) 11: beep mode (with $f_{OSC2} = 8\text{ MHz}$) = ~500 Hz (output beep signal ~ 50% duty cycle) The beep output signal is available in active halt mode but has to be disabled to reduce the consumption.

10.2.8 MCC register map and reset values

Table 30. Main clock controller register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
002Ch	MCCSR Reset value	MCO 0	CP1 0	CP0 0	SMS 0	TB1 0	TB0 0	OIE 0	OIF 0
002Dh	MCCBCR Reset value	0	0	0	0	0	0	BC1 0	BC0 0

10.3 PWM auto-reload timer (ART)

10.3.1 Introduction

The pulse width modulated auto-reload timer on-chip peripheral consists of an 8-bit auto-reload counter with compare/capture capabilities and of a 7-bit prescaler clock source.

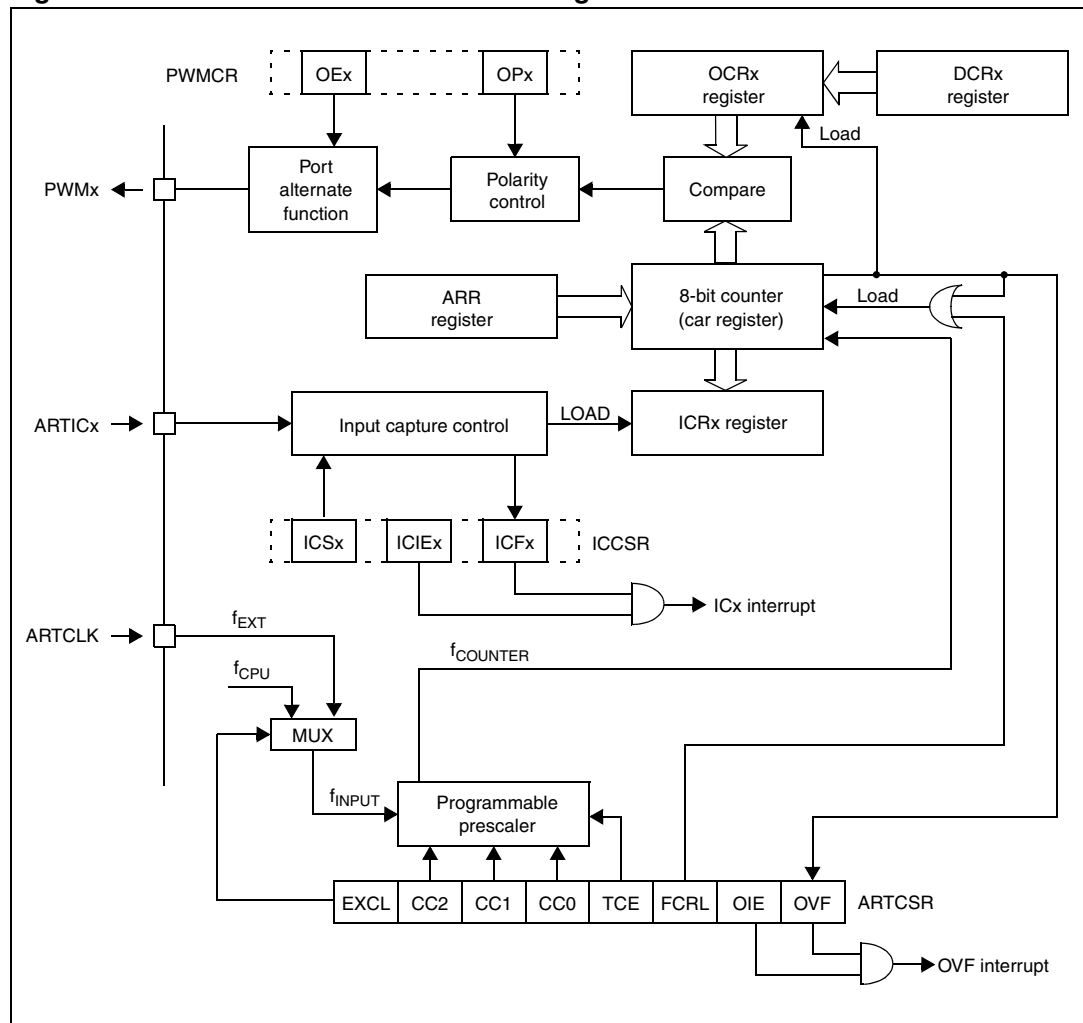
These resources allow five possible operating modes:

- Generation of up to 4 independent PWM signals
- Output compare and time base interrupt
- Up to two input capture functions
- External event detector
- Up to two external interrupt sources

The three first modes can be used together with a single counter frequency.

The timer can be used to wake up the MCU from wait and halt modes.

Figure 30. PWM auto-reload timer block diagram



10.3.2 Functional description

Counter

The free running 8-bit counter is fed by the output of the prescaler, and is incremented on every rising edge of the clock signal.

It is possible to read or write the contents of the counter on the fly by reading or writing the counter access register (ARTCAR).

When a counter overflow occurs, the counter is automatically reloaded with the contents of the ARTARR register (the prescaler is not affected).

Counter clock and prescaler

The counter clock frequency is given by:

$$f_{\text{COUNTER}} = f_{\text{INPUT}} / 2^{\text{CC}[2:0]}$$

The timer counter's input clock (f_{INPUT}) feeds the 7-bit programmable prescaler, which selects one of the 8 available taps of the prescaler, as defined by CC[2:0] bits in the

control/status register (ARTCSR). Thus the division factor of the prescaler can be set to 2^n (where $n = 0, 1, \dots, 7$).

This f_{INPUT} frequency source is selected through the EXCL bit of the ARTCSR register and can be either the f_{CPU} or an external input frequency f_{EXT} .

The clock input to the counter is enabled by the TCE (timer counter enable) bit in the ARTCSR register. When TCE is reset, the counter is stopped and the prescaler and counter contents are frozen. When TCE is set, the counter runs at the rate of the selected clock source.

Counter and prescaler initialization

After reset, the counter and the prescaler are cleared and $f_{\text{INPUT}} = f_{\text{CPU}}$.

The counter can be initialized by:

- Writing to the ARTARR register and then setting the FCRL (force counter reload) and the TCE (timer counter enable) bits in the ARTCSR register
- Writing to the ARTCAR counter access register

In both cases the 7-bit prescaler is also cleared, whereupon counting will start from a known value.

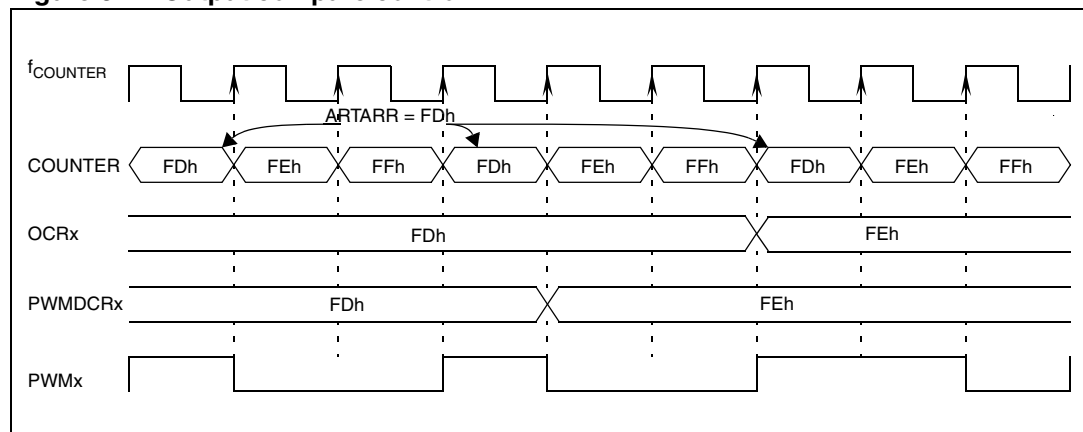
Direct access to the prescaler is not possible.

Output compare control

The timer compare function is based on four different comparisons with the counter (one for each PWMx output). Each comparison is made between the counter value and an output compare register (OCRx) value. This OCRx register cannot be accessed directly, it is loaded from the duty cycle register (PWMDCRx) at each overflow of the counter.

This double buffering method avoids glitch generation when changing the duty cycle on the fly.

Figure 31. Output compare control



Independent PWM signal generation

This mode allows up to four pulse width modulated signals to be generated on the PWMx output pins with minimum core processing overhead. This function is stopped during halt mode.

Each PWMx output signal can be selected independently using the corresponding OEx bit in the PWM control register (PWMCR). When this bit is set, the corresponding I/O pin is configured as output push-pull alternate function.

The PWM signals all have the same frequency which is controlled by the counter period and the ARTARR register value.

$$f_{\text{PWM}} = f_{\text{COUNTER}} / (256 - \text{ARTARR})$$

When a counter overflow occurs, the PWMx pin level is changed depending on the corresponding OPx (output polarity) bit in the PWMCR register. When the counter reaches the value contained in one of the output compare register (OCRx) the corresponding PWMx pin level is restored.

It should be noted that the reload values also affect the value and the resolution of the duty cycle of the PWM output signal. To obtain a signal on a PWMx pin, the contents of the OCRx register must be greater than the contents of the ARTARR register.

The maximum available resolution for the PWMx duty cycle is:

$$\text{Resolution} = 1 / (256 - \text{ARTARR})$$

Note: To get the maximum resolution (1/256), the ARTARR register must be 0. With this maximum resolution, 0% and 100% can be obtained by changing the polarity.

Figure 32. PWM auto-reload timer function

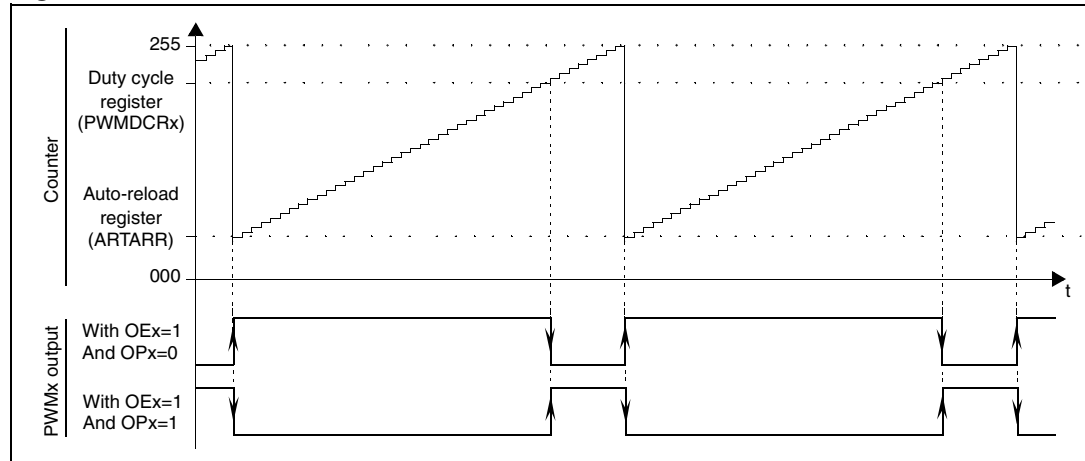
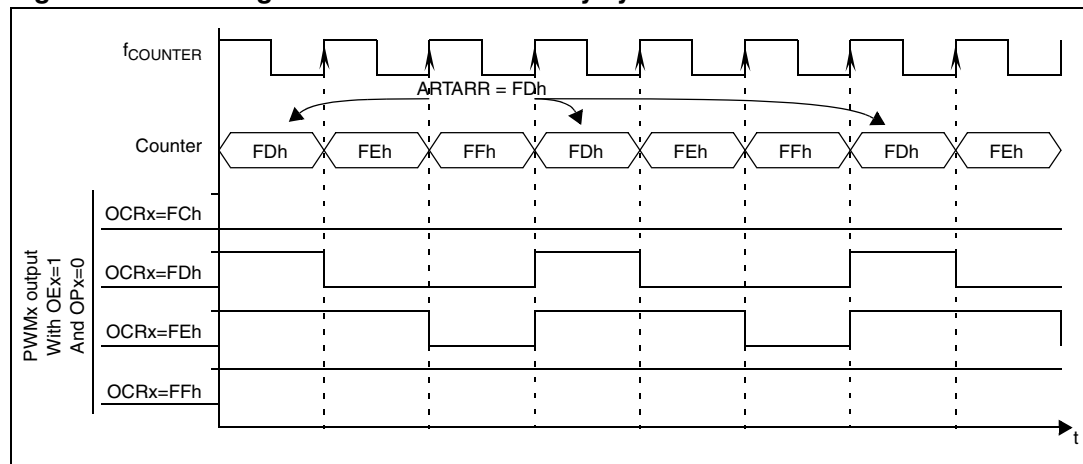


Figure 33. PWM signal from 0% to 100% duty cycle

Output compare and time base interrupt

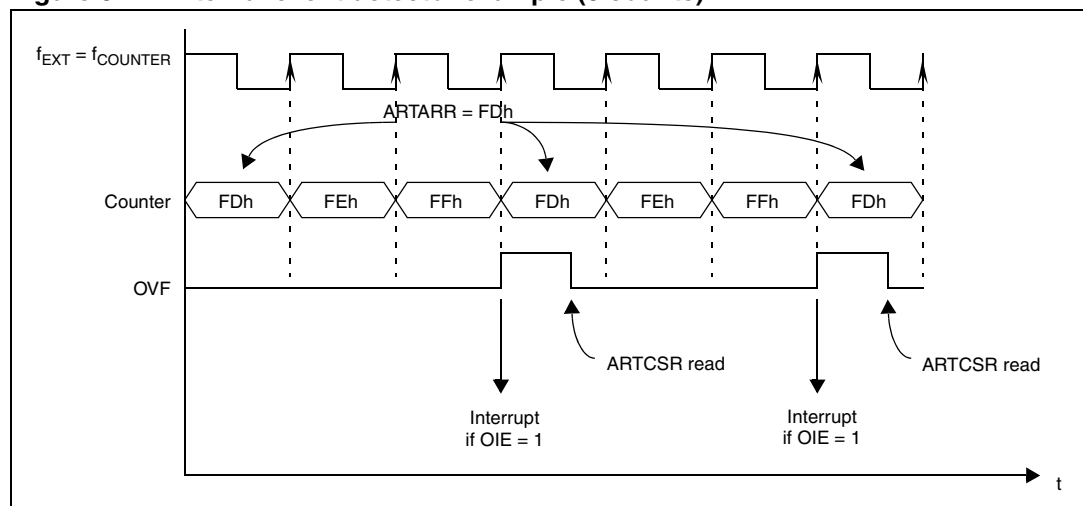
On overflow, the OVF flag of the ARTCSR register is set and an overflow interrupt request is generated if the overflow interrupt enable bit, OIE, in the ARTCSR register, is set. The OVF flag must be reset by the user software. This interrupt can be used as a time base in the application.

External clock and event detector mode

Using the f_{EXT} external prescaler input clock, the auto-reload timer can be used as an external clock event detector. In this mode, the ARTARR register is used to select the n_{EVENT} number of events to be counted before setting the OVF flag.

$$n_{EVENT} = 256 - ARTARR$$

Caution: The external clock function is not available in halt mode. If halt mode is used in the application, prior to executing the HALT instruction, the counter must be disabled by clearing the TCE bit in the ARTCSR register to avoid spurious counter increments.

Figure 34. External event detector example (3 counts)

Input capture function

This mode allows the measurement of external signal pulse widths through ARTICRx registers.

Each input capture can generate an interrupt independently on a selected input signal transition. This event is flagged by a set of the corresponding CFx bits of the input capture control/status register (ARTICCSR).

These input capture interrupts are enabled through the CIEx bits of the ARTICCSR register.

The active transition (falling or rising edge) is software programmable through the CSx bits of the ARTICCSR register.

The read only input capture registers (ARTICRx) are used to latch the auto-reload counter value when a transition is detected on the ARTICx pin (CFx bit set in ARTICCSR register). After fetching the interrupt vector, the CFx flags can be read to identify the interrupt source.

Note: *After a capture detection, data transfer in the ARTICRx register is inhibited until it is read (clearing the CFx bit).*

The timer interrupt remains pending while the CFx flag is set when the interrupt is enabled (CIEx bit set). This means that the ARTICRx register has to be read at each capture event to clear the CFx flag.

The timing resolution is given by auto-reload counter cycle time ($1/f_{\text{COUNTER}}$).

Note: *During halt mode, if both the input capture and the external clock are enabled, the ARTICRx register value is not guaranteed if the input capture pin and the external clock change simultaneously.*

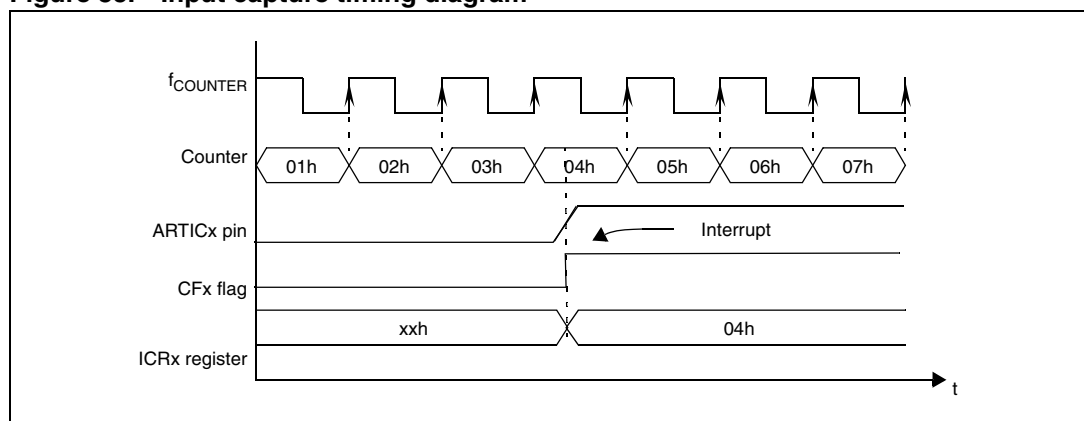
External interrupt capability

This mode allows the input capture capabilities to be used as external interrupt sources. The interrupts are generated on the edge of the ARTICx signal.

The edge sensitivity of the external interrupts is programmable (CSx bit of ARTICCSR register) and they are independently enabled through CIEx bits of the ARTICCSR register. After fetching the interrupt vector, the CFx flags can be read to identify the interrupt source.

During halt mode, the external interrupts can be used to wake up the microcontroller (if the CIEx bit is set).

Figure 35. Input capture timing diagram



10.3.3 ART registers

Control/status register (ARTCSR)

ARTCSR

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
EXCL	CC[2:0]			TCE	FCRL	OIE	OVF
R/W	R/W			R/W	R/W	R/W	R/W

Table 31. ARTCSR register description

Bit	Name	Function
7	EXCL	<i>External clock</i> This bit is set and cleared by software. It selects the input clock for the 7-bit prescaler. 0: CPU clock 1: External clock
6:4	CC[2:0]	<i>Counter clock control</i> These bits are set and cleared by software. They determine the prescaler division ratio from f_{INPUT} (see Table 32 on page 79).
3	TCE	<i>Timer counter enable</i> This bit is set and cleared by software. It puts the timer in the lowest power consumption mode. 0: Counter stopped (prescaler and counter frozen) 1: Counter running
2	FCRL	<i>Force counter reload</i> This bit is write-only and any attempt to read it will yield a logical zero. When set, it causes the contents of ARTARR register to be loaded into the counter, and the content of the prescaler register to be cleared in order to initialize the timer before starting to count.
1	OIE	<i>Overflow interrupt enable</i> This bit is set and cleared by software. It allows to enable/disable the interrupt which is generated when the OVF bit is set. 0: Overflow Interrupt disable 1: Overflow Interrupt enable
0	OVF	<i>Overflow flag</i> This bit is set by hardware and cleared by software reading the ARTCSR register. It indicates the transition of the counter from FFh to the ARTARR value. 0: New transition not yet reached 1: Transition reached

Table 32. Prescaler selection for ART

f_{COUNTER}	With $f_{\text{INPUT}} = 8 \text{ MHz}$	CC2	CC1	CC0
f_{INPUT}	8 MHz	0	0	0
$f_{\text{INPUT}}/2$	4 MHz	0	0	1
$f_{\text{INPUT}}/4$	2 MHz	0	1	0
$f_{\text{INPUT}}/8$	1 MHz	0	1	1
$f_{\text{INPUT}}/16$	500 kHz	1	0	0
$f_{\text{INPUT}}/32$	250 kHz	1	0	1
$f_{\text{INPUT}}/64$	125 kHz	1	1	0
$f_{\text{INPUT}}/128$	62.5 kHz	1	1	1

Counter access register (ARTCAR)ARTCAR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

CA[7:0]

R/W

Table 33. ARTCAR register description

Bit	Name	Function
7:0	CA[7:0]	<i>Counter access data</i> These bits can be set and cleared either by hardware or by software. The ARTCAR register is used to read or write the auto-reload counter 'on the fly' (while it is counting).

Auto-reload register (ARTARR)ARTARR Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
---	---	---	---	---	---	---	---

AR[7:0]

R/W

Table 34. ARTAAR register description

Bit	Name	Function
7:0	AR[7:0]	<i>Counter auto-reload data</i> These bits are set and cleared by software. They are used to hold the auto-reload value which is automatically loaded in the counter when an overflow occurs. At the same time, the PWM output levels are changed according to the corresponding OPx bit in the PWMCR register.

This register has two PWM management functions:

- Adjusting the PWM frequency
- Setting the PWM duty cycle resolution

Table 35. PWM frequency versus resolution

ARTARR value	Resolution	f_{PWM}	
		Min	Max
0	8-bit	~0.244 kHz	31.25 kHz
[0..127]	> 7-bit	~0.244 kHz	62.5 kHz
[128..191]	> 6-bit	~0.488 kHz	125 kHz
[192..223]	> 5-bit	~0.977 kHz	250 kHz
[224..239]	> 4-bit	~1.953 kHz	500 kHz

PWM control register (PWMCR)

PWMCR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
OE[3:0]				OP[3:0]			
R/W				R/W			

Table 36. PWMCR register description

Bit	Name	Function
7:4	OE[3:0]	<i>PWM output enable</i> These bits are set and cleared by software. They enable or disable the PWM output channels independently acting on the corresponding I/O pin. 0: PWM output disabled 1: PWM output enabled
3:0	OP[3:0]	<i>PWM output polarity</i> These bits are set and cleared by software. They independently select the polarity of the four PWM output signals (see Table 37).

Table 37. PWM output signal polarity selection

PWMx output level		OPx ⁽¹⁾
Counter ≤ OCRx	Counter > OCRx	
1	0	0
0	1	1

1. When an OPx bit is modified, the PWMx output signal polarity is immediately reversed.

Duty cycle registers (PWMDCRx)

PWMDCRx				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
DC[7:0]							
R/W							

Table 38. PWMDCRx register description

Bit	Name	Function
7:0	DC[7:0]	<i>Duty cycle data</i> These bits are set and cleared by software.

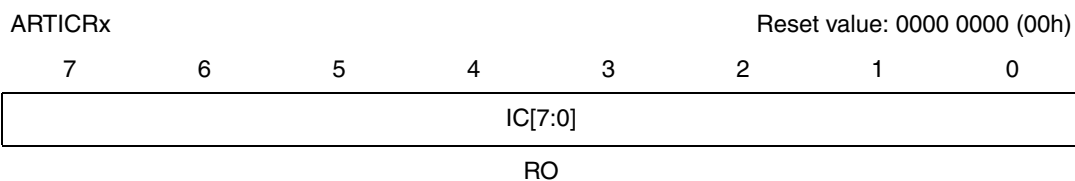
A PWMDCRx register is associated with the OCRx register of each PWM channel to determine the second edge location of the PWM signal (the first edge location is common to all channels and given by the ARTARR register). These PWMDCR registers allow the duty cycle to be set independently for each PWM channel.

Input capture control/status register (ARTICCSR)

ARTICCSR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
Reserved		CS[2:1]		CIE[2:1]		CF[2:1]	
-		R/W		R/W		R/W	

Table 39. ARTICCSR register description

Bit	Name	Function
7:6	-	Reserved, always read as 0.
5:4	CS[2:1]	<i>Capture sensitivity</i> These bits are set and cleared by software. They determine the trigger event polarity on the corresponding input capture channel. 0: Falling edge triggers capture on channel x 1: Rising edge triggers capture on channel x
3:2	CIE[2:1]	<i>Capture interrupt enable</i> These bits are set and cleared by software. They enable or disable the Input capture channel interrupts independently. 0: Input capture channel x interrupt disabled 1: Input capture channel x interrupt enabled
1:0	CF[2:1]	<i>Capture flag</i> These bits are set by hardware and cleared by software reading the corresponding ARTICRx register. Each CFx bit indicates that an input capture x has occurred. 0: No input capture on channel x 1: An input capture has occurred on channel x.

Input capture registers (ARTICRx)**Table 40. ARTICRx register description**

Bit	Name	Function
7:0	IC[7:0]	<i>Input capture data</i> These read only bits are set and cleared by hardware. An ARTICRx register contains the 8-bit auto-reload counter value transferred by the input capture channel x event.

Table 41. PWM auto-reload timer register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0073h	PWMDCR3 Reset value	DC7 0	DC6 0	DC5 0	DC4 0	DC3 0	DC2 0	DC1 0	DC0 0
0074h	PWMDCR2 Reset value	DC7 0	DC6 0	DC5 0	DC4 0	DC3 0	DC2 0	DC1 0	DC0 0
0075h	PWMDCR1 Reset value	DC7 0	DC6 0	DC5 0	DC4 0	DC3 0	DC2 0	DC1 0	DC0 0
0076h	PWMDCR0 Reset value	DC7 0	DC6 0	DC5 0	DC4 0	DC3 0	DC2 0	DC1 0	DC0 0
0077h	PWMCR Reset value	OE3 0	OE2 0	OE1 0	OE0 0	OP3 0	OP2 0	OP1 0	OP0 0
0078h	ARTCSR Reset value	EXCL 0	CC2 0	CC1 0	CC0 0	TCE 0	FCRL 0	RIE 0	OVF 0
0079h	ARTCAR Reset value	CA7 0	CA6 0	CA5 0	CA4 0	CA3 0	CA2 0	CA1 0	CA0 0
007Ah	ARTARR Reset value	AR7 0	AR6 0	AR5 0	AR4 0	AR3 0	AR2 0	AR1 0	AR0 0
007Bh	ARTICCSR Reset value	0	0	CS2 0	CS1 0	CIE2 0	CIE1 0	CF2 0	CF1 0
007Ch	ARTICR1 Reset value	IC7 0	IC6 0	IC5 0	IC4 0	IC3 0	IC2 0	IC1 0	IC0 0
007Dh	ARTICR2 Reset value	IC7 0	IC6 0	IC5 0	IC4 0	IC3 0	IC2 0	IC1 0	IC0 0

10.4 16-bit timer

10.4.1 Introduction

The timer consists of a 16-bit free-running counter driven by a programmable prescaler.

It may be used for a variety of purposes, including pulse length measurement of up to two input signals (*input capture*) or generation of up to two output waveforms (*output compare* and *PWM*).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the CPU clock prescaler.

Some ST7 devices have two on-chip 16-bit timers. They are completely independent, and do not share any resources. They are synchronized after a MCU reset as long as the timer clock frequencies are not modified.

This description covers one or two 16-bit timers. In ST7 devices with two timers, register names are prefixed with TA (Timer A) or TB (Timer B).

10.4.2 Main features

- Programmable prescaler: f_{CPU} divided by 2, 4 or 8
- Overflow status flag and maskable interrupt
- External clock input (must be at least four times slower than the CPU clock speed) with the choice of active edge
- 1 or 2 output compare functions each with:
 - 2 dedicated 16-bit registers
 - 2 dedicated programmable signals
 - 2 dedicated status flags
 - 1 dedicated maskable interrupt
- 1 or 2 input capture functions each with:
 - 2 dedicated 16-bit registers
 - 2 dedicated active edge selection signals
 - 2 dedicated status flags
 - 1 dedicated maskable interrupt
- Pulse width modulation mode (PWM)
- One pulse mode
- Reduced power mode
- 5 alternate functions on I/O ports (ICAP1, ICAP2, OCMP1, OCMP2, EXTCLK)^(a)

The block diagram is shown in [Figure 36: Timer block diagram on page 85](#).

a. Some timer pins may not be available (not bonded) in some ST7 devices. Refer to [Section 2: Package pinout and pin description on page 15](#). When reading an input signal on a non-bonded pin, the value is always '1'.

10.4.3 Functional description

Counter

The main block of the programmable timer is a 16-bit free running upcounter and its associated 16-bit registers. The 16-bit registers are made up of two 8-bit registers called high and low.

Counter register (CR)

- Counter high register (CHR) is the most significant byte (MS byte)
- Counter low register (CLR) is the least significant byte (LS byte)

Alternate counter register (ACR)

- Alternate counter high register (ACHR) is the most significant byte (MS byte)
- Alternate counter low register (ACLR) is the least significant byte (LS byte)

These two read-only 16-bit registers contain the same value but with the difference that reading the ACLR register does not clear the TOF bit (timer overflow flag), located in the status register, (SR), (see [16-bit read sequence \(from either the counter register or alternate counter register\) on page 86](#)).

Writing in the CLR register or ACLR register resets the free running counter to the FFFCh value.

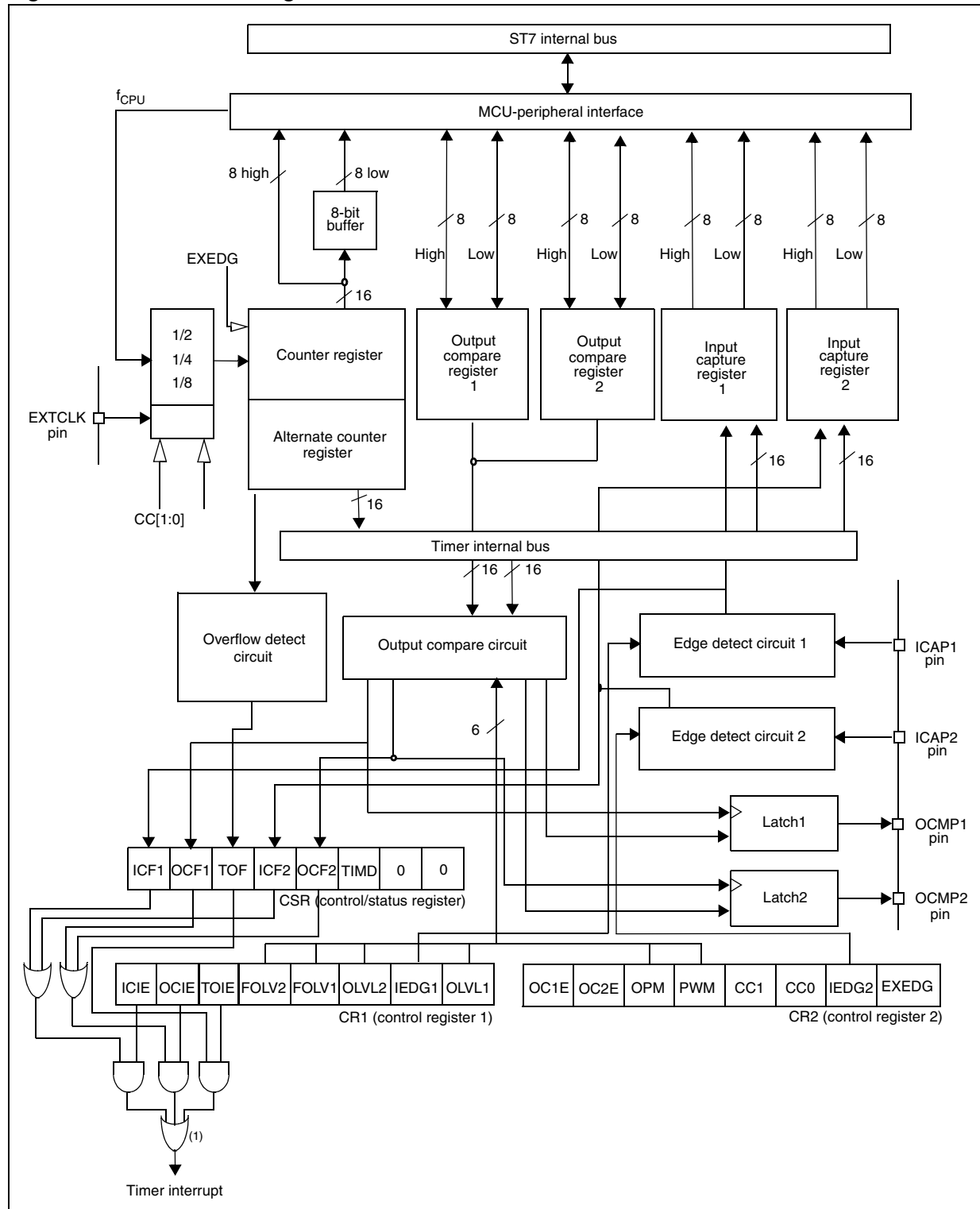
Both counters have a reset value of FFFCh (this is the only value which is reloaded in the 16-bit timer). The reset value of both counters is also FFFCh in one pulse mode and PWM mode.

The timer clock depends on the clock control bits (bits 3 and 2) of the CR2 register, as illustrated in [Table 46: CR2 register description on page 100](#). The value in the counter register repeats every 131072, 262144 or 524288 CPU clock cycles depending on the CC[1:0] bits. The timer frequency can be $f_{CPU}/2$, $f_{CPU}/4$, $f_{CPU}/8$ or an external frequency.

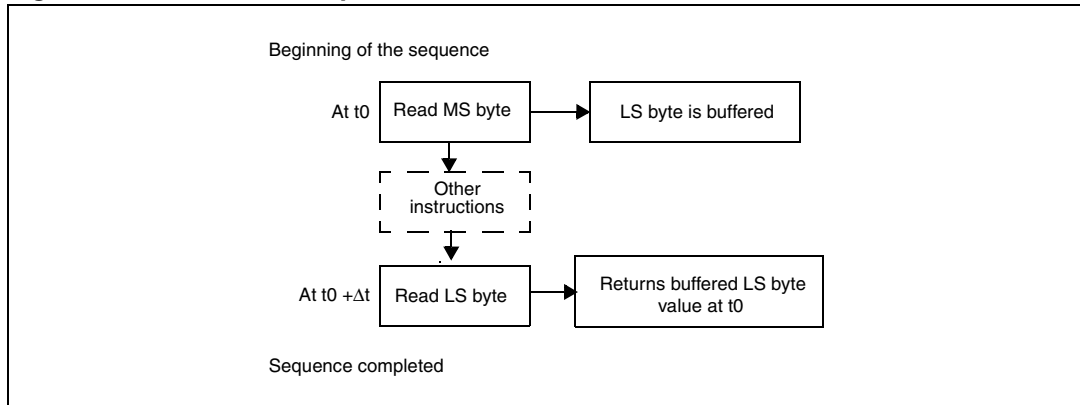
Caution: In Flash devices, timer A functionality has the following restrictions:

- TAOC2HR and TAOC2LR registers are write only
- Input capture 2 is not implemented
- The corresponding interrupts cannot be used (ICF2, OCF2 forced by hardware to zero)

Figure 36. Timer block diagram



1. If IC, OC and TO interrupt requests have separate vectors then the last OR is not present (see [Table 14: Interrupt mapping on page 47](#)).

16-bit read sequence (from either the counter register or alternate counter register)**Figure 37. 16-bit read sequence**

The user must read the MS byte first, then the LS byte value is buffered automatically.

This buffered value remains unchanged until the 16-bit read sequence is completed, even if the user reads the MS byte several times.

After a complete reading sequence, if only the CLR register or ACLR register are read, they return the LS byte of the count value at the time of the read.

Whatever the timer mode used (input capture, output compare, one pulse mode or PWM mode) an overflow occurs when the counter rolls over from FFFFh to 0000h then:

- The TOF bit of the SR register is set
- A timer interrupt is generated if the TOIE bit of the CR1 register is set and the I bit of the CC register is cleared

If one of these conditions is false, the interrupt remains pending to be issued as soon as they are both true.

Clearing the overflow interrupt request is done in two steps:

1. Reading the SR register while the TOF bit is set
2. An access (read or write) to the CLR register

Note: *The TOF bit is not cleared by accesses to ACLR register. The advantage of accessing the ACLR register rather than the CLR register is that it allows simultaneous use of the overflow function and reading the free running counter at random times (for example, to measure elapsed time) without the risk of clearing the TOF bit erroneously.*

The timer is not affected by wait mode.

In halt mode, the counter stops counting until the mode is exited. Counting then resumes from the previous count (MCU awakened by an interrupt) or from the reset count (MCU awakened by a reset).

External clock

The external clock (where available) is selected if CC0 = 1 and CC1 = 1 in the CR2 register.

The status of the EXEDG bit in the CR2 register determines the type of level transition on the external clock pin EXTCLK that triggers the free running counter.

The counter is synchronized with the falling edge of the internal CPU clock.

A minimum of four falling edges of the CPU clock must occur between two consecutive active edges of the external clock; thus the external clock frequency must be less than a quarter of the CPU clock frequency.

Figure 38. Counter timing diagram, internal clock divided by 2

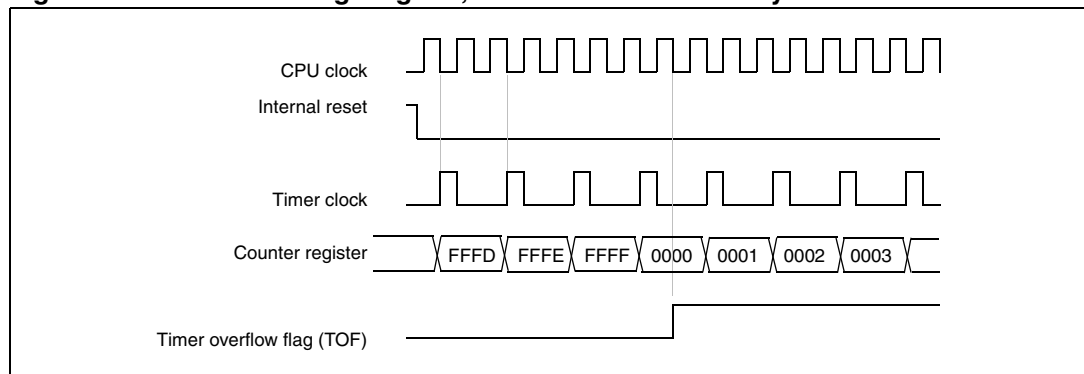


Figure 39. Counter timing diagram, internal clock divided by 4

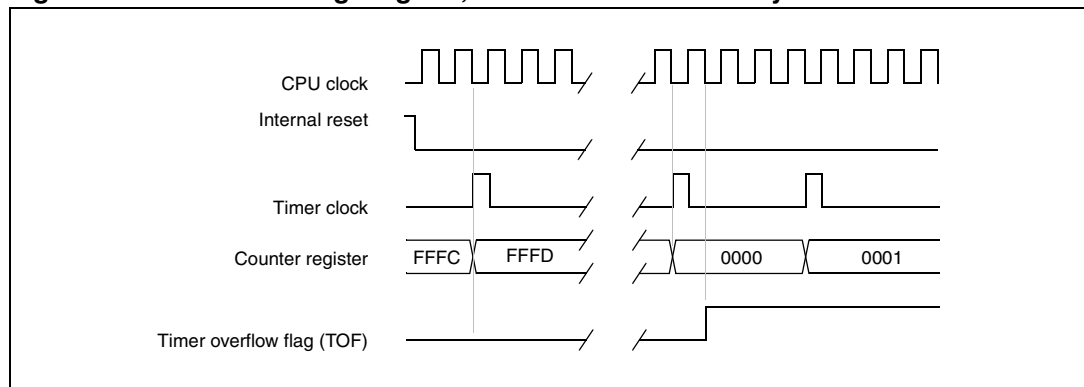
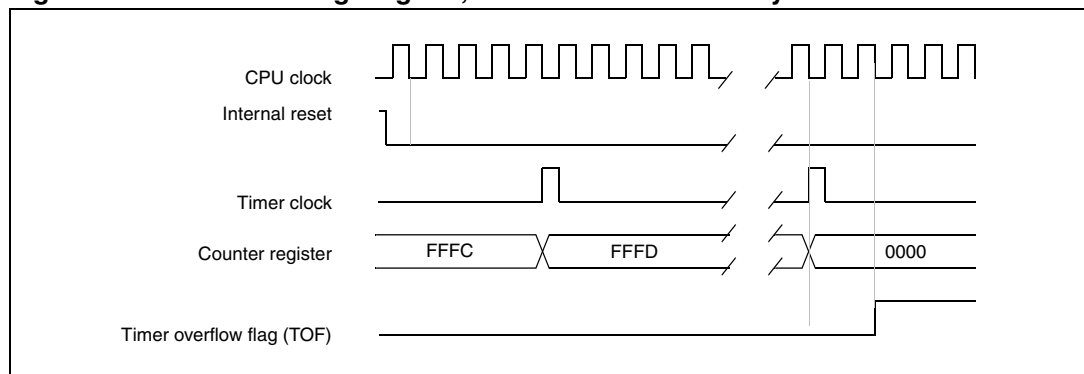


Figure 40. Counter timing diagram, internal clock divided by 8



Note: The MCU is in reset state when the internal reset signal is high, when it is low the MCU is running.

Input capture

In this section, the index, i , may be 1 or 2 because there are 2 input capture functions in the 16-bit timer.

The two 16-bit input capture registers (IC1R and IC2R) are used to latch the value of the free running counter after a transition is detected on the ICAP i pin (see below).

	MSB	LSB
ICiR	ICiHR	ICiLR

ICiR register is a read-only register.

The active transition is software programmable through the IEDG i bit of control registers (CRi).

Timing resolution is one count of the free running counter: ($f_{CPU}/CC[1:0]$).

Procedure

To use the input capture function select the following in the CR2 register:

- The timer clock (CC[1:0]) (see [Table 46: CR2 register description on page 100](#))
- The edge of the active transition on the ICAP2 pin with the IEDG2 bit (the ICAP2 pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

Select the following in the CR1 register:

- Set the ICIE bit to generate an interrupt after an input capture coming from either the ICAP1 pin or the ICAP2 pin.
- Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input or input with pull-up without interrupt if this configuration is available).

When an input capture occurs:

- ICF i bit is set
- The ICiR register contains the value of the free running counter on the active transition on the ICAP i pin (see [Figure 42: Input capture timing diagram\(1\) on page 89](#)).
- A timer interrupt is generated if the ICIE bit is set and the I bit is cleared in the CC register. Otherwise, the interrupt remains pending until both conditions become true.

Clearing the input capture interrupt request (i.e. clearing the ICF i bit) is done in two steps:

1. By reading the SR register while the ICF i bit is set
2. By accessing (reading or writing) the ICiLR register

- Note:
- 1 After reading the ICiHR register, transfer of input capture data is inhibited and ICFi is never set until the ICiLR register is also read.
 - 2 The ICiR register contains the free running counter value which corresponds to the most recent input capture.
 - 3 The two input capture functions can be used together even if the timer also uses the 2 output compare functions.
 - 4 In one pulse mode and PWM mode only input capture 2 can be used.
 - 5 The alternate inputs (ICAP1 and ICAP2) are always directly connected to the timer. So any transitions on these pins activates the input capture function.
Moreover if one of the ICAPi pins is configured as an input and the second one as an output, an interrupt can be generated if the user toggles the output pin and if the ICIE bit is set. This can be avoided if the input capture function i is disabled by reading the ICiHR (see note 1).
 - 6 The TOF bit can be used with interrupt generation in order to measure events that go beyond the timer range (FFFFh).

Figure 41. Input capture block diagram

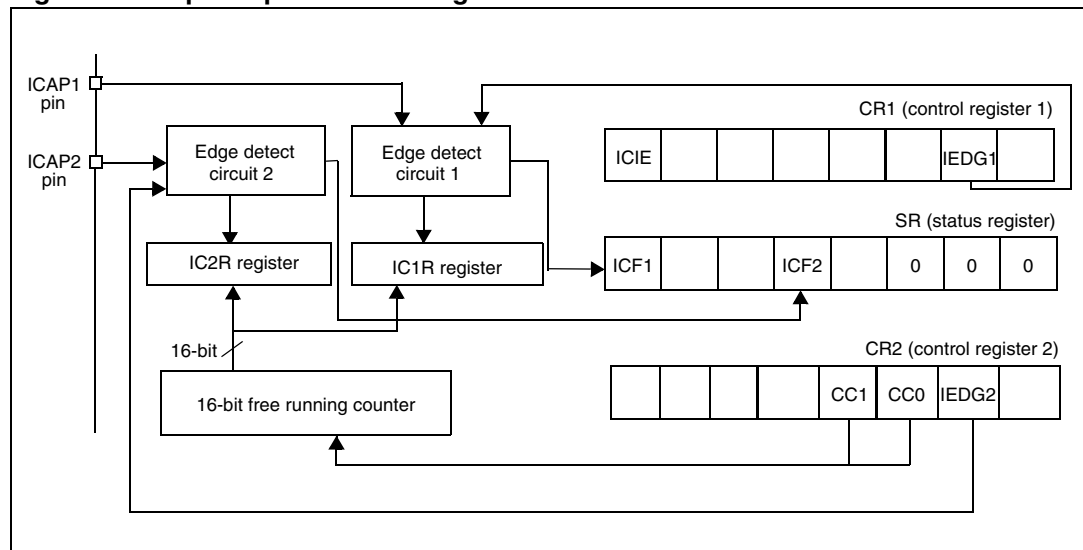
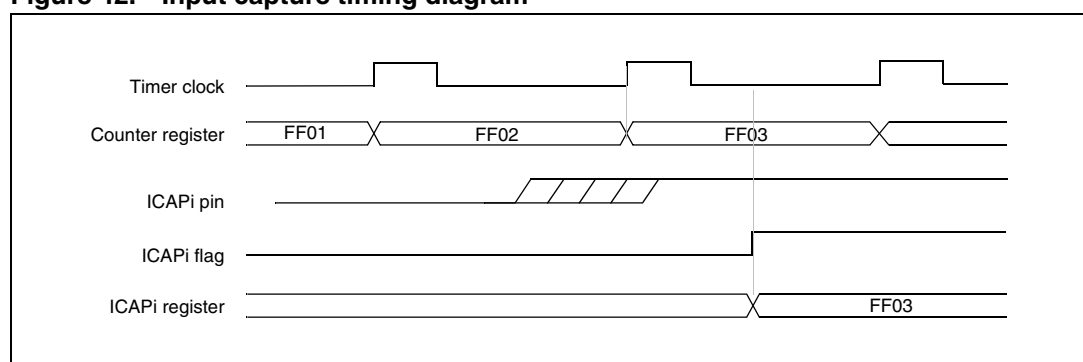


Figure 42. Input capture timing diagram⁽¹⁾



1. The rising edge is the active edge.

Output compare

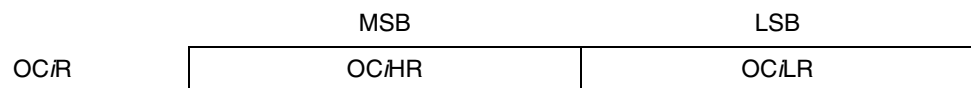
In this section, the index, i , may be 1 or 2 because there are 2 output compare functions in the 16-bit timer.

This function can be used to control an output waveform or indicate when a period of time has elapsed.

When a match is found between the output compare register and the free running counter, the output compare function:

- Assigns pins with a programmable value if the OC/E bit is set
- Sets a flag in the status register
- Generates an interrupt if enabled

Two 16-bit registers, output compare register 1 (OC1R) and output compare register 2 (OC2R) contain the value to be compared to the counter register each timer clock cycle (see below).



These registers are readable and writable and are not affected by the timer hardware. A reset event changes the OC/R value to 8000h.

Timing resolution is one count of the free running counter: $(f_{\text{CPU}}/CC[1:0])$.

Procedure

To use the output compare function, select the following in the CR2 register:

- Set the OC/E bit if an output is needed then the OCMP i pin is dedicated to the output compare i signal.
- Select the timer clock (CC[1:0]) (see [Table 46: CR2 register description on page 100](#))

Select the following in the CR1 register:

- Select the OLVL i bit to be applied to the OCMP i pins after the match occurs
- Set the OCIE bit to generate an interrupt if it is needed

When a match is found between OCR i register and CR register:

- OCF i bit is set
- The OCMP i pin takes the OLVL i bit value (OCMP i pin latch is forced low during reset)
- A timer interrupt is generated if the OCIE bit is set in the CR1 register and the I bit is cleared in the CC register (CC).

The OCiR register value required for a specific timing application can be calculated using the following formula:

$$\Delta \text{ OCiR} = \frac{\Delta t * f_{\text{CPU}}}{\text{PRESC}}$$

Where:

Δt = Output compare period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits, see [Table 46: CR2 register description on page 100](#))

If the timer clock is an external clock, the formula is:

$$\Delta \text{ OCiR} = \Delta t * f_{\text{EXT}}$$

Where:

Δt = Output compare period (in seconds)

f_{EXT} = External timer clock frequency (in hertz)

Clearing the output compare interrupt request (i.e. clearing the OCFi bit) is done by:

1. Reading the SR register while the OCFi bit is set
2. Accessing (reading or writing) the OCiLR register

The following procedure is recommended to prevent the OCFi bit from being set between the time it is read and the write to the OCiR register:

- Write to the OCiHR register (further compares are inhibited)
- Read the SR register (first step of the clearance of the OCFi bit, which may be already set)
- Write to the OCiLR register (enables the output compare function and clears the OCFi bit)

- Note:**
- 1 After a processor write cycle to the OCiHR register, the output compare function is inhibited until the OCiLR register is also written.
 - 2 If the OCiE bit is not set, the OCMPi pin is a general I/O port and the OLVLi bit does not appear when a match is found but an interrupt could be generated if the OCiE bit is set.
 - 3 In both internal and external clock modes, OCFi and OCMPi are set while the counter value equals the OCiR register value (see [Figure 44: Output compare timing diagram, fTIMER = fCPU/2 on page 92](#) for an example with $f_{\text{CPU}}/2$ and [Figure 45: Output compare timing diagram, fTIMER = fCPU/4 on page 92](#) for an example with $f_{\text{CPU}}/4$). This behavior is the same in OPM or PWM mode.
 - 4 The output compare functions can be used both for generating external events on the OCMPi pins even if the input capture mode is also used.
 - 5 The value in the 16-bit OCiR register and the OLVi bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed timeout.

Forced compare output capability

When the FOLV i bit is set by software, the OLV i bit is copied to the OCMP i pin. The OLV i bit has to be toggled in order to toggle the OCMP i pin when it is enabled (OC E bit = 1). The OCF i bit is then not set by hardware, and thus no interrupt request is generated.

The FOLV i bits have no effect in both one pulse mode and PWM mode.

Figure 43. Output compare block diagram

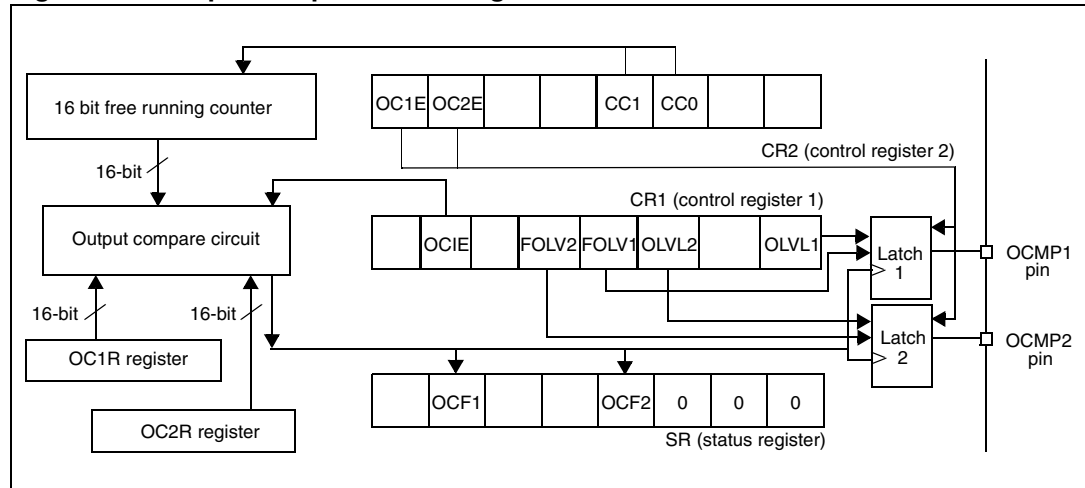


Figure 44. Output compare timing diagram, $f_{\text{TIMER}} = f_{\text{CPU}}/2$

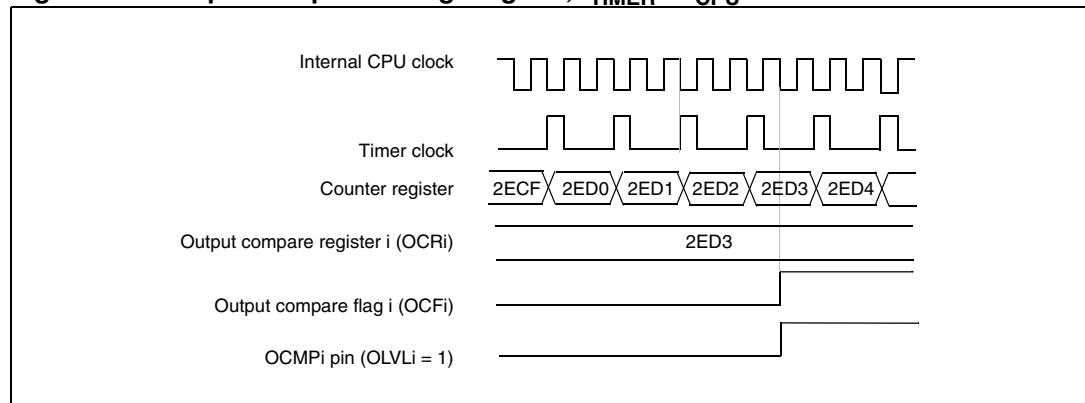
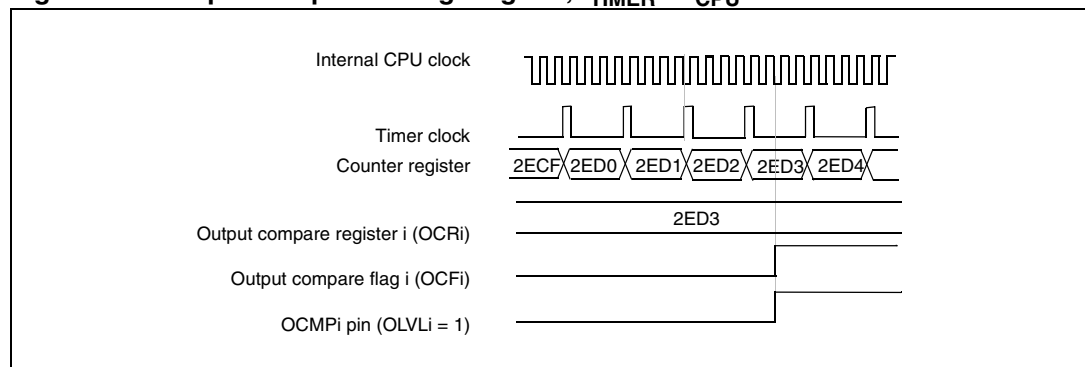


Figure 45. Output compare timing diagram, $f_{\text{TIMER}} = f_{\text{CPU}}/4$



One pulse mode

One pulse mode enables the generation of a pulse when an external event occurs. This mode is selected via the OPM bit in the CR2 register.

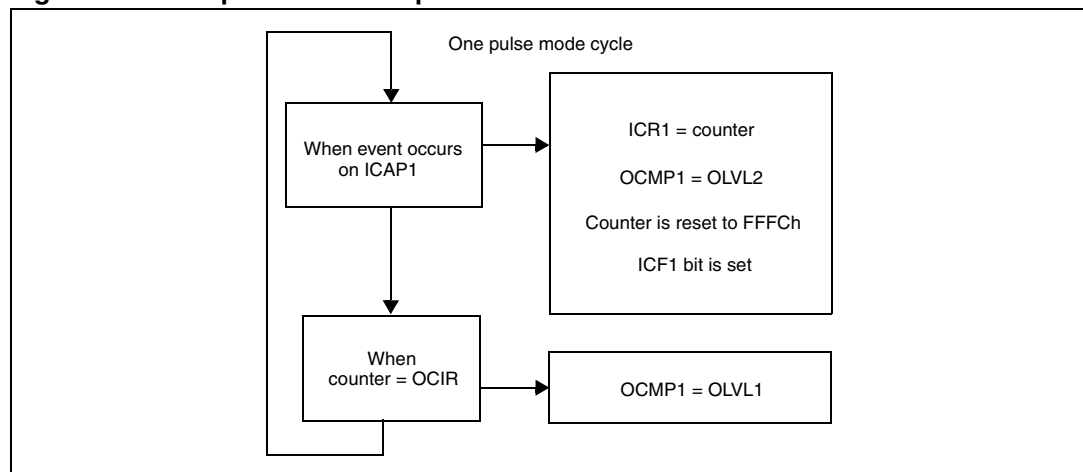
The one pulse mode uses the input capture1 function and the output compare1 function.

Procedure

To use one pulse mode:

1. Load the OC1R register with the value corresponding to the length of the pulse using the appropriate formula below according to the timer clock source used
2. Select the following in the CR1 register:
 - Using the OVL1 bit, select the level to be applied to the OCMP1 pin after the pulse
 - Using the OVL2 bit, select the level to be applied to the OCMP1 pin during the pulse
 - Select the edge of the active transition on the ICAP1 pin with the IEDG1 bit (the ICAP1 pin must be configured as floating input)
3. Select the following in the CR2 register:
 - Set the OC1E bit (the OCMP1 pin is then dedicated to the output compare 1 function)
 - Set the OPM bit
 - Select the timer clock CC[1:0] (see [Table 46: CR2 register description on page 100](#))

Figure 46. One pulse mode sequence



Then, on a valid event on the ICAP1 pin, the counter is initialized to FFFCh and OVL2 bit is loaded on the OCMP1 pin, the ICF1 bit is set and the value FFFDh is loaded in the IC1R register.

Because the ICF1 bit is set when an active edge occurs, an interrupt can be generated if the ICIE bit is set.

Clearing the input capture interrupt request (i.e. clearing the ICF*i* bit) is done in two steps:

1. Reading the SR register while the ICF*i* bit is set
2. Accessing (reading or writing) the IC1LR register

The OC1R register value required for a specific timing application can be calculated using the following formula:

$$\text{OC1R value} = \frac{t \cdot f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

t = Pulse period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on the CC[1:0] bits, see [Table 46: CR2 register description on page 100](#))

If the timer clock is an external clock the formula is:

$$\text{OC1R} = t \cdot f_{\text{EXT}} - 5$$

Where:

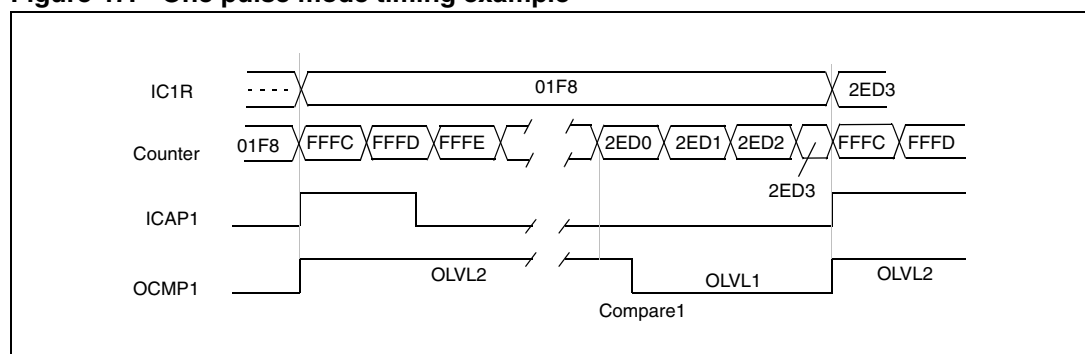
t = Pulse period (in seconds)

f_{EXT} = External timer clock frequency (in hertz)

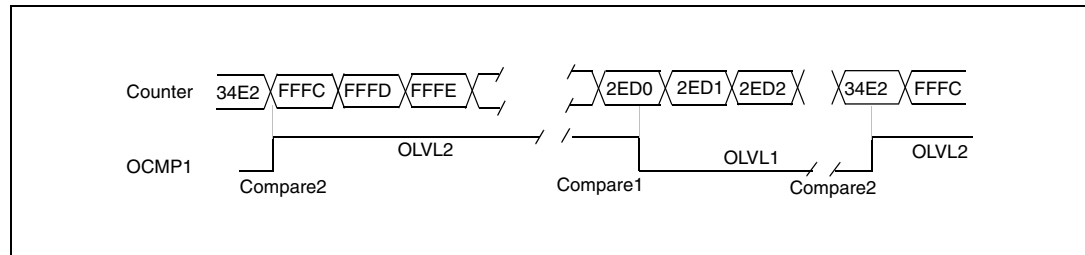
When the value of the counter is equal to the value of the contents of the OC1R register, the OLVL1 bit is output on the OCMP1 pin, (see [Figure 47](#)).

- Note:**
- 1 The OCF1 bit cannot be set by hardware in one pulse mode but the OCF2 bit can generate an output compare interrupt.
 - 2 When the pulse width modulation (PWM) and one pulse mode (OPM) bits are both set, the PWM mode is the only active one.
 - 3 If OLVL1 = OLVL2 a continuous signal is seen on the OCMP1 pin.
 - 4 The ICAP1 pin cannot be used to perform input capture. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each time a valid edge occurs on the ICAP1 pin and ICF1 can also generate interrupt if ICIE is set.
 - 5 When one pulse mode is used OC1R is dedicated to this mode. Nevertheless OC2R and OCF2 can be used to indicate a period of time has elapsed but cannot generate an output waveform because the level OLVL2 is dedicated to the one pulse mode.

Figure 47. One pulse mode timing example⁽¹⁾



1. IEDG1 = 1, OC1R = 2ED0h, OLVL1 = 0, OLVL2 = 1.

Figure 48. Pulse width modulation mode timing example with 2 output compare functions⁽¹⁾

1. OC1R = 2ED0h, OC2R = 34E2, OLVL1 = 0, OLVL2 = 1

Note: On timers with only one output compare register, a fixed frequency PWM signal can be generated using the output compare and the counter overflow to define the pulse length

Pulse width modulation mode

Pulse width modulation (PWM) mode enables the generation of a signal with a frequency and pulse length determined by the value of the OC1R and OC2R registers.

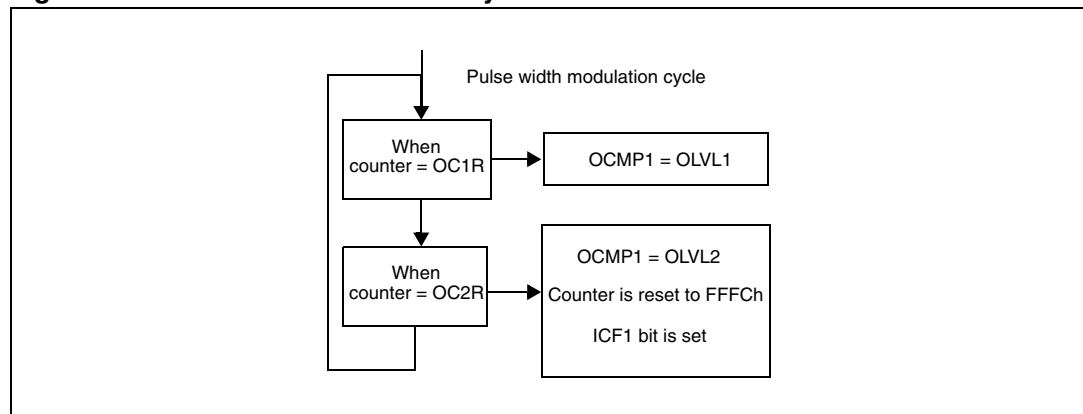
Pulse width modulation mode uses the complete output compare 1 function plus the OC2R register, and so this functionality cannot be used when PWM mode is activated.

In PWM mode, double buffering is implemented on the output compare registers. Any new values written in the OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2) to avoid spikes on the PWM output pin (OCMP1).

Procedure

To use pulse width modulation mode:

1. Load the OC2R register with the value corresponding to the period of the signal using the appropriate formula below according to the timer clock source used
2. Load the OC1R register with the value corresponding to the period of the pulse if (OLVL1 = 0 and OLVL2 = 1) using the appropriate formula below according to the timer clock source used
3. Select the following in the CR1 register:
 - Using the OLVL1 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC1R register
 - Using the OLVL2 bit, select the level to be applied to the OCMP1 pin after a successful comparison with the OC2R register
4. Select the following in the CR2 register:
 - Set OC1E bit (the OCMP1 pin is then dedicated to the output compare 1 function)
 - Set the PWM bit
 - Select the timer clock (CC[1:0]) (see [Table 46: CR2 register description on page 100](#))

Figure 49. Pulse width modulation cycle

If OLVL1 = 1 and OLVL2 = 0 the length of the positive pulse is the difference between the OC2R and OC1R registers.

If OLVL1 = OLVL2 a continuous signal is seen on the OCMP1 pin.

The OC/R register value required for a specific timing application can be calculated using the following formula:

$$\text{OC/R value} = \frac{t \cdot f_{\text{CPU}}}{\text{PRESC}} - 5$$

Where:

t = Signal or pulse period (in seconds)

f_{CPU} = CPU clock frequency (in hertz)

PRESC = Timer prescaler factor (2, 4 or 8 depending on CC[1:0] bits, see [Table 46: CR2 register description on page 100](#))

If the timer clock is an external clock the formula is:

$$\text{OC/R} = t \cdot f_{\text{EXT}} - 5$$

Where:

t = Signal or pulse period (in seconds)

f_{EXT} = External timer clock frequency (in hertz)

The output compare 2 event causes the counter to be initialized to FFFCh (see [Figure 48: Pulse width modulation mode timing example with 2 output compare functions\(1\) on page 95](#)).

- Note:
- 1 After a write instruction to the OCiHR register, the output compare function is inhibited until the OCiLR register is also written.
 - 2 The OCF1 and OCF2 bits cannot be set by hardware in PWM mode, therefore the output compare interrupt is inhibited.
 - 3 The ICF1 bit is set by hardware when the counter reaches the OC2R value and can produce a timer interrupt if the ICIE bit is set and the I bit is cleared.
 - 4 In PWM mode the ICAP1 pin cannot be used to perform input capture because it is disconnected from the timer. The ICAP2 pin can be used to perform input capture (ICF2 can be set and IC2R can be loaded) but the user must take care that the counter is reset each period and ICF1 can also generate an interrupt if ICIE is set.
 - 5 When the pulse width modulation (PWM) and one pulse mode (OPM) bits are both set, the PWM mode is the only active one.

10.4.4 Low power modes

Table 42. Effect of low power modes on 16-bit timer

Mode	Description
Wait	No effect on 16-bit timer. Timer interrupts cause the device to exit from wait mode.
Halt	16-bit timer registers are frozen. In halt mode, the counter stops counting until halt mode is exited. Counting resumes from the previous count when the MCU is woken up by an interrupt with 'exit from halt mode' capability or from the counter reset value when the MCU is woken up by a reset. If an input capture event occurs on the ICAP <i>i</i> pin, the input capture detection circuitry is armed. Consequently, when the MCU is woken up by an interrupt with 'exit from halt mode' capability, the ICF <i>i</i> bit is set, and the counter value present when exiting from halt mode is captured into the IC <i>i</i> R register.

10.4.5 Interrupts

Table 43. 16-bit timer interrupt control/wake-up capability⁽¹⁾

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
Input capture 1 event/counter reset in PWM mode	ICF1	ICIE	Yes	No
Input capture 2 event	ICF2			
Output compare 1 event (not available in PWM mode)	OCF1	OCIE		
Output compare 2 event (not available in PWM mode)	OCF2			
Timer overflow event	TOF	TOIE		

1. The 16-bit timer interrupt events are connected to the same interrupt vector (see [Section 7: Interrupts on page 36](#)). These events generate an interrupt if the corresponding enable control bit is set and the interrupt mask in the CC register is reset (RIM instruction).

10.4.6 Summary of timer modes

Table 44. Summary of timer modes

Modes	Timer resources			
	Input capture 1	Input capture 2	Output compare 1	Output compare 2
Input capture ⁽¹⁾ and/or ⁽²⁾	Yes	Yes	Yes	Yes
Output compare ⁽¹⁾ and/or ⁽²⁾				
One pulse mode	No	Not recommended ⁽¹⁾	No	Partially ⁽²⁾
PWM mode		Not recommended ⁽³⁾		No

1. See note 4 in [One pulse mode on page 93](#)

2. See note 5 in [One pulse mode on page 93](#)

3. See note 4 in [Pulse width modulation mode on page 95](#)

10.4.7 16-bit timer registers

Each timer is associated with three control and status registers, and with six pairs of data registers (16-bit values) relating to the two input captures, the two output compares, the counter and the alternate counter.

Control register 1 (CR1)

CR1 Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
ICIE	OCIE	TOIE	FOLV2	FOLV1	OLVL2	IEDG1	OLVL1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 45. CR1 register description

Bit	Bit name	Function
7	ICIE	Input capture interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is generated whenever the ICF1 or ICF2 bit of the SR register is set
6	OCIE	Output compare interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is generated whenever the OCF1 or OCF2 bit of the SR register is set
5	TOIE	Timer overflow interrupt enable 0: Interrupt is inhibited 1: A timer interrupt is enabled whenever the TOF bit of the SR register is set

Table 45. CR1 register description (continued)

Bit	Bit name	Function
4	FOLV2	Forced output compare 2 This bit is set and cleared by software. 0: No effect on the OCMP2 pin 1: Forces the OLVL2 bit to be copied to the OCMP2 pin, if the OC2E bit is set and even if there is no successful comparison
3	FOLV1	Forced output compare 1 This bit is set and cleared by software. 0: No effect on the OCMP1 pin 1: Forces OLVL1 to be copied to the OCMP1 pin, if the OC1E bit is set and even if there is no successful comparison
2	OLVL2	Output level 2 This bit is copied to the OCMP2 pin whenever a successful comparison occurs with the OC2R register and OCxE is set in the CR2 register. This value is copied to the OCMP1 pin in one pulse mode and pulse width modulation mode.
1	IEDG1	Input edge 1 This bit determines which type of level transition on the ICAP1 pin triggers the capture. 0: A falling edge triggers the capture 1: A rising edge triggers the capture
0	OLVL1	Output level 1 The OLVL1 bit is copied to the OCMP1 pin whenever a successful comparison occurs with the OC1R register and the OC1E bit is set in the CR2 register.

Control register 2 (CR2)

CR2

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
OC1E	OC2E	OPM	PWM	CC[1:0]		IEDG2	EXEDG
R/W	R/W	R/W	R/W	R/W		R/W	R/W

Table 46. CR2 register description

Bit	Bit name	Function
7	OC1E	Output compare 1 pin enable This bit is used only to output the signal from the timer on the OCMP1 pin (OLV1 in output compare mode, both OLV1 and OLV2 in PWM and one-pulse mode). Whatever the value of the OC1E bit, the output compare 1 function of the timer remains active. 0: OCMP1 pin alternate function disabled (I/O pin free for general-purpose I/O) 1: OCMP1 pin alternate function enabled
6	OC2E	Output compare 2 pin enable This bit is used only to output the signal from the timer on the OCMP2 pin (OLV2 in output compare mode). Whatever the value of the OC2E bit, the output compare 2 function of the timer remains active. 0: OCMP2 pin alternate function disabled (I/O pin free for general-purpose I/O) 1: OCMP2 pin alternate function enabled
5	OPM	One pulse mode 0: One pulse mode is not active 1: One pulse mode is active, the ICAP1 pin can be used to trigger one pulse on the OCMP1 pin; the active transition is given by the IEDG1 bit. The length of the generated pulse depends on the contents of the OC1R register.
4	PWM	Pulse width modulation 0: PWM mode is not active 1: PWM mode is active, the OCMP1 pin outputs a programmable cyclic signal; the length of the pulse depends on the value of OC1R register; the period depends on the value of OC2R register.
3:2	CC[1:0]	Clock control The timer clock mode depends on the following bits: 00: timer clock = $f_{CPU}/4$ 01: timer clock = $f_{CPU}/2$ 10: timer clock = $f_{CPU}/8$ 11: timer clock = external clock (where available) <i>Note: If the external clock pin is not available, programming the external clock configuration stops the counter.</i>

Table 46. CR2 register description (continued)

Bit	Bit name	Function
1	IEDG2	Input edge 2 This bit determines which type of level transition on the ICAP2 pin triggers the capture. 0: A falling edge triggers the capture 1: A rising edge triggers the capture
0	EXEDG	External clock edge This bit determines which type of level transition on the external clock pin EXTCLK triggers the counter register. 0: A falling edge triggers the counter register 1: A rising edge triggers the counter register

Control/status register (CSR)

CSR

Reset value: xxxx x0xx (xxh)

7	6	5	4	3	2	1	0
ICF1	OCF1	TOF	ICF2	OCF2	TIMD	Reserved	
RO	RO	RO	RO	RO	R/W	-	

Table 47. CSR register description

Bit	Bit name	Function
7	ICF1	Input capture flag 1 0: No input capture (reset value) 1: An input capture has occurred on the ICAP1 pin or the counter has reached the OC2R value in PWM mode. To clear this bit, first read the SR register, then read or write the low byte of the IC1R (IC1LR) register.
6	OCF1	Output compare flag 1 0: No match (reset value) 1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.
5	TOF	Timer overflow flag 0: No timer overflow (reset value) 1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register. <i>Note: Reading or writing the ACLR register does not clear TOF</i>
4	ICF2	Input capture flag 2 0: No input capture (reset value) 1: An input capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.

Table 47. CSR register description (continued)

Bit	Bit name	Function
3	OCF2	Output compare flag 2 0: No match (reset value) 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disables the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled. 0: Timer enabled 1: Timer prescaler, counter and outputs disabled
1:0	-	Reserved, must be kept cleared

Input capture 1 high register (IC1HR)

This is an 8-bit read only register that contains the high part of the counter value (transferred by the input capture 1 event).

IC1HR				Reset value: undefined			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input capture 1 low register (IC1LR)

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 1 event).

IC1LR				Reset value: undefined			
7	6	5	4	3	2	1	0
MSB							LSB
R	R	R	R	R	R	R	R

Output compare 1 high register (OC1HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC1HR				Reset value: 1000 0000 (80h)			
7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 1 low register (OC1LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC1LR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 2 high register (OC2HR)

This is an 8-bit register that contains the high part of the value to be compared to the CHR register.

OC2HR				Reset value: 1000 0000 (80h)			
7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Output compare 2 low register (OC2LR)

This is an 8-bit register that contains the low part of the value to be compared to the CLR register.

OC2LR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Counter high register (CHR)

This is an 8-bit register that contains the high part of the counter value.

CHR				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Counter low register (CLR)

This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after accessing the CSR register clears the TOF bit.

CLR				Reset value: 1111 1100 (FCh)			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Alternate counter high register (ACHR)

This is an 8-bit register that contains the high part of the counter value.

ACHR				Reset value: 1111 1111 (FFh)			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Alternate counter low register (ACLR)

This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to CSR register does not clear the TOF bit in the CSR register.

ACLR				Reset value: 1111 1100 (FCh)			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input capture 2 high register (IC2HR)

This is an 8-bit read only register that contains the high part of the counter value (transferred by the input capture 2 event).

IC2HR				Reset value: undefined			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input capture 2 low register (IC2LR)

This is an 8-bit read only register that contains the low part of the counter value (transferred by the input capture 2 event).

IC2LR				Reset value: undefined			
7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

16-bit timer register map and reset values**Table 48. 16-bit timer register map and reset values**

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
Timer A: 32 Timer B: 42	CR1 Reset value	ICIE 0	OCIE 0	TOIE 0	FOLV2 0	FOLV1 0	OLVL2 0	IEDG1 0	OLVL1 0
Timer A: 31 Timer B: 41	CR2 Reset value	OC1E 0	OC2E 0	OPM 0	PWM 0	CC1 0	CC0 0	IEDG2 0	EXEDG 0
Timer A: 33 Timer B: 43	CSR Reset value	ICF1 x	OCF1 x	TOF x	ICF2 x	OCF2 x	TIMD 0	- x	- x
Timer A: 34 Timer B: 44	IC1HR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 35 Timer B: 45	IC1LR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 36 Timer B: 46	OC1HR Reset value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 37 Timer B: 47	OC1LR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 3E Timer B: 4E	OC2HR Reset value	MSB 1	0	0	0	0	0	0	LSB 0
Timer A: 3F Timer B: 4F	OC2LR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
Timer A: 38 Timer B: 48	CHR Reset value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 39 Timer B: 49	CLR Reset value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3A Timer B: 4A	ACHR Reset value	MSB 1	1	1	1	1	1	1	LSB 1
Timer A: 3B Timer B: 4B	ACLR Reset value	MSB 1	1	1	1	1	1	0	LSB 0
Timer A: 3C Timer B: 4C	IC2HR Reset value	MSB x	x	x	x	x	x	x	LSB x
Timer A: 3D Timer B: 4D	IC2LR Reset value	MSB x	x	x	x	x	x	x	LSB x

10.5 Serial peripheral interface (SPI)

10.5.1 Introduction

The serial peripheral interface (SPI) allows full-duplex, synchronous, serial communication with external devices. An SPI system may consist of a master and one or more slaves however the SPI interface cannot be a master in a multi-master system.

10.5.2 Main features

- Full duplex synchronous transfers (on 3 lines)
- Simplex synchronous transfers (on 2 lines)
- Master or slave operation
- Six master mode frequencies ($f_{\text{CPU}}/4$ max.)
- $f_{\text{CPU}}/2$ max. slave mode frequency (see note below)
- $\overline{\text{SS}}$ management by software or hardware
- Programmable clock polarity and phase
- End of transfer interrupt flag
- Write collision, master mode fault and overrun flags

Note: In slave mode, continuous transmission is not possible at maximum frequency due to the software overhead for clearing status flags and to initiate the next transmission sequence.

10.5.3 General description

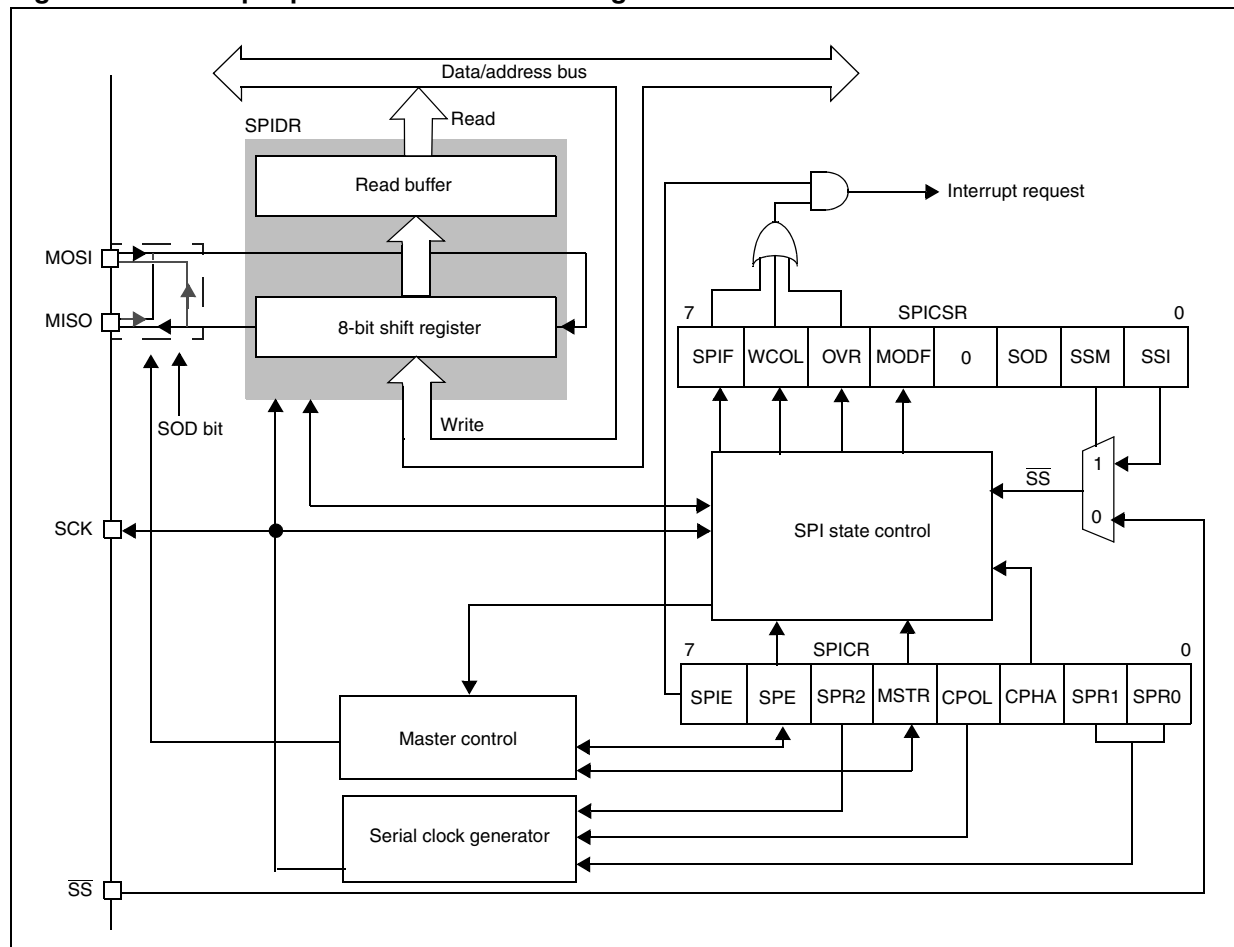
[Figure 50: Serial peripheral interface block diagram on page 107](#) shows the serial peripheral interface (SPI) block diagram. There are three registers:

- SPI control register (SPICR)
- SPI control/status register (SPICSR)
- SPI data register (SPIDR)

The SPI is connected to external devices through four pins:

- MISO: Master in/slave out data
- MOSI: Master out / slave in data
- SCK: Serial clock out by SPI masters and input by SPI slaves
- $\overline{\text{SS}}$: Slave select:

This input signal acts as a 'chip select' to let the SPI master communicate with slaves individually and to avoid contention on the data lines. Slave $\overline{\text{SS}}$ inputs can be driven by standard I/O ports on the master MCU.

Figure 50. Serial peripheral interface block diagram

Functional description

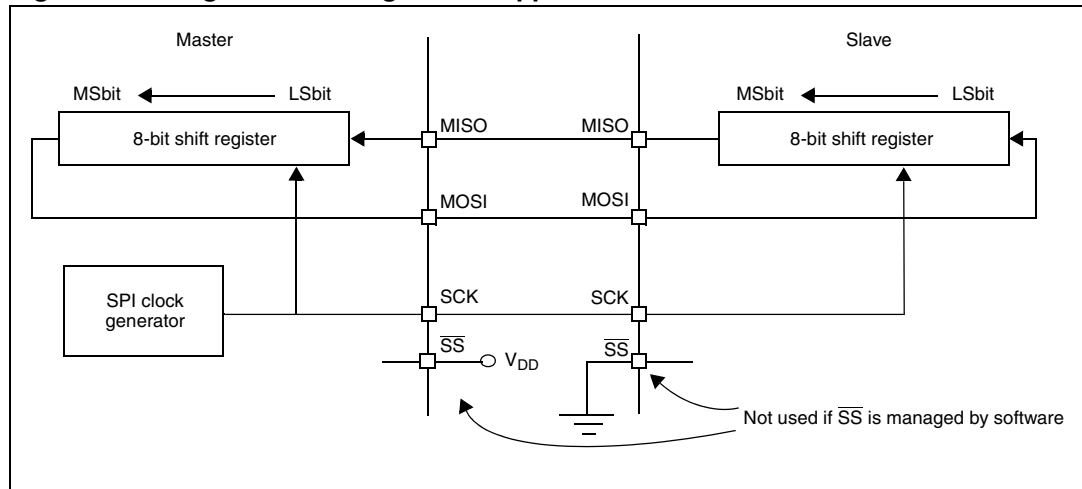
A basic example of interconnections between a single master and a single slave is illustrated in [Figure 51: Single master/single slave application on page 108](#).

The MOSI pins are connected together and the MISO pins are connected together. In this way data is transferred serially between master and slave (most significant bit first).

The communication is always initiated by the master. When the master device transmits data to a slave device via MOSI pin, the slave device responds by sending data to the master device via the MISO pin. This implies full duplex communication with both data out and data in synchronized with the same clock signal (which is provided by the master device via the SCK pin).

To use a single data line, the MISO and MOSI pins must be connected at each node (in this case only simplex communication is possible).

Four possible data/clock timing relationships may be chosen (see [Figure 54: Data clock timing diagram on page 112](#)) but master and slave must be programmed with the same timing mode.

Figure 51. Single master/single slave application

Slave select management

As an alternative to using the \overline{SS} pin to control the slave select signal, the application can choose to manage the slave select signal by software. This is configured by the SSM bit in the SPICSR register (see [Figure 53: Hardware/software slave select management on page 109](#))

In software management, the external \overline{SS} pin is free for other application uses and the internal \overline{SS} signal level is driven by writing to the SSI bit in the SPICSR register.

In master mode:

- \overline{SS} internal must be held high continuously

In slave mode:

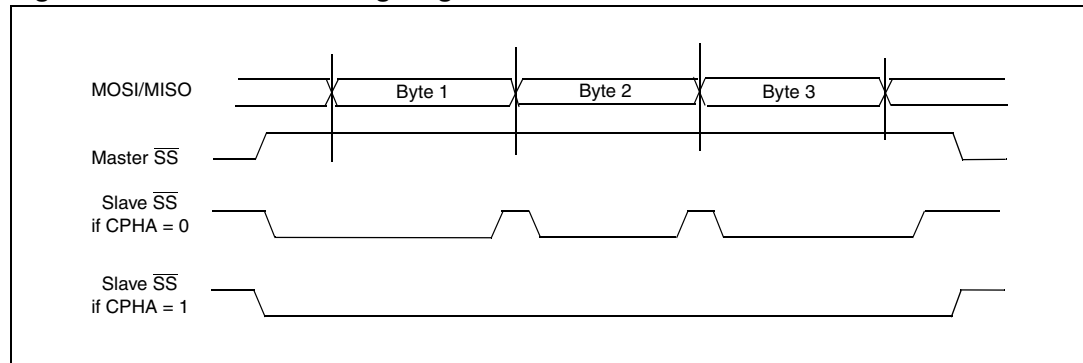
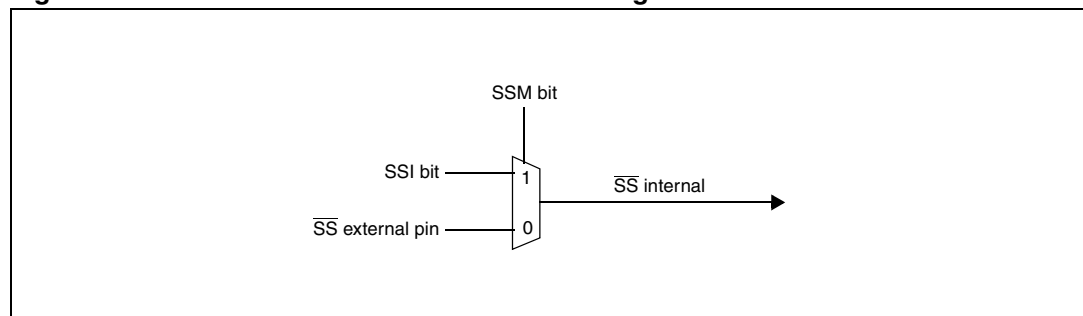
There are two cases depending on the data/clock timing relationship (see [Figure 52: Generic SS timing diagram on page 109](#)):

If CPHA = 1 (data latched on 2nd clock edge):

- \overline{SS} internal must be held low during the entire transmission. This implies that in single slave applications the \overline{SS} pin either can be tied to V_{SS}, or made free for standard I/O by managing the \overline{SS} function by software (SSM = 1 and SSI = 0 in the in the SPICSR register)

If CPHA = 0 (data latched on 1st clock edge):

- \overline{SS} internal must be held low during byte transmission and pulled high between each byte to allow the slave to write to the shift register. If \overline{SS} is not pulled high, a write collision error occurs when the slave writes to the shift register (see [Write collision error \(WCOL\) on page 113](#)).

Figure 52. Generic \overline{SS} timing diagram**Figure 53. Hardware/software slave select management****Master mode operation**

In master mode, the serial clock is output on the SCK pin. The clock frequency, polarity and phase are configured by software (refer to the description of the SPICSR register).

Note: The idle state of SCK must correspond to the polarity selected in the SPICSR register (by pulling up SCK if CPOL = 1 or pulling down SCK if CPOL = 0).

To operate the SPI in master mode, perform the following steps in order:

1. Write to the SPICR register:
 - Select the clock frequency by configuring the SPR[2:0] bits
 - Select the clock polarity and clock phase by configuring the CPOL and CPHA bits.
[Figure 54: Data clock timing diagram on page 112](#) shows the four possible configurations.

Note: The slave must have the same CPOL and CPHA settings as the master.

2. Write to the SPICSR register:
 - Either set the SSM bit and set the SSI bit or clear the SSM bit and tie the \overline{SS} pin high for the complete byte transmit sequence.
3. Write to the SPICR register:
 - Set the MSTR and SPE bits

Note: If the SPICSR register is not written first, the SPICR register setting (MSTR bit) may be not taken into account.

The transmit sequence begins when software writes a byte in the SPIDR register.

Master mode transmit sequence

When software writes to the SPIDR register, the data byte is loaded into the 8-bit shift register and then shifted out serially to the most significant bit of the MOSI pin first.

When data transfer is complete:

- The SPIF bit is set by hardware
- An interrupt request is generated if the SPIE bit is set and the interrupt mask in the CCR register is cleared.

Clearing the SPIF bit is performed by the following software sequence:

1. An access to the SPICSR register while the SPIF bit is set
2. A read to the SPIDR register

Note: While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

Slave mode operation

In slave mode, the serial clock is received on the SCK pin from the master device.

To operate the SPI in slave mode:

1. Write to the SPICSR register to perform the following actions:
 - Select the clock polarity and clock phase by configuring the CPOL and CPHA bits (see [Figure 54: Data clock timing diagram on page 112](#))

Note: The slave must have the same CPOL and CPHA settings as the master.

- Manage the \overline{SS} pin as described in [Slave select management on page 108](#) and [Figure 52: Generic SS timing diagram on page 109](#). If CPHA = 1 \overline{SS} must be held low continuously. If CPHA = 0 \overline{SS} must be held low during byte transmission and pulled up between each byte to let the slave write in the shift register.
2. Write to the SPICR register to clear the MSTR bit and set the SPE bit to enable the SPI I/O functions.

Slave mode transmit sequence

When software writes to the SPIDR register, the data byte is loaded into the 8-bit shift register and then shifted out serially to the most significant bit of the MISO pin first.

The transmit sequence begins when the slave device receives the clock signal and the most significant bit of the data on its MOSI pin.

When data transfer is complete:

- The SPIF bit is set by hardware
- An interrupt request is generated if SPIE bit is set and interrupt mask in the CCR register is cleared.

Clearing the SPIF bit is performed by the following software sequence:

1. An access to the SPICSR register while the SPIF bit is set
2. A write or a read to the SPIDR register

Note: While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

The SPIF bit can be cleared during a second transmission; however, it must be cleared before the second SPIF bit in order to prevent an overrun condition (see [Overrun condition \(OVR\) on page 113](#)).

10.5.4 Clock phase and clock polarity

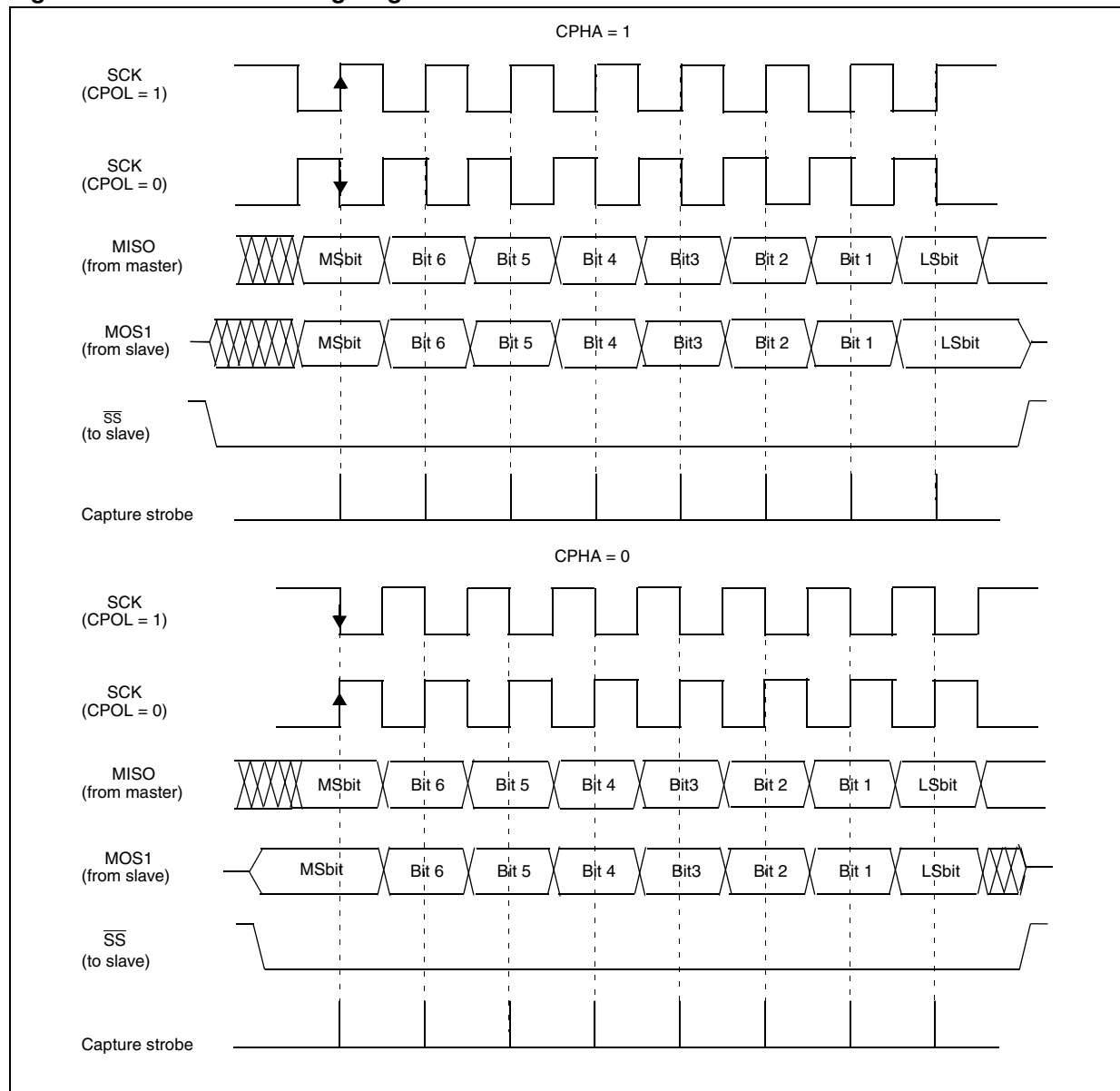
Four possible timing relationships may be chosen by software, using the CPOL and CPHA bits (see [Figure 54: Data clock timing diagram on page 112](#)).

Note: The idle state of SCK must correspond to the polarity selected in the SPICSR register (by pulling up SCK if CPOL = 1 or pulling down SCK if CPOL = 0).

The combination of the CPOL clock polarity and CPHA (clock phase) bits selects the data capture clock edge

[Figure 54: Data clock timing diagram on page 112](#), shows an SPI transfer with the four combinations of the CPHA and CPOL bits. The diagram may be interpreted as a master or slave timing diagram where the SCK pin, the MISO pin, the MOSI pin are directly connected between the master and the slave device.

Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.

Figure 54. Data clock timing diagram

1. This figure should not be used as a replacement for parametric information. Refer to [Section 12: Electrical characteristics on page 173](#).

10.5.5 Error flags

Master mode fault (MODF)

Master mode fault occurs when the master device has its \overline{SS} pin pulled low.

When a master mode fault occurs:

- The MODF bit is set and an SPI interrupt request is generated if the SPIE bit is set
- The SPE bit is reset. This blocks all output from the device and disables the SPI peripheral.
- The MSTR bit is reset, thus forcing the device into slave mode

Clearing the MODF bit is done through a software sequence:

1. A read access to the SPICSR register while the MODF bit is set
2. A write to the SPICR register

Note: To avoid any conflicts in an application with multiple slaves, the \overline{SS} pin must be pulled high during the MODF bit clearing sequence. The SPE and MSTR bits may be restored to their original state during or after this clearing sequence.

Hardware does not allow the user to set the SPE and MSTR bits while the MODF bit is set except in the MODF bit clearing sequence.

Overrun condition (OVR)

An overrun condition occurs, when the master device has sent a data byte and the slave device has not cleared the SPIF bit issued from the previously transmitted byte.

When an overrun occurs, the OVR bit is set and an interrupt request is generated if the SPIE bit is set.

In this case, the receiver buffer contains the byte sent after the SPIF bit was last cleared. A read to the SPIDR register returns this byte. All other bytes are lost.

The OVR bit is cleared by reading the SPICSR register.

Write collision error (WCOL)

A write collision occurs when the software tries to write to the SPIDR register while a data transfer is taking place with an external device. When this happens, the transfer continues uninterrupted and the software write is unsuccessful.

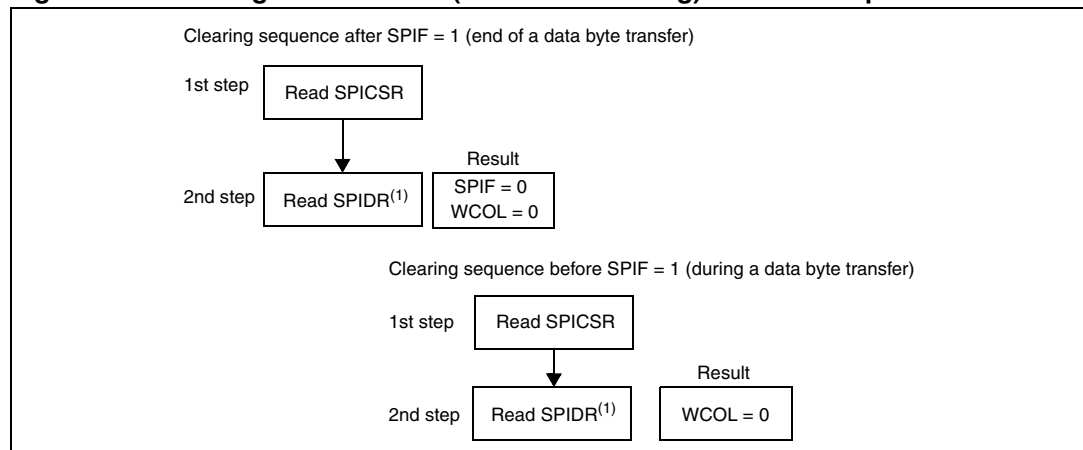
Write collisions can occur both in master and slave mode. See also [Slave select management on page 108](#).

Note: A 'read collision' never occurs since the received data byte is placed in a buffer in which access is always synchronous with the MCU operation.

The WCOL bit in the SPICSR register is set if a write collision occurs.

No SPI interrupt is generated when the WCOL bit is set (the WCOL bit is a status flag only).

Clearing the WCOL bit is done through a software sequence (see [Figure 55: Clearing the WCOL bit \(write collision flag\) software sequence on page 114](#)).

Figure 55. Clearing the WCOL bit (write collision flag) software sequence

1. Writing to the SPIDR register instead of reading it does not reset the WCOL bits.

Single master systems

A typical single master system may be configured, using an MCU as the master and four MCUs as slaves (see [Figure 56: Single master/multiple slave configuration on page 115](#)).

The master device selects the individual slave devices by using four pins of a parallel port to control the four \overline{SS} pins of the slave devices.

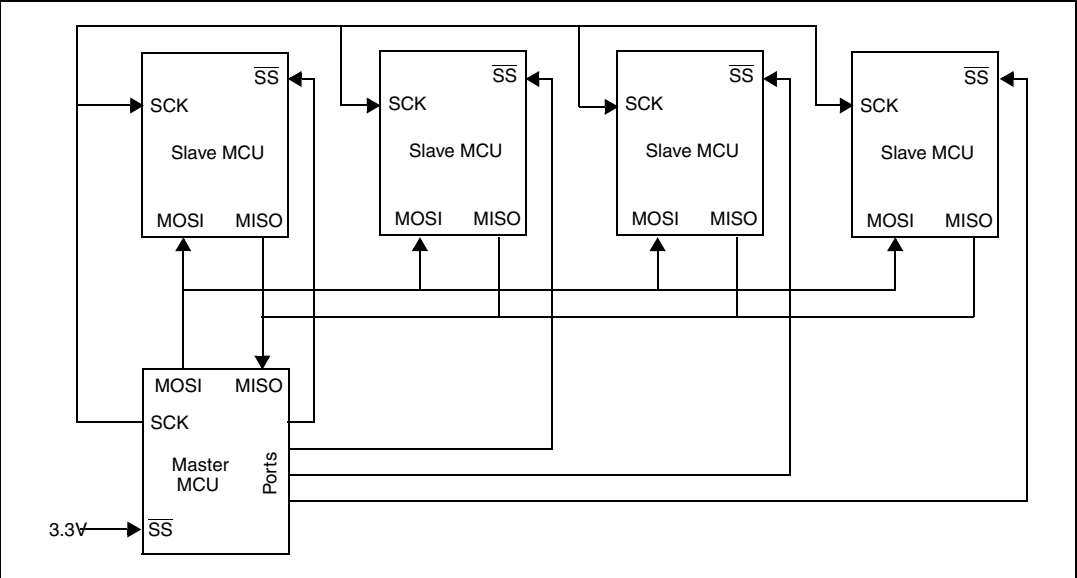
The \overline{SS} pins are pulled high during reset since the master device ports are forced to be inputs at that time, thus disabling the slave devices.

Note: *To prevent a bus conflict on the MISO line the master allows only one active slave device during a transmission.*

For more security, the slave device may respond to the master with the received data byte. Then the master receives the previous byte back from the slave device if all MISO and MOSI pins are connected and the slave has not written to its SPIDR register.

Other transmission security methods can use ports for handshake lines or data bytes with command fields.

Figure 56. Single master/multiple slave configuration



10.5.6 Low power modes

Table 49. Effect of low power modes on SPI

Mode	Description
Wait	No effect on SPI. SPI interrupt events cause the device to exit from wait mode.
Halt	SPI registers are frozen. In halt mode, the SPI is inactive. SPI operation resumes when the MCU is woken up by an interrupt with 'exit from halt mode' capability. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetching). If several data are received before the wake-up event, then an overrun error is generated. This error can be detected after the fetch of the interrupt routine that woke up the device.

Using the SPI to wake up the MCU from halt mode

In slave configuration, the SPI is able to wake up the ST7 device from halt mode through a SPIF interrupt. The data received is subsequently read from the SPIDR register when the software is running (interrupt vector fetch). If multiple data transfers have been performed before software clears the SPIF bit, then the OVR bit is set by hardware.

Note: When waking up from halt mode, if the SPI remains in slave mode, it is recommended to perform an extra communications cycle to bring the SPI from halt mode state to normal state. If the SPI exits from slave mode, it returns to normal state immediately.

Caution: The SPI can wake up the ST7 from halt mode only if the slave select signal (external \overline{SS} pin or the SSI bit in the SPICSR register) is low when the ST7 enters halt mode. So if slave selection is configured as external (see [Slave select management on page 108](#)), make sure the master drives a low level on the \overline{SS} pin when the slave enters halt mode.

10.5.7 Interrupts

Table 50. SPI interrupt control/wake-up capability⁽¹⁾

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
SPI end of transfer event	SPIF	SPIE	Yes	Yes
Master mode fault event	MODF			No
Overrun error	OVR			

1. The SPI interrupt events are connected to the same interrupt vector (see [Section 7: Interrupts on page 36](#)). They generate an interrupt if the corresponding enable control bit is set and the interrupt mask in the CC register is reset (RIM instruction).

10.5.8 SPI registers

Control register (SPICR)

SPICR

Reset value: 0000 xxxx (0xh)

7	6	5	4	3	2	1	0
SPIE	SPE	SPR2	MSTR	CPOL	CPHA	SPR[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Table 51. SPICR register description

Bit	Bit name	Function
7	SPIE	Serial peripheral interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SPI interrupt is generated whenever SPIF = 1, MODF = 1 or OVR = 1 in the SPICSR register
6	SPE	Serial peripheral output enable This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS} = 0$ (see Master mode fault (MODF) on page 113). The SPE bit is cleared by reset, so the SPI peripheral is not initially connected to the external pins. 0: I/O pins free for general purpose I/O 1: SPI I/O pin alternate functions enabled
5	SPR2	Divider enable This bit is set and cleared by software and is cleared by reset. It is used with the SPR[1:0] bits to set the baud rate (see bits [1:0] below). 0: Divider by 2 enabled 1: Divider by 2 disabled <i>Note: The SPR2 bit has no effect in slave mode</i>

Table 51. SPICR register description (continued)

Bit	Bit name	Function
4	MSTR	<p>Master mode</p> <p>This bit is set and cleared by software. It is also cleared by hardware when, in master mode, $\overline{SS} = 0$ (see Master mode fault (MODF) on page 113).</p> <p>0: Slave mode 1: Master mode. The function of the SCK pin changes from an input to an output and the functions of the MISO and MOSI pins are reversed.</p>
3	CPOL	<p>Clock polarity</p> <p>This bit is set and cleared by software. This bit determines the idle state of the serial clock. The CPOL bit affects both the master and slave modes.</p> <p>0: SCK pin has a low level idle state 1: SCK pin has a high level idle state</p> <p><i>Note: If CPOL is changed at the communication byte boundaries, the SPI must be disabled by resetting the SPE bit.</i></p>
2	CPHA	<p>Clock phase</p> <p>This bit is set and cleared by software.</p> <p>0: The first clock transition is the first data capture edge 1: The second clock transition is the first capture edge</p> <p><i>Note: The slave must have the same CPOL and CPHA settings as the master.</i></p>
1:0	SPR[1:0]	<p>Serial clock frequency</p> <p>These bits are set and cleared by software. Used with the SPR2 bit, they select the baud rate of the SPI serial clock SCK output by the SPI in master mode:</p> <p>100: serial clock = $f_{CPU}/4$ 000: serial clock = $f_{CPU}/8$ 001: serial clock = $f_{CPU}/16$ 110: serial clock = $f_{CPU}/32$ 010: serial clock = $f_{CPU}/64$ 011: serial clock = $f_{CPU}/128$</p> <p><i>Note: These 2 bits have no effect in slave mode.</i></p>

Control/status register (SPICSR)

SPICSR

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
SPIF	WCOL	OVR	MODF	Reserved	SOD	SSM	SSI
RO	RO	RO	RO	-	R/W	R/W	R/W

Table 52. SPICSR register description

Bit	Bit name	Function
7	SPIF	<p>Serial peripheral data transfer flag</p> <p>This bit is set by hardware when a transfer has been completed. An interrupt is generated if SPIE = 1 in the SPICR register. It is cleared by a software sequence (an access to the SPICSR register followed by a write or a read to the SPIDR register).</p> <p>0: Data transfer is in progress or the flag has been cleared 1: Data transfer between the device and an external device has been completed</p> <p><i>Note: While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.</i></p>
6	WCOL	<p>Write collision status</p> <p>This bit is set by hardware when a write to the SPIDR register is done during a transmit sequence. It is cleared by a software sequence (see Figure 55: Clearing the WCOL bit (write collision flag) software sequence on page 114).</p> <p>0: No write collision occurred 1: A write collision has been detected</p>
5	OVR	<p>SPI overrun error</p> <p>This bit is set by hardware when the byte currently being received in the shift register is ready to be transferred into the SPIDR register while SPIF = 1 (see Overrun condition (OVR) on page 113). An interrupt is generated if SPIE = 1 in SPICR register. The OVR bit is cleared by software reading the SPICSR register.</p> <p>0: No overrun error 1: Overrun error detected</p>
4	MODF	<p>Mode fault flag</p> <p>This bit is set by hardware when the \overline{SS} pin is pulled low in master mode (see Master mode fault (MODF) on page 113). An SPI interrupt can be generated if SPIE = 1 in the SPICSR register. This bit is cleared by a software sequence (an access to the SPICR register while MODF = 1 followed by a write to the SPICR register).</p> <p>0: No master mode fault detected 1: A fault in master mode has been detected</p>
3	-	Reserved, must be kept cleared.
2	SOD	<p>SPI output disable</p> <p>This bit is set and cleared by software. When set, it disables the alternate function of the SPI output (MOSI in master mode/MISO in slave mode).</p> <p>0: SPI output enabled (if SPE = 1) 1: SPI output disabled</p>

Table 52. SPICSR register description (continued)

Bit	Bit name	Function
1	SSM	\overline{SS} management This bit is set and cleared by software. When set, it disables the alternate function of the SPI \overline{SS} pin and uses the SSI bit value instead. See Slave select management on page 108 . 0: Hardware management (\overline{SS} managed by external pin) 1: Software management (internal \overline{SS} signal controlled by SSI bit. External \overline{SS} pin free for general-purpose I/O)
0	SSI	\overline{SS} internal mode This bit is set and cleared by software. It acts as a 'chip select' by controlling the level of the \overline{SS} slave select signal when the SSM bit is set. 0: Slave selected 1: Slave deselected

Data I/O register (SPIDR)

SPIDR							Reset value: undefined
7	6	5	4	3	2	1	0
D[7:0]							
R/W							

The SPIDR register is used to transmit and receive data on the serial bus. In a master device, a write to this register initiates transmission/reception of another byte.

Note: *During the last clock cycle the SPIF bit is set, a copy of the received data byte in the shift register is moved to a buffer. When the user reads the serial peripheral data I/O register, the buffer is actually being read.*

While the SPIF bit is set, all writes to the SPIDR register are inhibited until the SPICSR register is read.

Warning: A write to the SPIDR register places data directly into the shift register for transmission.

A read to the SPIDR register returns the value located in the buffer and not the content of the shift register (see [Figure 50: Serial peripheral interface block diagram on page 107](#)).

SPI register map and reset values

Table 53. SPI register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0021h	SPIDR Reset value	MSB x	x	x	x	x	x	x	LSB x
0022h	SPICR Reset value	SPIE 0	SPE 0	SPR2 0	MSTR 0	CPOL x	CPHA x	SPR1 x	SPR0 x
0023h	SPICSR Reset value	SPIF 0	WCOL 0	OVR 0	MODF 0		SOD 0	SSM 0	SSI 0

10.6 Serial communications interface (SCI)

10.6.1 Introduction

The SCI offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The SCI offers a very wide range of baud rates using two baud rate generator systems.

10.6.2 Main features

- Full duplex, asynchronous communications
- NRZ standard format (mark/space)
- Dual baud rate generator systems
- Independently programmable transmit and receive baud rates up to 500K baud
- Programmable data word length (8 or 9 bits)
- Receive buffer full, transmit buffer empty and end of transmission flags
- Two receiver wake up modes:
 - Address bit (MSB)
 - Idle line
- Muting function for multiprocessor configurations
- Separate enable bits for transmitter and receiver
- Four error detection flags:
 - Overrun error
 - Noise error
 - Frame error
 - Parity error
- Five interrupt sources with flags:
 - Transmit data register empty
 - Transmission complete
 - Receive data register full
 - Idle line received
 - Overrun error detected

- Parity control:
 - Transmits parity bit
 - Checks parity of received data byte
- Reduced power consumption mode

10.6.3 General description

The interface is externally connected to another device by two pins (see [Figure 58: Word length programming on page 124](#)):

- TDO: Transmit data output. When the transmitter and the receiver are disabled, the output pin returns to its I/O port configuration. When the transmitter and/or the receiver are enabled and nothing is to be transmitted, the TDO pin is at high level.
- RDI: Receive data input is the serial data input. Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise.

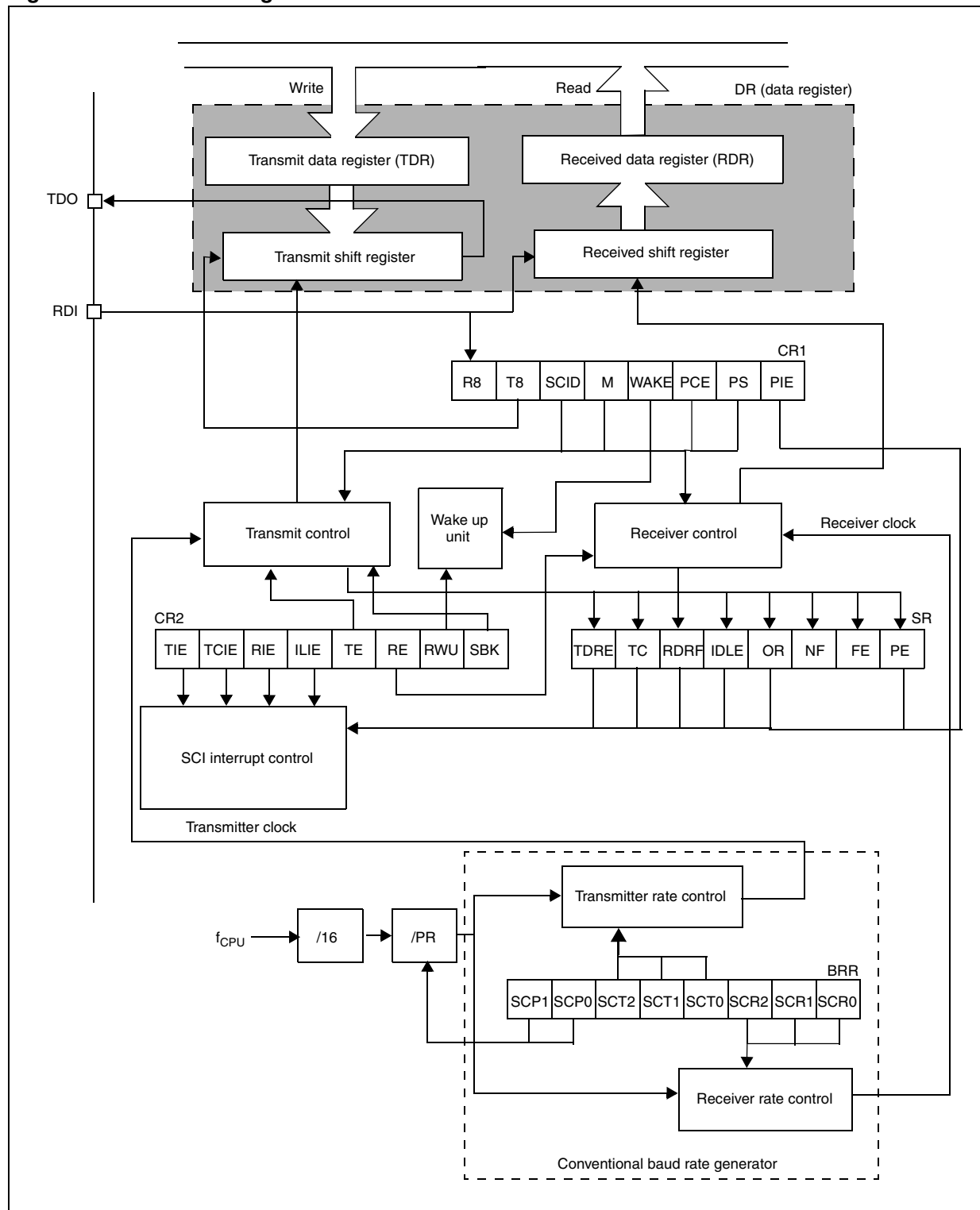
Through these pins, serial data is transmitted and received as frames comprising:

- An idle line prior to transmission or reception
- A start bit
- A data word (8 or 9 bits) least significant bit first
- A stop bit indicating that the frame is complete

This interface uses two types of baud rate generator:

- A conventional type for commonly-used baud rates
- An extended type with a prescaler offering a very wide range of baud rates even with non-standard oscillator frequencies.

Figure 57. SCI block diagram



10.6.4 Functional description

The block diagram of the serial control interface, is shown in [Figure 57: SCI block diagram on page 122](#). It contains 6 dedicated registers:

- Two control registers (SCICR1 and SCICR2)
- A status register (SCISR)
- A baud rate register (SCIBRR)
- An extended prescaler receiver register (SCIERPR)
- An extended prescaler transmitter register (SCIETPR)

Refer to the register descriptions in [Section 10.6.7: SCI registers on page 134](#) for the definitions of each bit.

Serial data format

Word length may be selected as being either 8 or 9 bits by programming the M bit in the SCICR1 register (see [Figure 57: SCI block diagram on page 122](#)).

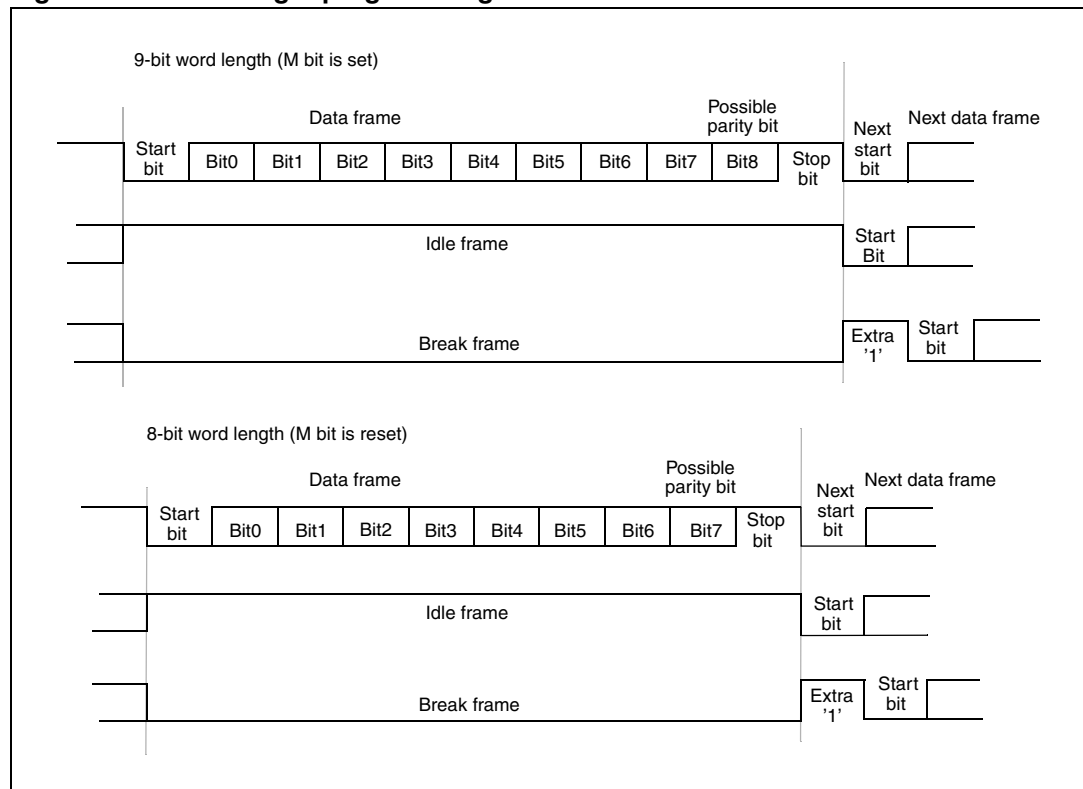
The TDO pin is in low state during the start bit.

The TDO pin is in high state during the stop bit.

An idle character is interpreted as an entire frame of '1's followed by the start bit of the next frame which contains data.

A break character is interpreted on receiving '0's for some multiple of the frame period. At the end of the last break frame the transmitter inserts an extra '1' bit to acknowledge the start bit.

Transmission and reception are driven by their own baud rate generator.

Figure 58. Word length programming

Transmitter

The transmitter can send data words of either 8 or 9 bits depending on the M bit status. When the M bit is set, word length is 9 bits and the 9th bit (the MSB) has to be stored in the T8 bit in the SCICR1 register.

Character transmission

During an SCI transmission, data shifts out least significant bit first on the TDO pin. In this mode, the SCIDR register consists of a buffer (TDR) between the internal bus and the transmit shift register (see [Figure 57: SCI block diagram on page 122](#)).

Procedure

- Select the M bit to define the word length
- Select the desired baud rate using the SCIBRR and the SCIETPR registers
- Set the TE bit to assign the TDO pin to the alternate function and to send an idle frame as first transmission
- Access the SCISR register and write the data to send in the SCIDR register (this sequence clears the TDRE bit). Repeat this sequence for each data to be transmitted.

Clearing the TDRE bit is always performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

The TDRE bit is set by hardware and it indicates:

- The TDR register is empty
- The data transfer is beginning
- The next data can be written in the SCIDR register without overwriting the previous data

This flag generates an interrupt if the TIE bit is set and the I bit is cleared in the CCR register.

When a transmission is taking place, a write instruction to the SCIDR register stores the data in the TDR register and which is copied in the shift register at the end of the current transmission.

When no transmission is taking place, a write instruction to the SCIDR register places the data directly in the shift register, the data transmission starts, and the TDRE bit is immediately set.

When a frame transmission is complete (after the stop bit) the TC bit is set and an interrupt is generated if the TCIE is set and the I bit is cleared in the CCR register.

Clearing the TC bit is performed by the following software sequence:

1. An access to the SCISR register
2. A write to the SCIDR register

Note: The TDRE and TC bits are cleared by the same software sequence.

Break characters

Setting the SBK bit loads the shift register with a break character. The break frame length depends on the M bit (see [Figure 58: Word length programming on page 124](#)).

As long as the SBK bit is set, the SCI send break frames to the TDO pin. After clearing this bit by software the SCI insert a logic 1 bit at the end of the last break frame to guarantee the recognition of the start bit of the next frame.

Idle characters

Setting the TE bit drives the SCI to send an idle frame before the first data frame.

Clearing and then setting the TE bit during a transmission sends an idle frame after the current word.

Note: Resetting and setting the TE bit causes the data in the TDR register to be lost. Therefore the best time to toggle the TE bit is when the TDRE bit is set i.e. before writing the next byte in the SCIDR.

Receiver

The SCI can receive data words of either 8 or 9 bits. When the M bit is set, word length is 9 bits and the MSB is stored in the R8 bit in the SCICR1 register.

Character reception

During a SCI reception, data shifts with least significant bit first through the RDI pin. In this mode, the SCIDR register consists of a buffer (RDR) between the internal bus and the received shift register (see [Figure 57: SCI block diagram on page 122](#)).

Procedure

- Select the M bit to define the word length
- Select the desired baud rate using the SCIBRR and the SCIERPR registers
- Set the RE bit, this enables the receiver which begins searching for a start bit

When a character is received:

- The RDRF bit is set. It indicates that the content of the shift register is transferred to the RDR.
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CCR register
- The error flags can be set if a frame error, noise or an overrun error has been detected during reception.

Clearing the RDRF bit is performed by the following software sequence done by:

1. An access to the SCISR register
2. A read to the SCIDR register

The RDRF bit must be cleared before the end of the reception of the next character to avoid an overrun error.

Break character

When a break character is received, the SCI handles it as a framing error.

Idle character

When an idle frame is detected, there is the same procedure as a data received character plus an interrupt if the ILIE bit is set and the I bit is cleared in the CCR register.

Overrun error

An overrun error occurs when a character is received when RDRF has not been reset. Data cannot be transferred from the shift register to the RDR register as long as the RDRF bit is not cleared.

When an overrun error occurs:

- The OR bit is set
- The RDR content is not lost
- The shift register is overwritten
- An interrupt is generated if the RIE bit is set and the I bit is cleared in the CCR register

The OR bit is reset by an access to the SCISR register followed by a SCIDR register read operation.

Noise error

Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise. Normal data bits are considered valid if three consecutive samples (8th, 9th, 10th) have the same bit value, otherwise the NF flag is set. In the case of start bit detection, the NF flag is set on the basis of an algorithm combining both valid edge detection and three samples (8th, 9th, 10th). Therefore, to prevent the NF flag getting set during start bit reception, there should be a valid edge detection as well as three valid samples.

When noise is detected in a frame:

- The NF flag is set at the rising edge of the RDRF bit
- Data is transferred from the shift register to the SCIDR register
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

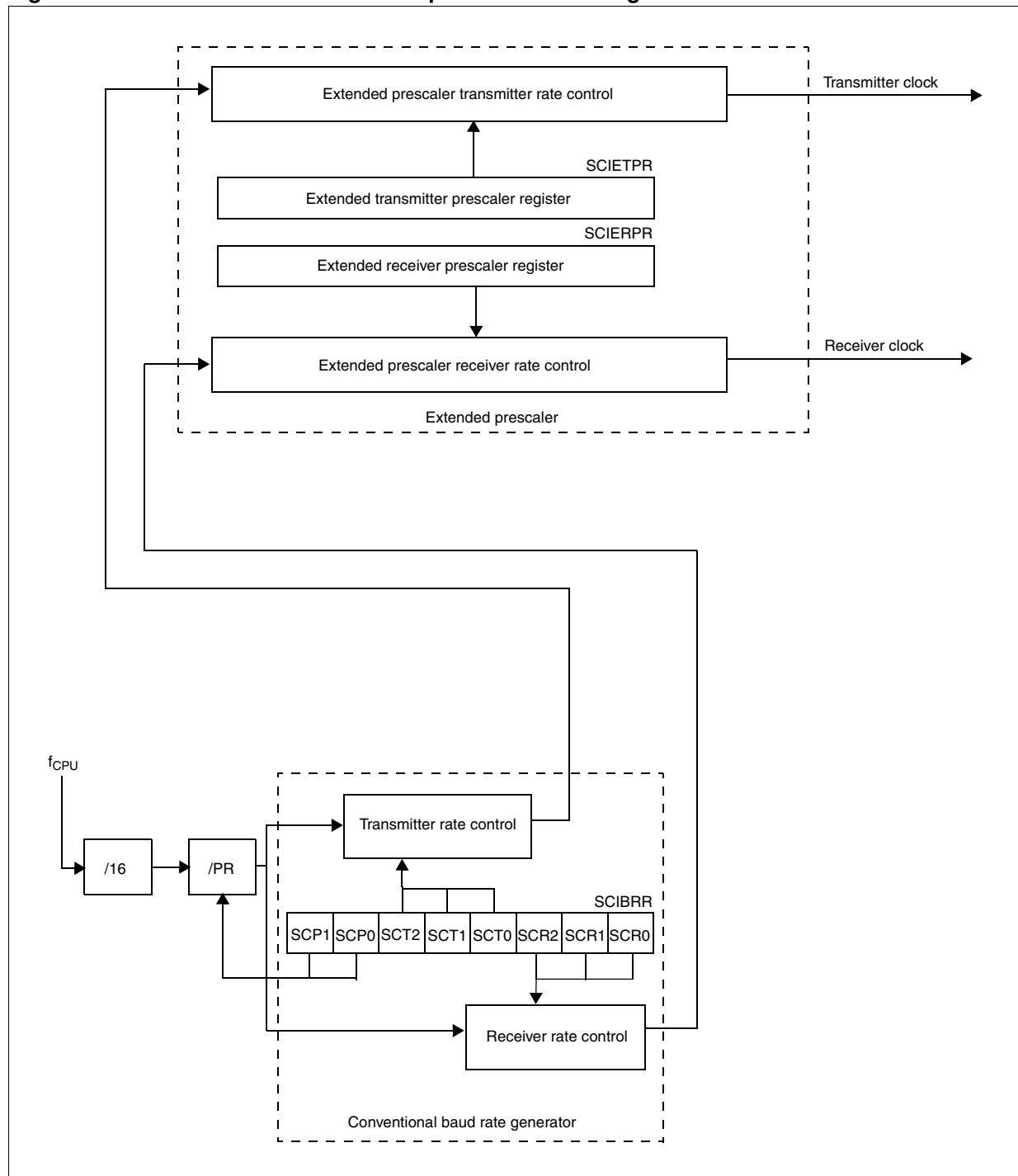
The NF flag is reset by a SCISR register read operation followed by a SCIDR register read operation.

During reception, if a false start bit is detected (example, 8th, 9th, 10th samples are 011,101,110), the frame is discarded and the receiving sequence is not started for this frame. There is no RDRF bit set for this frame and the NF flag is set internally (not accessible to the user). This NF flag is accessible along with the RDRF bit when a next valid frame is received.

Note: If the application start bit is not long enough to match the above requirements, then the NF flag may get set due to the short start bit. In this case, the NF flag may be ignored by the application software when the first valid byte is received.

See also [Noise error causes on page 132](#).

Figure 59. SCI baud rate and extended prescaler block diagram



Framing error

A framing error is detected when:

- The stop bit is not recognized on reception at the expected time, following either a de-synchronization or excessive noise.
- A break is received

When the framing error is detected:

- the FE bit is set by hardware
- Data is transferred from the Shift register to the SCIDR register
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The FE bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

Conventional baud rate generation

The baud rate for the receiver and transmitter (Rx and Tx) are set independently and calculated as follows:

$$Tx = \frac{f_{CPU}}{(16 \cdot PR) \cdot TR} \quad Rx = \frac{f_{CPU}}{(16 \cdot PR) \cdot RR}$$

where:

PR = 1, 3, 4 or 13 (see SCP[1:0] bits)

TR = 1, 2, 4, 8, 16, 32, 64, 128 (see SCT[2:0] bits)

RR = 1, 2, 4, 8, 16, 32, 64, 128 (see SCR[2:0] bits)

All these bits are in the SCIBRR register (see [Baud rate register \(SCIBRR\) on page 139](#)).

Example: If f_{CPU} is 8 MHz (normal mode) and if PR = 13 and TR = RR = 1, the transmit and receive baud rates are 38400 baud.

Note: The baud rate registers **MUST NOT** be changed while the transmitter or the receiver is enabled.

Extended baud rate generation

The extended prescaler option gives a very fine tuning on the baud rate, using a 255 value prescaler, whereas the conventional baud rate generator retains industry standard software compatibility.

The extended baud rate generator block diagram is described in [Figure 59: SCI baud rate and extended prescaler block diagram on page 128](#).

The output clock rate sent to the transmitter or to the receiver is the output from the 16 divider divided by a factor ranging from 1 to 255 set in the SCIERPR or the SCIETPR register.

Note: The extended prescaler is activated by setting the SCIETPR or SCIERPR register to a value other than zero.

The baud rates are calculated as follows:

$$T_x = \frac{f_{CPU}}{16 \cdot ETPR \cdot (PR \cdot TR)} \quad R_x = \frac{f_{CPU}}{16 \cdot ERPR \cdot (PR \cdot RR)}$$

where:

ETPR = 1,.. 255 (see [Extended transmit prescaler division register \(SCIETPR\) on page 140](#))

ERPR = 1,.. 255 (see [Extended receive prescaler division register \(SCIERPR\) on page 140](#))

Receiver muting and wakeup feature

In multiprocessor configurations it is often desirable that only the intended message recipient should actively receive the full message contents, thus reducing redundant SCI service overhead for all non addressed receivers.

The non addressed devices may be placed in sleep mode by means of the muting function.

Setting the RWU bit by software puts the SCI in sleep mode:

None of the reception status bits can be set.

All the receive interrupts are inhibited.

A muted receiver may be awakened by one of the following two ways:

- by idle line detection if the WAKE bit is reset
- by address mark detection if the WAKE bit is set

Receiver wakes-up by idle line detection when the receive line has recognized an idle frame. Then the RWU bit is reset by hardware but the IDLE bit is not set.

Receiver wakes-up by address mark detection when it received a '1' as the most significant bit of a word, thus indicating that the message is an address. The reception of this particular word wakes up the receiver, resets the RWU bit and sets the RDRF bit, which allows the receiver to receive this word normally and to use it as an address word.

Caution: In mute mode, do not write to the SCICR2 register. If the SCI is in mute mode during the read operation (RWU = 1) and an address mark wake up event occurs (RWU is reset) before the write operation, the RWU bit is set again by this write operation. Consequently the address byte is lost and the SCI is not woken up from mute mode.

Parity control

Parity control (generation of parity bit in transmission and parity checking in reception) can be enabled by setting the PCE bit in the SCICR1 register. Depending on the frame length defined by the M bit, the possible SCI frame formats are as listed in [Table 54](#).

Table 54. Frame formats⁽¹⁾

M bit	PCE bit	SCI frame
0	0	SB 8 bit data STB
0	1	SB 7-bit data PB STB
1	0	SB 9-bit data STB
1	1	SB 8-bit data PB STB

1. Legend: SB = start bit, STB = stop bit, PB = parity bit.

Note: *In case of wake up by an address mark, the MSB bit of the data is taken into account and not the parity bit*

Even parity

The parity bit is calculated to obtain an even number of '1s' inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example, data = 00110101; 4 bits set => parity bit is 0 if even parity is selected (PS bit = 0).

Odd parity

The parity bit is calculated to obtain an odd number of '1s' inside the frame made of the 7 or 8 LSB bits (depending on whether M is equal to 0 or 1) and the parity bit.

Example, data = 00110101; 4 bits set => parity bit is 1 if odd parity is selected (PS bit = 1).

Transmission mode

If the PCE bit is set then the MSB bit of the data written in the data register is not transmitted but is changed by the parity bit.

Reception mode

If the PCE bit is set then the interface checks if the received data byte has an even number of '1s' if even parity is selected (PS = 0) or an odd number of '1s' if odd parity is selected (PS = 1). If the parity check fails, the PE flag is set in the SCISR register and an interrupt is generated if PIE is set in the SCICR1 register.

SCI clock tolerance

During reception, each bit is sampled 16 times. The majority of the 8th, 9th and 10th samples is considered as the bit value. For a valid bit detection, all the three samples should have the same value otherwise the noise flag (NF) is set. For example: if the 8th, 9th and 10th samples are 0, 1 and 1 respectively, then the bit value is '1', but the noise flag bit is set because the three samples values are not the same.

Consequently, the bit length must be long enough so that the 8th, 9th and 10th samples have the desired bit value. This means the clock frequency should not vary more than 6/16 (37.5%) within one bit. The sampling clock is resynchronized at each start bit, so that when receiving 10 bits (1 start bit, 1 data byte, 1 stop bit), the clock deviation must not exceed 3.75%.

Note: *The internal sampling clock of the microcontroller samples the pin value on every falling edge. Therefore, the internal sampling clock and the time the application expects the sampling to take place may be out of sync. For example: If the baud rate is 15.625 kbaud (bit length is 64µs), then the 8th, 9th and 10th samples are at 28µs, 32µs and 36µs respectively (the first sample starting ideally at 0µs). But if the falling edge of the internal clock occurs just before the pin value changes, the samples would then be out of sync by ~4µs. This means the entire bit length must be at least 40µs (36µs for the 10th sample + 4µs for synchronization with the internal sampling clock).*

Clock deviation causes

The causes which contribute to the total deviation are:

- D_{TRA} : Deviation due to transmitter error (local oscillator error of the transmitter or the transmitter is transmitting at a different baud rate)
- D_{QUANT} : Error due to the baud rate quantization of the receiver
- D_{REC} : Deviation of the local oscillator of the receiver. This deviation can occur during the reception of one complete SCI message assuming that the deviation has been compensated at the beginning of the message
- D_{TCL} : Deviation due to the transmission line (generally due to the transceivers)

All the deviations of the system should be added and compared to the SCI clock tolerance:

$$D_{TRA} + D_{QUANT} + D_{REC} + D_{TCL} < 3.75\%$$

Noise error causes

See also description of noise error in [Receiver on page 125](#).

Start bit

The noise flag (NF) is set during start bit reception if one of the following conditions occurs:

1. A valid falling edge is not detected. A falling edge is considered to be valid if the 3 consecutive samples before the falling edge occurs are detected as '1' and, after the falling edge occurs, during the sampling of the 16 samples, if one of the samples numbered 3, 5 or 7 is detected as a '1'.
2. During sampling of the 16 samples, if one of the samples numbered 8, 9 or 10 is detected as a '1'.

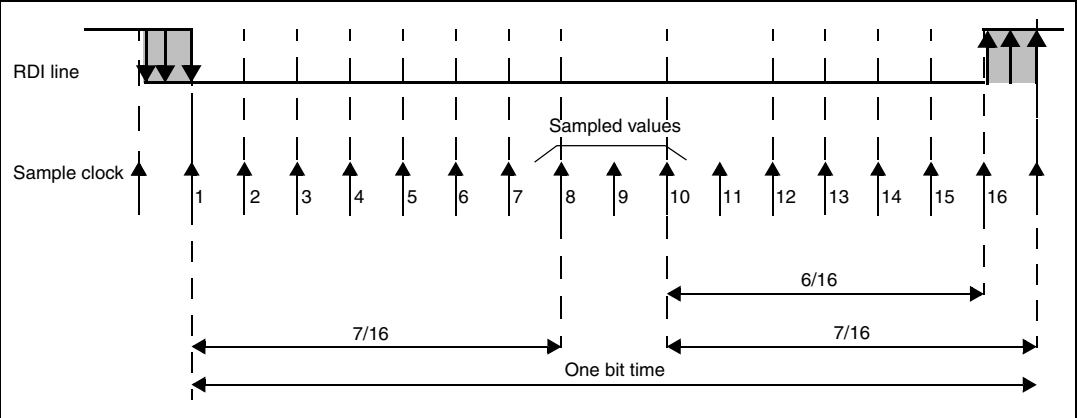
Therefore, a valid start bit must satisfy both the above conditions to prevent the noise flag getting set.

Data bits

The noise flag (NF) is set during normal data bit reception if the following condition occurs: During the sampling of 16 samples, if all three samples numbered 8, 9 and 10 are not the same. The majority of the 8th, 9th and 10th samples is considered as the bit value.

Therefore, a valid data bit must have samples 8, 9 and 10 at the same value to prevent the noise flag being set.

Figure 60. Bit sampling in reception mode



10.6.5 Low power modes

Table 55. Effect of low power modes on SCI

Mode	Description
Wait	No effect on SCI. SCI interrupts cause the device to exit from wait mode.
Halt	SCI registers are frozen. In Halt mode, the SCI stops transmitting/receiving until halt mode is exited.

10.6.6 Interrupts

The SCI interrupt events are connected to the same interrupt vector.

These events generate an interrupt if the corresponding enable control bit is set and the interrupt mask in the CC register is reset (RIM instruction).

Table 56. SCI interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
Transmit data register empty	TDRE	TIE	Yes	No
Transmission complete	TC	TCIE		
Received data ready to be read	RDRF	RIE		
Overrun error detected	OR			
Idle line detected	IDLE	ILIE		
Parity error	PE	PIE		

10.6.7 SCI registers

Status register (SCISR)

SCISR				Reset value: 1100 0000 (C0h)			
7	6	5	4	3	2	1	0
TDRE	TC	RDRF	IDLE	OR	NF	FE	PE
RO	RO	RO	RO	RO	RO	RO	RO

Table 57. SCISR register description

Bit	Bit name	Function
7	TDRE	<p>Transmit data register empty</p> <p>This bit is set by hardware when the content of the TDR register has been transferred into the shift register. An interrupt is generated if the TIE bit = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).</p> <p>0: Data is not transferred to the shift register 1: Data is transferred to the shift register</p> <p><i>Note: Data are not transferred to the shift register unless the TDRE bit is cleared.</i></p>
6	TC	<p>Transmission complete</p> <p>This bit is set by hardware when transmission of a frame containing data is complete. An interrupt is generated if TCIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a write to the SCIDR register).</p> <p>0: Transmission is not complete 1: Transmission is complete</p> <p><i>Note: TC is not set after the transmission of a preamble or a break.</i></p>
5	RDRF	<p>Received data ready flag</p> <p>This bit is set by hardware when the content of the RDR register has been transferred to the SCIDR register. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).</p> <p>0: Data are not received 1: Received data are ready to be read</p>
4	IDLE	<p>Idle line detect</p> <p>This bit is set by hardware when an idle line is detected. An interrupt is generated if the ILIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).</p> <p>0: No idle line is detected 1: Idle line is detected</p> <p><i>Note: The IDLE bit is not set again until the RDRF bit is set (i.e. a new idle line occurs).</i></p>

Table 57. SCISR register description (continued)

Bit	Bit name	Function
3	OR	<p>Overrun error</p> <p>This bit is set by hardware when the word currently being received in the shift register is ready to be transferred into the RDR register while RDRF = 1. An interrupt is generated if RIE = 1 in the SCICR2 register. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).</p> <p>0: No overrun error 1: Overrun error is detected</p> <p><i>Note: When the IDLE bit is set the RDR register content is not lost but the shift register is overwritten.</i></p>
2	NF	<p>Noise flag</p> <p>This bit is set by hardware when noise is detected on a received frame. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).</p> <p>0: No noise is detected 1: Noise is detected</p> <p><i>Note: The NF bit does not generate an interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt.</i></p>
1	FE	<p>Framing error</p> <p>This bit is set by hardware when a de-synchronization, excessive noise or a break character is detected. It is cleared by a software sequence (an access to the SCISR register followed by a read to the SCIDR register).</p> <p>0: No framing error is detected 1: Framing error or break character is detected</p> <p><i>Note: The FE bit does not generate an interrupt as it appears at the same time as the RDRF bit which itself generates an interrupt. If the word currently being transferred causes both frame error and overrun error, it is transferred and only the OR bit is set.</i></p>
0	PE	<p>Parity error</p> <p>This bit is set by hardware when a parity error occurs in receiver mode. It is cleared by a software sequence (a read to the status register followed by an access to the SCIDR data register). An interrupt is generated if PIE = 1 in the SCICR1 register.</p> <p>0: No parity error 1: Parity error</p>

Control register 1 (SCICR1)

SCICR1

Reset value: x000 0000 (x0h)

7	6	5	4	3	2	1	0
R8	T8	SCID	M	WAKE	PCE	PS	PIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 58. SCICR1 register description

Bit	Bit name	Function
7	R8	Receive data bit 8 This bit is used to store the 9th bit of the received word when M = 1.
6	T8	Transmit data bit 8 This bit is used to store the 9th bit of the transmitted word when M = 1.
5	SCID	Disabled for low power consumption When this bit is set the SCI prescalers and outputs are stopped at the end of the current byte transfer in order to reduce power consumption. This bit is set and cleared by software. 0: SCI enabled 1: SCI prescaler and outputs disabled
4	M	Word length This bit determines the word length. It is set or cleared by software. 0: 1 Start bit, 8 Data bits, 1 Stop bit 1: 1 Start bit, 9 Data bits, 1 Stop bit <i>Note: The M bit must not be modified during a data transfer (both transmission and reception).</i>
3	WAKE	Wake up method This bit determines the SCI wake up method, it is set or cleared by software. 0: Idle line 1: Address mark
2	PCE	Parity control enable This bit selects the hardware parity control (generation and detection). When the parity control is enabled, the computed parity is inserted at the MSB position (9th bit if M = 1; 8th bit if M = 0) and parity is checked on the received data. This bit is set and cleared by software. Once it is set, PCE is active after the current byte (in reception and in transmission). 0: Parity control disabled 1: Parity control enabled

Table 58. SCICR1 register description (continued)

Bit	Bit name	Function
1	PS	Parity selection This bit selects the odd or even parity when the parity generation/detection is enabled (PCE bit set). It is set and cleared by software. The parity is selected after the current byte. 0: Even parity 1: Odd parity
0	PIE	Parity interrupt enable This bit enables the interrupt capability of the hardware parity control when a parity error is detected (PE bit set). It is set and cleared by software. 0: Parity error interrupt disabled 1: Parity error interrupt enabled

Control register 2 (SCICR2)

SCICR2

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 59. SCICR2 register description

Bit	Bit name	Function
7	TIE	Transmitter interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TDRE = 1 in the SCISR register
6	TCIE	Transmission complete interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever TC = 1 in the SCISR register
5	RIE	Receiver interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever OR = 1 or RDRF = 1 in the SCISR register
4	ILIE	Idle line interrupt enable This bit is set and cleared by software. 0: Interrupt is inhibited 1: An SCI interrupt is generated whenever IDLE = 1 in the SCISR register

Table 59. SCICR2 register description (continued)

Bit	Bit name	Function
3	TE	<p>Transmitter enable</p> <p>This bit enables the transmitter. It is set and cleared by software.</p> <p>0: Transmitter is disabled</p> <p>1: Transmitter is enabled</p> <p><i>Note 1: During transmission, an '0' pulse on the TE bit ('0' followed by '1') sends a preamble (idle line) after the current word.</i></p> <p><i>Note 2: When TE is set there is a 1 bit-time delay before the transmission starts.</i></p> <p>Caution The TDO pin is free for general purpose I/O only when the TE and RE bits are both cleared (or if TE is never set).</p>
2	RE	<p>Receiver enable</p> <p>This bit enables the receiver. It is set and cleared by software.</p> <p>0: Receiver is disabled</p> <p>1: Receiver is enabled and begins searching for a start bit</p>
1	RWU	<p>Receiver wake up</p> <p>This bit determines if the SCI is in mute mode or not. It is set and cleared by software and can be cleared by hardware when a wake up sequence is recognized.</p> <p>0: Receiver in active mode</p> <p>1: Receiver in mute mode</p> <p><i>Note: Before selecting mute mode (setting the RWU bit), the SCI must receive some data first, otherwise it cannot function in mute mode with wake up by idle line detection.</i></p>
0	SBK	<p>Send break</p> <p>This bit set is used to send break characters. It is set and cleared by software.</p> <p>0: No break character is transmitted</p> <p>1: Break characters are transmitted</p> <p><i>Note: If the SBK bit is set to '1' and then to '0', the transmitter sends a BREAK word at the end of the current word.</i></p>

Data register (SCIDR)

Contains the received or transmitted data character, depending on whether it is read from or written to.

SCIDR	Reset value: undefined						
7	6	5	4	3	2	1	0
DR[7:0]							
R/W							

The data register performs a double function (read and write) since it is composed of two registers, one for transmission (TDR) and one for reception (RDR).

The TDR register provides the parallel interface between the internal bus and the output shift register (see [Figure 57: SCI block diagram on page 122](#)).

The RDR register provides the parallel interface between the input shift register and the internal bus (see [Figure 57](#)).

Baud rate register (SCIBRR)

SCIBRR

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
SCP[1:0]		SCT[2:0]			SCR[2:0]		
R/W		R/W			R/W		

Table 60. SCIBRR register description

Bit	Bit name	Function
7:6	SCP[1:0]	First SCI prescaler These 2 prescaling bits allow several standard clock division ranges: 00: PR prescaling factor = 1 01: PR prescaling factor = 3 10: PR prescaling factor = 4 11: PR prescaling factor = 13
5:3	SCT[2:0]	SCI transmitter rate divisor These 3 bits, in conjunction with the SCP1 and SCP0 bits define the total division applied to the bus clock to yield the transmit rate clock in conventional baud rate generator mode: 000: TR dividing factor = 1 001: TR dividing factor = 2 010: TR dividing factor = 4 011: TR dividing factor = 8 100: TR dividing factor = 16 101: TR dividing factor = 32 110: TR dividing factor = 64 111: TR dividing factor = 128
2:0	SCR[2:0]	SCI receiver rate divisor These 3 bits, in conjunction with the SCP[1:0] bits define the total division applied to the bus clock to yield the receive rate clock in conventional baud rate generator mode: 000: RR dividing factor = 1 001: RR dividing factor = 2 010: RR dividing factor = 4 011: RR dividing factor = 8 100: RR dividing factor = 16 101: RR dividing factor = 32 110: RR dividing factor = 64 111: RR dividing factor = 128

Extended receive prescaler division register (SCIERPR)

Allows setting of the extended prescaler rate division factor for the receive circuit.

SCIERPR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
ERPR[7:0]							
R/W							

Table 61. SCIERPR register description

Bit	Bit name	Function
7:0	ERPR[7:0]	<p>8-bit extended receive prescaler register</p> <p>The extended baud rate generator is activated when a value different from 00h is stored in this register. Therefore the clock frequency issued from the 16 divider (see Figure 59: SCI baud rate and extended prescaler block diagram on page 128) is divided by the binary factor set in the SCIERPR register (in the range 1 to 255). The extended baud rate generator is not used after a reset.</p>

Extended transmit prescaler division register (SCIETPR)

Allows setting of the external prescaler rate division factor for the transmit circuit.

SCIETPR				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
ETPR[7:0]							
R/W							

Table 62. SCIETPR register description

Bit	Bit name	Function
7:0	ETPR[7:0]	<p>8-bit extended transmit prescaler register</p> <p>The extended baud rate generator is activated when a value different from 00h is stored in this register. Therefore the clock frequency issued from the 16 divider (see Figure 59) is divided by the binary factor set in the SCIETPR register (in the range 1 to 255). The extended baud rate generator is not used after a reset.</p>

Baud rate selection**Table 63. Baud rate selection**

Symbol	Parameter	Conditions			Standard	Baud rate	Unit
		f _{CPU}	Accuracy vs. standard	Prescaler			
f _{Tx} f _{Rx}	Communication frequency	8 MHz	~0.16%	Conventional mode TR (or RR)=128, PR=13 TR (or RR)=32, PR=13 TR (or RR)=16, PR=13 TR (or RR)=8, PR=13 TR (or RR)=4, PR=13 TR (or RR)=16, PR=3 TR (or RR)=2, PR=13 TR (or RR)=1, PR=13	300 1200 2400 4800 9600 10400 19200 38400	~300.48 ~1201.92 ~2403.84 ~4807.69 ~9615.38 ~10416.67 ~19230.77 ~38461.54	Hz
			~0.79%	Extended mode ETPR (or ERPR) = 35, TR (or RR) = 1, PR = 1	14400	~14285.71	

SCI register map and reset values**Table 64. SCI register map and reset values**

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0050h	SCISR Reset value	TDRE 1	TC 1	RDRF 0	IDLE 0	OR 0	NF 0	FE 0	PE 0
0051h	SCIDR Reset value	MSB x	x	x	x	x	x	x	LSB x
0052h	SCIBRR Reset value	SCP1 0	SCP0 0	SCT2 0	SCT1 0	SCT0 0	SCR2 0	SCR1 0	SCR0 0
0053h	SCICR1 Reset value	R8 x	T8 0	SCID 0	M 0	WAKE 0	PCE 0	PS 0	PIE 0
0054h	SCICR2 Reset value	TIE 0	TCIE 0	RIE 0	ILIE 0	TE 0	RE 0	RWU 0	SBK 0
0055h	SCIERPR Reset value	MSB 0	0	0	0	0	0	0	LSB 0
0057h	SCIPETPR Reset value	MSB 0	0	0	0	0	0	0	LSB 0

10.7 I²C bus interface (I²C)

10.7.1 Introduction

The I²C bus interface serves as an interface between the microcontroller and the serial I²C bus. It provides both multimaster and slave functions, and controls all I²C bus-specific sequencing, protocol, arbitration and timing. It supports fast I²C mode (400 kHz).

10.7.2 Main features

- Parallel-bus/I²C protocol converter
- Multimaster capability
- 7-bit/10-bit addressing
- SMBus V1.1 compliant
- Transmitter/receiver flag
- End-of-byte transmission flag
- Transfer problem detection

I²C master features

- Clock generation
- I²C bus busy flag
- Arbitration lost flag
- End of byte transmission flag
- Transmitter/receiver flag
- Start bit detection flag
- Start and stop generation

I²C slave features

- Stop bit detection
- I²C bus busy flag
- Detection of misplaced start or stop condition
- Programmable I²C address detection
- Transfer problem detection
- End-of-byte transmission flag
- Transmitter/receiver flag

10.7.3 General description

In addition to receiving and transmitting data, this interface converts it from serial to parallel format and from parallel to serial format, using either an interrupt or polled handshake. The interrupts are enabled or disabled by software. The interface is connected to the I²C bus by a data pin (SDA) and by a clock pin (SCL). It can be connected both with a standard I²C bus and a fast I²C bus. This selection is made by software.

Mode selection

The interface can operate in the four following modes:

- Slave transmitter/receiver
- Master transmitter/receiver

By default, it operates in slave mode.

The interface automatically switches from slave to master after it generates a start condition and from master to slave in case of arbitration loss or a stop generation, allowing then Multimaster capability.

Communication flow

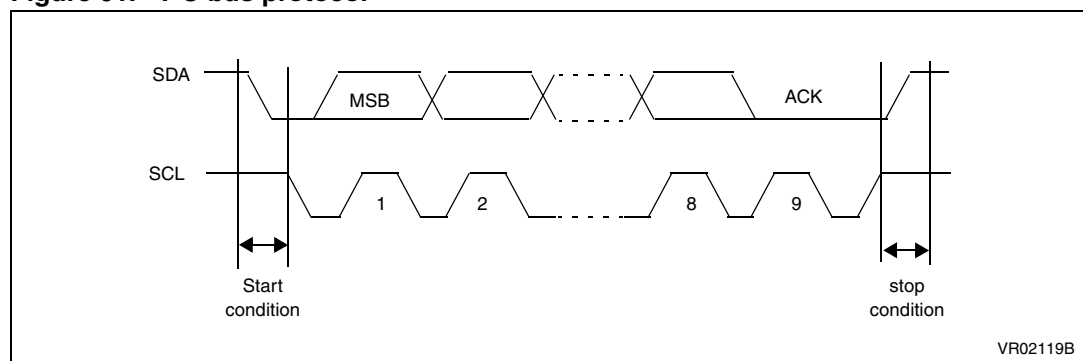
In master mode, it initiates a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. Both start and stop conditions are generated in master mode by software.

In slave mode, the interface is capable of recognizing its own address (7- or 10-bit), and the general call address. The general call address detection may be enabled or disabled by software.

Data and addresses are transferred as 8-bit bytes, MSB first. The first byte(s) following the start condition contain the address (one in 7-bit mode, two in 10-bit mode). The address is always transmitted in master mode.

A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must send an acknowledge bit to the transmitter. Refer to [Figure 61](#).

Figure 61. I²C bus protocol



Acknowledge may be enabled and disabled by software.

The I²C interface address and/or general call address can be selected by software.

The speed of the I²C interface may be selected between standard (up to 100 kHz) and fast I²C (up to 400 kHz).

SDA/SCL line control

Transmitter mode

The interface holds the clock line low before transmission to wait for the microcontroller to write the byte in the data register.

Receiver mode

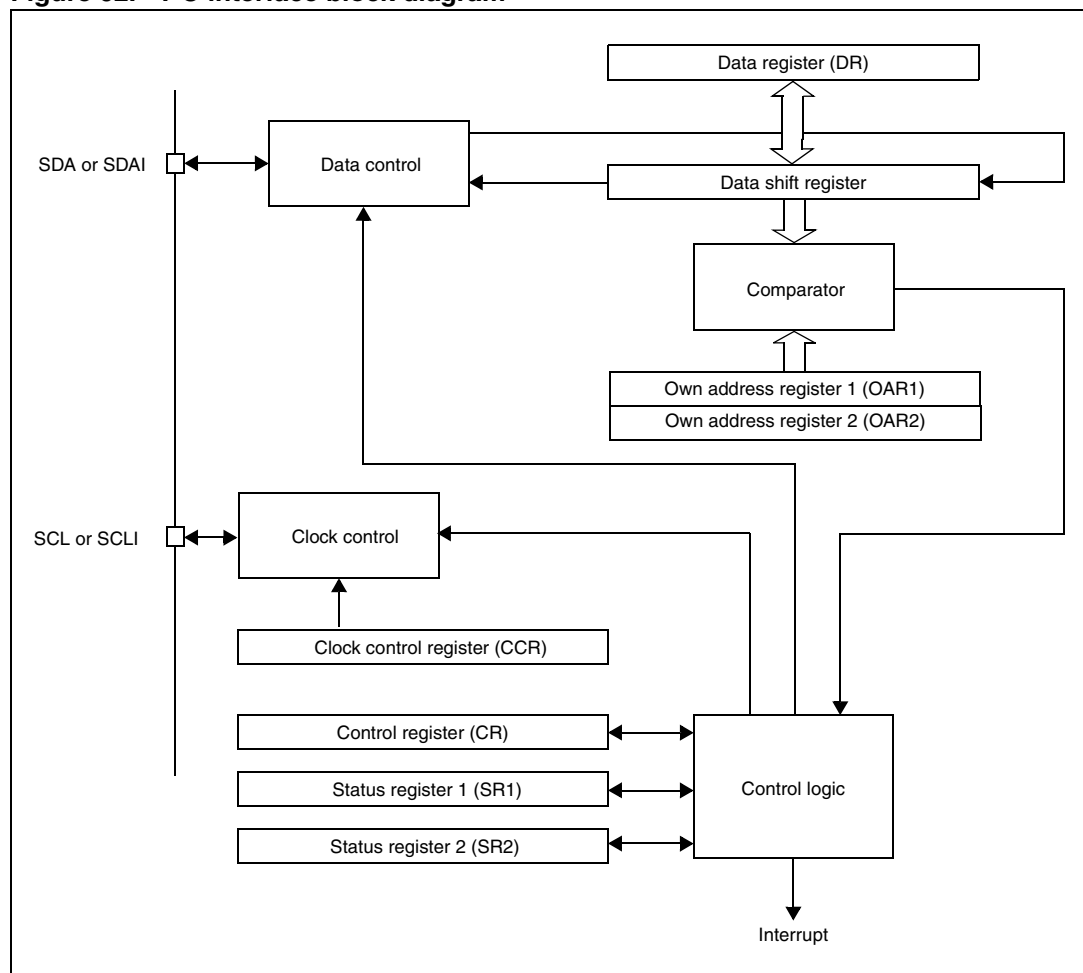
The interface holds the clock line low after reception to wait for the microcontroller to read the byte in the data register.

The SCL frequency (f_{SCL}) is controlled by a programmable clock divider which depends on the I²C bus mode.

When the I²C cell is enabled, the SDA and SCL ports must be configured as floating inputs. In this case, the value of the external pull-up resistor used depends on the application.

When the I²C cell is disabled, the SDA and SCL ports revert to being standard I/O port pins.

Figure 62. I²C interface block diagram



10.7.4 Functional description

Refer to the CR, SR1 and SR2 registers in [Section 10.7.7](#) for the bit definitions.

By default the I²C interface operates in slave mode (M/SL bit is cleared) except when it initiates a transmit or receive sequence.

First the interface frequency must be configured using the FRI bits in the OAR2 register.

Slave mode

As soon as a start condition is detected, the address is received from the SDA line and sent to the shift register; then it is compared with the address of the interface or the general call address (if selected by software).

Note: In 10-bit addressing mode, the comparison includes the header sequence (11110xx0) and the two most significant bits of the address.

Header matched (10-bit mode only): The interface generates an acknowledge pulse if the ACK bit is set.

Address not matched: The interface ignores it and waits for another start condition.

Address matched: The interface generates in sequence:

- An acknowledge pulse if the ACK bit is set
- EVF and ADSL bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV1).

Next, in 7-bit mode read the DR register to determine from the least significant bit (data direction bit) if the slave must enter receiver or transmitter mode.

In 10-bit mode, after receiving the address sequence the slave is always in receive mode. It will enter transmit mode on receiving a repeated start condition followed by the header sequence with matching address bits and the least significant bit set (11110xx1).

Slave receiver

Following the address reception and after the SR1 register has been read, the slave receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

- An acknowledge pulse if the ACK bit is set
- EVF and BTF bits are set with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV2).

Slave transmitter

Following the address reception and after SR1 register has been read, the slave sends bytes from the DR register to the SDA line via the internal shift register.

The slave waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV3).

When the acknowledge pulse is received, the EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

Closing slave communication

After the last data byte is transferred, a stop condition is generated by the master. The interface detects this condition and sets the EVF and STOPF bits with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR2 register (see [Figure 63: Transfer sequencing EV4](#)).

Error cases

- **BERR:** Detection of a stop or a start condition during a byte transfer. In this case, the EVF and the BERR bits are set with an interrupt if the ITE bit is set.
If it is a stop then the interface discards the data, released the lines and waits for another Start condition.
If it is a start then the interface discards the data and waits for the next slave address on the bus.
- **AF:** Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set with an interrupt if the ITE bit is set.
The AF bit is cleared by reading the I²CSR2 register. However, if read before the completion of the transmission, the AF flag will be set again, thus possibly generating a new interrupt. Software must ensure either that the SCL line is back at 0 before reading the SR2 register, or be able to correctly handle a second interrupt during the 9th pulse of a transmitted byte.

Note: In case of errors, the SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. While AF = 1, the SCL line may be held low due to SB or BTF flags that are set at the same time. It is then necessary to release both lines by software.

How to release the SDA/SCL lines

Set and subsequently clear the STOP bit while BTF is set. The SDA/SCL lines are released after the transfer of the current byte.

SMBus compatibility

The ST7 I²C is compatible with the SMBus V1.1 protocol. It supports all SMBus addressing modes, SMBus bus protocols and CRC-8 packet error checking. Refer to *SMBus slave driver for ST7 I²C peripheral* (AN1713).

Master mode

To switch from default slave mode to master mode a start condition generation is needed.

Start condition

Setting the START bit while the BUSY bit is cleared causes the interface to switch to master mode (M/SL bit set) and generates a start condition.

Once the start condition is sent, the EVF and SB bits are set by hardware with an interrupt if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the DR register with the slave address, **holding the SCL line low** (see [Figure 63: Transfer sequencing EV5](#)).

Slave address transmission

Next, the slave address is sent to the SDA line via the internal shift register.

In 7-bit addressing mode, one address byte is sent.

In 10-bit addressing mode, sending the first byte including the header sequence causes the EVF bit to be set by hardware with interrupt generation if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV9).

Then the second address byte is sent by the interface.

After completion of this transfer (and acknowledge from the slave if the ACK bit is set), the EVF bit is set by hardware with interrupt generation if the ITE bit is set.

Then the master waits for a read of the SR1 register followed by a write in the CR register (for example set PE bit), **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV6).

Next, the master must enter receiver or transmitter mode.

Note: In 10-bit addressing mode, to switch the master to receiver mode, software must generate a repeated start condition and resend the header sequence with the least significant bit set (11110xx1).

Master receiver

Following the address transmission and after SR1 and CR registers have been accessed, the master receives bytes from the SDA line into the DR register via the internal shift register. After each byte the interface generates in sequence:

- Acknowledge pulse if the ACK bit is set
- EVF and BTF bits are set by hardware with an interrupt if the ITE bit is set.

Then the interface waits for a read of the SR1 register followed by a read of the DR register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV7).

To close the communication: Before reading the last byte from the DR register, set the STOP bit to generate the stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

Note: In order to generate the non-acknowledge pulse after the last received data byte, the ACK bit must be cleared just before reading the second last data byte.

Master transmitter

Following the address transmission and after SR1 register has been read, the master sends bytes from the DR register to the SDA line via the internal shift register.

The master waits for a read of the SR1 register followed by a write in the DR register, **holding the SCL line low** (see [Figure 63: Transfer sequencing](#) EV8).

When the acknowledge bit is received, the interface sets the EVF and BTF bits with an interrupt if the ITE bit is set.

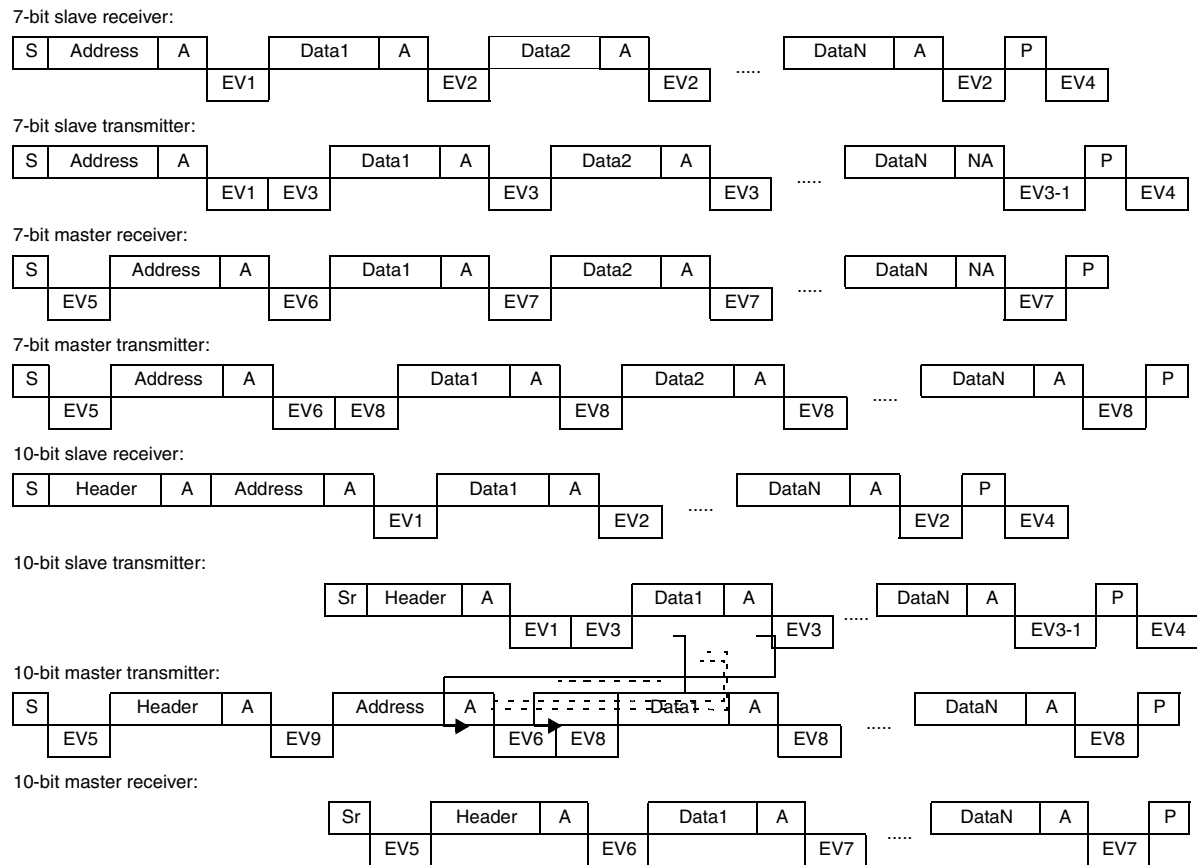
To close the communication: After writing the last byte to the DR register, set the STOP bit to generate the Stop condition. The interface goes automatically back to slave mode (M/SL bit cleared).

Error cases

- **BERR:** Detection of a stop or a start condition during a byte transfer. In this case, the EVF and BERR bits are set by hardware with an interrupt if ITE is set. Note that BERR will not be set if an error is detected during the first or second pulse of each 9-bit transaction:
 - **Single master mode**
If a start or stop is issued during the first or second pulse of a 9-bit transaction, the BERR flag will not be set and transfer will continue however the BUSY flag will be reset. To work around this, slave devices should issue a NACK when they receive a misplaced start or stop. The reception of a NACK or BUSY by the master in the middle of communication makes it possible to re-initiate transmission.
 - **Multimaster mode**
Normally the BERR bit would be set whenever unauthorized transmission takes place while transfer is already in progress. However, an issue will arise if an external master generates an unauthorized start or stop while the I²C master is on the first or second pulse of a 9-bit transaction. It is possible to work around this by polling the BUSY bit during I²C master mode transmission. The resetting of the BUSY bit can then be handled in a similar manner as the BERR flag being set.
- **AF:** Detection of a non-acknowledge bit. In this case, the EVF and AF bits are set by hardware with an interrupt if the ITE bit is set. To resume, set the start or stop bit. The AF bit is cleared by reading the I²CSR2 register. However, if read before the completion of the transmission, the AF flag will be set again, thus possibly generating a new interrupt. Software must ensure either that the SCL line is back at 0 before reading the SR2 register, or be able to correctly handle a second interrupt during the 9th pulse of a transmitted byte.
- **ARLO:** Detection of an arbitration lost condition. In this case the ARLO bit is set by hardware (with an interrupt if the ITE bit is set and the interface goes automatically back to slave mode (the M/SL bit is cleared).

Note: In all the above cases, the SCL line is not held low. However, the SDA line can remain low due to possible '0' bits transmitted last. It is then necessary to release both lines by software.

Figure 63. Transfer sequencing

**Legend:**

S = Start, Sr = Repeated start, P = Stop, A = Acknowledge, NA = Non-acknowledge, EVx = Event (with interrupt if ITE = 1)

EV1: EVF = 1, ADSL = 1, cleared by reading SR1 register

EV2: EVF = 1, BTF = 1, cleared by reading SR1 register followed by reading DR register

EV3: EVF = 1, BTF = 1, cleared by reading SR1 register followed by writing DR register.

EV3-1: EVF = 1, AF = 1, BTF = 1; AF is cleared by reading SR1 register. BTF is cleared by releasing the lines (STOP = 1, STOP = 0) or by writing DR register (DR = FFh). **Note:** If lines are released by STOP = 1, STOP = 0, the subsequent EV4 is not seen

EV4: EVF = 1, STOPF = 1, cleared by reading SR2 register

EV5: EVF = 1, SB = 1, cleared by reading SR1 register followed by writing DR register

EV6: EVF = 1, cleared by reading SR1 register followed by writing CR register (for example PE = 1)

EV7: EVF = 1, BTF = 1, cleared by reading SR1 register followed by reading DR register

EV8: EVF = 1, BTF = 1, cleared by reading SR1 register followed by writing DR register

EV9: EVF = 1, ADD10 = 1, cleared by reading SR1 register followed by writing DR register

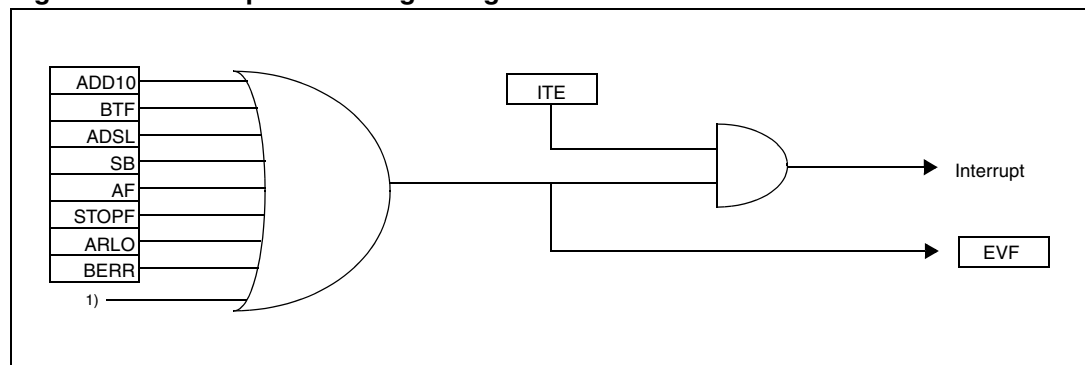
10.7.5 Low power modes

Table 65. Effect of low power modes on I²C

Mode	Effect
Wait	No effect on I ² C interface. I ² C interrupts cause the device to exit from wait mode.
Halt	I ² C registers are frozen. In halt mode, the I ² C interface is inactive and does not acknowledge data on the bus. The I ² C interface resumes operation when the MCU is woken up by an interrupt with 'exit from halt mode' capability.

10.7.6 Interrupts

Figure 64. Interrupt control logic diagram



1. EVF can also be set by EV6 or an error from the SR2 register.

Table 66. I²C interrupt control/wake-up capability

Interrupt event	Event flag	Enable control bit	Exit from wait	Exit from halt
10-bit address sent event (master mode)	ADD10	ITE	Yes	No
End of byte transfer event	BTF			
Address matched event (slave mode)	ADSEL			
Start bit generation event (master mode)	SB			
Acknowledge failure event	AF			
Stop detection event (slave mode)	STOPF			
Arbitration lost event (multimaster configuration)	ARLO			
Bus error event	BERR			

Note: The I²C interrupt events are connected to the same interrupt vector (see [Chapter 7: Interrupts](#)). They generate an interrupt if the corresponding enable control bit is set and the I-bit in the CC register is reset (RIM instruction).

10.7.7 Register description

I²C control register (CR)

CR							Reset value: 0000 0000 (00h)
7	6	5	4	3	2	1	0
Reserved		PE	ENG C	START	ACK	STOP	ITE
-		R/W	R/W	R/W	R/W	R/W	R/W

Table 67. CR register description

Bit	Name	Function
7:6	-	Reserved, forced to 0 by hardware.
5	PE	<p>Peripheral enable</p> <p>This bit is set and cleared by software.</p> <p>0: Peripheral disabled</p> <p>1: Master/slave capability</p> <p><i>Note 1: When PE = 0, all the bits of the CR register and the SR register except the STOP bit are reset. All outputs are released while PE = 0</i></p> <p><i>Note 2: When PE = 1, the corresponding I/O pins are selected by hardware as alternate functions.</i></p> <p><i>Note 3: To enable the I²C interface, write the CR register TWICE with PE = 1 as the first write only activates the interface (only PE is set).</i></p>
4	ENG C	<p>Enable general call</p> <p>This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE = 0). The 00h general call address is acknowledged (01h ignored).</p> <p>0: General call disabled</p> <p>1: General call enabled</p> <p><i>Note: In accordance with the I²C standard, when GCAL addressing is enabled, an I²C slave can only receive data. It will not transmit data to the master.</i></p>
3	START	<p>Generation of a start condition</p> <p>This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE = 0) or when the start condition is sent (with interrupt generation if ITE = 1).</p> <p>In master mode</p> <p>0: No start generation</p> <p>1: Repeated start generation</p> <p>In slave mode</p> <p>0: No start generation</p> <p>1: Start generation when the bus is free</p>
2	ACK	<p>Acknowledge enable</p> <p>This bit is set and cleared by software. It is also cleared by hardware when the interface is disabled (PE = 0).</p> <p>0: No acknowledge returned</p> <p>1: Acknowledge returned after an address byte or a data byte is received</p>

Table 67. CR register description (continued)

Bit	Name	Function
1	STOP	<p>Generation of a stop condition</p> <p>This bit is set and cleared by software. It is also cleared by hardware in master mode.</p> <p><i>Note: This bit is not cleared when the interface is disabled (PE = 0).</i></p> <p>In master mode</p> <p>0: No stop generation</p> <p>1: Stop generation after the current byte transfer or after the current start condition is sent. The STOP bit is cleared by hardware when the stop condition is sent.</p> <p>In slave mode</p> <p>0: No stop generation</p> <p>1: Release the SCL and SDA lines after the current byte transfer (BTF = 1). In this mode the STOP bit has to be cleared by software.</p>
0	ITE	<p>Interrupt enable</p> <p>This bit is set and cleared by software and cleared by hardware when the interface is disabled (PE = 0).</p> <p>0: Interrupts disabled</p> <p>1: Interrupts enabled</p> <p>Refer to Figure 64: Interrupt control logic diagram on page 150 and Table 66: I2C interrupt control/wake-up capability on page 150 for the relationship between the events and the interrupt. SCL is held low when the ADD10, SB, BTF or ADSL flags or an EV6 event (see Figure 63: Transfer sequencing on page 149) is detected.</p>

I²C status register 1 (SR1)

SR1				Reset value: 0000 0000 (00h)			
7	6	5	4	3	2	1	0
EVF	ADD10	TRA	BUSY	BTF	ADSL	M/SL	SB
RO	RO	RO	RO	RO	RO	RO	RO

Table 68. SR1 register description

Bit	Name	Function
7	EVF	<p>Event flag</p> <p>This bit is set by hardware as soon as an event occurs. It is cleared by software reading the SR2 register in case of an error event or as described in Figure 63: Transfer sequencing on page 149. It is also cleared by hardware when the interface is disabled (PE = 0).</p> <p>0: No event</p> <p>1: One of the following events has occurred:</p> <p>BTF = 1 (byte received or transmitted)</p> <p>ADSL = 1 (address matched in slave mode while ACK = 1)</p> <p>SB = 1 (start condition generated in Master mode)</p> <p>AF = 1 (no acknowledge received after byte transmission)</p> <p>STOPF = 1 (stop condition detected in slave mode)</p> <p>ARLO = 1 (arbitration lost in master mode)</p> <p>BERR = 1 (bus error, misplaced start or stop condition detected)</p> <p>ADD10 = 1 (master has sent header byte)</p> <p>Address byte successfully transmitted in master mode</p>

Table 68. SR1 register description (continued)

Bit	Name	Function
6	ADD10	<p>10-bit addressing in master mode</p> <p>This bit is set by hardware when the master has sent the first byte in 10-bit address mode. It is cleared by software reading SR2 register followed by a write in the DR register of the second address byte. It is also cleared by hardware when the peripheral is disabled (PE = 0).</p> <p>0: No ADD10 event occurred. 1: Master has sent first address byte (header)</p>
5	TRA	<p>Transmitter/receiver</p> <p>When BTF is set, TRA = 1 if a data byte has been transmitted. It is cleared automatically when BTF is cleared. It is also cleared by hardware after detection of stop condition (STOPF = 1), loss of bus arbitration (ARLO = 1) or when the interface is disabled (PE = 0).</p> <p>0: Data byte received (if BTF = 1) 1: Data byte transmitted</p>
4	BUSY	<p>Bus busy</p> <p>This bit is set by hardware on detection of a start condition and cleared by hardware on detection of a stop condition. It indicates a communication in progress on the bus. The BUSY flag of the I²C SR1 register is cleared if a bus error occurs.</p> <p>0: No communication on the bus 1: Communication ongoing on the bus</p> <p><i>Note: The BUSY flag is NOT updated when the interface is disabled (PE = 0). This can have consequences when operating in multimaster mode: A second active I²C master commencing a transfer with an unset BUSY bit can cause a conflict resulting in lost data. A software workaround consists of checking that the I²C is not busy before enabling the I²C multimaster cell.</i></p>
3	BTF	<p>Byte transfer finished</p> <p>This bit is set by hardware as soon as a byte is correctly received or transmitted with interrupt generation if ITE = 1. It is cleared by software reading SR1 register followed by a read or write of DR register. It is also cleared by hardware when the interface is disabled (PE = 0). Following a byte transmission, this bit is set after reception of the acknowledge clock pulse. In case an address byte is sent, this bit is set only after the EV6 event (see Figure 63: Transfer sequencing on page 149). BTF is cleared by reading SR1 register followed by writing the next byte in DR register. Following a byte reception, this bit is set after transmission of the acknowledge clock pulse if ACK = 1. BTF is cleared by reading SR1 register followed by reading the byte from DR register.</p> <p>The SCL line is held low while BTF = 1.</p> <p>0: Byte transfer not done 1: Byte transfer succeeded</p>
2	ADSL	<p>Address matched (slave mode)</p> <p>This bit is set by hardware as soon as the received slave address matched with the OAR register content or a general call is recognized. An interrupt is generated if ITE = 1. It is cleared by software reading SR1 register or by hardware when the interface is disabled (PE = 0). The SCL line is held low while ADSL = 1.</p> <p>0: Address mismatched or not received 1: Received address matched</p>

Table 68. SR1 register description (continued)

Bit	Name	Function
1	M/SL	Master/slave This bit is set by hardware as soon as the interface is in master mode (writing START = 1). It is cleared by hardware after detecting a stop condition on the bus or a loss of arbitration (ARLO = 1). It is also cleared when the interface is disabled (PE = 0). 0: Slave mode 1: Master mode
0	SB	Start bit (master mode) This bit is set by hardware as soon as the start condition is generated (following a write START = 1). An interrupt is generated if ITE = 1. It is cleared by software reading SR1 register followed by writing the address byte in DR register. It is also cleared by hardware when the interface is disabled (PE = 0). 0: No start condition 1: Start condition generated

I²C status register 2 (SR2)

SR2

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved			AF	STOPF	ARLO	BERR	GCAL
-			RO	RO	RO	RO	RO

Table 69. SR2 register description

Bit	Name	Function
7:5	-	Reserved, forced to 0 by hardware
4	AF	Acknowledge failure This bit is set by hardware when no acknowledge is returned. An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0). The SCL line is not held low while AF = 1 but by other flags (SB or BTF) that are set at the same time. 0: No acknowledge failure 1: Acknowledge failure <i>Note: When an AF event occurs, the SCL line is not held low; however, the SDA line can remain low if the last bits transmitted are all 0. It is then necessary to release both lines by software.</i>
3	STOPF	Stop detection (slave mode) This bit is set by hardware when a stop condition is detected on the bus after an acknowledge (if ACK = 1). An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0). The SCL line is not held low while STOPF = 1. 0: No stop condition detected 1: Stop condition detected

Table 69. SR2 register description (continued)

Bit	Name	Function
2	ARLO	<p>Arbitration lost</p> <p>This bit is set by hardware when the interface loses the arbitration of the bus to another master. An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0).</p> <p>After an ARLO event the interface switches back automatically to slave mode (M/SL = 0). The SCL line is not held low while ARLO = 1.</p> <p>0: No arbitration lost detected 1: Arbitration lost detected</p> <p><i>Note: In a multimaster environment, when the interface is configured in master receive mode it does not perform arbitration during the reception of the acknowledge bit. Mishandling of the ARLO bit from the I²C SR2 register may occur when a second master simultaneously requests the same data from the same slave and the I²C master does not acknowledge the data. The ARLO bit is then left at 0 instead of being set.</i></p>
1	BERR	<p>Bus error</p> <p>This bit is set by hardware when the interface detects a misplaced start or stop condition. An interrupt is generated if ITE = 1. It is cleared by software reading SR2 register or by hardware when the interface is disabled (PE = 0). The SCL line is not held low while BERR = 1.</p> <p>0: No misplaced start or stop condition 1: Misplaced start or stop condition</p> <p><i>Note: If a bus error occurs, a stop or a repeated start condition should be generated by the Master to re-synchronize communication, get the transmission acknowledged and the bus released for further communication.</i></p>
0	GCAL	<p>General call (slave mode)</p> <p>This bit is set by hardware when a general call address is detected on the bus while ENGCG = 1. It is cleared by hardware detecting a stop condition (STOPF = 1) or when the interface is disabled (PE = 0).</p> <p>0: No general call address detected on bus 1: General call address detected on bus</p>

I²C clock control register (CCR)

CCR							Reset value: 0000 0000 (00h)
7	6	5	4	3	2	1	0
FM/SM		CC[6:0]					
R/W				R/W			

Table 70. CCR register description

Bit	Name	Function
7	FM/SM	Fast/standard I ² C mode This bit is set and cleared by software. It is not cleared when the interface is disabled (PE = 0). 0: Standard I ² C mode 1: Fast I ² C mode
6:0	CC[6:0]	7-bit clock divider These bits select the speed of the bus (f _{SCL}) depending on the I ² C mode. They are not cleared when the interface is disabled (PE = 0). Refer to Chapter 12: Electrical characteristics for the table of values. <i>Note: The programmed f_{SCL} assumes no load on SCL and SDA lines.</i>

I²C data register (DR)

DR							Reset value: 0000 0000 (00h)
7	6	5	4	3	2	1	0
D[7:0]							
R/W							

Table 71. DR register description

Bit	Name	Function
7:0	D[7:0]	8-bit data register These bits contain the byte to be received or transmitted on the bus. Transmitter mode: Byte transmission starts automatically when the software writes in the DR register. Receiver mode: The first data byte is received automatically in the DR register using the least significant bit of the address. Then, the following data bytes are received one by one after reading the DR register.

I²C own address register (OAR1)

OAR1

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 72. OAR1 register description

Bit	Name	Function	
		7-bit addressing mode	10-bit addressing mode
7:1	ADD[7:1]	Interface address These bits define the I ² C bus address of the interface. They are not cleared when the interface is disabled (PE = 0).	Not applicable
0	ADD0	Address direction bit This bit is 'don't care', the interface acknowledges either 0 or 1. It is not cleared when the interface is disabled (PE = 0). Address 01h is always ignored.	
7:0	ADD[7:0]	Not applicable	Interface address These are the least significant bits of the I ² C bus address of the interface. They are not cleared when the interface is disabled (PE = 0).

I²C own address register (OAR2)

OAR2

Reset value: 0100 0000 (40h)

7	6	5	4	3	2	1	0
FR[1:0]		Reserved			ADD[9:8]		Reserved
R/W		-			R/W		-

Table 73. OAR2 register description

Bit	Name	Function
7:6	FR[1:0]	Frequency bits These bits are set by software only when the interface is disabled (PE = 0). To configure the interface to I ² C specified delays, select the value corresponding to the CPU frequency f_{CPU} . 00: $f_{CPU} < 6$ MHz 01: $f_{CPU} = 6$ to 8 MHz
5:3	-	Reserved
2:1	ADD[9:8]	Interface address These are the most significant bits of the I ² C bus address of the interface (10-bit mode only). They are not cleared when the interface is disabled (PE = 0).
0	-	Reserved

Table 74. I²C register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0018h	I ² CCR Reset value	0	0	PE 0	ENG 0	START 0	ACK 0	STOP 0	ITE 0
0019h	I ² CSR1 Reset value	EVF 0	ADD10 0	TRA 0	BUSY 0	BTF 0	ADSL 0	M/SL 0	SB 0
001Ah	I ² CSR2 Reset value	0	0	0	AF 0	STOPF 0	ARLO 0	BERR 0	GCAL 0
001Bh	I ² CCCR Reset value	FM/SM 0	CC6 0	CC5 0	CC4 0	CC3 0	CC2 0	CC1 0	CC0 0
001Ch	I ² COAR1 Reset value	ADD7 0	ADD6 0	ADD5 0	ADD4 0	ADD3 0	ADD2 0	ADD1 0	ADD0 0
001Dh	I ² COAR2 Reset value	FR1 0	FR0 1	0	0	0	ADD9 0	ADD8 0	0
001Eh	I ² CDR Reset value	MSB 0	0	0	0	0	0	0	LSB 0

10.8 10-bit A/D converter (ADC)

10.8.1 Introduction

The on-chip analog to digital converter (ADC) peripheral is a 10-bit, successive approximation converter with internal sample and hold circuitry. This peripheral has up to 16 multiplexed analog input channels (refer to device pin out description) that allow the peripheral to convert the analog voltage levels from up to 16 different sources.

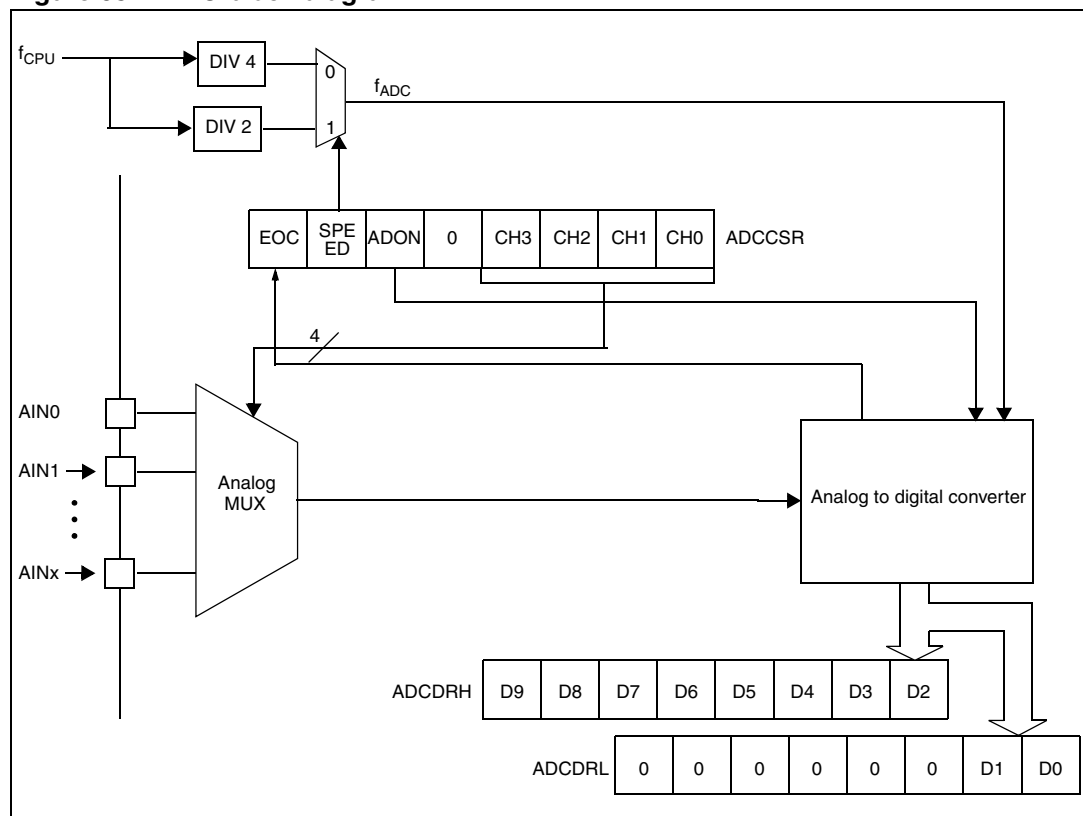
The result of the conversion is stored in a 10-bit data register. The A/D converter is controlled through a control/status register.

10.8.2 Main features

- 10-bit conversion
- Up to 16 channels with multiplexed input
- Linear successive approximation
- Data register (DR) which contains the results
- Conversion complete status flag
- On/off bit (to reduce consumption)

The block diagram is shown in [Figure 65: ADC block diagram on page 159](#).

Figure 65. ADC block diagram



10.8.3 Functional description

The conversion is monotonic, meaning that the result never decreases if the analog input does not decrease and never increases if the analog input does not increase.

If the input voltage (V_{AIN}) is greater than V_{AREF} (high-level voltage reference) then the conversion result is FFh in the ADCDRH register and 03h in the ADCDRL register (without overflow indication).

If the input voltage (V_{AIN}) is lower than V_{SSA} (low-level voltage reference) then the conversion result in the ADCDRH and ADCDRL registers is 00 00h.

The A/D converter is linear and the digital result of the conversion is stored in the ADCDRH and ADCDRL registers. The accuracy of the conversion is described in [Section 12: Electrical characteristics on page 173](#).

R_{AIN} is the maximum recommended impedance for an analog input signal. If the impedance is too high, this results in a loss of accuracy due to leakage and sampling not being completed in the allotted time.

A/D converter configuration

The analog input ports must be configured as input, no pull-up, no interrupt. Refer to [Section 9: I/O ports on page 56](#). Using these pins as analog inputs does not affect the ability of the port to be read as a logic input.

In the ADCCSR register select the CS[3:0] bits to assign the analog channel to convert.

Starting the conversion

In the ADCCSR register set the ADON bit to enable the A/D converter and to start the conversion. From this time on, the ADC performs a continuous conversion of the selected channel.

When a conversion is complete:

- The EOC bit is set by hardware
- The result is in the ADCDR register

A read to the ADCDRH or a write to any bit of the ADCCSR register resets the EOC bit.

To read the 10 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRL register
3. Read the ADCDRH register. This clears EOC automatically

Note: The data is not latched, so both the low and the high data register must be read before the next conversion is complete, so it is recommended to disable interrupts while reading the conversion result.

To read only 8 bits, perform the following steps:

1. Poll the EOC bit
2. Read the ADCDRH register. This clears EOC automatically

Changing the conversion channel

The application can change channels during conversion. When software modifies the CH[3:0] bits in the ADCCSR register, the current conversion is stopped, the EOC bit is cleared, and the A/D converter starts converting the newly selected channel.

10.8.4 Low power modes

Note: The A/D converter may be disabled by resetting the ADON bit. This feature allows reduced power consumption when no conversion is needed.

Table 75. Effect of low power modes on 10-bit ADC

Mode	Description
Wait	No effect on A/D converter
Halt	A/D converter disabled. After wake-up from halt mode, the A/D converter requires a stabilization time t_{STAB} (see Section 12: Electrical characteristics on page 173) before accurate conversions can be performed.

10.8.5 Interrupts

None.

10.8.6 10-bit ADC registers

Control/status register (ADCCSR)

ADCCSR					Reset value: 0000 0000 (00h)		
7	6	5	4	3	2	1	0
EOC	SPEED	ADON	Reserved	CH[3:0]			
RO	R/W	R/W	-	R/W			

Table 76. ADCCSR register description

Bit	Bit name	Function
7	EOC	End of conversion This bit is set by hardware. It is cleared by hardware when software reads the ADCDRH register or writes to any bit of the ADCCSR register. 0: Conversion is not complete 1: Conversion complete
6	SPEED	ADC clock selection This bit is set and cleared by software. 0: $f_{\text{ADC}} = f_{\text{CPU}}/4$ 1: $f_{\text{ADC}} = f_{\text{CPU}}/2$
5	ADON	A/D converter on This bit is set and cleared by software. 0: Disable ADC and stop conversion 1: Enable ADC and start conversion

Table 76. ADCCSR register description (continued)

Bit	Bit name	Function
4	-	Reserved, must be kept cleared.
3:0	CH[3:0]	<p>Channel selection</p> <p>These bits are set and cleared by software. They select the analog input to convert:</p> <p>0000: channel pin = AIN0 0001: channel pin = AIN1 0010: channel pin = AIN2 0011: channel pin = AIN3 0100: channel pin = AIN4 0101: channel pin = AIN5 0110: channel pin = AIN6 0111: channel pin = AIN7 1000: channel pin = AIN8 1001: channel pin = AIN9 1010: channel pin = AIN10 1011: channel pin = AIN11 1100: channel pin = AIN12 1101: channel pin = AIN13 1110: channel pin = AIN14 1111: channel pin = AIN15</p> <p><i>Note: The number of channels is device dependent. Refer to Section 2: Package pinout and pin description on page 15.</i></p>

Data register (ADCDRH)

ADCDRH							Reset value: 0000 0000 (00h)
7	6	5	4	3	2	1	0
D[9:2]							
RO							

Table 77. ADCDRH register description

Bit	Bit name	Function
7:0	D[9:2]	MSB of converted analog value

Data register (ADCDRL)

ADCDRL

Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
Reserved						D[1:0]	
-						RO	

Table 78. ADCDRL register description

Bit	Bit name	Function
7:2	-	Reserved, must be kept cleared
1:0	D[1:0]	LSB of converted analog value

ADC register map and reset value**Table 79. ADC register map and reset values**

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0070h	ADCCSR Reset value	EOC 0	SPEED 0	ADON 0		CH3 0	CH2 0	CH1 0	CH0 0
0071h	ADCDRH Reset value	D9 0	D8 0	D7 0	D6 0	D5 0	D4 0	D3 0	D2 0
0072h	ADCDRL Reset value	0	0	0	0	0	0	D1 0	D0 0

11 Instruction set

11.1 CPU addressing modes

The CPU features 17 different addressing modes which can be classified in 7 main groups (see [Table 80](#)).

Table 80. CPU addressing mode groups

Addressing mode	Example
Inherent	nop
Immediate	ld A,#\$55
Direct	ld A,\$55
Indexed	ld A,(\$55,X)
Indirect	ld A,([\$55],X)
Relative	jrne loop
Bit operation	bset byte,#5

The CPU instruction set is designed to minimize the number of bytes required per instruction. To do so, most of the addressing modes may be subdivided in two sub-modes called long and short:

- Long addressing mode is more powerful because it can use the full 64 Kbyte address space, however it uses more bytes and more CPU cycles.
- Short addressing mode is less powerful because it can generally only access page zero (0000h - 00FFh range), but the instruction size is more compact, and faster. All memory to memory instructions use short addressing modes only (CLR, CPL, NEG, BSET, BRES, BTJT, BTJF, INC, DEC, RLC, RRC, SLL, SRL, SRA, SWAP)

The ST7 assembler optimizes the use of long and short addressing modes.

Table 81. CPU addressing mode overview

Mode			Syntax	Destination	Pointer address	Pointer size	Length (bytes)
Inherent			nop				+ 0
Immediate			ld A,#\$55				+ 1
Short	Direct		ld A,\$10	00..FF			+ 1
Long	Direct		ld A,\$1000	0000..FFFF			+ 2
No offset	Direct	Indexed	ld A,(X)	00..FF			+ 0
Short	Direct	Indexed	ld A,(\$10,X)	00..1FE			+ 1
Long	Direct	Indexed	ld A,(\$1000,X)	0000..FFFF			+ 2
Short	Indirect		ld A,[\$10]	00..FF	00..FF	byte	+ 2
Long	Indirect		ld A,[\$10.w]	0000..FFFF	00..FF	word	+ 2
Short	Indirect	Indexed	ld A,([\$10],X)	00..1FE	00..FF	byte	+ 2
Long	Indirect	Indexed	ld A,([\$10.w],X)	0000..FFFF	00..FF	word	+ 2
Relative	Direct		jrne loop	PC+/-127			+ 1
Relative	Indirect		jrne [\$10]	PC+/-127	00..FF	byte	+ 2
Bit	Direct		bset \$10,#7	00..FF			+ 1
Bit	Indirect		bset [\$10],#7	00..FF	00..FF	byte	+ 2
Bit	Direct	Relative	btjt \$10,#7,skip	00..FF			+ 2
Bit	Indirect	Relative	btjt [\$10],#7,skip	00..FF	00..FF	byte	+ 3

11.1.1 Inherent instructions

All inherent instructions consist of a single byte. The opcode fully specifies all the required information for the CPU to process the operation.

Table 82. Inherent instructions

Inherent Instruction	Function
NOP	No operation
TRAP	S/W interrupt
WFI	Wait for interrupt (low power mode)
HALT	Halt oscillator (lowest power mode)
RET	Sub-routine return
IRET	Interrupt sub-routine return
SIM	Set interrupt mask (level 3)
RIM	Reset interrupt mask (level 0)
SCF	Set carry flag
RCF	Reset carry flag
RSP	Reset stack pointer
LD	Load
CLR	Clear
PUSH/POP	Push/pop to/from the stack
INC/DEC	Increment/decrement
TNZ	Test negative or zero
CPL, NEG	1 or 2 complement
MUL	Byte multiplication
SLL, SRL, SRA, RLC, RRC	Shift and rotate operations
SWAP	Swap nibbles

11.1.2 Immediate instructions

Immediate instructions have two bytes, the first byte contains the opcode, the second byte contains the operand value.

Table 83. Immediate instructions

Immediate Instruction	Function
LD	Load
CP	Compare
BCP	Bit compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic operations

11.1.3 Direct instructions

In direct instructions, the operands are referenced by their memory address.

The direct addressing mode consists of two sub-modes:

- Direct instructions (short)
The address is a byte, thus requiring only one byte after the opcode, but only allows 00 - FF addressing space.
- Direct instructions (long)
The address is a word, thus allowing 64 Kbyte addressing space, but requires 2 bytes after the opcode.

11.1.4 Indexed instructions (no offset, short, long)

In this mode, the operand is referenced by its memory address, which is defined by the unsigned addition of an index register (X or Y) with an offset.

The indexed addressing mode consists of three sub-modes:

- Indexed (no offset)
There is no offset (no extra byte after the opcode), and allows 00 - FF addressing space.
- Indexed (short)
The offset is a byte, thus requires only one byte after the opcode and allows 00 - 1FE addressing space.
- Indexed (long)
The offset is a word, thus allowing 64 Kbyte addressing space and requires 2 bytes after the opcode.

11.1.5 Indirect instructions (short, long)

The required data byte to do the operation is found by its memory address, located in memory (pointer).

The pointer address follows the opcode. The indirect addressing mode consists of two sub-modes:

- Indirect (short)
The pointer address is a byte, the pointer size is a byte, thus allowing 00 - FF addressing space, and requires 1 byte after the opcode.
- Indirect (long)
The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

11.1.6 Indirect indexed instructions (short, long)

This is a combination of indirect and short indexed addressing modes. The operand is referenced by its memory address, which is defined by the unsigned addition of an index register value (X or Y) with a pointer value located in memory. The pointer address follows the opcode.

The indirect indexed addressing mode consists of two sub-modes:

- Indirect indexed (short)
The pointer address is a byte, the pointer size is a byte, thus allowing 00 - 1FE addressing space, and requires 1 byte after the opcode.
- Indirect indexed (long)
The pointer address is a byte, the pointer size is a word, thus allowing 64 Kbyte addressing space, and requires 1 byte after the opcode.

Table 84. Instructions supporting direct, indexed, indirect and indirect indexed addressing modes

Long and short instructions	Function
LD	Load
CP	Compare
AND, OR, XOR	Logical operations
ADC, ADD, SUB, SBC	Arithmetic addition/subtraction operations
BCP	Bit compare

Table 85. Short instructions and functions

Short instructions only	Function
CLR	Clear
INC, DEC	Increment/decrement
TNZ	Test negative or zero
CPL, NEG	1 or 2 complement
BSET, BRES	Bit operations
BTJT, BTJF	Bit test and jump operations
SLL, SRL, SRA, RLC, RRC	Shift and rotate operations
SWAP	Swap nibbles
CALL, JP	Call or jump subroutine

11.1.7 Relative mode instructions (direct, indirect)

This addressing mode is used to modify the PC register value, by adding an 8-bit signed offset to it.

Table 86. Relative mode instructions (direct and indirect)

Available relative direct/indirect instructions	Function
JRxx	Conditional jump
CALLR	Call relative

The relative addressing mode consists of two sub-modes:

- Relative (direct)
The offset follows the opcode.
- Relative (indirect)
The offset is defined in memory, which address follows the opcode.

11.2 Instruction groups

The ST7 family devices use an instruction set consisting of 63 instructions. The instructions may be subdivided into 13 main groups as illustrated in the following table:

Table 87. Instruction groups

Group	Instructions							
Load and transfer	LD	CLR						
Stack operation	PUSH	POP	RSP					
Increment/decrement	INC	DEC						
Compare and tests	CP	TNZ	BCP					
Logical operations	AND	OR	XOR	CPL	NEG			
Bit operation	BSET	BRES						
Conditional bit test and branch	BTJT	BTJF						
Arithmetic operations	ADC	ADD	SUB	SBC	MUL			
Shift and rotates	SLL	SRL	SRA	RLC	RRC	SWAP	SLA	
Unconditional jump or call	JRA	JRT	JRF	JP	CALL	CALLR	NOP	RET
Conditional branch	JRxx							
Interruption management	TRAP	WFI	HALT	IRET				
Condition code flag modification	SIM	RIM	SCF	RCF				

11.3 Using a prebyte

The instructions are described with one to four opcodes.

In order to extend the number of available opcodes for an 8-bit CPU (256 opcodes), three different prebyte opcodes are defined. These prebytes modify the meaning of the instruction they precede.

The whole instruction becomes:

PC-2	End of previous instruction
PC-1	Prebyte
PC	Opcode
PC+1	Additional word (0 to 2) according to the number of bytes required to compute the effective address

These prebytes enable instructions in Y as well as indirect addressing modes to be implemented. They precede the opcode of the instructions in X or the instructions using direct addressing mode. The prebytes are:

PDY 90	Replace an X based instruction using immediate, direct, indexed, or inherent addressing mode by a Y one
PIX 92	Replace an instruction using direct, direct bit, or direct relative addressing mode to an instruction using the corresponding indirect addressing mode It also changes an instruction using X indexed addressing mode to an instruction using indirect X indexed addressing mode
PIY 91	Replace an instruction using X indirect indexed addressing mode by a Y one

Table 88. Instruction set overview

Mnemo	Description	Function/example	Dst	Src	I1	H	I0	N	Z	C
ADC	Add with carry	$A = A + M + C$	A	M		H		N	Z	C
ADD	Addition	$A = A + M$	A	M		H		N	Z	C
AND	Logical And	$A = A \cdot M$	A	M				N	Z	
BCP	Bit compare A, memory	tst (A . M)	A	M				N	Z	
BRES	Bit reset	bres byte, #3	M							
BSET	Bit set	bset byte, #3	M							
BTJF	Jump if bit is false (0)	btjf byte, #3, Jmp1	M							C
BTJT	Jump if bit is true (1)	btjt byte, #3, Jmp1	M							C
CALL	Call subroutine									
CALLR	Call subroutine relative									
CLR	Clear		reg, M					0	1	
CP	Arithmetic compare	tst(reg - M)	reg	M				N	Z	C
CPL	One complement	$A = FFH - A$	reg, M					N	Z	1
DEC	Decrement	dec Y	reg, M					N	Z	
HALT	Halt				1		0			
IRET	Interrupt routine return	pop CC, A, X, PC			I1	H	I0	N	Z	C
INC	Increment	inc X	reg, M					N	Z	
JP	Absolute jump	jp [TBL.w]								
JRA	Jump relative always									
JRT	Jump relative									
JRF	Never jump	jrf *								
JRIH	Jump if ext. INT pin = 1	(ext. INT pin high)								
JRIL	Jump if ext. INT pin = 0	(ext. INT pin low)								
JRH	Jump if H = 1	H = 1 ?								
JRNH	Jump if H = 0	H = 0 ?								
JRM	Jump if I1:0 = 11	I1:0 = 11 ?								
JRNM	Jump if I1:0 <> 11	I1:0 <> 11 ?								
JRMI	Jump if N = 1 (minus)	N = 1 ?								
JRPL	Jump if N = 0 (plus)	N = 0 ?								
JREQ	Jump if Z = 1 (equal)	Z = 1 ?								
JRNE	Jump if Z = 0 (not equal)	Z = 0 ?								
JRC	Jump if C = 1	C = 1 ?								
JRNC	Jump if C = 0	C = 0 ?								
JRULT	Jump if C = 1	Unsigned <								
JRUGE	Jump if C = 0	Jmp if unsigned >=								

Table 88. Instruction set overview (continued)

Mnemo	Description	Function/example	Dst	Src	I1	H	I0	N	Z	C
JRUGT	Jump if (C + Z = 0)	Unsigned >								
JRULE	Jump if (C + Z = 1)	Unsigned <=								
LD	Load	dst <= src	reg, M	M, reg				N	Z	
MUL	Multiply	X, A = X * A	A, X, Y	X, Y, A		0				0
NEG	Negate (2's compl)	neg \$10	reg, M					N	Z	C
NOP	No operation									
OR	OR operation	A = A + M	A	M				N	Z	
POP	Pop from the stack	pop reg	reg	M						
		pop CC	CC	M	I1	H	I0	N	Z	C
PUSH	Push onto the stack	push Y	M	reg, CC						
RCF	Reset carry flag	C = 0								0
RET	Subroutine return									
RIM	Enable interrupts	I1:0 = 10 (level 0)			1		0			
RLC	Rotate left true C	C <= A <= C	reg, M					N	Z	C
RRC	Rotate right true C	C => A => C	reg, M					N	Z	C
RSP	Reset stack pointer	S = max allowed								
SBC	Subtract with carry	A = A - M - C	A	M				N	Z	C
SCF	Set carry flag	C = 1								1
SIM	Disable interrupts	I1:0 = 11 (level 3)			1		1			
SLA	Shift left arithmetic	C <= A <= 0	reg, M					N	Z	C
SLL	Shift left logic	C <= A <= 0	reg, M					N	Z	C
SRL	Shift right logic	0 => A => C	reg, M					0	Z	C
SRA	Shift right arithmetic	A7 => A => C	reg, M					N	Z	C
SUB	Subtraction	A = A - M	A	M				N	Z	C
SWAP	SWAP nibbles	A7-A4 <=> A3-A0	reg, M					N	Z	
TNZ	Test for neg and zero	tnz lbl1						N	Z	
TRAP	S/W trap	S/W interrupt			1		1			
WFI	Wait for interrupt				1		0			
XOR	Exclusive OR	A = A XOR M	A	M				N	Z	

12 Electrical characteristics

12.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS} .

12.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25^\circ\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

12.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25^\circ\text{C}$, $V_{DD} = 3.3\text{V}$. They are given only as design guidelines and are not tested.

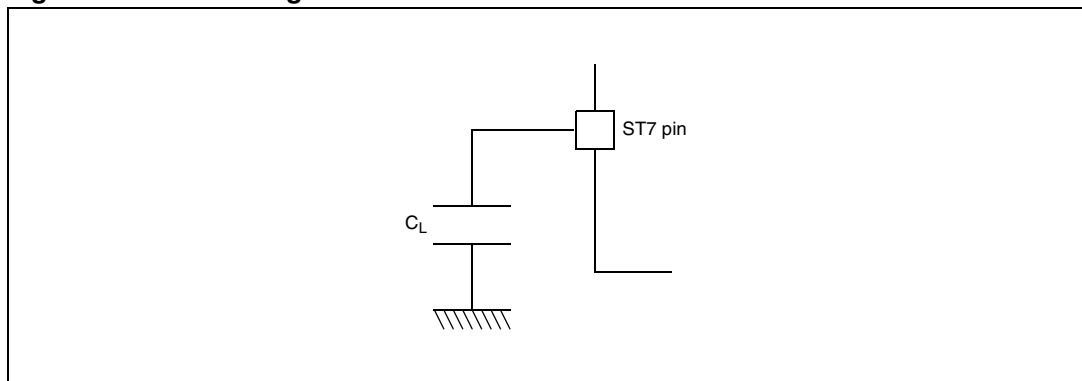
12.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

12.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 66](#).

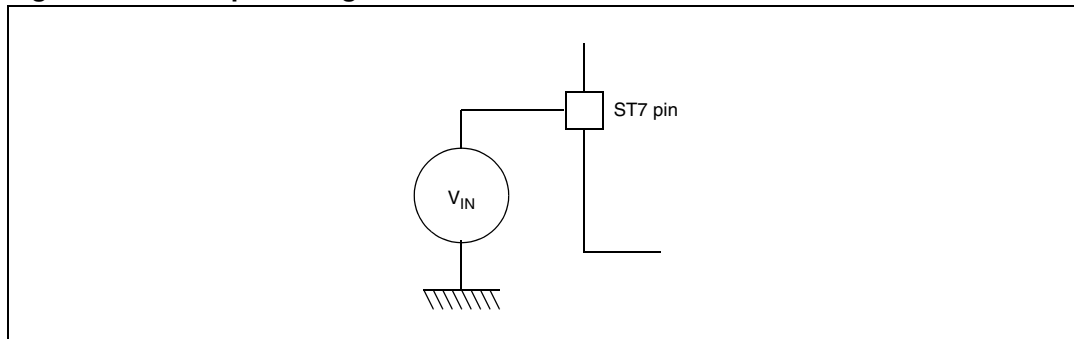
Figure 66. Pin loading conditions



12.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 67](#).

Figure 67. Pin input voltage



12.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.2.1 Voltage characteristics

Table 89. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V _{DD} - V _{SS}	Supply voltage	6.5	V
V _{PP} - V _{SS}	Programming voltage	13	
V _{IN} ⁽¹⁾⁽²⁾	Input voltage on true open drain pin	V _{SS} -0.3 to +6.5	
	Input voltage on any other pin	V _{SS} -0.3 to V _{DD} +0.3	
ΔV _{DDx} and ΔV _{SSx}	Variations between different digital power pins	50	mV
V _{SSA} - V _{SSx}	Variations between digital and analog ground pins	50	
V _{ESD(HBM)}	Electrostatic discharge voltage (human body model)	See Section 12.7.3: Absolute maximum ratings (electrical sensitivity) on page 188	
V _{ESD(MM)}	Electrostatic discharge voltage (machine model)		

1. Directly connecting the \overline{RESET} and I/O pins to V_{DD} or V_{SS} could damage the device if an unintentional internal reset is generated or an unexpected change of the I/O configuration occurs (for example, due to a corrupted program counter). To guarantee safe operation, this connection has to be made through a pull-up or pull-down resistor (typical: 4.7k Ω for \overline{RESET} , 10k Ω for I/Os). For the same reason, unused I/O pins must not be directly tied to V_{DD} or V_{SS} .
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

12.2.2 Current characteristics

Table 90. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD}	Total current into V_{DD} power lines (source) ⁽¹⁾	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink) ⁽¹⁾	150	mA
I_{IO}	Output current sunk by any standard I/O and control pin	20	mA
	Output current sunk by any high sink I/O pin	40	mA
	Output current source by any I/Os and control pin	- 25	mA
$I_{INJ(PIN)}^{(2)(3)}$	Injected current on V_{PP} pin	± 5	mA
	Injected current on \overline{RESET} pin	± 5	mA
	Injected current on OSC1 and OSC2 pins	± 5	mA
	Injected current on any other pin ⁽⁴⁾⁽⁵⁾	± 5	mA
$\Sigma I_{INJ(PIN)}^{(2)}$	Total injected current (sum of all I/O and control pins) ⁽⁴⁾	± 25	mA

1. All power (V_{DD}) and ground (V_{SS}) lines must always be connected to the external supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected
3. Negative injection disturbs the analog performance of the device. See [Note 2](#) in [Table 117: ADC accuracy with VDD = 3.3V on page 204](#).
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.
5. True open drain I/O port pins do not accept positive injection.

12.2.3 Thermal characteristics

Table 91. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (see Section 13.2: Thermal characteristics on page 206)		

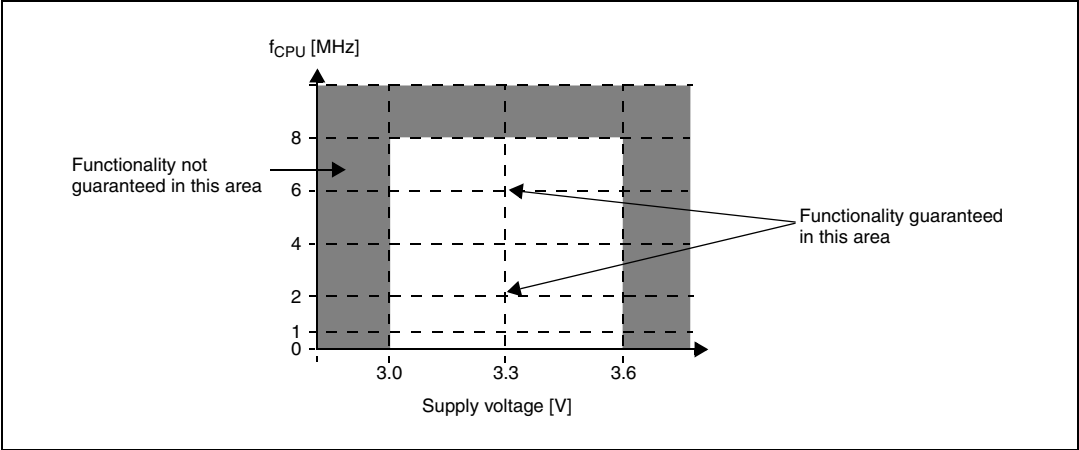
12.3 Operating conditions

Table 92. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f _{CPU}	Internal clock frequency		0	8	MHz
V _{DD}	Operating voltage (except Flash write/erase)		3.0	3.6	V
	Operating voltage for Flash write/erase	V _{PP} = 11.4 to 12.6V			
T _A	Ambient temperature range		-40	85	°C

Warning: Do not connect 12V to V_{PP} before V_{DD} is powered on, as this may damage the device.

Figure 68. f_{CPU} max versus V_{DD}



12.4 Supply current characteristics

The following current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To get the total device consumption, the two current values must be added (except for halt mode for which the clock is stopped).

12.4.1 Current consumption

Table 93. Current consumption

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
I _{DD}	Supply current in run mode ⁽²⁾	f _{OSC} = 2MHz, f _{CPU} = 1MHz f _{OSC} = 4MHz, f _{CPU} = 2MHz f _{OSC} = 8MHz, f _{CPU} = 4MHz f _{OSC} = 16MHz, f _{CPU} = 8MHz	0.65 1.0 1.7 3.1	1.5 2.1 4.2 8	mA
	Supply current in slow mode ⁽²⁾	f _{OSC} = 2MHz, f _{CPU} = 62.5kHz f _{OSC} = 4MHz, f _{CPU} = 125kHz f _{OSC} = 8MHz, f _{CPU} = 250kHz f _{OSC} = 16MHz, f _{CPU} = 500kHz	0.29 0.32 0.4 0.6	0.8 1 1.6 2.5	
	Supply current in wait mode ⁽²⁾	f _{OSC} = 2MHz, f _{CPU} = 1MHz f _{OSC} = 4MHz, f _{CPU} = 2MHz f _{OSC} = 8MHz, f _{CPU} = 4MHz f _{OSC} = 16MHz, f _{CPU} = 8MHz	0.4 0.6 1.0 1.7	1.1 1.5 2 3.5	
	Supply current in slow wait mode ⁽²⁾	f _{OSC} = 2MHz, f _{CPU} = 62.5kHz f _{OSC} = 4MHz, f _{CPU} = 125kHz f _{OSC} = 8MHz, f _{CPU} = 250kHz f _{OSC} = 16MHz, f _{CPU} = 500kHz	250 280 300 420	700 800 1000 1300	μA
	Supply current in halt mode ⁽³⁾	-40°C ≤ T _A ≤ +85°C	<1	10	
	Supply current in active halt mode ⁽⁴⁾	f _{OSC} = 2MHz f _{OSC} = 4MHz f _{OSC} = 8MHz f _{OSC} = 16MHz	220 250 300 350	420 450 500 600	

1. Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
2. Measurements are made in the following conditions:
 - Program executed from RAM, CPU running with RAM access. The increase in consumption when executing from Flash is 50%.
 - All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
 - All peripherals in reset state
 - Clock input (OSC1) driven by external square wave
 - In slow and slow wait mode, f_{CPU} is based on f_{OSC} divided by 32
 To obtain the total current consumption of the device, add the clock source ([Section 12.5.3: Crystal and ceramic resonator oscillators on page 182](#)) and the peripheral power consumption ([Section 12.4.3: On-chip peripherals on page 180](#)).
3. All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load). Data based on characterization results, tested in production at V_{DD} max. and f_{CPU} max.
4. Data based on characterization results, not tested in production. All I/O pins in push-pull 0 mode (when applicable) with a static value at V_{DD} or V_{SS} (no load); clock input (OSC1) driven by external square wave. To obtain the total current consumption of the device, add the clock source consumption ([Section 12.5.3: Crystal and ceramic resonator oscillators on page 182](#)).

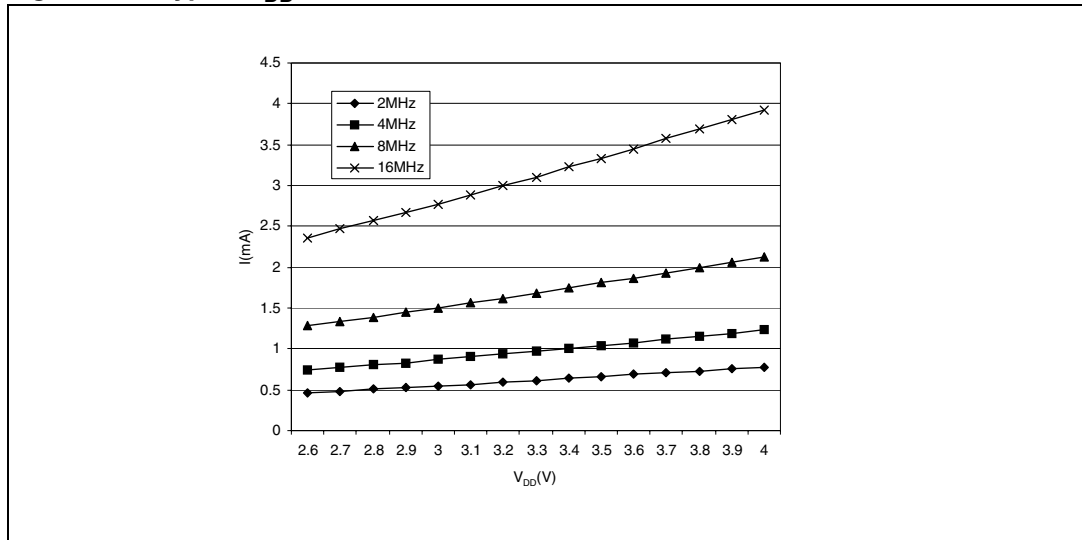
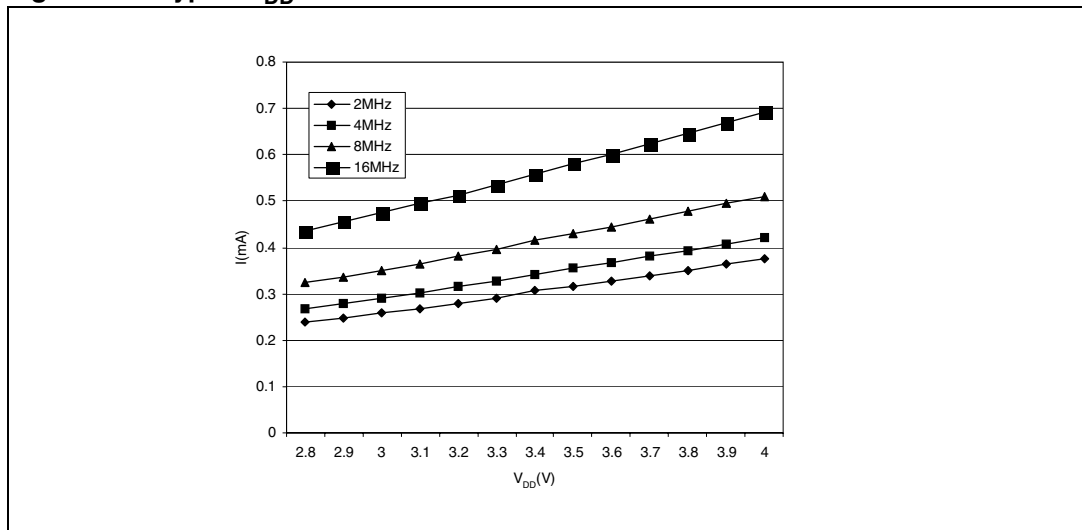
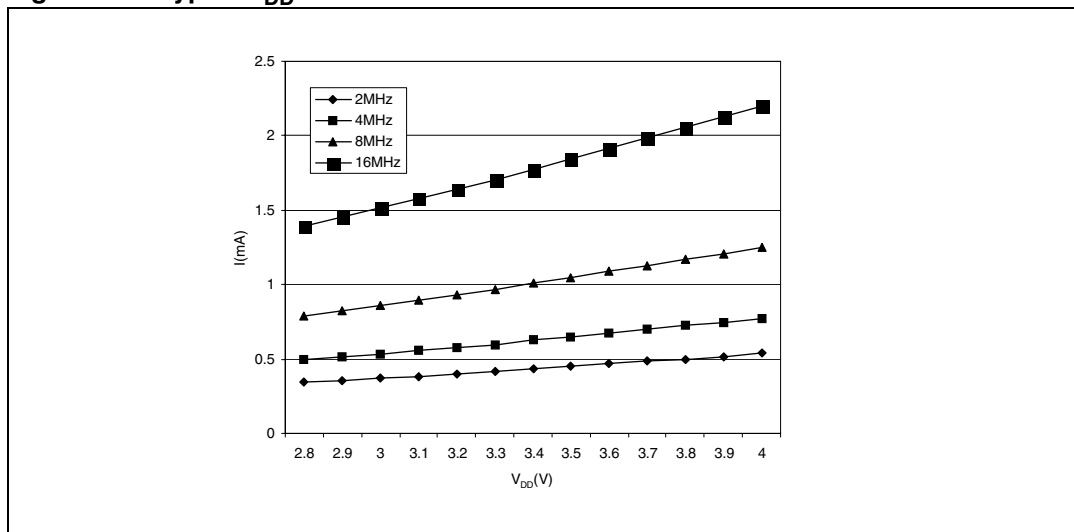
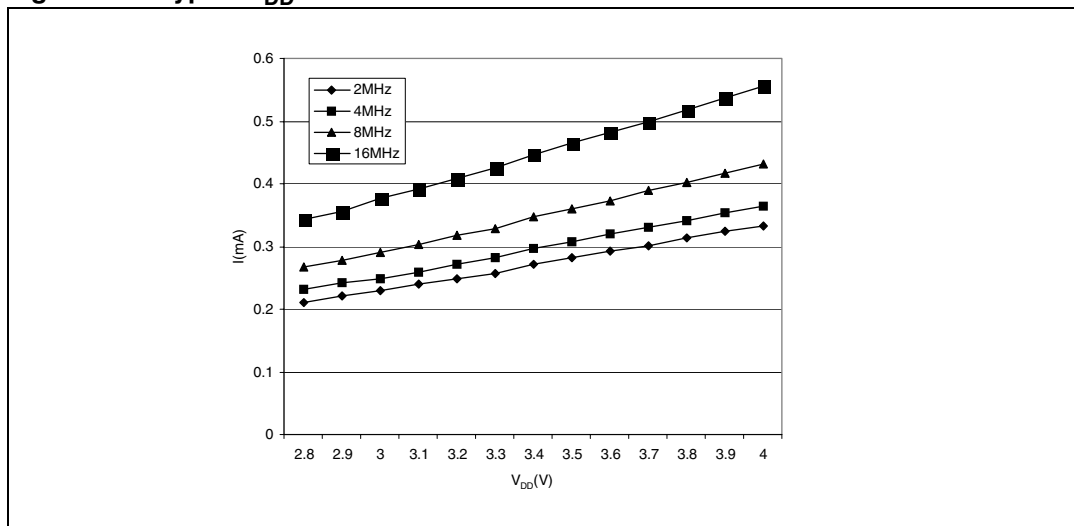
Power consumption vs f_{CPU} **Figure 69. Typical I_{DD} in run mode****Figure 70. Typical I_{DD} in slow mode**

Figure 71. Typical I_{DD} in wait modeFigure 72. Typical I_{DD} in slow wait mode

12.4.2 Supply and clock managers

The previous current consumption specified for the ST7 functional operating modes over temperature range does not take into account the clock source current consumption. To obtain the total device consumption, the two current values must be added (except for halt mode).

Table 94. Oscillators, PLL and LVD current consumption

Symbol	Parameter	Conditions	Typ	Max	Unit
I _{DD(RCIN)}	Supply current of internal RC oscillator		625		μA
I _{DD(RES)}	Supply current of resonator oscillator ⁽¹⁾⁽²⁾		see Section 12.5.3: Crystal and ceramic resonator oscillators on page 182		
I _{DD(PLL)}	PLL supply current	V _{DD} = 3.3V	360		

1. Data based on characterization results done with the external components specified in [Section 12.5.3](#), not tested in production

2. As the oscillator is based on a current source, the consumption does not depend on the voltage.

12.4.3 On-chip peripherals

Table 95. On-chip peripherals

Symbol	Parameter	Conditions	Typ	Unit
$I_{DD(TIM)}$	16-bit timer supply current ⁽¹⁾	$T_A = 25^\circ C, f_{CPU} = 4 \text{ MHz}, V_{DD} = 3.3V$	20	μA
$I_{DD(ART)}$	ART PWM supply current ⁽²⁾		50	μA
$I_{DD(SPI)}$	SPI supply current ⁽³⁾		250	μA
$I_{DD(SCI)}$	SCI supply current ⁽⁴⁾			μA
$I_{DD(I^2C)}$	I ² C supply current ⁽⁵⁾		100	μA
$I_{DD(ADC)}$	ADC supply current when converting ⁽⁶⁾		300	μA

1. Data based on a differential I_{DD} measurement between reset configuration (timer counter running at $f_{CPU}/4$) and timer counter stopped (only TIMD bit set). Data valid for one timer.

2. Data based on a differential I_{DD} measurement between reset configuration (timer stopped) and timer counter enabled (only TCE bit set).

3. Data based on a differential I_{DD} measurement between reset configuration (SPI disabled) and a permanent SPI master communication at maximum speed (data sent equal to 55h). This measurement includes the pad toggling consumption.

4. Data based on a differential I_{DD} measurement between SCI low power state (SCID =1) and a permanent SCI data transmit sequence.

5. Data based on a differential I_{DD} measurement between reset configuration (I²C disabled) and a permanent I²C master communication at 100 kHz (data sent equal to 55h). This measurement includes the pad toggling consumption (27k ohm external pull-up on clock and data lines).

6. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

12.5 Clock and timing characteristics

Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A .

12.5.1 General timings

Table 96. General timings

Symbol	Parameter	Conditions	Min	Typ ⁽¹⁾	Max	Unit
$t_{c(INST)}$	Instruction cycle time		2	3	12	t_{CPU}
		$f_{CPU} = 8\text{MHz}$	250	375	1500	ns
$t_{v(IT)}$	Interrupt reaction time ⁽²⁾ $t_{v(IT)} = \Delta t_{c(INST)} + 10$		10		22	t_{CPU}
		$f_{CPU} = 8\text{MHz}$	1.25		2.75	μs

1. Data based on typical application software

2. Time measured between interrupt event and interrupt vector fetch. $\Delta t_{c(INST)}$ is the number of t_{CPU} cycles needed to finish the current instruction execution.

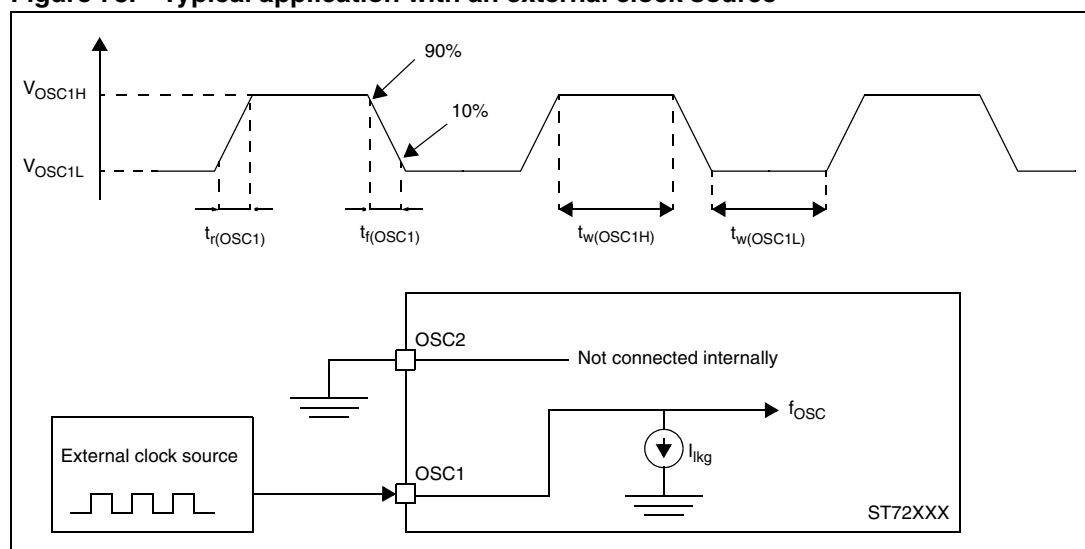
12.5.2 External clock source

Table 97. External clock source

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OSC1H}	OSC1 input pin high level voltage	see Figure 73	$V_{DD} - 1$		V_{DD}	V
V_{OSC1L}	OSC1 input pin low level voltage		V_{SS}		$V_{SS} + 1$	
$t_{w(OSC1H)}$ $t_{w(OSC1L)}$	OSC1 high or low time ⁽¹⁾		5			ns
$t_{r(OSC1)}$ $t_{f(OSC1)}$	OSC1 rise or fall time ⁽¹⁾				15	
I_{lkg}	OSC1 Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 73. Typical application with an external clock source



12.5.3 Crystal and ceramic resonator oscillators

The ST7 internal clock can be supplied with four different crystal/ceramic resonator oscillators. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal/ceramic resonator manufacturer for more details (frequency, package, accuracy...).

Table 98. Oscillator parameters

Symbol	Parameter	Conditions	Min	Max	Unit
f_{OSC}	Oscillator frequency ⁽¹⁾	LP: Low power oscillator MP: Medium power oscillator MS: Medium speed oscillator HS: High speed oscillator	1 >2 >4 >8	2 4 8 16	MHz
R_F	Feedback resistor ⁽²⁾		20	40	k Ω
C_{L1} C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal or ceramic resonator (R_S) ⁽³⁾	$R_S = 200\Omega$ LP oscillator (1-2 MHz) $R_S = 200\Omega$ MP oscillator (2-4 MHz) $R_S = 200\Omega$ MS oscillator (4-8 MHz) $R_S = 100\Omega$ HS oscillator (8-16 MHz)	20 20 15 15	60 50 35 35	pF
i_2	OSC2 driving current	$V_{IN} = V_{SS}$ LP oscillator (1-2 MHz) MP oscillator (2-4 MHz) MS oscillator (4-8 MHz) HS oscillator (8-16 MHz)	80 160 310 610	150 250 460 910	μA

1. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small R_S value. Refer to crystal/ceramic resonator manufacturer for more details.
2. Data based on characterization results, not tested in production. The relatively low value of the R_F resistor offers good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the microcontroller is used in tough humidity conditions.
3. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5pF to 25pF range (typ.) designed for high-frequency applications and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10pF can be used as a rough estimate of the combined pin and board capacitance)

Figure 74. Typical application with a crystal or ceramic resonator

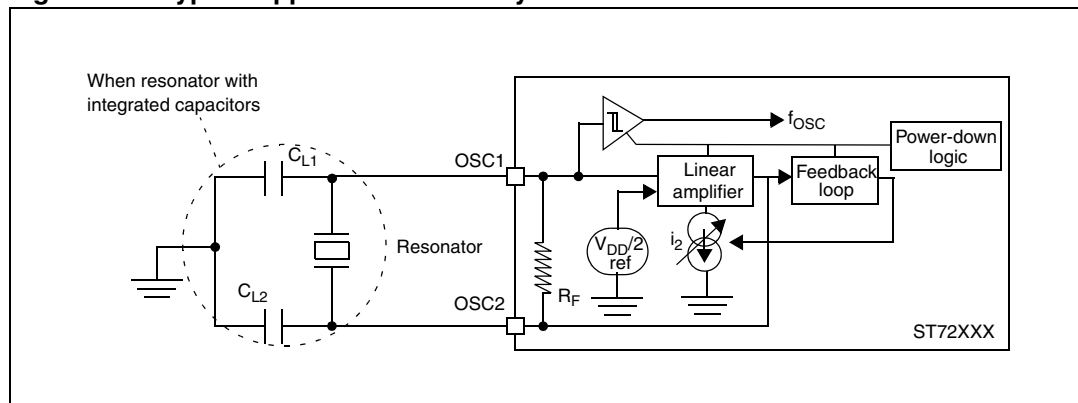


Table 99. Examples of typical resonators⁽¹⁾

Supplier	f _{OSC} (MHz)	Typical ceramic resonators	
		Reference	Recommended OSCRANGE option bit configuration
Murata	2	CSTCC2M00G56A-R0	MP mode ⁽²⁾
	4	CSTCR4M00G55B-R0	MP mode
	8	CSTCE8M00G52A-R0	HS mode
	16	CSTCE16M0V51A-R0	HS mode

1. Resonator characteristics given by the ceramic resonator manufacturer
2. LP mode is not recommended for 2 MHz resonators because the peak to peak amplitude is too small (>0.8V).

12.5.4 RC oscillators

Table 100. RC oscillators

Symbol	Parameter	Conditions ⁽¹⁾	Min	Typ	Max	Unit
f _{OSC(RCINT)}	Internal RC oscillator frequency	T _A = 25°C, V _{DD} = 3.3V	2	3.5	5.6	MHz

1. f_{CPU} = f_{OSC(RCINT)}/2. The PLL must be disabled if the internal RC clock source is used.

12.5.5 PLL characteristics

Table 101. PLL characteristics

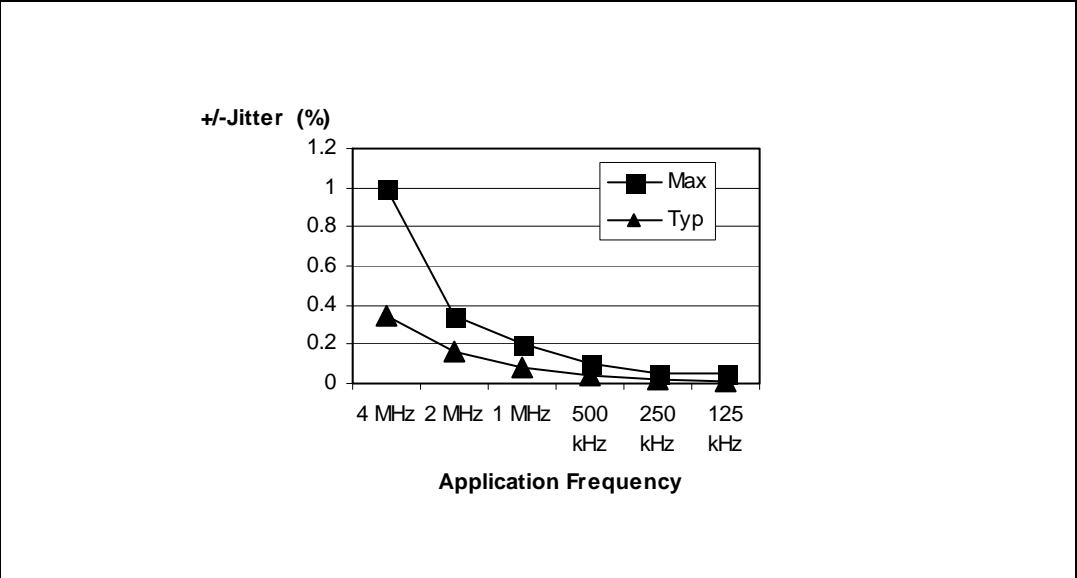
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{OSC}	PLL input frequency range		2		4	MHz
Δ f _{CPU} /f _{CPU}	Instantaneous PLL jitter ⁽¹⁾	f _{OSC} = 4 MHz		0.7	2	%

1. Data characterized but not tested.

The user must take the PLL jitter into account in the application (for example in serial communication or sampling of high frequency signals). The PLL jitter is a periodic effect, which is integrated over several CPU cycles. Therefore the longer the period of the application signal, the less it is impacted by the PLL jitter.

Figure 75: Integrated PLL jitter vs signal frequency on page 184 shows the PLL jitter integrated on application signals in the range 125 kHz to 2 MHz. At frequencies of less than 125 KHz, the jitter is negligible.

Figure 75. Integrated PLL jitter vs signal frequency



1. Measurement conditions: $f_{CPU} = 8\text{MHz}$

12.6 Memory characteristics

12.6.1 RAM and hardware registers

Table 102. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{RM}	Data retention mode ⁽¹⁾	Halt mode (or reset)	1.6			V

1. Minimum V_{DD} supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Not tested in production.

12.6.2 Flash memory

Table 103. Characteristics of dual voltage HDFlash memory

Dual voltage HDFlash memory						
Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
f _{CPU}	Operating frequency	Read mode	0		8	MHz
		Write/erase mode	1		8	
V _{PP}	Programming voltage ⁽²⁾	3V ≤ V _{DD} ≤ 3.6V	11.4		12.6	V
I _{DD}	Supply current ⁽³⁾	Write/erase		<10		μA
I _{PP}	V _{PP} current ⁽³⁾	Read (V _{PP} = 12V)			200	μA
		Write/erase			30	mA
t _{VPP}	Internal V _{PP} stabilization time			10		μs
t _{RET}	Data retention time	T _A = 55°C	20			years
N _{RW}	Write erase cycles	T _A = 85°C	100			cycles
T _{PROG} T _{ERASE}	Programming or erasing temperature range		-40	25	85	°C

1. Data based on characterization results, not tested in production

2. V_{PP} must be applied only during the programming or erasing operation and not permanently for reliability reasons

3. Data based on simulation results, not tested in production

12.7 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

12.7.1 Functional electromagnetic susceptibility (EMS)

Based on a simple running application on the product (toggling two LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- ESD: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000 - 4 - 2 standard.
- FTB: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000 - 4 - 4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the $\overline{\text{RESET}}$ pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 104. Electromagnetic test results

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3V$, $T_A = +25^\circ C$, $f_{OSC} = 8MHz$ Conforms to IEC 1000 - 4 - 2	3B
V_{FFTB}	Fast transient voltage burst limits to be applied through 100pF on V_{DD} and V_{DD} pins to induce a functional disturbance	$V_{DD} = 3.3V$, $T_A = +25^\circ C$, $f_{OSC} = 8MHz$ Conforms to IEC 1000 - 4 - 4	4A

12.7.2 Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling two LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm SAE J 1752/3 which specifies the board and the loading of each pin.

Table 105. EMI emissions

Sym.	Parameter	Conditions	Monitored frequency band	Max vs. [f_{osc}/f_{cpu}]		Unit
				8/4MHz	16/8MHz	
S _{EMI}	Peak level ⁽¹⁾	V _{DD} = 3.3V, T _A = +25°C LQFP44 package Test conforming to SAE J 1752/3	0.1 MHz to 30 MHz	10	10	dBμV
			30 MHz to 130 MHz	16	20	
			130 MHz to 1 GHz	8	12	
			SAE EMI level	2	2.5	-

1. Data based on characterization results, not tested in production.

12.7.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard. For more details, refer to the application note AN1181.

Table 106. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Max value ⁽¹⁾	Unit
V _{ESD(HBM)}	Electrostatic discharge voltage (Human body model)	T _A = +25°C conforming to AEC-Q100-002	H1C	2000	V
V _{ESD(MM)}	Electrostatic discharge voltage (Machine model)	T _A = +25°C conforming to AEC-Q100-003	M2	200	
V _{ESD(CDM)}	Electrostatic discharge voltage (Charged device model)	T _A = +25°C conforming to AEC-Q100-011	C4	1000	

1. Data based on characterization results, not tested in production

Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78 and AEC-Q100/004 IC latch-up standards.

Electrical sensitivities

Table 107. Latch-up results

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T _A = +125°C conforming to JESD 78 and AEC-Q100/004	II level A

12.8 I/O port pin characteristics

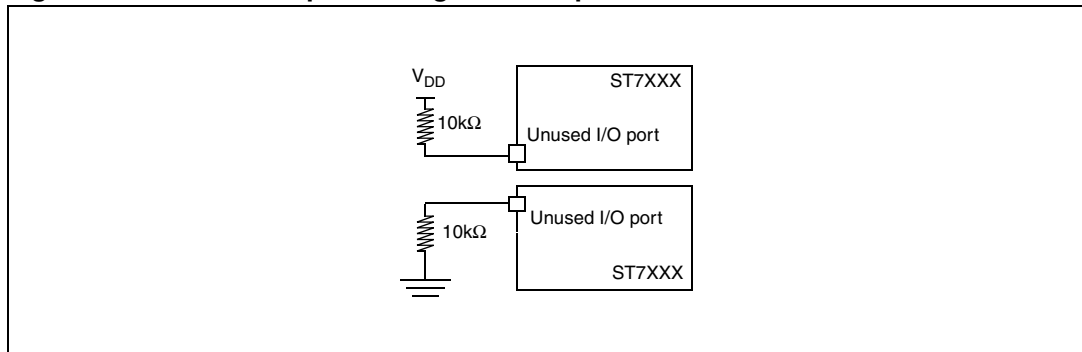
12.8.1 General characteristics

Subject to general operating conditions for V_{DD} , f_{OSC} , and T_A unless otherwise specified.

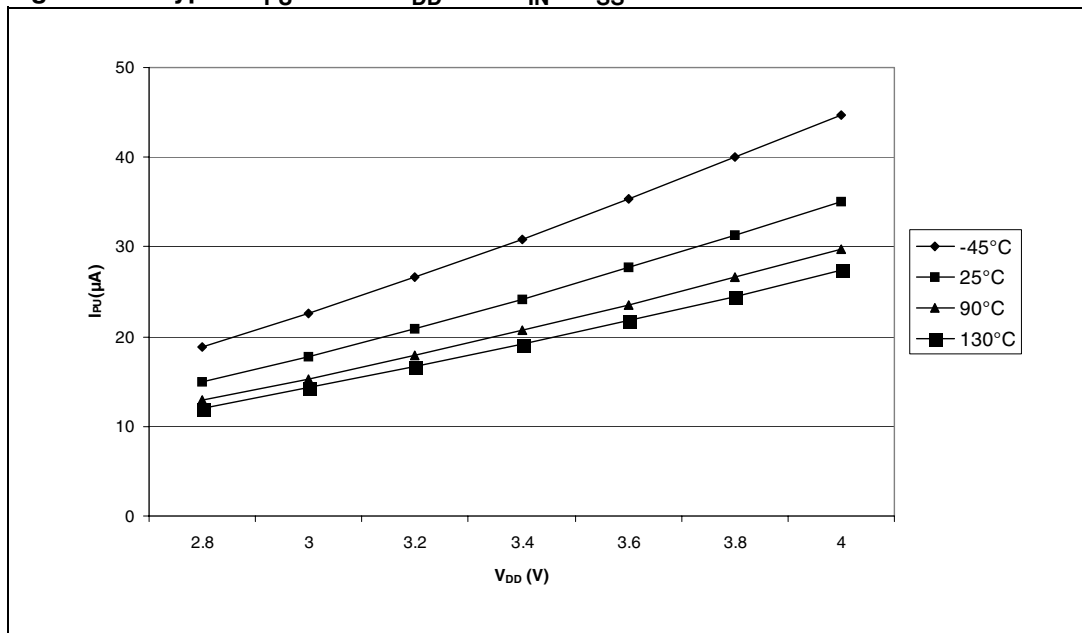
Table 108. I/O general port pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage (standard voltage devices) ⁽¹⁾				$0.3 \times V_{DD}$	V
V_{IH}	Input high level voltage ⁽¹⁾		$0.7 \times V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis ⁽²⁾			0.7		
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on I/O pins				± 4	mA
$\Sigma I_{INJ(PIN)}$ ⁽³⁾	Total injected current (sum of all I/O and control pins)				± 25	
I_{lkg}	Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			± 1	μA
I_S	Static current consumption induced by each floating input pin	Floating input mode ⁽⁴⁾⁽⁵⁾		200		
R_{PU}	Weak pull-up equivalent resistor ⁽⁶⁾	$V_{IN} = V_{SS}$, $V_{DD} = 3.3V$	50	120	250	k Ω
C_{IO}	I/O pin capacitance			5		pF
$t_{f(I/O)out}$	Output high to low level fall time ⁽¹⁾	$C_L = 50pF$ between 10% and 90%		25		ns
$t_{r(I/O)out}$	Output low to high level rise time ⁽¹⁾			25		
$t_{w(IT)in}$	External interrupt pulse time ⁽⁷⁾		1			t_{CPU}

1. Data based on characterization results, not tested in production.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
3. When the current limitation is not possible, the V_{IN} maximum must be respected, otherwise refer to $I_{INJ(PIN)}$ specification. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. Refer to [Section 12.2.2: Current characteristics on page 175](#) for more details.
4. Static peak current value taken at a fixed V_{IN} value, based on design simulation and technology characteristics, not tested in production. This value depends on V_{DD} and temperature values.
5. The Schmitt trigger that is connected to every I/O port is disabled for analog inputs only when ADON bit is ON and the particular ADC channel is selected (with port configured in input floating mode). When the ADON bit is OFF, static current consumption may result. This can be avoided by keeping the input voltage of this pin close to VDD or VSS.
6. The R_{PU} pull-up equivalent resistor is based on a resistive transistor (corresponding I_{PU} current characteristics described in [Figure 77: Typical IPU versus VDD with VIN = VSS on page 190](#)).
7. To generate an external interrupt, a minimum pulse width has to be applied on an I/O port pin configured as an external interrupt source.

Figure 76. Unused I/O pins configured as input

1. I/O can be left unconnected if it is configured as output (0 or 1) by the software. This has the advantage of greater EMC robustness and lower cost.

Figure 77. Typical I_{PU} versus V_{DD} with $V_{IN} = V_{SS}$ 

12.8.2 Output driving current

Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Table 109. Output driving current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for a standard I/O pin when 8 pins are sunk at same time (see Figure 78)	$I_{IO} = +2\text{mA}$		0.25	0.5	V
	Output low level voltage for a high sink I/O pin when 4 pins are sunk at same time (see Figure 79 and Figure 81)	$I_{IO} = +8\text{mA}$, $V_{DD} = 3.3\text{V}$		0.27	0.6	
$V_{OH}^{(2)}$	Output high level voltage for an I/O pin when 4 pins are sourced at same time (see Figure 80 and Figure 83)	$I_{IO} = -2\text{mA}$	$V_{DD} - 0.8$	3		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Section 12.2.2: Current characteristics on page 175](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in [Section 12.2.2](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} . True open drain I/O pins do not have V_{OH} .

Figure 78. Typical V_{OL} versus I_{IO} at $V_{DD} = 3.3\text{V}$ (standard ports)

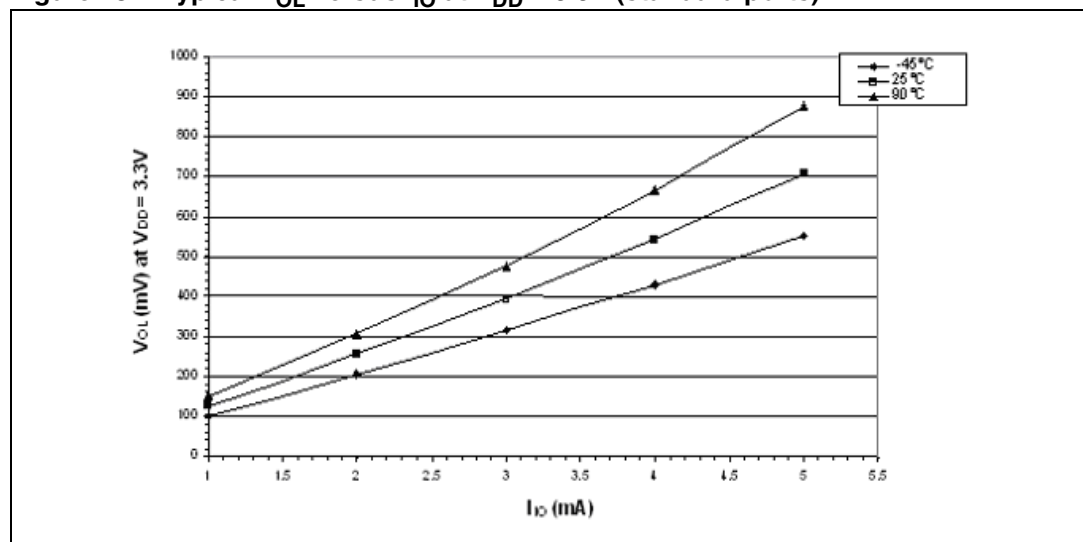


Figure 79. Typical V_{OL} versus I_{IO} at $V_{DD} = 3.3V$ (high-sink ports)

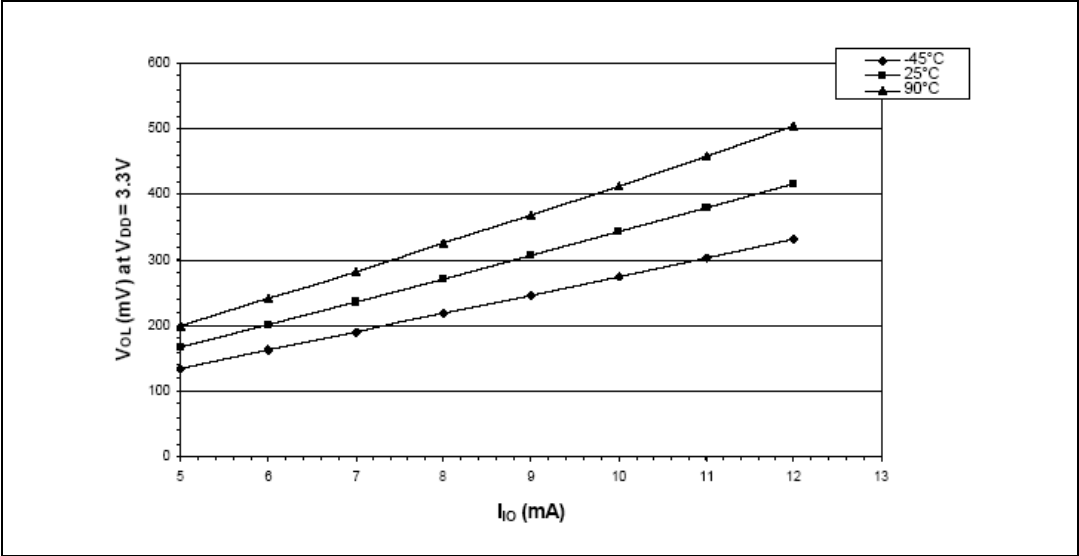


Figure 80. Typical V_{OH} versus I_{IO} at $V_{DD} = 3.3V$

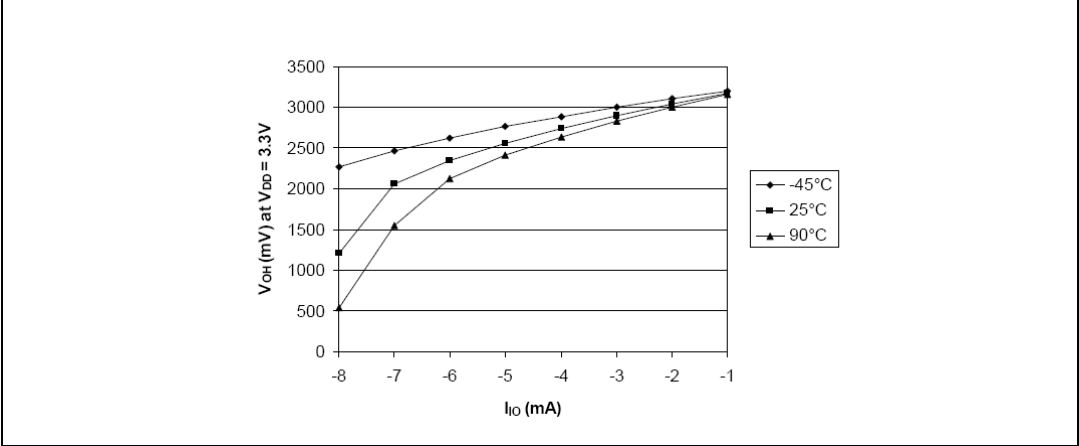


Figure 81. Typical V_{OL} versus V_{DD} at $I_{IO} = 2mA$

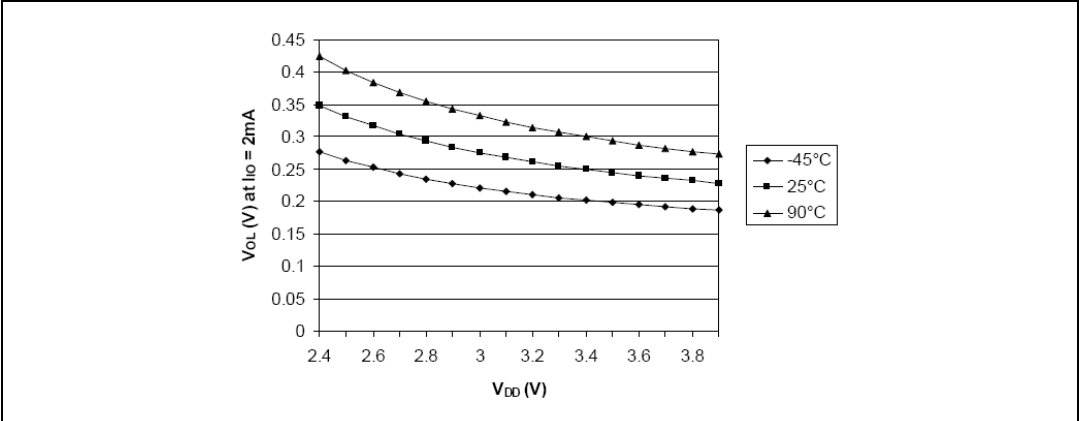
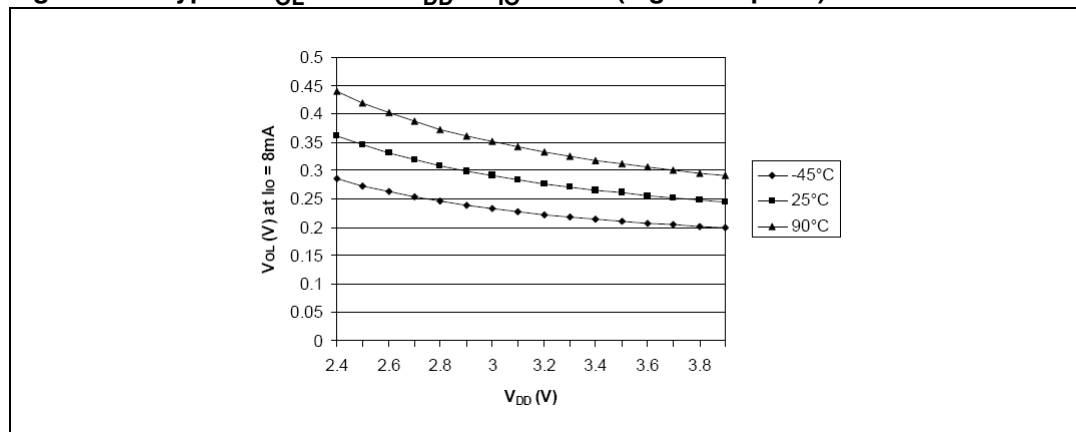
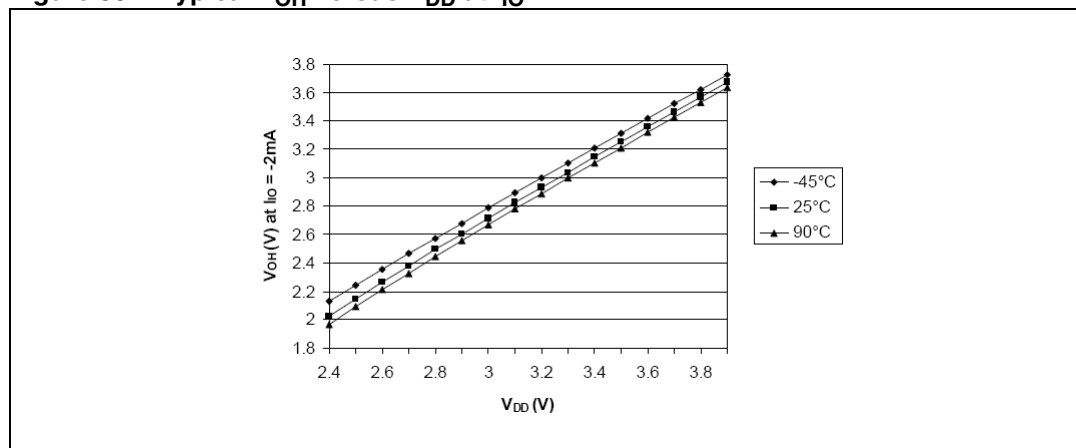


Figure 82. Typical V_{OL} versus V_{DD} at $I_{IO} = 8\text{mA}$ (high-sink ports)Figure 83. Typical V_{OH} versus V_{DD} at $I_{IO} = -2\text{mA}$ 

12.9 Control pin characteristics

12.9.1 Asynchronous $\overline{\text{RESET}}$ pin

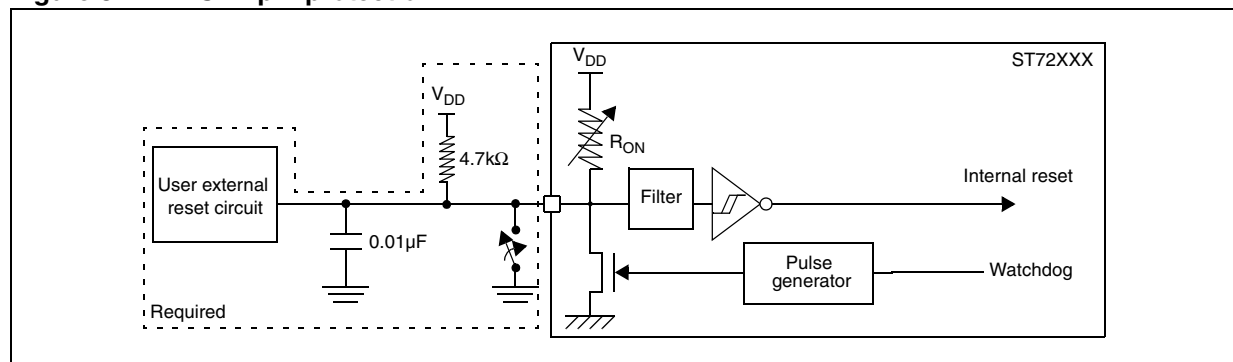
Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Table 110. Asynchronous $\overline{\text{RESET}}$ pin

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage ⁽¹⁾				$0.3 \times V_{DD}$	V
V_{IH}	Input high level voltage ⁽¹⁾		$0.7 \times V_{DD}$			
V_{hys}	Schmitt trigger voltage hysteresis ⁽²⁾			1.32		
V_{OL}	Output low level voltage ⁽³⁾	$V_{DD} = 3.3V$, $I_{IO} = +2mA$		0.2	0.5	V
I_{IO}	Driving current on $\overline{\text{RESET}}$ pin			2		mA
R_{ON}	Weak pull-up equivalent resistor	$V_{DD} = 3.3V$	20	30	120	k Ω
$t_{w(RSTL)out}$	Generated reset pulse duration	Internal reset sources	20	30	$42^{(4)}$	μs
$t_{h(RSTL)in}$	External reset pulse hold time ⁽⁵⁾		2.5			μs
$t_{g(RSTL)in}$	Filtered glitch duration ⁽⁶⁾			200		ns

1. Data based on characterization results, not tested in production
2. Hysteresis voltage between Schmitt trigger switching levels
3. The I_{IO} current sunk must always respect the absolute maximum rating specified in [Section 12.2.2: Current characteristics on page 175](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
4. Data guaranteed by design, not tested in production.
5. To guarantee the reset of the device, a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on the $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.
6. The reset network (the resistor and two capacitors) protects the device against parasitic resets, especially in noisy environments.

Figure 84. $\overline{\text{RESET}}$ pin protection



1. The reset network protects the device against parasitic resets.
2. The output of the external reset circuit must have an open-drain output to drive the ST7 reset pad. Otherwise the device can be damaged when the ST7 generates an internal reset (watchdog).
3. Whatever the reset source is (internal or external), the user must ensure that the level on the $\overline{\text{RESET}}$ pin can go below the V_{IL} max. level specified in [Section 12.9.1: Asynchronous \$\overline{\text{RESET}}\$ pin](#). Otherwise the reset is not taken into account internally.
4. Because the reset circuit is designed to allow the internal reset to be output in the $\overline{\text{RESET}}$ pin, the user must ensure that the current sunk on the RESET pin (by an external pull-up for example) is less than the absolute maximum value specified for $I_{INJ(RES)}$ in [Section 12.2.2: Current characteristics on page 175](#).

12.9.2 ICCSEL/V_{PP} pin

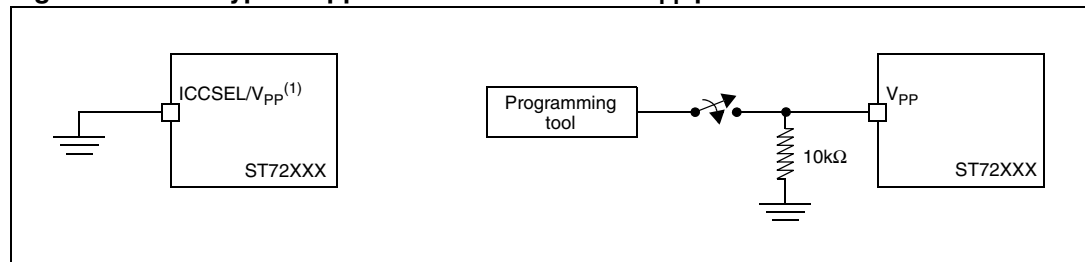
Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Table 111. ICCSEL/V_{PP} pin characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	Input low level voltage ⁽¹⁾		V_{SS}	0.2	V
V_{IH}	Input high level voltage ⁽¹⁾		$V_{DD} - 0.1$	12.6	
I_{lkg}	Input leakage current	$V_{IN} = V_{SS}$		± 1	μA

1. Data based on design simulation and/or technology characteristics, not tested in production.

Figure 85. Two typical applications with ICCSEL/V_{PP} pin



1. When ICC mode is not required by the application, ICCSEL/V_{PP} pin must be tied to V_{SS} .

12.10 Timer peripheral characteristics

Subject to general operating conditions for V_{DD} , f_{OSC} , and T_A unless otherwise specified.

Refer to [Section 9: I/O ports on page 56](#) for more details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output...).

Data based on design simulation and/or characterization results, not tested in production.

12.10.1 16-bit timer

Table 112. 16-bit timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time		1			t_{CPU}
$t_{res(PWM)}$	PWM resolution time		2			
		$f_{CPU} = 8 \text{ MHz}$	250			ns
f_{EXT}	Timer external clock frequency		0		$f_{CPU}/4$	MHz
f_{PWM}	PWM repetition rate		0		$f_{CPU}/4$	
Res_{PWM}	PWM resolution				16	bit

12.11 Communication interface characteristics

12.11.1 Serial peripheral interface (SPI)

Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified. Data based on design simulation and/or characterization results, not tested in production.

When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends on the I/O port configuration. Refer to [Section 9: I/O ports on page 56](#) for more details on the input/output alternate function characteristics (\overline{SS} , SCK, MOSI, MISO).

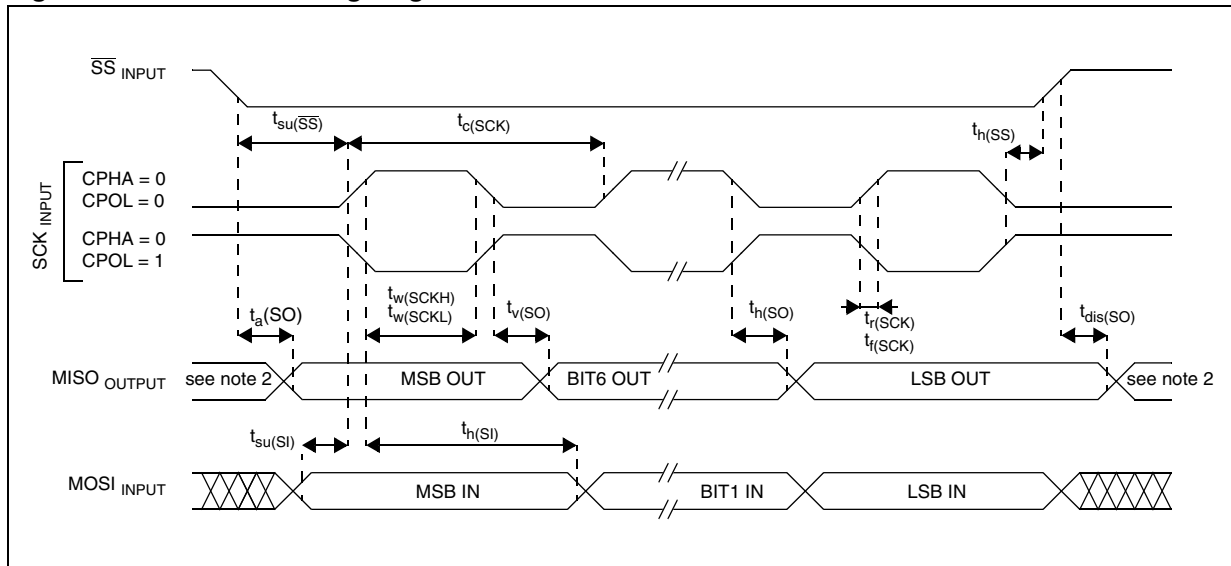
Table 113. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master $f_{CPU} = 8\text{ MHz}$	$f_{CPU}/128 = 0.0625$	$f_{CPU}/4 = 2$	MHz
		Slave $f_{CPU} = 8\text{ MHz}$	0	$f_{CPU}/2 = 4$	
$t_r(SCK)$ $t_f(SCK)$	SPI clock rise and fall time		See Table 2: Device pin description (LQFP44) on page 16		
$t_{su}(\overline{SS})^{(1)}$	\overline{SS} setup time ⁽²⁾	Slave	$t_{CPU} + 50$		ns
$t_h(\overline{SS})^{(1)}$	\overline{SS} hold time		120		
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master Slave	100 90		
$t_{su(MI)}^{(1)}$ $t_{su(SI)}^{(1)}$	Data input setup time	Master Slave	100 100		
$t_h(MI)^{(1)}$ $t_h(SI)^{(1)}$	Data input hold time	Master Slave	100 100		
$t_a(SO)^{(1)}$	Data output access time	Slave	0	120	
$t_{dis}(SO)^{(1)}$	Data output disable time			240	
$t_v(SO)^{(1)}$	Data output valid time	Slave (after enable edge)		90	
$t_h(SO)^{(1)}$	Data output hold time		0		
$t_v(MO)^{(1)}$	Data output valid time	Master (after enable edge)		120	
$t_h(MO)^{(1)}$	Data output hold time		0		

1. Data based on design simulation and/or characterization results, not tested in production

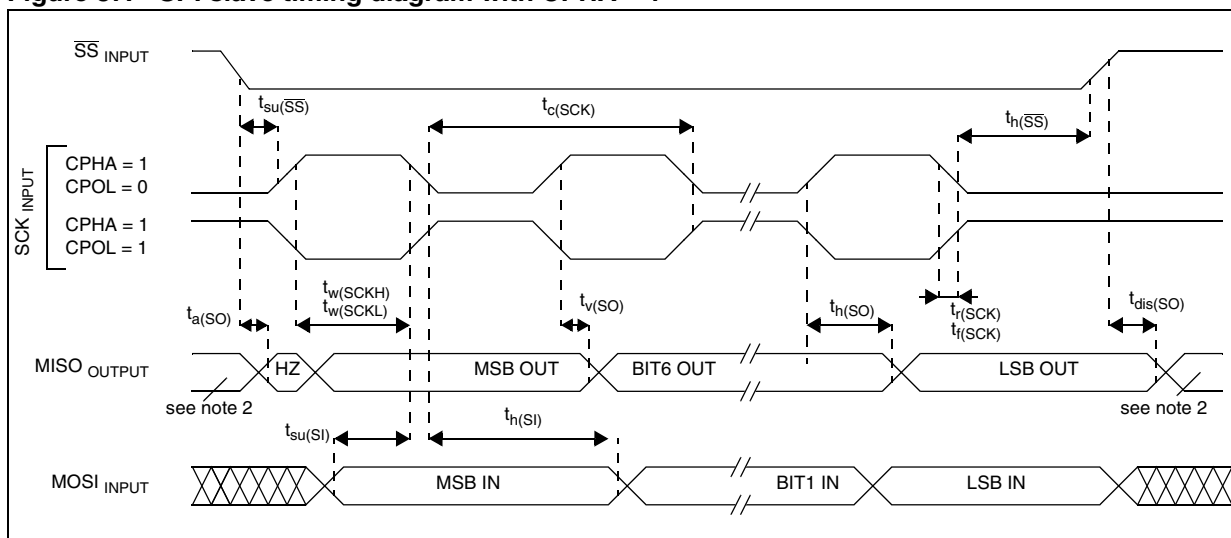
2. Depends on f_{CPU} . For example, if $f_{CPU} = 8\text{ MHz}$, then $t_{CPU} = 1/f_{CPU} = 125\text{ ns}$ and $t_{su}(\overline{SS}) = 175\text{ ns}$.

Figure 86. SPI slave timing diagram with CPHA = 0



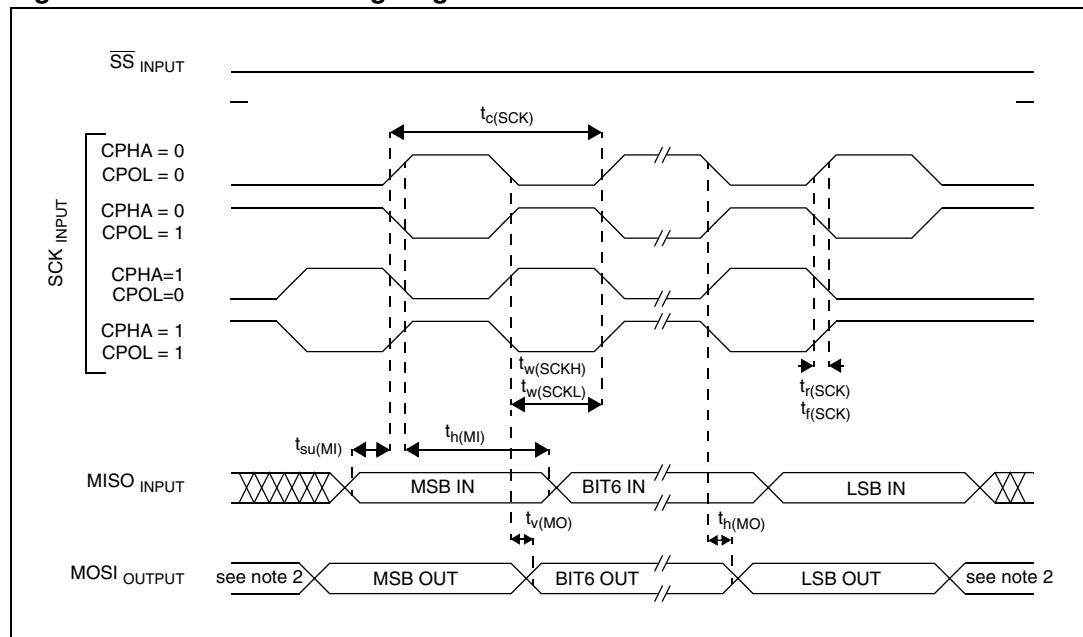
1. Measurement points are made at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends of the I/O port configuration.

Figure 87. SPI slave timing diagram with CPHA = 1



1. Measurement points are made at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. When no communication is on-going the data output line of the SPI (MOSI in master mode, MISO in slave mode) has its alternate function capability released. In this case, the pin status depends of the I/O port configuration.

Figure 88. SPI master timing diagram



12.11.2 I²C - inter IC control interface

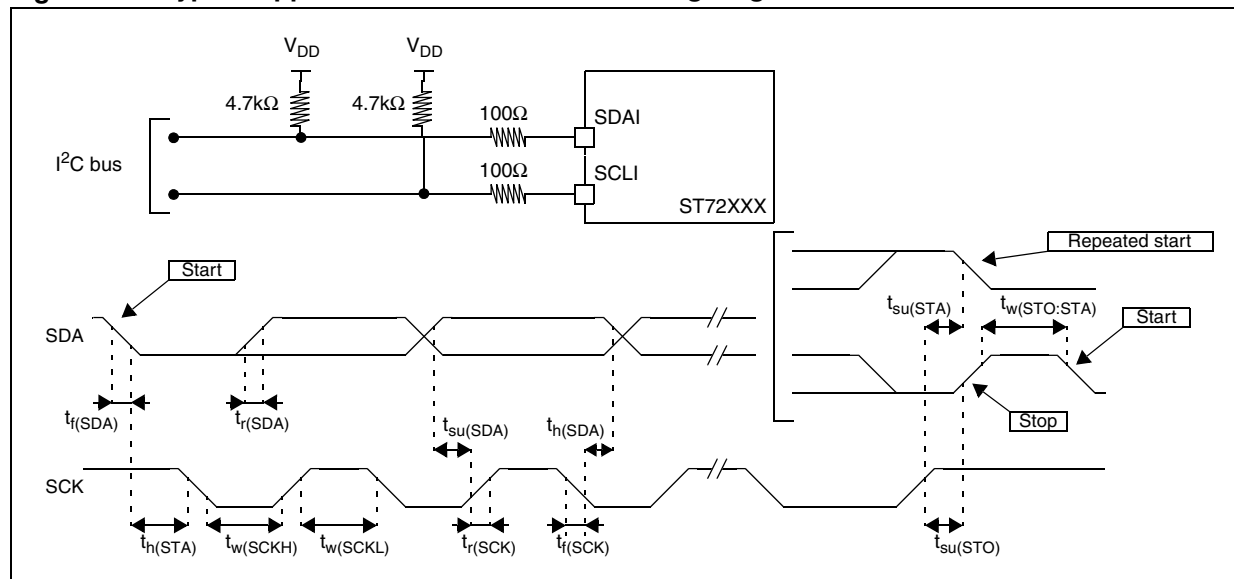
Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Refer to [Section 12.8: I/O port pin characteristics on page 189](#) for more details on the input/output alternate function characteristics (SDAI and SCLI). The ST7 I²C interface meets the requirements of the standard I²C communication protocol described in the following table.

Table 114. I²C control interface characteristics

Symbol	Parameter	Standard mode I ² C		Fast mode I ² C ⁽¹⁾		Unit
		Min ⁽²⁾	Max ⁽²⁾	Min ⁽²⁾	Max ⁽²⁾	
t _w (SCLL)	SCL clock low time	4.7		1.3		μs
t _w (SCLH)	SCL clock high time	4.0		0.6		
t _{su} (SDA)	SDA setup time	250		100		ns
t _h (SDA)	SDA data hold time	0 ⁽³⁾		0 ⁽⁴⁾	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time		1000	20 + 0.1C _b	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time		300			
t _h (STA)	START condition hold time	4.0		0.6		μs
t _{su} (STA)	Repeated START condition setup time	4.7				
t _{su} (STO)	STOP condition setup time	4.0				
t _w (STO:STA)	STOP to START condition time (bus free)	4.7		1.3		
C _b	Capacitive load for each bus line		400		400	pF

1. At 4 MHz f_{CPU} , maximum I²C speed (400 kHz) is not achievable. In this case, maximum I²C speed will be approximately 260 kHz.
2. Data based on standard I²C protocol requirement, not tested in production.
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 89. Typical application with I²C bus and timing diagram⁽¹⁾

1. Measurement points are made at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

The following table provides the values to be written in the I²CCCR register to obtain the required I²C SCL line frequency.

Table 115. SCL frequency table⁽¹⁾

f _{SCL} (kHz)	I ² CCCR value							
	f _{CPU} = 4 MHz				f _{CPU} = 8 MHz			
	V _{DD} = 4.1V		V _{DD} = 5V		V _{DD} = 4.1V		V _{DD} = 5V	
	R _P = 3.3kΩ	R _P = 4.7kΩ	R _P = 3.3kΩ	R _P = 4.7kΩ	R _P = 3.3kΩ	R _P = 4.7kΩ	R _P = 3.3kΩ	R _P = 4.7kΩ
400	Not achievable				83h			
300	Not achievable				85h			
200	83h				8Ah	89h	8Ah	
100	10h				24h	23h	24h	23h
50	24h				4Ch			
20	5Fh				FFh			

1. Legend: R_P = external pull-up resistance; f_{SCL} = I²C speed

Note: For speeds around 200 kHz, the achieved speed can have a $\pm 5\%$ tolerance.
 For other speed ranges, the achieved speed can have a $\pm 2\%$ tolerance.
 The above variations depend on the accuracy of the external components used.

12.12 10-bit ADC characteristics

Subject to general operating conditions for V_{DD} , f_{CPU} , and T_A unless otherwise specified.

Table 116. 10-bit ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{ADC}	ADC clock frequency		0.4		2	MHz
V _{AREF}	Analog reference voltage		V _{DD}		V _{DD}	V
V _{AIN}	Conversion voltage range ⁽¹⁾		V _{SSA}		V _{AREF}	
I _{lkg}	Input leakage current for analog input ⁽²⁾				±250	nA
R _{AIN}	External input impedance				see Figure 90 and Figure 91	kΩ
C _{AIN}	External capacitor on analog input					pF
f _{AIN}	Variation frequency of analog input signal					Hz
C _{ADC}	Internal sample and hold capacitor			12		pF
t _{ADC}	Conversion time (sample + hold) f _{CPU} = 8 MHz, speed = 0, f _{ADC} = 2 MHz		7.5			μs
	Number of sample capacitor loading cycles		4			1/f _{ADC}
	Number of hold conversion cycles		11			

1. Data based on characterization results, not tested in production.
2. Injecting negative current on adjacent pins may result in increased leakage currents. Software filtering of the converted analog value is recommended.

Figure 90. R_{AIN} maximum versus f_{ADC} with $C_{AIN} = 0$ pF⁽¹⁾

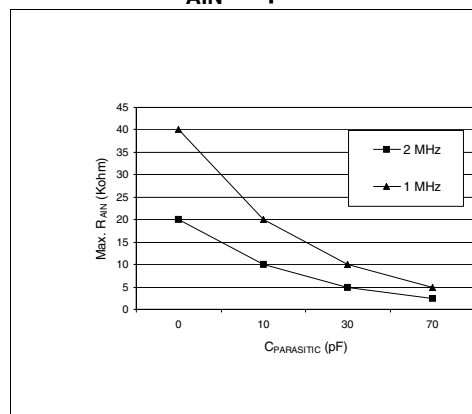
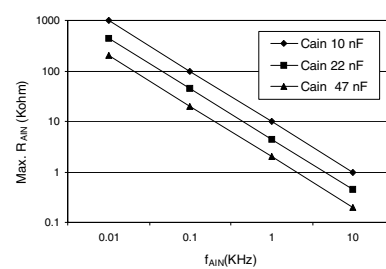
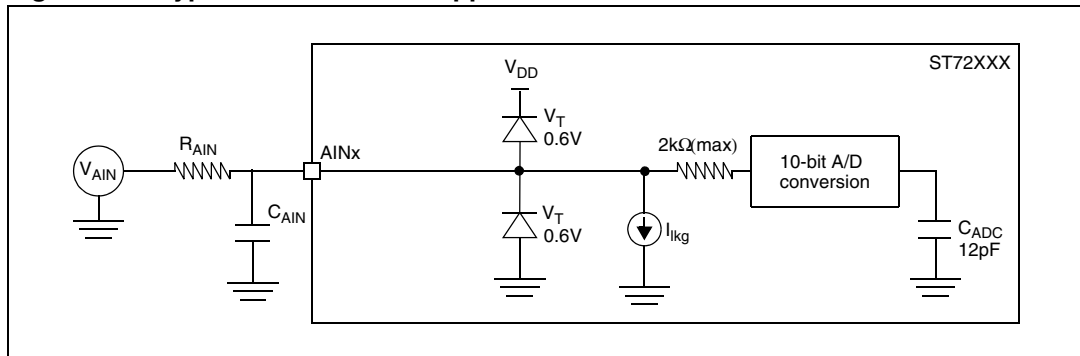


Figure 91. Recommended C_{AIN} and R_{AIN} values⁽²⁾



1. $C_{PARASITIC}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.
2. This graph shows that, depending on the input signal variation (f_{AIN}), C_{AIN} can be increased for stabilization time and decreased to allow the use of a larger serial resistor (R_{AIN}).

Figure 92. Typical A/D converter application



12.12.1 Analog power supply and reference pins

Depending on the MCU pin count, the package may feature separate V_{AREF} and V_{SSA} analog power supply pins. These pins supply power to the A/D converter cell and function as the high and low reference voltages for the conversion. In some packages, V_{AREF} and V_{SSA} pins are not available (refer to [Section 2: Package pinout and pin description on page 15](#)). In this case the analog supply and reference pads are internally bonded to the V_{DD} and V_{SS} pins.

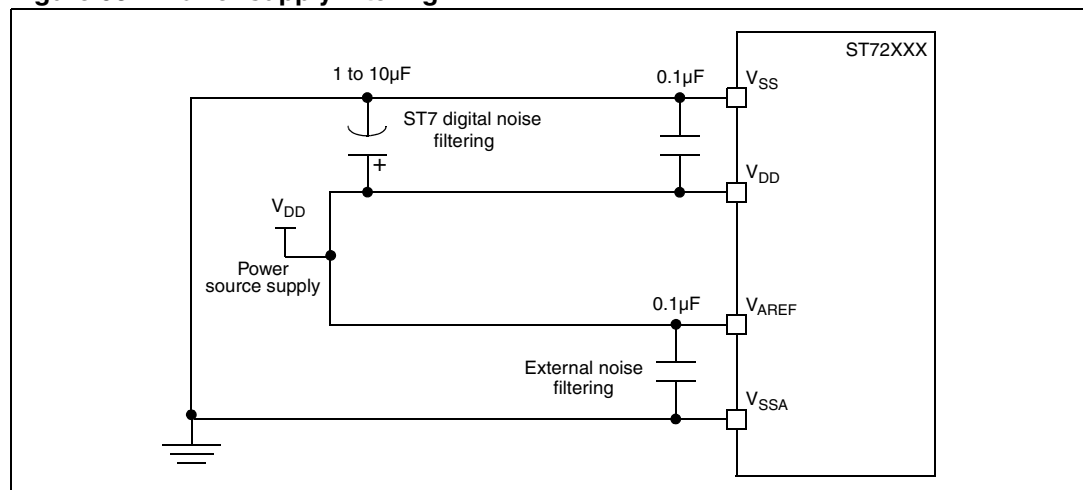
Separation of the digital and analog power pins allow board designers to improve A/D performance. Conversion accuracy can be impacted by voltage drops and noise in the event of heavily loaded or badly decoupled power supply lines (see [Section 12.12.2: General PCB design guidelines on page 203](#)).

12.12.2 General PCB design guidelines

To obtain best results, some general design and layout rules should be followed when designing the application PCB to shield the noise-sensitive, analog physical interface from noise-generating CMOS logic signals.

- Use separate digital and analog planes. The analog ground plane should be connected to the digital ground plane via a single point on the PCB.
- Filter power to the analog power planes. It is recommended to connect capacitors, with good high frequency characteristics, between the power and ground lines, placing 0.1 μF and optionally, if needed 10pF capacitors as close as possible to the ST7 power supply pins and a 1 to 10 μF capacitor close to the power source (see [Figure 93](#)).
- The analog and digital power supplies should be connected in a star network. Do not use a resistor, as V_{AREF} is used as a reference voltage by the A/D converter and any resistance would cause a voltage drop and a loss of accuracy.
- Properly place components and route the signal traces on the PCB to shield the analog inputs. Analog signals paths should run over the analog ground plane and be as short as possible. Isolate analog signals from digital signals that may switch while the analog inputs are being sampled by the A/D converter. Do not toggle digital outputs on the same I/O port as the A/D input being converted.

Figure 93. Power supply filtering



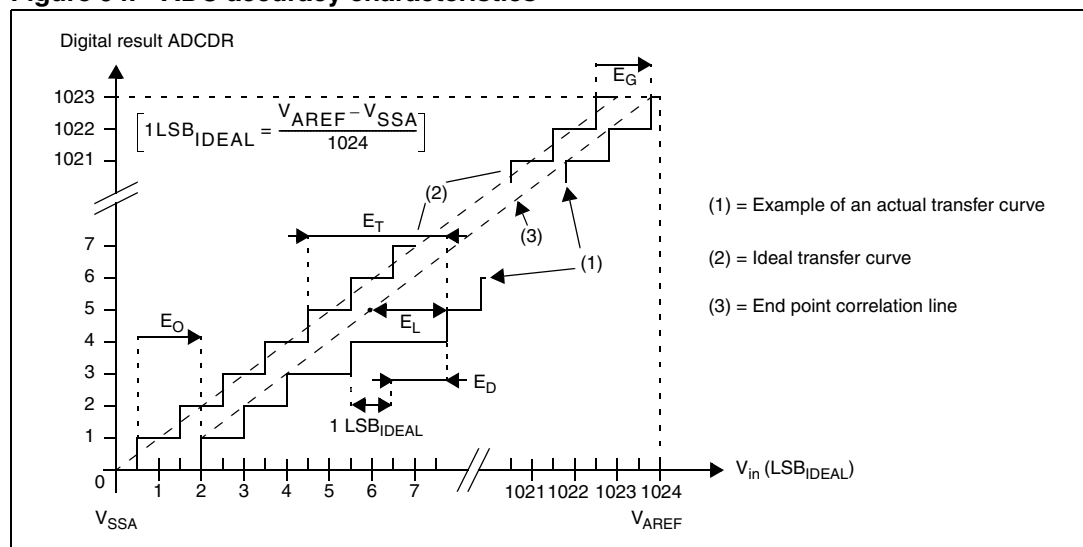
12.12.3 ADC accuracy

Table 117. ADC accuracy with $V_{DD} = 3.3V$

Symbol	Parameter	Conditions	Typ	Max ⁽¹⁾	Unit
$ E_T $	Total unadjusted error ⁽²⁾	CPU in Run mode @ $f_{ADC} = 2 \text{ MHz}$	3	4	LSB
$ E_O $	Offset error ⁽²⁾		2	3	
$ E_G $	Gain error ⁽²⁾		0.5	2.5	
$ E_D $	Differential linearity error ⁽²⁾		1	2	
$ E_L $	Integral linearity error ⁽²⁾		1	3	

1. Data based on characterization results, monitored in production to guarantee 99.73% within \pm max value from -40°C to 85°C ($\pm 3\sigma$ distribution limits).
2. ADC accuracy vs. negative injection current: Injecting negative current may reduce the accuracy of the conversion being performed on another analog input. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 12.8: I/O port pin characteristics on page 189](#) does not affect the ADC accuracy.

Figure 94. ADC accuracy characteristics



Legend:

- E_T = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves
- E_O = Offset error: deviation between the first actual transition and the first ideal one
- E_G = Gain error: deviation between the last ideal transition and the last actual one
- E_D = Differential linearity error: maximum deviation between actual steps and the ideal one
- E_L = Integral linearity error: maximum deviation between any actual transition and the end point correlation line

13 Package characteristics

13.1 Package mechanical data

Figure 95. 44-pin low profile quad flat package outline

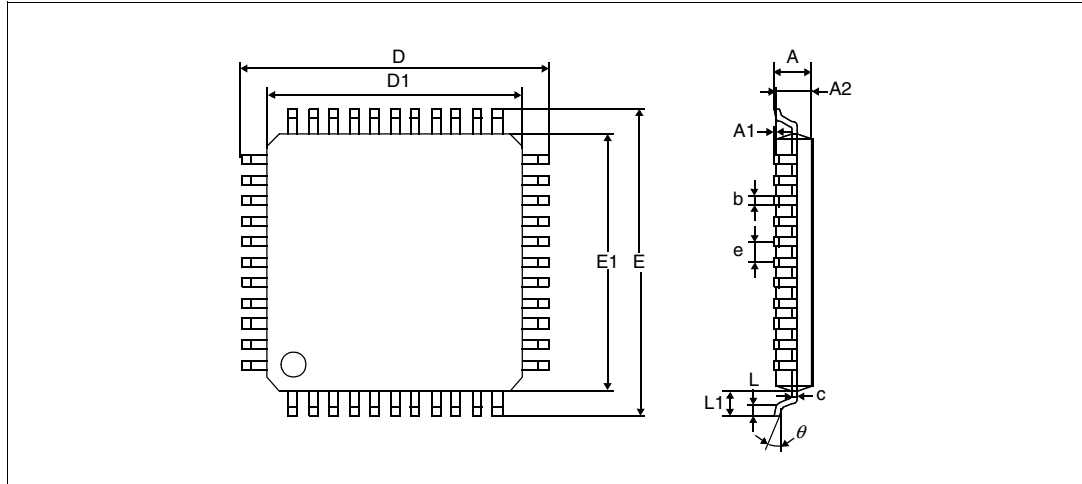


Table 118. 44-pin low profile quad flat package mechanical data

Dim.	mm			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.300	0.370	0.450	0.0118	0.0146	0.0177
C	0.090		0.200	0.0035		0.0079
D		12.000			0.4724	
D1		10.000			0.3937	
E		12.000			0.4724	
E1		10.000			0.3937	
e		0.800			0.0315	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

13.2 Thermal characteristics

Table 119. Thermal characteristics

Symbol	Ratings	Value	Unit
R_{thJA}	Package thermal resistance (junction to ambient) LQFP44 10 x 10	52	°C/W
P_D	Power dissipation ⁽¹⁾	500	mW
T_{Jmax}	Maximum junction temperature ⁽²⁾	110	°C

1. The maximum power dissipation is obtained from the formula $P_D = (T_J - T_A)/R_{thJA}$. The power dissipation of an application can be defined by the user with the formula: $P_D = P_{INT} + P_{PORT}$ where P_{INT} is the chip internal power ($I_{DD} \times V_{DD}$) and P_{PORT} is the port power dissipation depending on the ports used in the application.
2. The maximum chip-junction temperature is based on technology characteristics.

13.3 Soldering information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Compatibility

ECOPACK[®] LQFP packages are fully compatible with lead (Pb) containing soldering process (see application note AN2034).

Table 120. Soldering compatibility (wave and reflow soldering process)

Package	Plating material devices	Pb solder paste	Pb-free solder paste
LQFP44	Sn (pure Tin)	Yes	Yes

14 Device configuration and ordering information

14.1 Introduction

The device is available for production in user programmable versions (Flash) as well as in factory coded versions (FASTROM).

ST72P321BL-Auto devices are factory advanced service technique ROM (FASTROM) versions: They are factory-programmed HDFSFlash devices.

Flash devices are shipped to customers with a default content (FFh). This implies that Flash devices have to be configured by the customer using the option bytes.

14.2 Flash devices

14.2.1 Flash configuration

Table 121. Flash option bytes

Static option byte 0								Static option byte 1							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
WDG		Reserved						FMP_R	Res	RSTC	OSCTYPE		OSCRANGE		PLL OFF
HALT	SW										1	0	2	1	0
Default	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1

The option bytes allow the hardware configuration of the microcontroller to be selected. They have no address in the memory map and can be accessed only in programming mode (for example using a standard ST7 programming tool). The default content of the Flash is fixed to FFh. To program the Flash devices directly using ICP, Flash devices are shipped to customers with the internal RC clock source enabled.

Table 122. Option byte 0 description

Bit	Name	Function
OPT7	WDG HALT	Watchdog reset on halt This option bit determines if a reset is generated when entering halt mode while the watchdog is active. 0: No reset generation when entering halt mode 1: Reset generation when entering halt mode
OPT6	WDG SW	Hardware or software watchdog This option bit selects the watchdog type 0: Hardware (watchdog always enabled) 1: Software (watchdog to be enabled by software)
OPT5:1	-	Reserved (must be kept at default value)

Table 122. Option byte 0 description

Bit	Name	Function
OPT0	FMP_R	Flash memory readout protection Readout protection, when selected, provides a protection against program memory content extraction and against write access to Flash memory. Erasing the option bytes when the FMP_R option is selected causes the whole user memory to be erased first, after which the device can be reprogrammed. Refer to Section 4.3.1: Readout protection on page 23 and the <i>ST7 Flash programming reference manual</i> for more details. 0: Readout protection enabled 1: Readout protection disabled

Table 123. Option byte 1 description

Bit	Name	Function
OPT7	-	Reserved (must be kept at default value)
OPT6	RSTC	Reset clock cycle selection This option bit selects the number of CPU cycles applied during the reset phase and when exiting halt mode. For resonator oscillators, it is advised to select 4096 due to the long crystal stabilization time. 0: Reset phase with 4096 CPU cycles 1: Reset phase with 256 CPU cycles
OPT5:4	OSCTYPE[1:0]	Oscillator type These option bits select the ST7 main clock source type: 00: Clock source = Resonator oscillator 01: Reserved 10: Clock source = Internal RC oscillator 11: Clock source = External source
OPT3:1	OSCRANGE[2:0]	Oscillator range When the resonator oscillator type is selected, these option bits select the resonator oscillator current source corresponding to the frequency range of the used resonator. When the external clock source is selected, these bits are set to medium power (2 ~ 4 MHz). 000: Typical frequency range (LP) = >1 ~ 2 MHz 001: Typical frequency range (MP) = >2 ~ 4 MHz 010: Typical frequency range (MS) = >4 ~ 8 MHz 011: Typical frequency range (HS) = >8 ~ 16 MHz
OPT0	PLL OFF	PLL activation This option bit activates the PLL which allows multiplication by two of the main input clock frequency. The PLL is guaranteed only with an input frequency between 2 and 4 MHz. For this reason, the PLL must not be used with the internal RC oscillator. 0: PLL x2 enabled 1: PLL x2 disabled Caution 1: The PLL can be enabled only if the OSCRANGE (OPT3:1) bits are configured to 'MP - 2 ~ 4 MHz'. Otherwise, the device functionality is not guaranteed. Caution 2: When the PLL is used with an external clock signal, the clock signal must be available on the OSCIN pin before the reset signal is released.

14.2.2 Flash ordering information

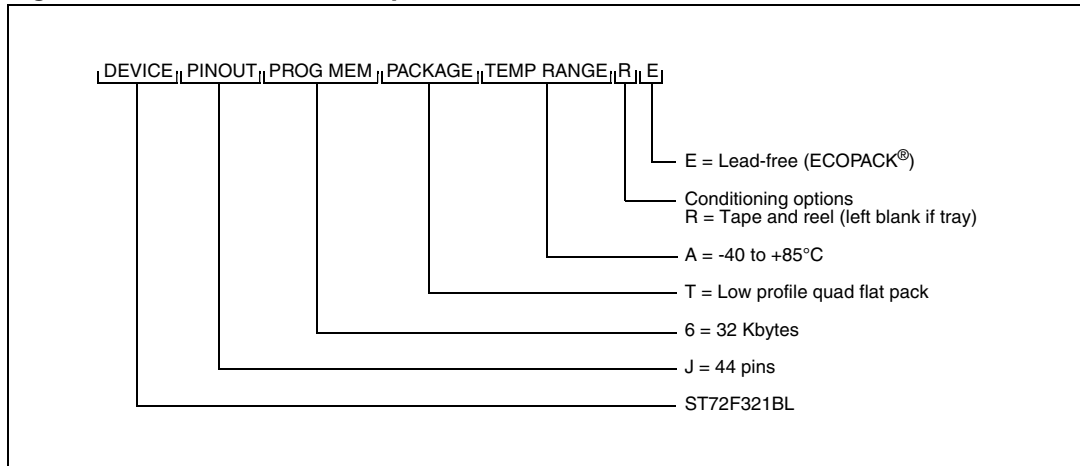
Table 124 serves as a guide for ordering.

Table 124. Flash user programmable device types

Order code ⁽¹⁾	Package	Flash memory (Kbytes)	Temperature range
ST72F321BLJ6TARE	LQFP44	32	-40°C to +85°C

1. R = Tape and reel (left blank if tray)

Figure 96. Flash commercial product code structure



14.3 FASTROM device ordering information and transfer of customer code

Customer code is made up of the FASTROM contents and the list of the selected options (if any). The FASTROM contents are to be sent on diskette, or by electronic means, with the S19 hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected options are communicated to STMicroelectronics using the correctly completed option list appended.

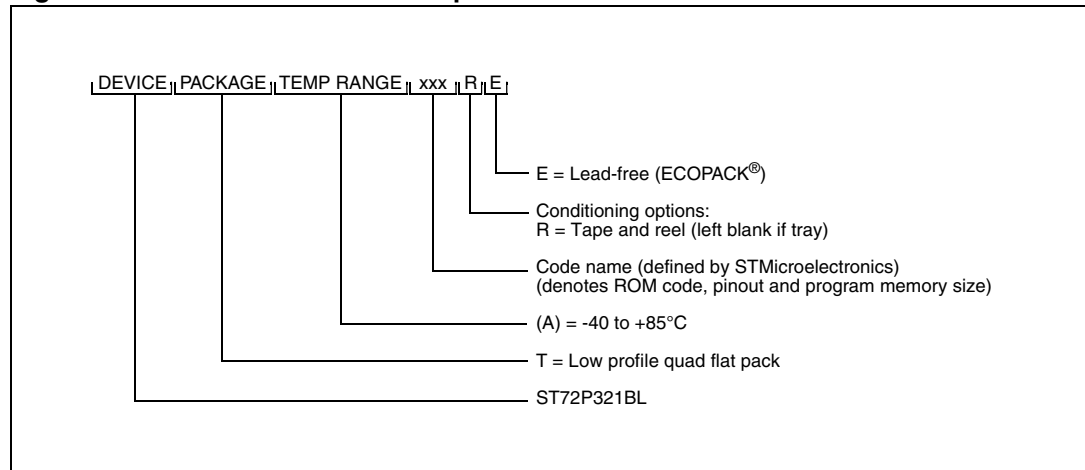
Refer to application note AN1635 for information on the counter listing returned by ST after code has been transferred.

Table 125: FASTROM factory coded device types on page 210 serves as a guide for ordering. The STMicroelectronics sales organization are pleased to provide detailed information on contractual points.

Table 125. FASTROM factory coded device types

Order code ⁽¹⁾	Package	Memory (Kbytes)	Temperature range
ST72P321BL(J6)T(A)xxxRE	LQFP44	32	-40°C to +85°C

1. The three characters in parentheses which represent the pinout, program memory size and temperature range are for reference only and are not visible in the final commercial product order code.
 'xxx' represents the code name defined by STMicroelectronics: It denotes the ROM code, pinout and program memory size.
 R = Tape and reel (left blank if tray)

Figure 97. FASTROM commercial product code structure

ST72P321BL (3.3V) FASTROM microcontroller option list

(Last update: January 2008)

Customer:
 Address:
 Contact:
 Phone No:
 Reference/FASTROM code:

The FASTROM code name is assigned by STMicroelectronics.
 FASTROM code must be sent in .S19 format. .Hex extension cannot be processed.

Device type/memory size/package (check only one option):

FASTROM 32K

LQFP44: [] ST72P321BL(J6)T(A)

Conditioning (check only one option):

LQFP packaged product [] Tape and reel [] Tray

Special marking: [] No [] Yes "....." (10 characters max)
 Authorized characters are letters, digits, '.', '/', and spaces only.

Clock source selection: [] Resonator [] LP: Low power resonator (1 to 2 MHz)
 [] MP: Medium power resonator (2 to 4 MHz)
 [] MS: Medium speed resonator (4 to 8 MHz)
 [] HS: High speed resonator (8 to 16 MHz)
 [] Internal RC
 [] External clock (sets MP medium power resonator in OSC RANGE of option byte)

PLL⁽¹⁾⁽²⁾: [] Disabled [] Enabled

Reset delay: [] 256 cycles [] 4096 cycles

Watchdog selection: [] Software activation [] Hardware activation

Watchdog reset on halt: [] Reset [] No reset

Readout protection: [] Disabled [] Enabled

Date
 Signature

Note 1: PLL must be disabled if internal RC Network is selected

Note 2: The PLL can be enabled only if the resonator is configured to 'Medium power: 2 to 4 MHz'

Please download the latest version of this option list from www.st.com

14.4 Development tools

14.4.1 Introduction

Development tools for the ST7 microcontrollers include a complete range of hardware systems and software tools from STMicroelectronics and third-party tool suppliers. The range of tools includes solutions to help you evaluate microcontroller peripherals, develop and debug your application, and program your microcontrollers.

14.4.2 Evaluation tools and starter kits

ST offers complete, affordable starter kits and full-featured evaluation boards that allow you to evaluate microcontroller features and quickly start developing ST7 applications. Starter kits are complete, affordable hardware/software tool packages that include features and samples to help you quickly start developing your application. ST evaluation boards are open-design, embedded systems, which are developed and documented to serve as references for your application design. They include sample application software to help you demonstrate, learn about and implement your ST7's features.

14.4.3 Development and debugging tools

Application development for ST7 is supported by fully optimizing C compilers and the ST7 assembler-linker toolchain, which are all seamlessly integrated in the ST7 integrated development environments in order to facilitate the debugging and fine-tuning of your application. The cosmic C compiler is available in a free version that outputs up to 16 Kbytes of code.

The range of hardware tools includes cost effective ST7-DVP3 series emulators. These tools are supported by the ST7 Toolset from STMicroelectronics, which includes the STVD7 integrated development environment (IDE) with high-level language debugger, editor, project manager and integrated programming interface.

14.4.4 Programming tools

During the development cycle, the ST7-DVP3 and ST7-EMU3 series emulators and the RLink provide in-circuit programming capability for programming the Flash microcontroller on your application board.

ST also provides a low-cost dedicated in-circuit programmer, the ST7-STICK, as well as ST7 socket boards which provide all the sockets required for programming any of the devices in a specific ST7 subfamily on a platform that can be used with any tool with in-circuit programming capability for ST7.

For production programming of ST7 devices, ST's third-party tool partners also provide a complete range of gang and automated programming solutions, which are ready to integrate into your production environment.

For additional ordering codes for spare parts, accessories and tools available for the ST7 (including from third party manufacturers), refer to the online product selector at www.st.com.

Table 126. Development tool order codes for the ST72321BL family

Supported products	Emulation				Programming
	ST7 DVP3 series		ST7 EMU3 series		ICC socket board
	Emulator	Connection kit	Emulator	Active probe and T.E.B.	
ST72321BLJ6	ST7MDT20-DVP3	ST7MDT20-T44/DVP	ST7MDT20J-EMU3	ST7MDT20J-TEB	ST7SB20J/xx ⁽¹⁾

1. Add suffix /EU, /UK, /US for the power supply of your region.

14.4.5 Socket and emulator adapter information

For information on the type of socket that is supplied with the emulator, refer to the suggested list of sockets in [Table 127](#).

Note: Before designing the board layout, it is recommended to check the overall dimensions of the socket as they may be greater than the dimensions of the device.

For footprint and other mechanical information about these sockets and adapters, refer to the manufacturer's datasheet.

Table 127. Suggested list of socket types

Device	Socket (supplied with ST7MDT20J-EMU3)	Emulator adapter (supplied with ST7MDT20J-EMU3)
LQFP44 10 x10	YAMAICHI IC149-044-*52-*5	YAMAICHI ICP-044-5

14.5 ST7 application notes

All relevant ST7 application notes can be found on www.st.com

15 Known limitations

15.1 All Flash devices

15.1.1 Safe connection of OSC1/OSC2 pins

The OSC1 and/or OSC2 pins must not be left unconnected, otherwise the ST7 main oscillator may start and, in this configuration, could generate an f_{OSC} clock frequency in excess of the allowed maximum (>16 MHz), putting the ST7 in an unsafe/undefined state. Refer to [Section 6.4: Multi-oscillator \(MO\) on page 32](#).

15.1.2 External interrupt missed

To avoid any risk of generating a parasitic interrupt, the edge detector is automatically disabled for one clock cycle during an access to either DDR and OR. Any input signal edge during this period is not detected and does not generate an interrupt.

This case can typically occur if the application refreshes the port configuration registers at intervals during runtime.

Workaround

The workaround is based on software checking the level on the interrupt pin before and after writing to the PxOR or PxDDR registers. If there is a level change (depending on the sensitivity programmed for this pin) the interrupt routine is invoked using the call instruction with three extra PUSH instructions before executing the interrupt routine (this is to make the call compatible with the IRET instruction at the end of the interrupt service routine).

But detection of the level change does not make sure that edge occurs during the critical one cycle duration and the interrupt has been missed. This may lead to occurrence of same interrupt twice (one hardware and another with software call).

To avoid this, a semaphore is set to '1' before checking the level change. The semaphore is changed to level '0' inside the interrupt routine. When a level change is detected, the semaphore status is checked and if it is '1' this means that the last interrupt has been missed. In this case, the interrupt routine is invoked with the call instruction.

There is another possible case that is, if writing to PxOR or PxDDR is done with global interrupts disabled (interrupt mask bit set). In this case, the semaphore is changed to '1' when the level change is detected. Detecting a missed interrupt is done after the global interrupts are enabled (interrupt mask bit reset) and by checking the status of the semaphore. If it is '1' this means that the last interrupt was missed and the interrupt routine is invoked with the call instruction.

To implement the workaround, the following software sequence is to be followed for writing into the PxOR/PxDDR registers. The example is for Port PF1 with falling edge interrupt sensitivity. The software sequence is given for both cases (global interrupt disabled/enabled).

Case 1: Writing to PxOR or PxDDR with global interrupts enabled:

```

LD A,#01
LD sema,A; set the semaphore to '1'
LD A,PFDR
AND A,#02
LD X,A; store the level before writing to PxOR/PxDDR
LD A,$90
LD PFDDR,A ; Write to PFDDR
LD A,$ff
LD PFOR,A ; Write to PFOR
LD A,PFDR
AND A,#02
LD Y,A; store the level after writing to PxOR/PxDDR
LD A,X; check for falling edge
cp A,#02
jrne OUT
TNZ Y
jrne OUT
LD A,sema ; check the semaphore status if edge is detected
CP A,#01
jrne OUT
call call_routine ; call the interrupt routine
OUT:LD A,#00
LD sema,A
.call_routine ; entry to call_routine
PUSH A
PUSH X
PUSH CC
.extl_rt ; entry to interrupt routine
LD A,#00
LD sema,A
IRET

```

Case 2: Writing to PxOR or PxDDR with global interrupts disabled:

```

SIM ; set the interrupt mask
LD A,PFDR
AND A,$02
LD X,A ; store the level before writing to PxOR/PxDDR
LD A,$90
LD PFDDR,A ; Write into PFDDR
LD A,$ff
LD PFOR,A ; Write to PFOR
LD A,PFDR
AND A,$02
LD Y,A ; store the level after writing to PxOR/PxDDR
LD A,X ; check for falling edge
cp A,$02
jrne OUT
TNZ Y
jrne OUT
LD A,$01
LD sema,A ; set the semaphore to '1' if edge is detected

```

```
RIM ; reset the interrupt mask
LD A,sema ; check the semaphore status
CP A,#$01
jrne OUT
call call_routine ; call the interrupt routine
RIM
OUT:RIM
JP while_loop
.call_routine ; entry to call_routine
PUSH A
PUSH X
PUSH CC
.extl_rt ; entry to interrupt routine
LD A,#$00
LD sema,A
IRET
```

15.1.3 Unexpected reset fetch

If an interrupt request occurs while a 'POP CC' instruction is executed, the interrupt controller does not recognize the source of the interrupt and, by default, passes the reset vector address to the CPU.

Workaround

To solve this issue, a 'POP CC' instruction must always be preceded by a 'SIM' instruction.

15.1.4 Clearing active interrupts outside interrupt routine

When an active interrupt request occurs at the same time as the related flag is being cleared, an unwanted reset may occur.

Note: Clearing the related interrupt mask does not generate an unwanted reset.

Concurrent interrupt context

The symptom does not occur when the interrupts are handled normally, that is, when:

- The interrupt flag is cleared within its own interrupt routine
- The interrupt flag is cleared within any interrupt routine
- The interrupt flag is cleared in any part of the code while this interrupt is disabled

If these conditions are not met, the symptom can be avoided by implementing the following sequence:

Perform SIM and RIM operation before and after resetting an active interrupt request.

Example:

```
SIM
Reset interrupt flag
RIM
```


Nested interrupt context

The symptom does not occur when the interrupts are handled normally, that is, when:

- The interrupt flag is cleared within its own interrupt routine
- The interrupt flag is cleared within any interrupt routine with higher or identical priority level
- The interrupt flag is cleared in any part of the code while this interrupt is disabled

If these conditions are not met, the symptom can be avoided by implementing the following sequence:

```
PUSH CC
SIM
Reset interrupt flag
POP CC
```

15.1.5 16-bit timer PWM mode

In PWM mode, the first PWM pulse is missed after writing the value FFFCh in the OC1R register (OC1HR, OC1LR). It leads to either full or no PWM during a period, depending on the OLVL1 and OLVL2 settings.

15.1.6 TIMD set simultaneously with OC interrupt**Description**

If the 16-bit timer is disabled at the same time as the output compare event occurs, then the output compare flag gets locked and cannot be cleared before the timer is enabled again.

Impact on the application

If output compare interrupt is enabled, then the output compare flag cannot be cleared in the timer interrupt routine. Consequently the interrupt service routine is called repeatedly and the application gets stuck which causes the watchdog reset if enabled by the application.

Workaround

Disable the timer interrupt before disabling the timer. While enabling, first enable the timer, then the timer interrupts.

Perform the following to disable the timer:

- TACR1 or TBCR1 = 0x00h; // Disable the compare interrupt
- TACSR1 or TBCSR1 = 0x40; // Disable the timer

Perform the following to enable the timer again:

- TACSR1 & or TBCSR1 & = ~0x40; // Enable the timer
- TACR1 or TBCR1 = 0x40; // Enable the compare interrupt

15.1.7 SCI wrong break duration

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

20 bits instead of 10 bits if M = 0

22 bits instead of 11 bits if M = 1.

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

Occurrence

The occurrence of the problem is random and proportional to the baud rate. With a transmit frequency of 19200 baud ($f_{CPU} = 8$ MHz and SCIBRR = 0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

- Disable interrupts
- Reset and set TE (IDLE request)
- Set and reset SBK (break request)
- Re-enable interrupts

15.1.8 I²C multimaster

In multimaster configurations, if the ST7 I²C receives a start condition from another I²C master after the START bit is set in the I²CCR register and before the start condition is generated by the ST7 I²C, it may ignore the start condition from the other I²C master. In this case, the ST7 master will receive a NACK from the other device. On reception of the NACK, ST7 can send a restart and slave address to re-initiate communication.

15.1.9 I²C exit from halt/active halt

Contrary to the behavior specified in the datasheet, the I²C interrupt is capable of exiting the device from halt/active halt mode.

16 Revision history

Table 128. Document revision history

Date	Revision	Changes
08-Jan-2008	Rev 1	Initial release
14-Jan-2008	Rev 2	<p>Section 6.3: Phase locked loop on page 31: Added caution regarding use of PLL with an external clock</p> <p>Table 95: On-chip peripherals on page 180: Added typical values for ART PWM and I²C supply current parameters</p> <p>Table 99: Examples of typical resonators on page 183: Changed 'MS' mode to 'MP' mode for f_{OSC} = 4MHz</p> <p>Table 123: Option byte 1 description on page 208:</p> <ul style="list-style-type: none"> - For OPT3:1 bits, added '>' to the first of each frequency range - For OPT0 bit, added a caution regarding use of PLL with an external clock

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