STH240N75F3-2, STH240N75F3-6

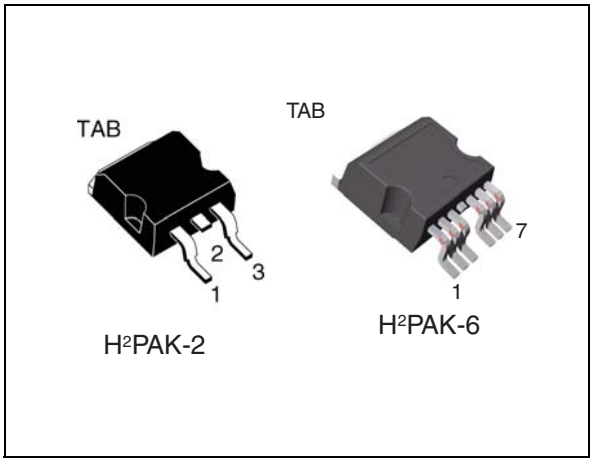
N-channel 75 V, 2.6 mΩ typ., 180 A STripFET™ III Power MOSFET in H²PAK-2 and H²PAK-6 packages

Datasheet – production data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STH240N75F3-2	75 V	< 3.0 mΩ	180 A
STH240N75F3-6			

- Conduction losses reduced
- Low profile, very low parasitic inductance



Applications

- Switching application

Description

These devices are N-channel enhancement mode Power MOSFETs produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

Figure 1. Internal schematic diagram

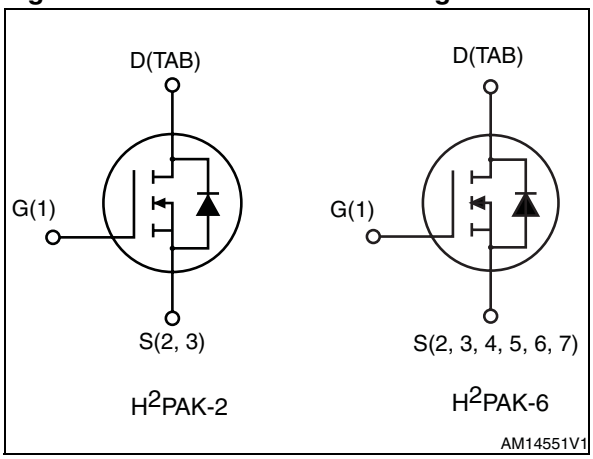


Table 1. Device summary

Order code	Marking	Package	Packaging
STH240N75F3-2	240N75F3	H²PAK-2	Tape and reel
STH240N75F3-6		H²PAK-6	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	180	A
I_D	Drain current (continuous) at T_C = 100 °C	170	A
I_{DM}(2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
	Derating factor	2	W/°C
E_{AS} (3)	Single pulse avalanche energy	600	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting Tj = 25 °C, I_D = 60 A, V_{DD} = 15 V.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	35	°C/W

1. When mounted on 1 inch2 FR-4 2 oz Cu.

2 Electrical characteristics

(Tcase = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	75			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 75 V, V_{DS} = 75 V, T_C =125 °C, V_{GS}= 0			10 100	µA µA
I_{GSS}	Gate body leakage current	V_{DS} = ± 20 V, V_{DS} = 0			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 90 A		2.6	3.0	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} =0	-	6800 1100 50	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}= 37.5 V, I_D= 120 A, V_{GS}= 10 V (see *Figure 14*)	-	87 30 26	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 37.5 V, I_D = 60 A R_G= 4.7 Ω, V_{GS}= 10 V, (see *Figure 13*)	-	25 70	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time		-	100 15	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SD} (1)	Source-drain current Source-drain current (pulsed)		-		180 720	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 120 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 120 A,di/dt = 100 A/µs V_{DD} = 30 V, T_j = 150 °C *(see Figure 15)*	-	80 180 4.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

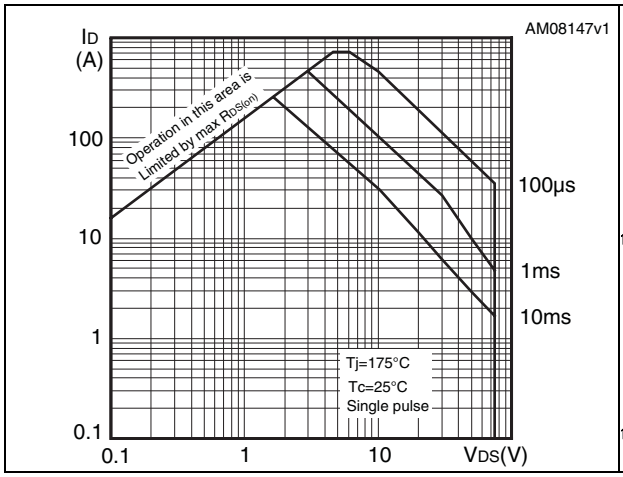


Figure 3. Thermal impedance

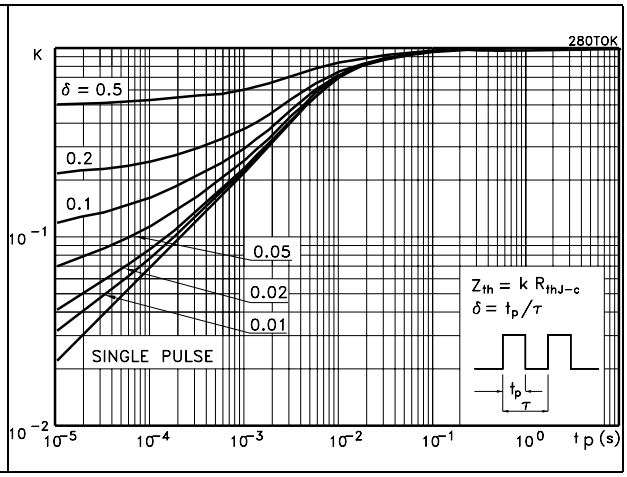


Figure 4. Output characteristics

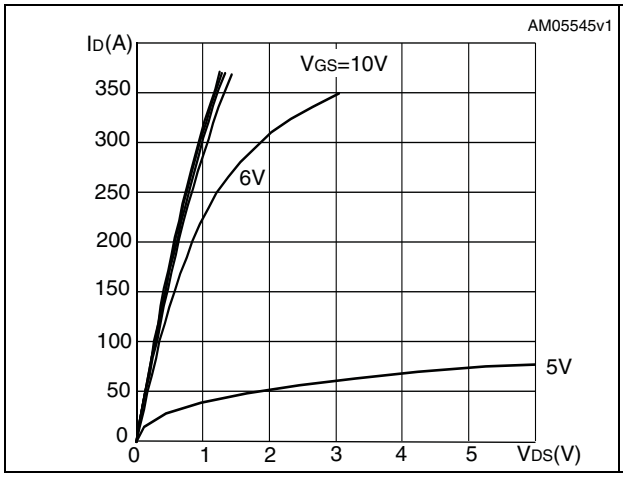


Figure 5. Transfer characteristics

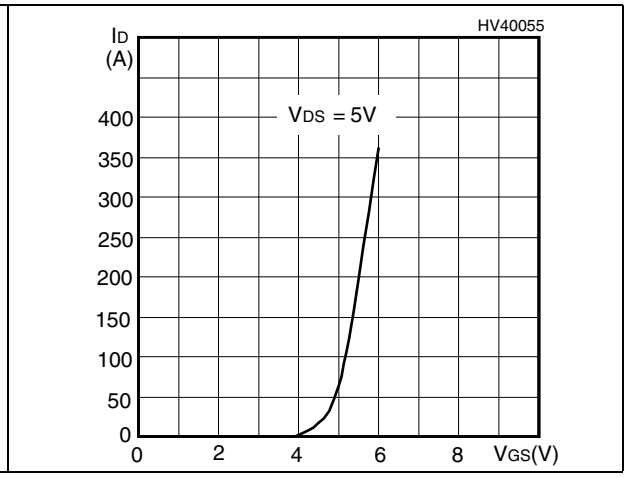


Figure 6. Normalized BV_{DSS} vs temperature

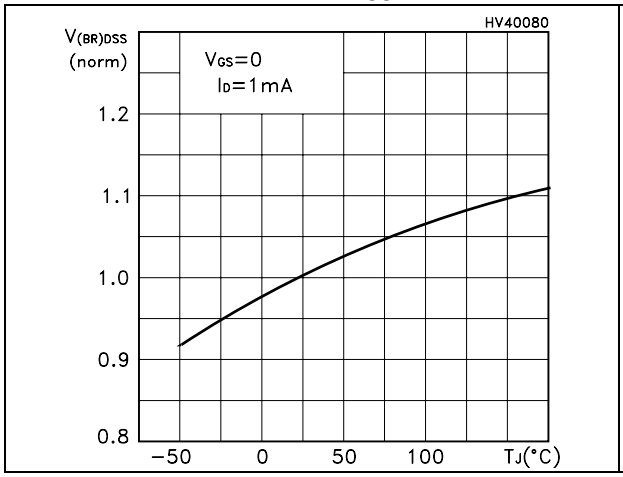


Figure 7. Static drain-source on-resistance

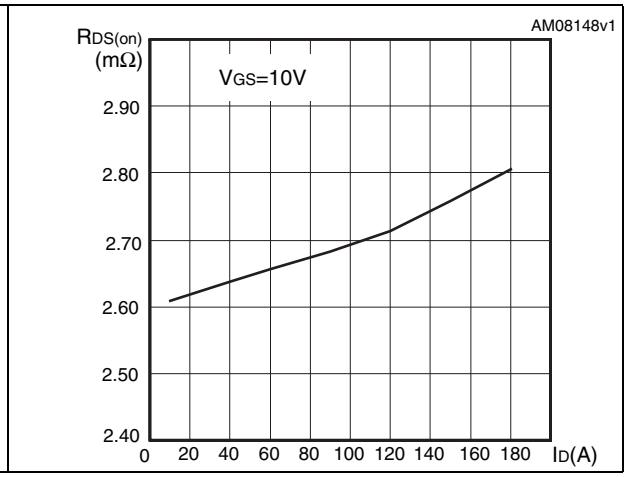


Figure 8. Gate charge vs gate-source voltage

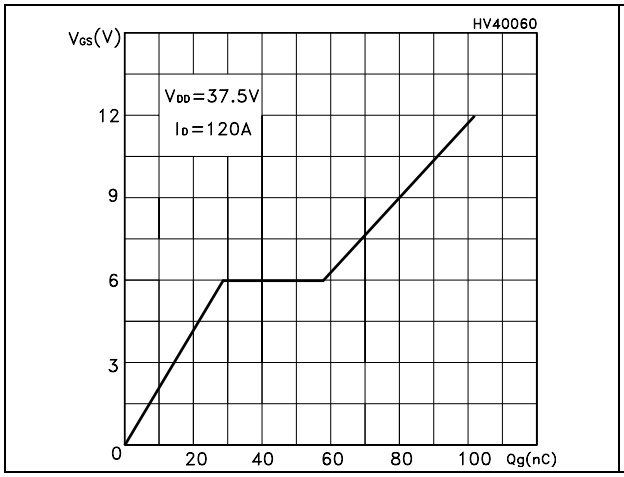


Figure 9. Capacitance variations

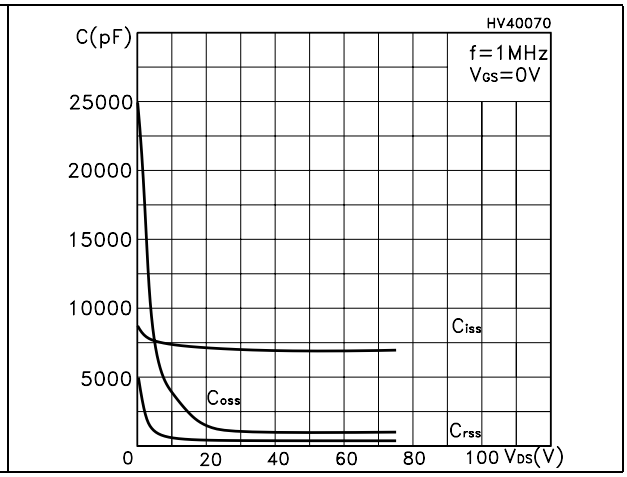


Figure 10. Normalized gate threshold voltage vs temperature

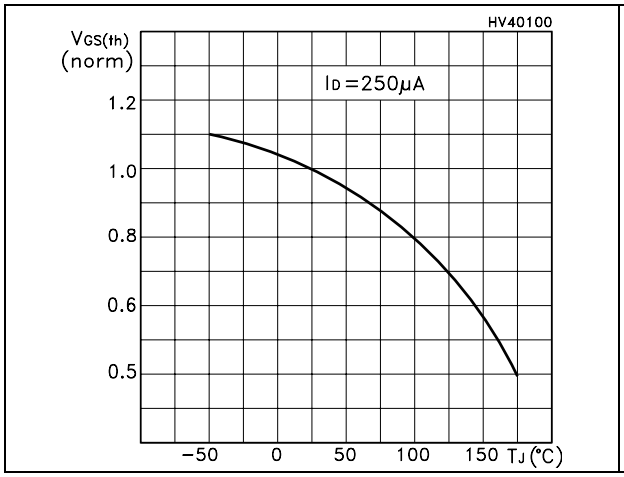


Figure 11. Normalized on-resistance vs temperature

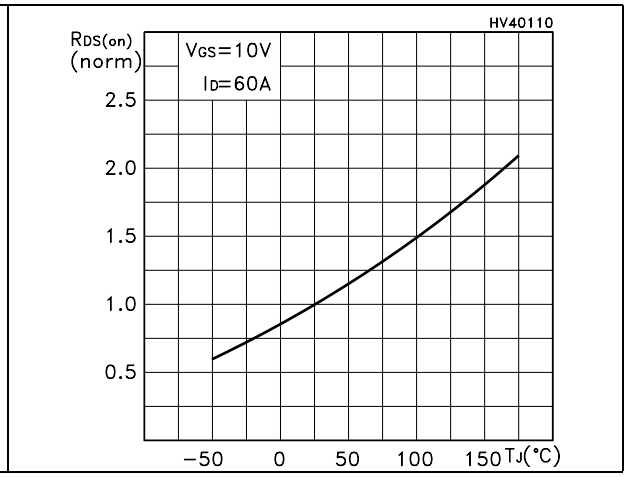
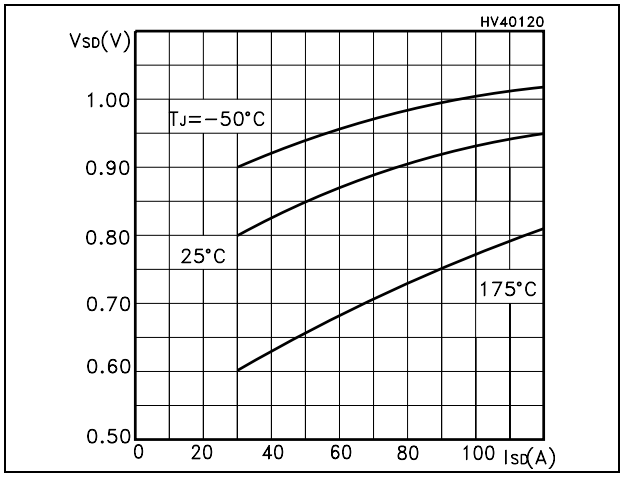


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

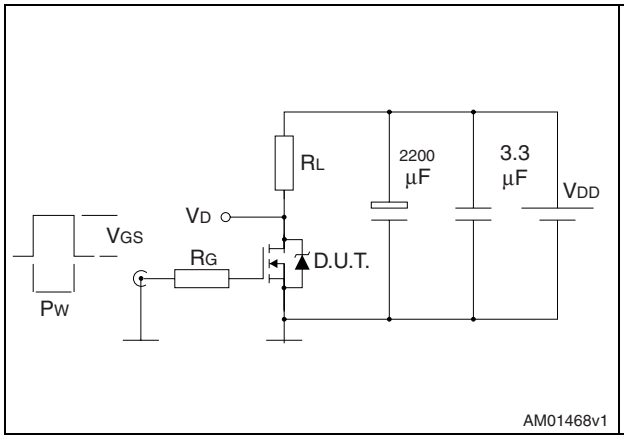


Figure 14. Gate charge test circuit

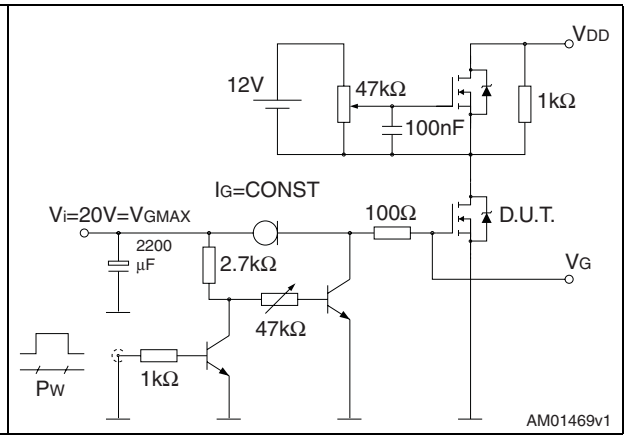


Figure 15. Test circuit for inductive load switching and diode recovery times

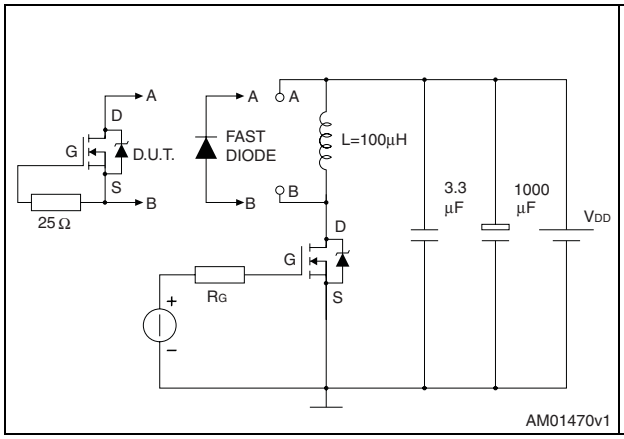


Figure 16. Unclamped inductive load test circuit

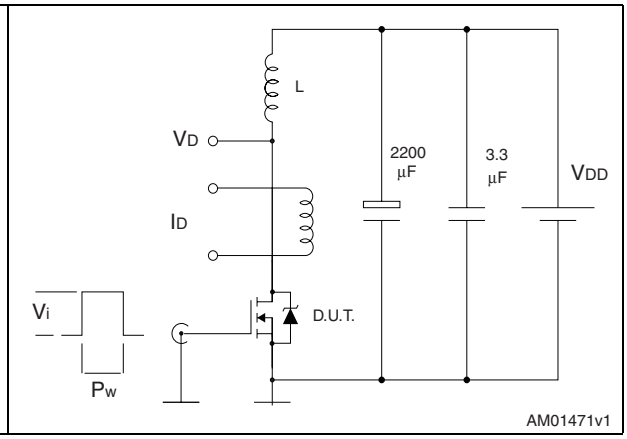


Figure 17. Unclamped inductive waveform

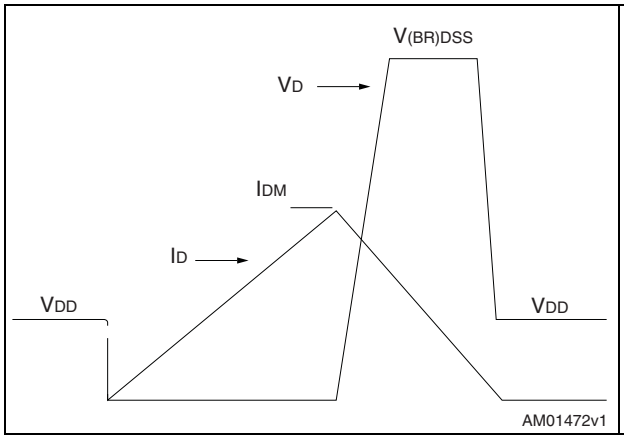
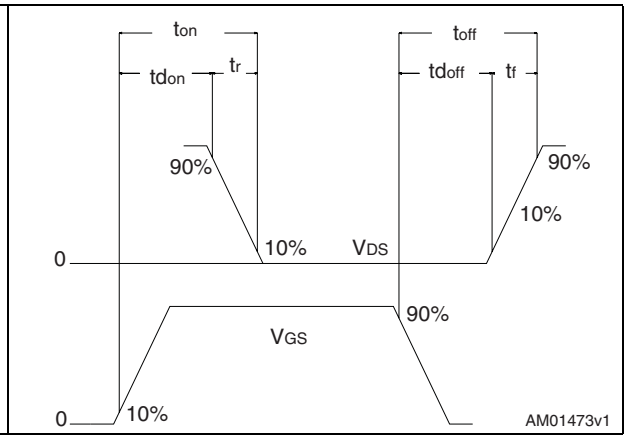


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 8. H²PAK-2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30	-	15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 19. H²PAK-2 drawing

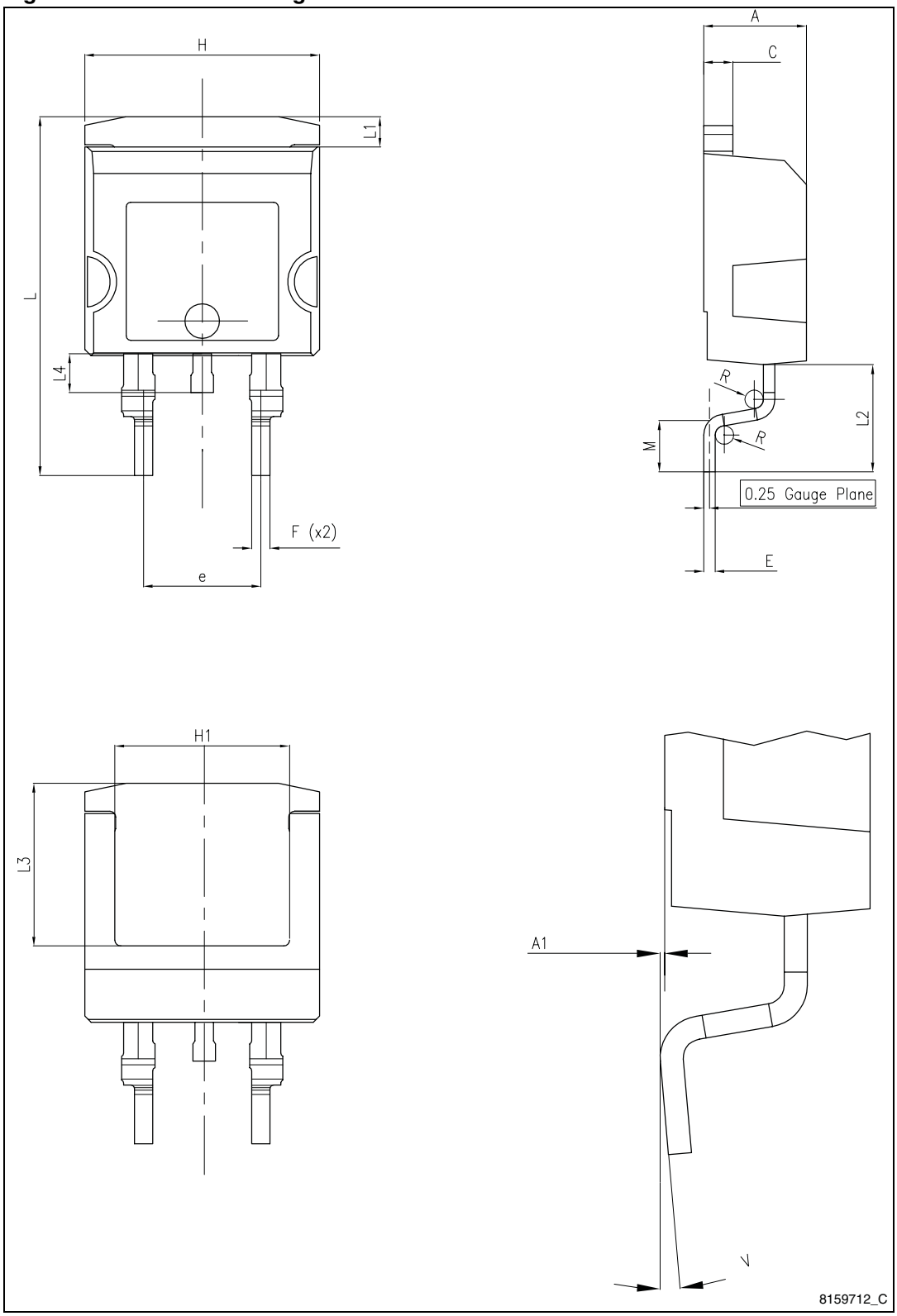


Figure 20. H²PAK-2 recommended footprint (dimensions in mm)

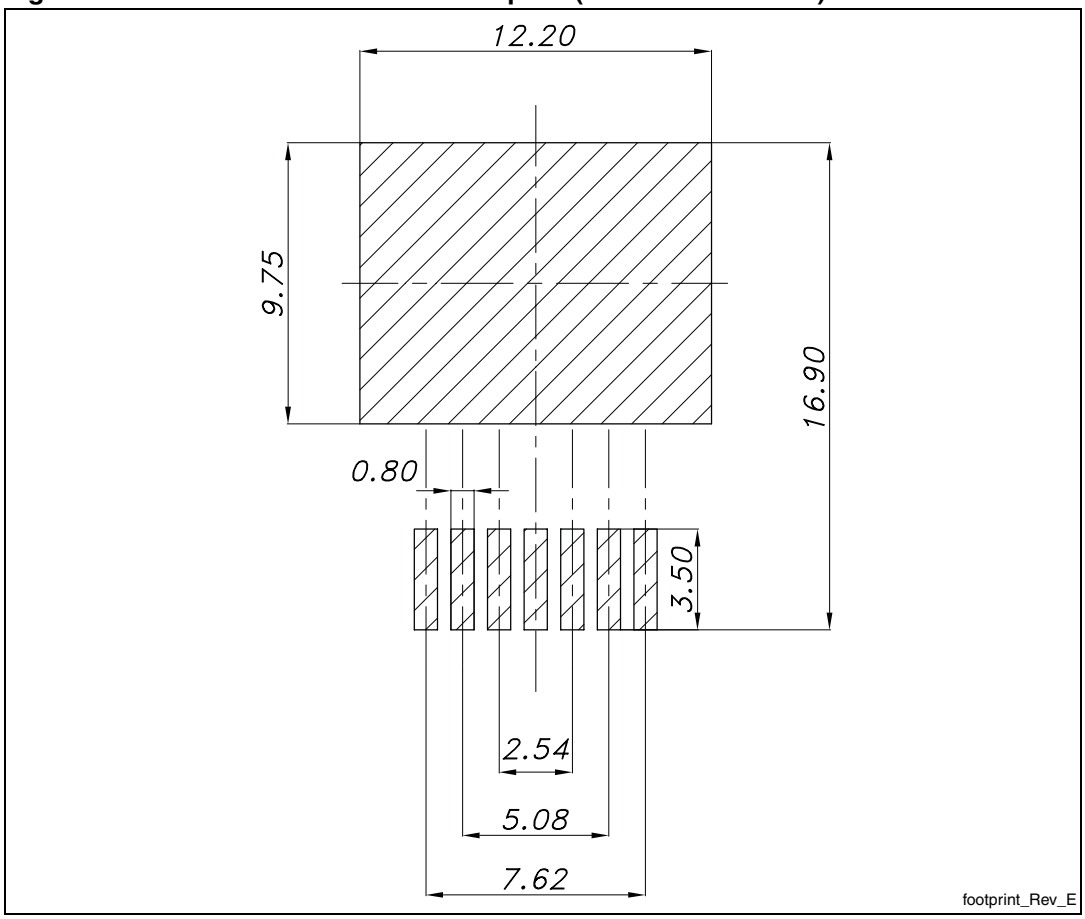


Table 9. H²PAK-6 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00	-	10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 21. H²PAK-6 drawing

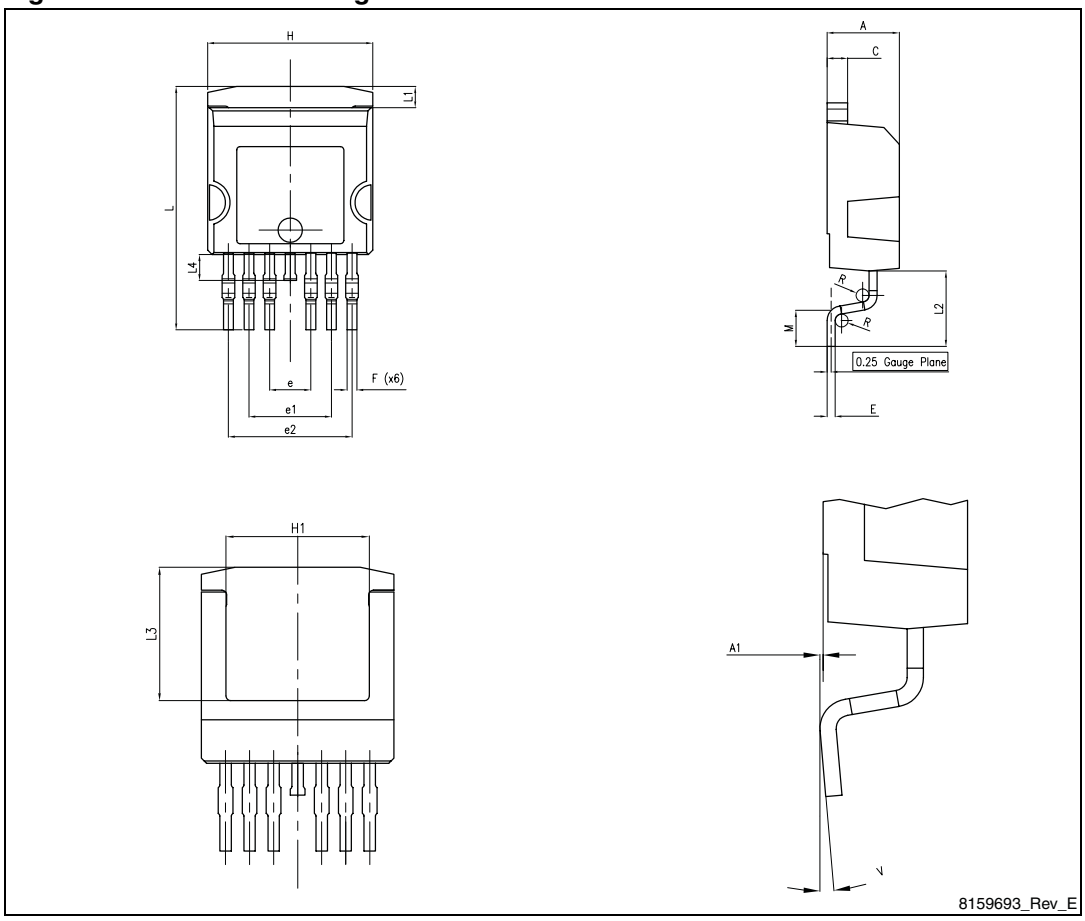
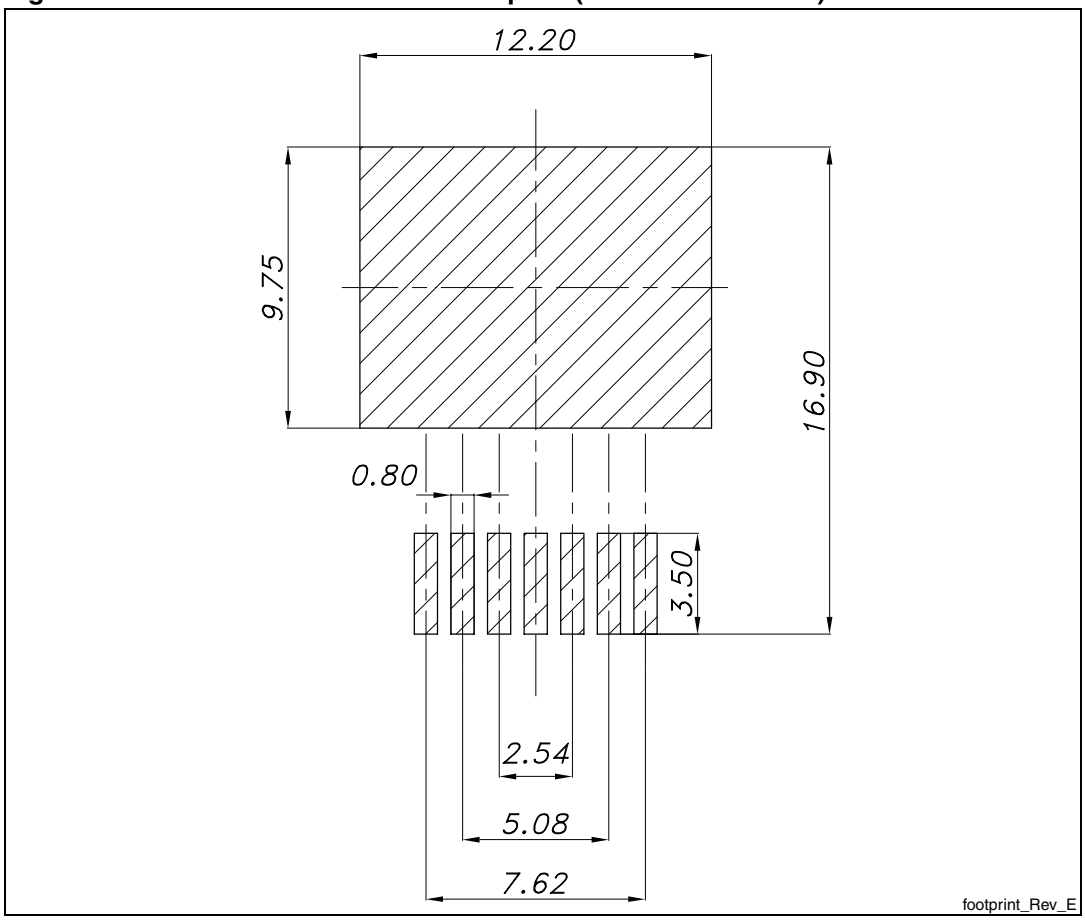


Figure 22. H²PAK-6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Table 10. H²PAK-2 and H²PAK-6 tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 23. Tape

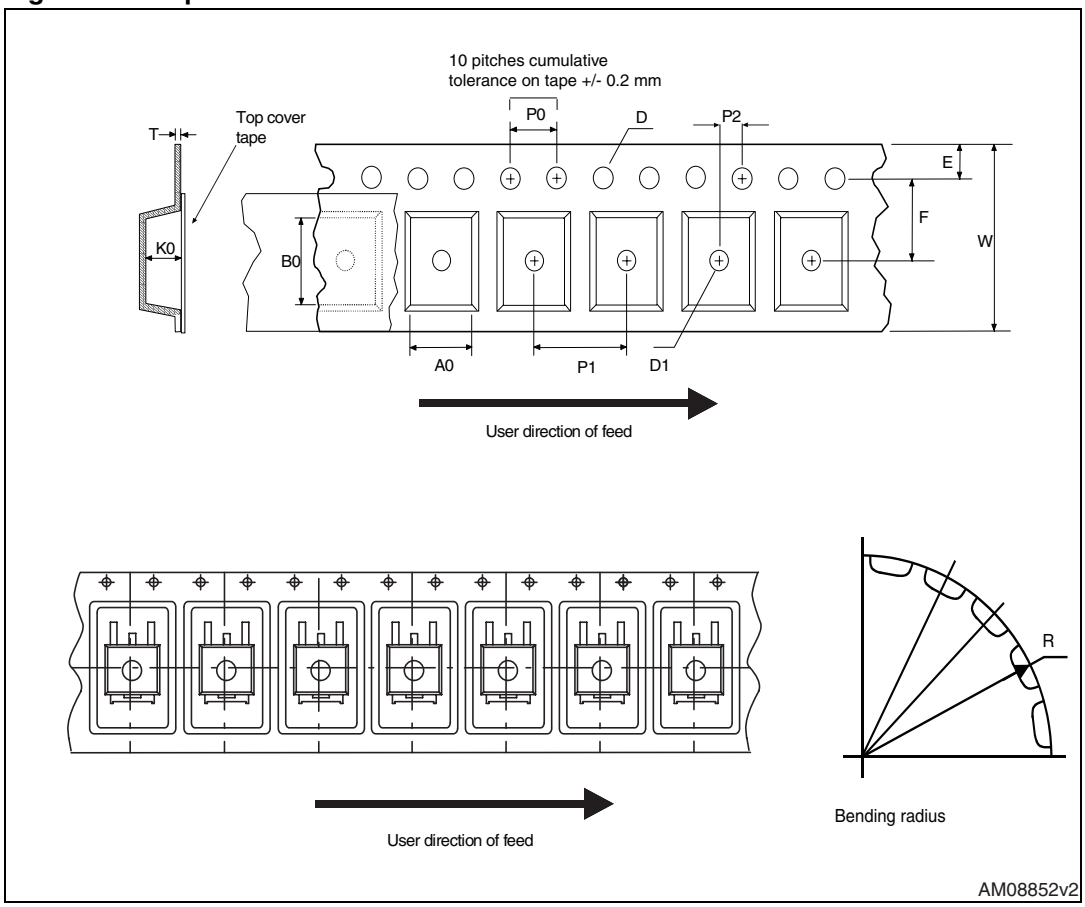
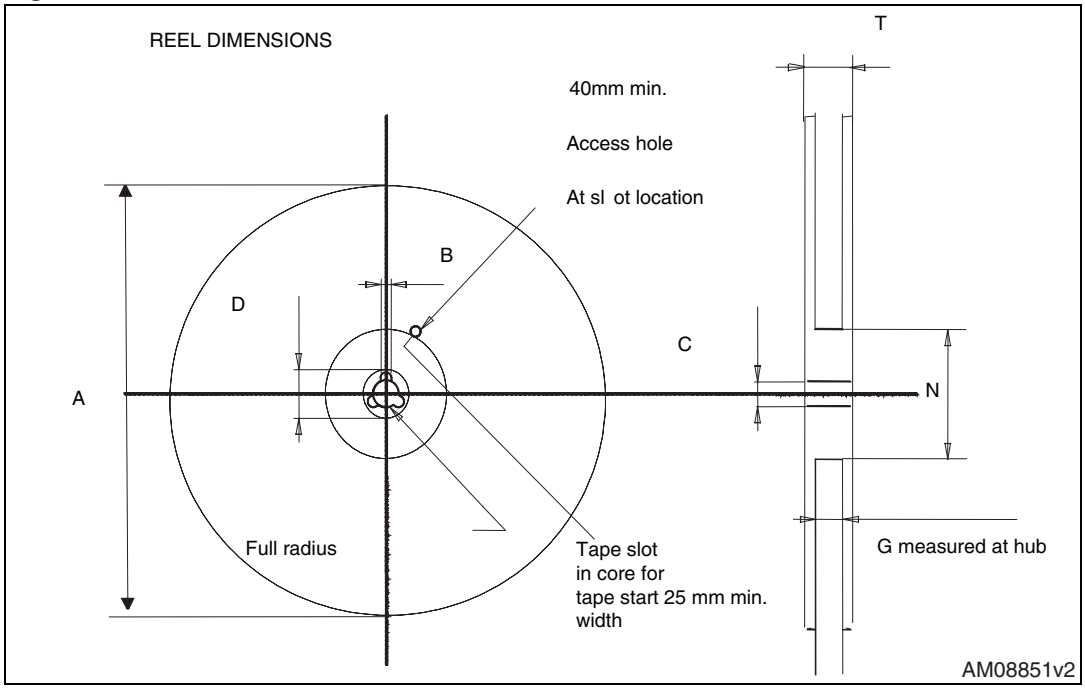


Figure 24. Reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-Oct-2011	1	Initial release.
02-Jul-2012	2	Added new device in H²PAK-2. *Table 1: Device summary* has been modified accordingly. *Table 8: H²PAK-2 mechanical data*, *Figure 19: H²PAK-2 drawing* and *Figure 20: H²PAK-2 recommended footprint (dimensions in mm)* have been added. Minor text changes.