STHVDAC-304M

High voltage BST capacitance controller

Datasheet – production data

Features

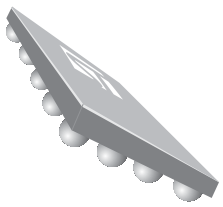
- Dedicated ASIC to control BST tunable capacitances
- Operation compliant with cellular systems requirements
- Integrated boost converter with 4 programmable outputs (from 0 to 30 V)
- Low power consumption
- MIPI RFFE serial interface 1.8 V
- Available in WLCSP for stand-alone or SiP module integration

Benefits

- RF tunable passive implementation in mobile phones to optimize the radiated performance

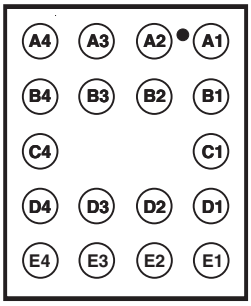
Applications

- Cellular antenna tunable matching network in multi-band GSM/WCDMA mobile phone
- Compatible with open loop antenna tuner applications



Lead-free, Flip Chip (18 bumps)

Figure 1. Pin configuration (bump view)



Description

The ST high voltage BST capacitance controller STHVDAC-304MF3 is a high voltage digital to analog converter (DAC), specifically designed to control and meet the wide tuning bias voltage requirement of the BST tunable capacitors.

It provides 4 independent high voltage outputs, thus having the capability to control 4 different capacitances in parallel. It is fully controlled through an RFFE serial interface.

BST capacitors are tunable capacitors intended for use in mobile phone applications, and dedicated to RF tunable applications. These tunable capacitors are controlled through a bias voltage ranging from 2 to 16 V. The implementation of BST tunable capacitors in mobile phones enables significant improvement in term of radiated performance, making the performance almost insensitive to the external environment.

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1 Electrical characteristics

Table 1. Absolute maximum ratings (limiting value)

Symbol	Parameter	Rating	Unit
AV_{DD}	Analog supply voltage	-0.3 to +5.5	V
VIO	Input/output supply voltage	-0.3 to +2	V
$V_{I/O}$	Input voltage logic lines (DATA, CLK)	-0.5 to VIO + 0.5	V
$V_{ESD\ (HBM)}$	Human body model, JESD22-A114-B, All I/O	2	kV
$V_{ESD\ (CDM)}$	Charge device model, JESD22-C101-C, All I/O	500	V
T_{stg}	Storage temperature range	-55 to +150	°C
T_j	Maximum junction temperature	150	°C

Table 2. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		Min.	Typ.	Max.	
T_{AMB_oP}	Operating ambient temperature	-25	-	+85	°C
AV_{DD}	Analog supply voltage	2.3	-	5	V
VIO	Input/output supply voltage	1.65	-	1.95	V
V_{IH}	Input voltage logic level HIGH (DATA, CLK)	0.7 · VIO	-	VIO + 0.3	V
V_{IL}	Input voltage logic level LOW (DATA, CLK)	-0.3	-	0.35 · VIO	V

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Table 3. DC characteristics

Conditions: AV_{DD} from 2.3 to 5 V, VIO from 1.65 to 1.95 V, T_{amb} from -25 °C to +85 °C unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.(1)**	**Max.**	**Unit**
I_{DD}	AV_{DD} supply current	Shutdown mode			5	µA
		Active mode (4 outputs active)		0.72	1	mA
IIO	VIO supply current	Shutdown mode			10	µA
		Active Mode: (4 outputs active) F_{CLK} = 13 MHz F_{CLK} = 26 MHz			 0.6 1	mA
I_{IH}	Input current logic level HIGH	Any mode, DATA, CLK	-2		2	µA
I_{IL}	Input current logic level LOW	Any mode, DATA, CLK	-2		2	µA

1. Typical value with typical application condition, V_{HV} = 20 V, AV_{DD} = 2.3 V, 25 °C, I_{load} = 4 · 1µA

Table 4. Boost converter characteristics

Conditions: AV_{DD} from 2.3 to 5 V, VIO from 1.65 to 1.95 V, T_{amb} from -25 °C to +85 °C unless otherwise specified)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{hv_low}	Minimum programmable output voltage	Active mode, DAC_boost = 0h		15		V
V_{hv_high}	Maximum programmable output voltage	Active mode, DAC_boost = Fh		30		V
Resolution	Boost voltage resolution	4 bits DAC		1		V
Error	DAC boost error	DAC A, DAC B, DAC C, DAC D	-6		+6	$\%V_{out}$

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Table 5. High voltage DAC output characteristics

Conditions: AV_{DD} from 2.3 to 5 V, VIO from 1.65 to 1.95V, T_{amb} from -25 °C to +85 °C, OUTA, OUTB, OUTC, OUT D, unless otherwise specified)						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
SHUTDOWN MODE						
Z_{out}	OUTA, OUTB, OUTC, OUTD output impedance		7			MΩ
ACTIVE MODE						
V_{OH}	OUTA, OUTB, OUTC, OUTD maximum output voltage	DAC A = DAC B = DAC C = DAC D = 88h DAC_boost = 5h (V_{HV} = 20 V), I_{OH} < 10 µA		16		V
V_{OL}	OUTA, OUTB, OUTC, OUTD minimum output voltage	DAC A = DAC B = DAC C = DAC D = 11h DAC_boost = 5h (V_{HV} = 20 V), I_{OL} < 10 µA		2		V
R_{PD}	OUTA, OUTB, OUTC, OUTD set in pull down mode	DAC A = DAC B = DAC C = DAC D = 00h DAC_boost from 0h to Fh			500	Ω
Resolution	Voltage resolution / OUTA, OUTB, OUTC, OUTD	8 bits DAC, full range 30 V		117		mV
V_{offset}	Zero scale offset	DAC A, DAC B, DAC C and DAC D	-2		+2	LSB
INL	Integral non linearity	DAC A, DAC B, DAC C and DAC D	-3		+3	LSB
DNL	Differential non linearity	DAC A, DAC B, DAC C and DAC D	-0.5		+0.5	LSB
Error	DAC error	DAC A, DAC B, DAC C and DAC D	-6		+6	%V_{out}
I_{sc}	Over current protection	Any DAC output			50	mA

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2 Functional block diagram

Figure 2. HVDAC functional block diagram

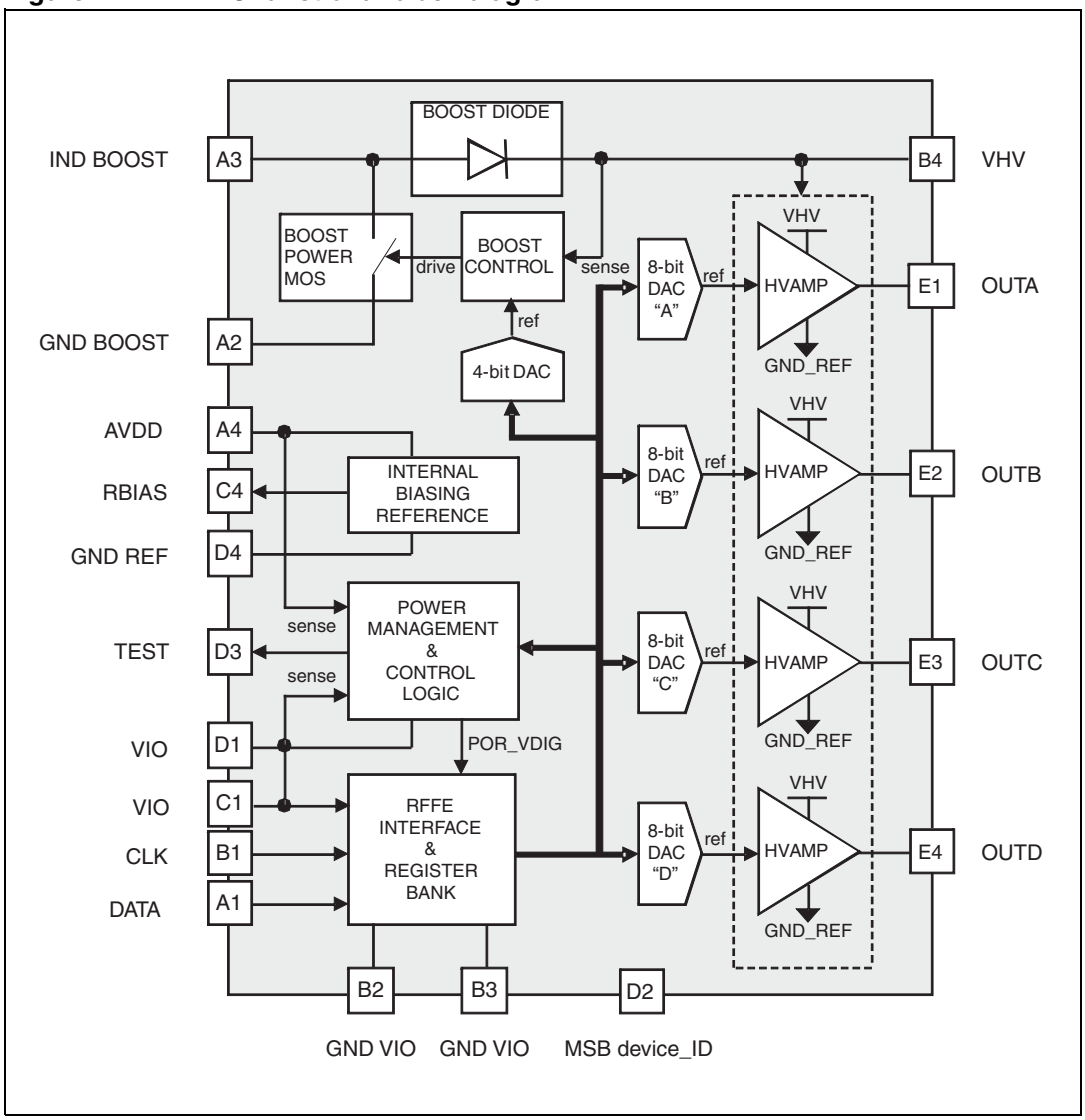

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Table 6. Signal descriptions

Pin number	Pin name	Description
A1	DATA	RFFE Serial interface / Serial DATA
A2	GND_BOOST	Ground
A3	IND_BOOST	Boost inductance
A4	AVDD	Analog supply voltage
B1	CLK	RFFE Serial interface / Serial CLOCK
B2	GND_VIO	Ground
B3	GND_VIO	Ground
B4	VHV	Boost High voltage output
C1	VIO	RFFE IO supply used as Digital supply voltage
C4	Rbias	Biasing reference resistance
D1	VIO	RFFE IO supply used as Digital supply voltage
D2	MSB_device_ID	Device_ID MSB tied GND or VIO
D3	TEST	Test pin / connected to GND in final application
D4	GND_REF	Analog ground
E1	OUTA	High voltage output A
E2	OUTB	High voltage output B
E3	OUTC	High voltage output C
E4	OUTD	High voltage output D

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3 Theory of operation

3.1 HVDAC output voltages

The DAC outputs are directly controlled by programming the 8-bit DAC (DAC A, DAC B, DAC C and DAC D) through the RFFE serial interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high voltage amplifier supplied from the boost converter (see HVDAC block diagram - *Figure 2*).

The DAC output voltages are scaled from 0 to 30 V, with 255 steps of 117 mV (30/255 = 0.11764 V). The nominal DAC output can be approximated to 117 mV x (DAC value).

For performance optimization, it is also possible to control the boost output voltage (V_{HV}) from 15 V to 30 V, by programming register #5 (4 bits / 1 V step). The default power mode is VHV = 15 V so it is recommended to program register #5 to 5h for 20 V.

For proper operation, ST recommends the operation of the DAC outputs 2 V below the actual boost output voltage (V_{HV}), to avoid clamping the HVDAC outputs to the boost output voltage.

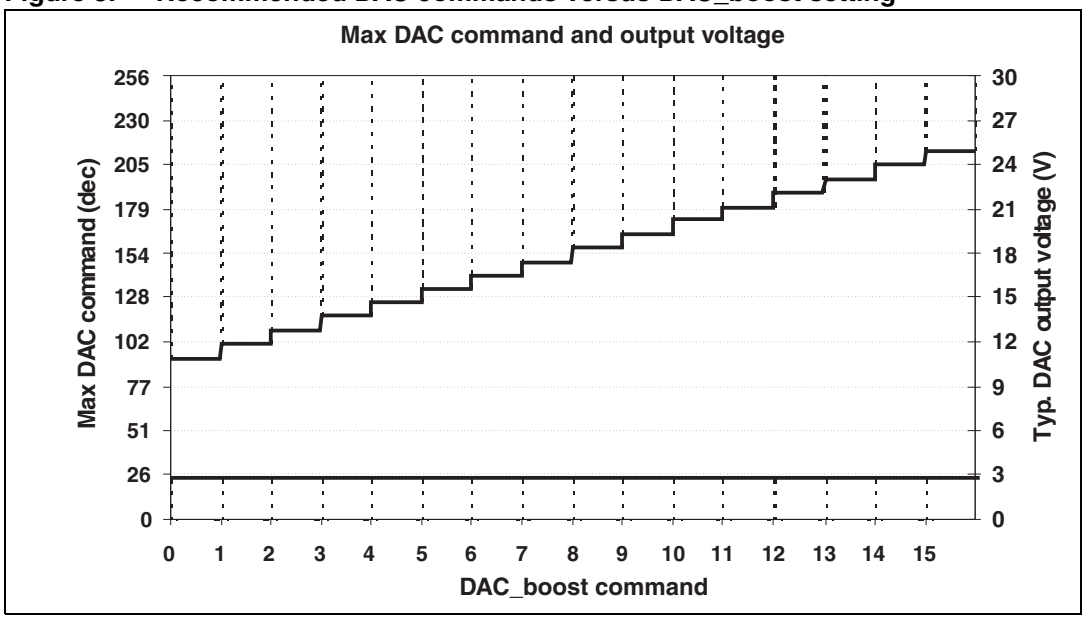
Recommended settings for DAC A, DAC B DAC C and DAC D are described in *Table 5.*, considering the overall HVDAC accuracy. These recommended settings are further described on *Figure 3*

Minimum DAC output voltage is also limited to 2 V, meaning minimum DAC command is equal to 11h (or 17d), independent of the DAC_boost setting.

DAC settings can be programmed outside this recommended operating range, but in this case the HVDAC performance (accuracy and noise) be outside the specified range.

If DAC value is set to 00h, then the corresponding output is directly connected to GND through a pull-down resistor (500 Ω).

Figure 3. Recommended DAC commands versus DAC_boost setting



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3.2 Operating modes

The following operating modes are accessible through the serial interface:

- **Shutdown mode:** The HVDAC is switched off, and all the blocks in the control ASIC are switched off. Power consumption is almost zero in this mode, the DAC outputs are in high Z state. The shutdown mode is set by writing to register 0 through the RFFE serial interface.
- **Active mode:** The HVDAC is switched on and the DAC outputs are fully controlled through the serial interface. The DAC settings can be dynamically modified and the outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or switched off according to application requirements. This mode is set and controlled through RFFE serial interface commands.

3.3 Power-on reset

Power-on reset is implemented on the VIO supply input, ensuring the HVDAC will be reset to default mode once VIO supply line rises above a given threshold (typically 1 V). This trigger will force all registers to their default value.

3.4 RFFE serial interface

The HVDAC is fully controlled through RFFE serial interface (DATA, CLOCK, VIO).

This interface is further described in the next sections of this document and is made compliant to the MIPI alliance specification for RF front end control Interface.

Sequence start condition (SSC): One rising edge followed by falling edge on DATA while CLK remains at logic level low. This is used by the STHVDAC to identify the start of a Command frame.

Parity (P): Each frame shall end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level one, including the parity bit, is odd.

Bus park cycle (BP): The purpose of the bus park cycle is to put the interface into a known state in preparation for a DATA signal control change. A single clock cycle that occurs when the DATA signal control may change between devices. The device releasing DATA will drive the DATA to logic level zero during the first half of the CLK clock cycle. Thereafter, the device releasing DATA shall put its DATA driver into high Z state. The bus park cycle is also used at the end of each command sequence.

3.5 Power-up / down sequence

Table 7 and *Figure 4* describe the HVDAC settling time requirements and recommended timing diagrams.

Switching from shutdown to active mode is triggered by setting the power mode bit in register 0.

Switching from active to shutdown mode is driven by unsetting the power mode bit in register 0.

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Following active mode command, the HVDAC will be operational after T_{active} (max 300 µs). A settling time of 50 µs max (T_{set}) is required following each DAC command in active mode. During this settling time the HVDAC output voltages will vary from the initial to the updated DAC command.

Active mode can be directly activated from shutdown. In any case the HVDAC will be operational only after T_{active} (max 300 µs).

3.6 Power supply sequencing

The ST HVDAC does not require any specific power supply sequencing. It is assumed that the AV_{DD} input will be directly supplied from the battery and will then be the first on.

3.7 Trigger Mode

To meet precise timing requirements and avoid RFFE interface traffic congestion at critical moments, trigger mode has been implemented in the RFFE interface.

Three triggers (TRIG0, TRIG1 and TRIG2) are available and can be controlled through the RFFE interface.

Registers 1 and 2 (DAC D and DAC C) are associated with TRIG0, register 3 (DAC B) is associated with TRIG1 and register 4 (DAC A) is associated with TRIG2. Each trigger can be activated independently.

3.7.1 Trigger mode enabled (default mode)

The different triggers are enabled by unsetting corresponding trigger mask bits in register 28. In this case, once in ACTIVE mode, the following sequence must be followed to control the HVDAC outputs:

- Send any valid register 1/2/3/4 write command sequence. The new register values will be temporarily stored in shadow registers
- Send a register28 write command sequence, setting trigger 2/1/0 bits and keeping trigger mask 2/1/0 bits low. The shadow registers will be loaded to destination registers and this will trigger the corresponding DAC outputs to their new values.

3.7.2 Trigger mode disabled

The different triggers are disabled by setting corresponding trigger mask bits in register 28.

In this case, any valid register 1/2/3/4 write command sequence is directly loaded to the destination register, directly triggering the corresponding DAC output to its new value.

3.8 Settling time

The STHVDAC will set the bias voltage of the tuner within 50µs after:

- Bus park (BP) of register28 write sequence data frame if trigger mode is enabled,
- Bus park (BP) of register1/2/3/4 write sequence data frame if trigger mode is disabled.

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3.9 Timing parameters

Table 7. Timing parameters for OUT A, OUT B, OUT C, OUT D

Conditions: AV_{DD} from 2.3 to 5 V, V_{IO} from 1.65 to 1.95 V, T_{amb} from -25 °C to +85 °C				
Symbol	**Parameter**	**Conditions**	**max.**	**Unit**
T_{active}	Activation time	Internal voltages activation time from shutdown to active mode C_{hv} = 22 nF at V_{HV}, default power mode	300	µs
T_{set+}	DAC outputs positive settling time	Positive settling time at 5%, equivalent load of 15 kΩ and 2 nF with C_{hv} = 22nF	50	µs
T_{set-}	DAC outputs negative settling time	Negative settling time at 5%, equivalent load of 15 kΩ and 2 nF with C_{hv} = 22nF	50	µs

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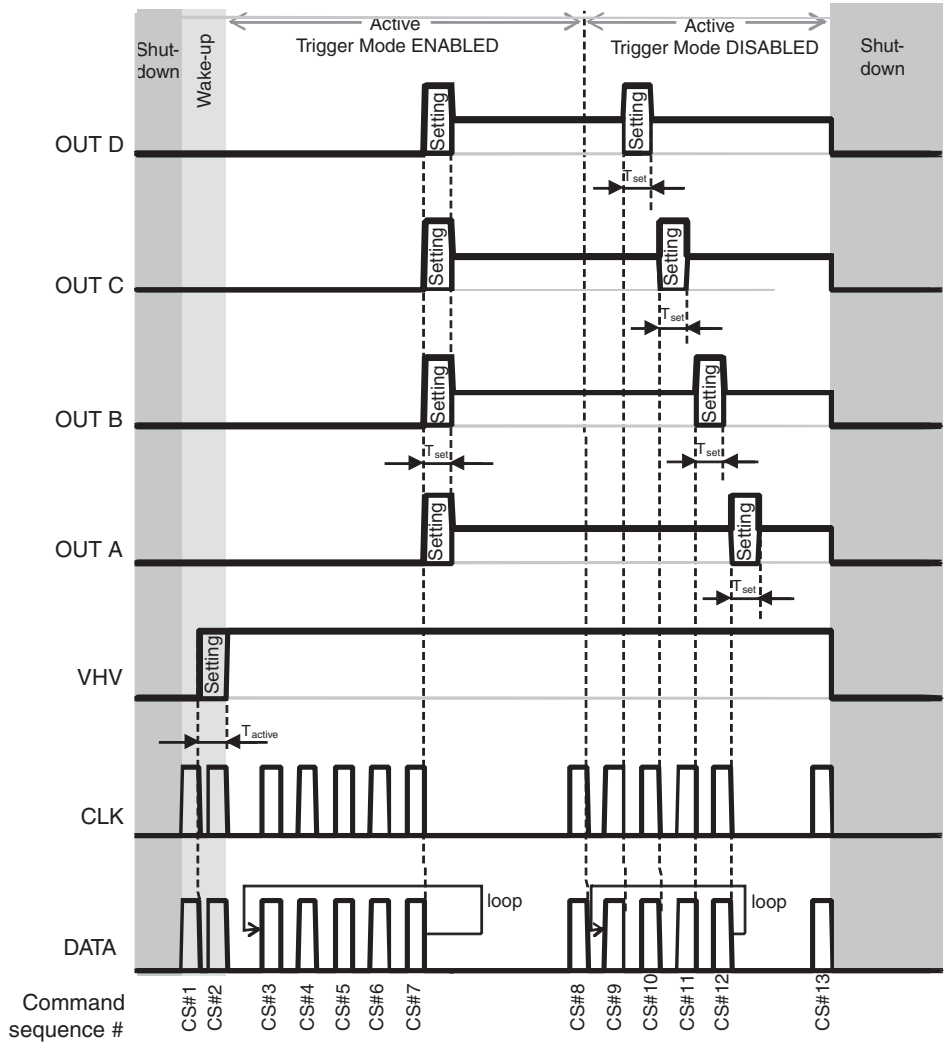
Figure 4. Timing diagram example



CS #	Description
1	Write REG0 - switch to ACTIVE mode
2	Write REG5 - program DAC_BOOST
3	Write REG1 - program DAC D
4	Write REG2 - program DAC C
5	Write REG3 - program DAC B
6	Write REG4 - program DAC A
7	Write REG28 - set the triggers
loop	Back to CS#3 to run loop mode, trigger enabled
8	Write REG28 - disable the triggers
9	Write REG1 - program DAC D
10	Write REG2 - program DAC C
11	Write REG3 - program DAC B
12	Write REG4 - program DAC A
loop	Back to CS#9 to run loop mode, trigger disabled
13	Write REG0 - switch to SHUTDOWN mode

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4 Register table

The HVDAC provides 8-bit registers. Register content is described in *Table 8*, and register default values are provided in *Table 9*.

Table 8. Register table

Reg #	Address	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type	Triggered
0	[00000]	Reserved		PWR Mode	Reserved	DAC A	DAC B	DAC C	DAC D	RW	no
1	[00001]	DAC D								RW	TRIG0
2	[00010]	DAC C								RW	TRIG0
3	[00011]	DAC B								RW	TRIG1
4	[00100]	DAC A								RW	TRIG2
5	[00101]	Reserved				DAC_BOOST				RW	no
28	[11100]	Reserved		Trig mask 2	Trig mask 1	Trig mask 0	TRIG2	TRIG1	TRIG0	RW	no
29	[11101]	Product ID								R	no
30	[11110]	Manufacturer ID [7,0]								R	no
31	[11111]	0	0	Manufacturer ID [9,8]		USID				RW	no

Table 9. Register default values

Reg #	Address	D7	D6	D5	D4	D3	D2	D1	D0
0	[00000]	0	0	0	0	0	0	0	0
1	[00001]	0	0	0	0	0	0	0	0
2	[00010]	0	0	0	0	0	0	0	0
3	[00011]	0	0	0	0	0	0	0	0
4	[00100]	0	0	0	0	0	0	0	0
5	[00101]	0	0	0	0	0	0	0	0
28	[11100]	0	0	0	0	0	0	0	0
29	[11101]	(1)	0	0	0	0	0	0	1
30	[11110]	0	0	0	0	0	1	0	0
31	[11111]	0	0	0	1	0	1	1	1

1. Reg #29 - D7 (MSB DEVICE ID) default value is directly tied to MSB_device_ID pin. This bit is set to 1 if MSB_device_ID pin is tied to VIO, and set to 0 if MSB_device_ID pin is tied to GND.

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5 RFFE interface

5.1 Register content description

Register content and control are described in Tables *10* to *13*.

Table 10. HVDAC mode selection - Reg#0

D7	D6	D5	D4	D3	D2	D1	D0	Comments
Reserved		PWR mode	Reserved	DAC A	DAC B	DAC C	DAC D	
0	0	0	0	X	X	X	X	Shutdown mode
0	0	1	0	0	0	0	0	Active mode / DAC outputs in high Z state
0	0	1	0	1	1	1	1	Active mode / DAC outputs in enabled

Table 11. HVDAC boost control- Reg#5

D7	D6	D5	D4	D3	D2	D1	D0	Comments
Reserved				DAC_BOOST				
0	0	0	0	0	0	0	0	V_{hv} = 15 V
0	0	0	0	0	0	0	1	V_{hv} = 16 V
0	0	0	0	0	0	1	0	V_{hv} = 17 V
0	0	0	0	0	0	1	1	V_{hv} = 18 V
0	0	0	0	0	1	0	0	V_{hv} = 19 V
0	0	0	0	0	1	0	1	V_{hv} = 20 V
0	0	0	0	0	1	1	0	V_{hv} = 21 V
0	0	0	0	0	1	1	1	V_{hv} = 22 V
0	0	0	0	1	0	0	0	V_{hv} = 23 V
0	0	0	0	1	0	0	1	V_{hv} = 24 V
0	0	0	0	1	0	1	0	V_{hv} = 25 V
0	0	0	0	1	0	1	1	V_{hv} = 26 V
0	0	0	0	1	1	0	0	V_{hv} = 27 V
0	0	0	0	1	1	0	1	V_{hv} = 28 V
0	0	0	0	1	1	1	0	V_{hv} = 29 V
0	0	0	0	1	1	1	1	V_{hv} = 30 V

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Table 12. HVDAC trigger control register - Reg#28

D7	D6	D5	D4	D3	D2	D1	D0	Comments
Reserved		Trig mask 2	Trig mask 1	Trig mask 0	TRIG2	TRIG1	TRIG0	
0	0	0	0	0	0	0	0	Triggers 2, 1, and 0 are unmasked. Triggers 2, 1, and 0 are disabled.
0	0	0	0	0	1	1	1	Triggers 2, 1, and 0 are unmasked. Triggers 2, 1, and 0 are enabled.
0	0	1	1	1	0	0	0	Triggers 2, 1, and 0 are masked.

Table 13. HVDAC unique slave identifier control- Reg#31

D7	D6	D5	D4	D3	D2	D1	D0	Comments
Spare		Manufacturer ID [9,8]		USID				
0	0	0	1	0	1	1	1	Default value
0	0	0	1	X	X	X	X	USID can be modified by RFFE master, see detailed programming procedure in MIPI RFFE specification.

5.2 Command and data frame structure

The STHVDAC-304MF3 RFFE interface has been implemented to support the following command sequences:

- Register 0 WRITE
- Register WRITE
- Register READ

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These supported command sequences are described in *Table 14*.

Table 14. Supported command sequences

	SSC(1)			Command frame									Data frame										
						Data [6,0]																	
Register 0 WRITE	0	1	0	USID(2)	1	0	Power mode	0	DAC A	DAC B	DAC C	DAC D	P(3)	BP(4)									
Register WRITE	0	1	0	USID	0	1	0	Reg address [4,0]					P	Data [7,0]								P	BP
Register READ	0	1	0	USID	0	1	1	Reg address [4,0]					P	BP	Data [7,0]							P	BP

1. SSC: Sequence start condition
2. USID: Unique slave identifier
3. P: Parity bit
4. BP: Bus park cycle

All frames are required to end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level 1, including the parity bit, is odd. In case the device detects a parity error, the frame is considered not valid and is ignored.

Table 15 shows a typical set of command sequences to start up and initialize the device, control the HVDAC outputs, either in triggered or untriggered mode, and then switch off the device.

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Table 15. Typical command sequences

CS#	Description	SSC			Command frame														Data frame									
					USID				R/W			Reg address [4,0]					P		Data [7,0]								P	BP
1	Write REG0 - switch to active mode	0	1	0	0	1	1	1	0	1	0	0	0	0	0	0	1		0	0	1	0	1	1	1	1	0	BP
2	Write REG5 - program DAC_BOOST	0	1	0	0	1	1	1	0	1	0	0	0	0	0	1	1		0	0	0	0	0	1	0	1	1	BP
3	Write REG1 - program DAC D	0	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0		0	0	0	0	0	0	0	0	1	BP
																			DAC D value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
4	Write REG2 - program DAC C	0	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0		0	0	0	0	0	0	0	0	1	BP
																			DAC C value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
5	Write REG3 - program DAC B	0	1	0	0	1	1	1	0	1	0	0	0	0	1	1	1		0	0	0	0	0	0	0	0	1	BP
																			DAC B value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
6	Write REG4 - program DAC A	0	1	0	0	1	1	1	0	1	0	0	0	1	0	0	0		0	0	0	0	0	0	0	0	1	BP
																			DAC A value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
7	Write REG28 - set the triggers	0	1	0	0	1	1	1	0	1	0	1	1	1	0	0	0		0	0	0	0	0	1	1	1	0	BP
Back to CS#3 to run in loop mode, trigger enabled																												
8	Write REG28 - disable the triggers	0	1	0	0	1	1	1	0	1	0	1	1	1	0	0	0		0	0	1	1	1	0	0	0	0	BP
9	Write REG1 - program DAC D	0	1	0	0	1	1	1	0	1	0	0	0	0	0	1	0		0	0	0	0	0	0	0	0	1	BP
																			DAC D value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
10	Write REG2 - program DAC C	0	1	0	0	1	1	1	0	1	0	0	0	0	1	0	0		0	0	0	0	0	0	0	0	1	BP
																			DAC C value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
11	Write REG3 - program DAC B	0	1	0	0	1	1	1	0	1	0	0	0	0	1	1	1		0	0	0	0	0	0	0	0	1	BP
																			DAC B value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
12	Write REG4 - program DAC A	0	1	0	0	1	1	1	0	1	0	0	0	1	0	0	0		0	0	0	0	0	0	0	0	1	BP
																			DAC A value								P	BP
																			1	1	1	1	1	1	1	1	1	BP
back to CS#9 to run in loop mode, trigger disabled																												
13	Write REG0 - switch to shutdown mode	0	1	0	0	1	1	1	0	1	0	0	0	0	0	0	1		0	0	0	0	0	0	0	0	1	BP

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6 Serial interface specification

Table 16. Interface specifications

Conditions: AV_{dd} from 2.3 to 5 V, VIO from 1.65 to 1.95 V, T_{amb} from -25 °C to +85 °C, unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
F_{CLK}	Clock frequency				26	MHz
T_{CLK}	Clock period		38.4			ns
T_{HIGH}	Clock high time		11.25			ns
T_{LOW}	Clock low time		11.25			ns
TD_{setup}	DATA setup time	Relative to 30% of CLK falling edge	1			ns
TD_{hold}	DATA hold time	Relative to 70% of CLK falling edge	5			ns
C_{CLK}	CLK pin input capacitance				5	pF
C_{DATA}	DATA pin input capacitance				5	pF

Figure 5. Register WRITE command sequence

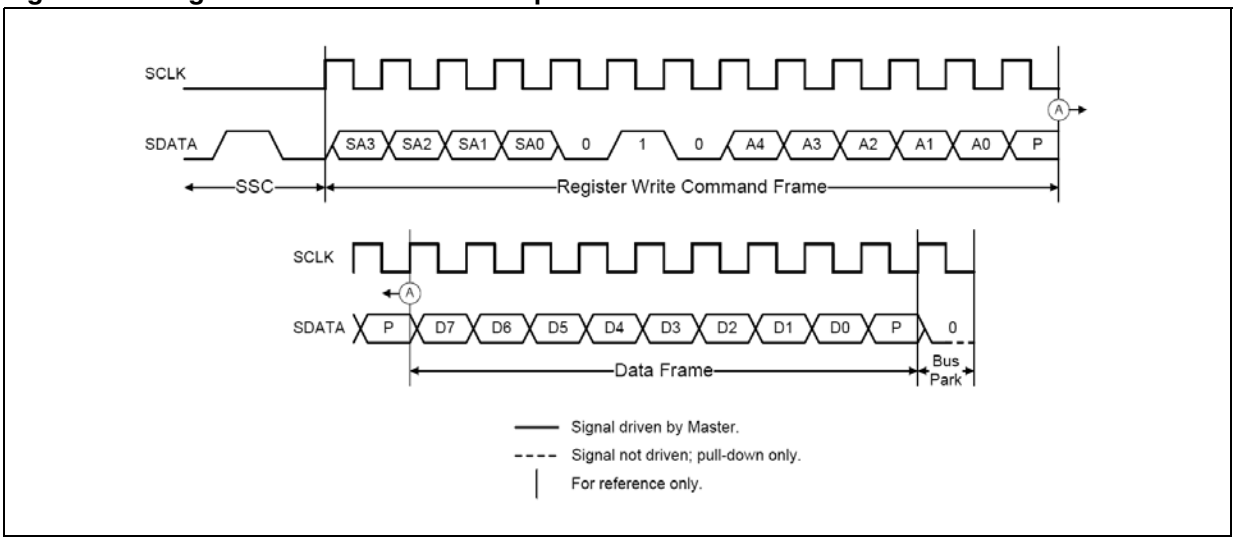

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Figure 6. Register Read command sequence

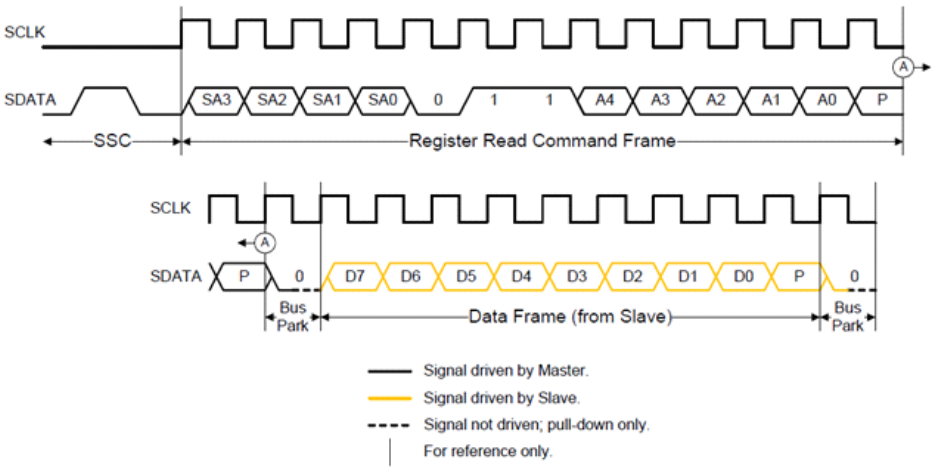
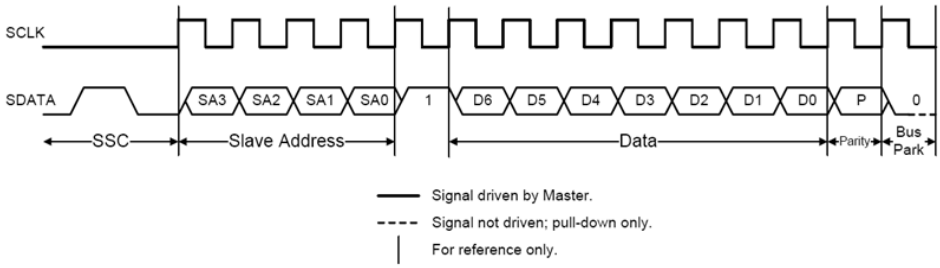


Figure 7. Register 0 WRITE command sequence



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7 Application information

Figure 8. Recommended application schematic

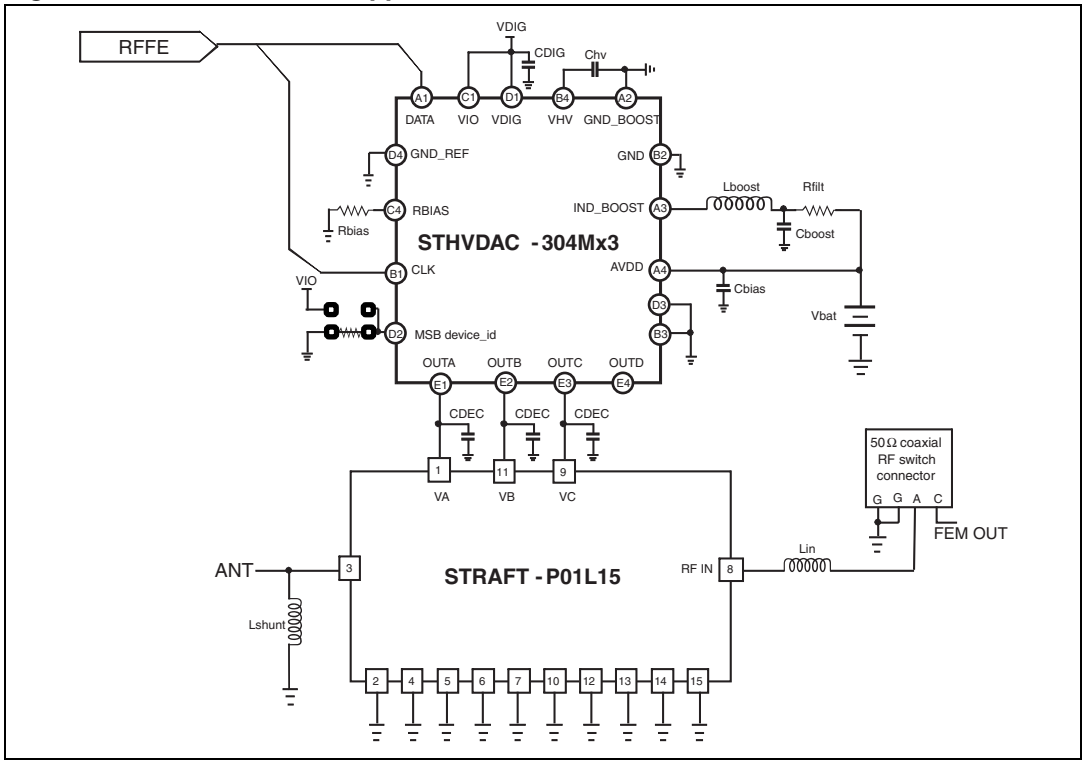

Figure 9. Recommended PCB layout

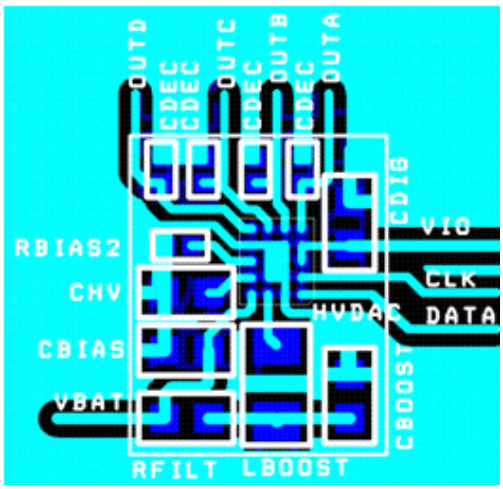

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Table 17. Recommended external BOM

Component	Description	Nominal value	Package (inch)	Package (mm)	Recommended P/N
C_{boost}	Boost supply capacitor	1 µF	0402	1005	Murata: GRM155R60J105KE19D
L_{boost}	Boost inductance	15 µH	0603	1608	COILCRAFT: 0603LS-153XGL
				2014	ABCO: LPS181210T-150M
R_{filt}	Decoupling resistor, 5%	3.3 Ω	0402	1005	Vishay: CRCW04023R30JNED
C_{dig}	Digital supply decoupling	100 nF	0402	1005	Murata: GRM155R71C104KA88D
C_{bias}	Analog supply decoupling	1 µF	0402	1005	Murata: GRM155R60J105KE19D
R_{bias}	Reference bias resistor, 1%	110 kΩ	0201	0603	Multicomp: MCRE000189
C_{hv}	Boost output capacitance, 50 V	22 nF	0402	1005	Murata: GRM155R71H223KA12 Semco: CL21B223KBCNNNC
C_{dec}	Decoupling capacitance, 50 V	100 pF	0201	0603	TDK: C0603COG1H101J

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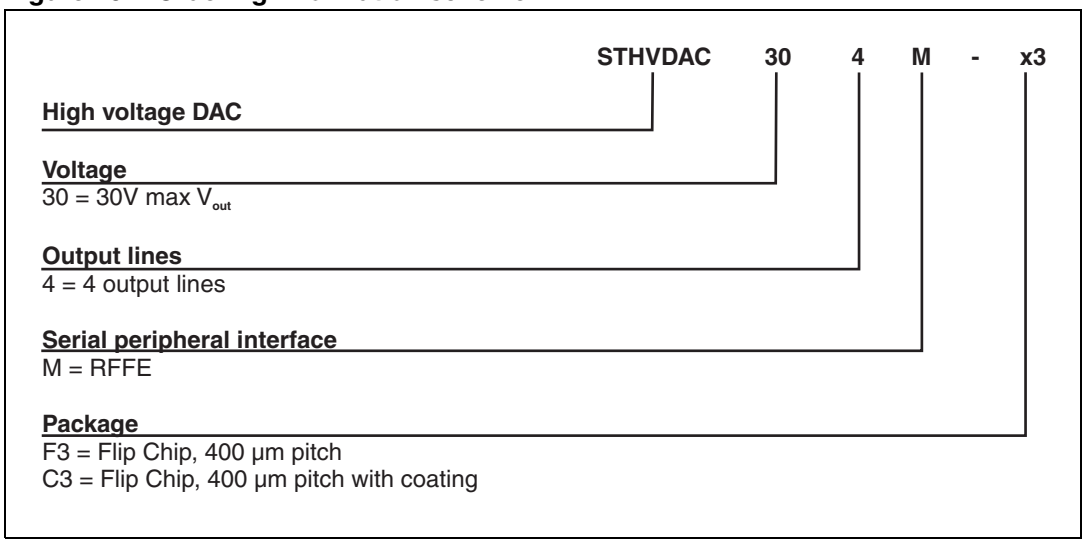
8 Ordering information schemes

Figure 10. Ordering information scheme



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9 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 11. Package dimensions

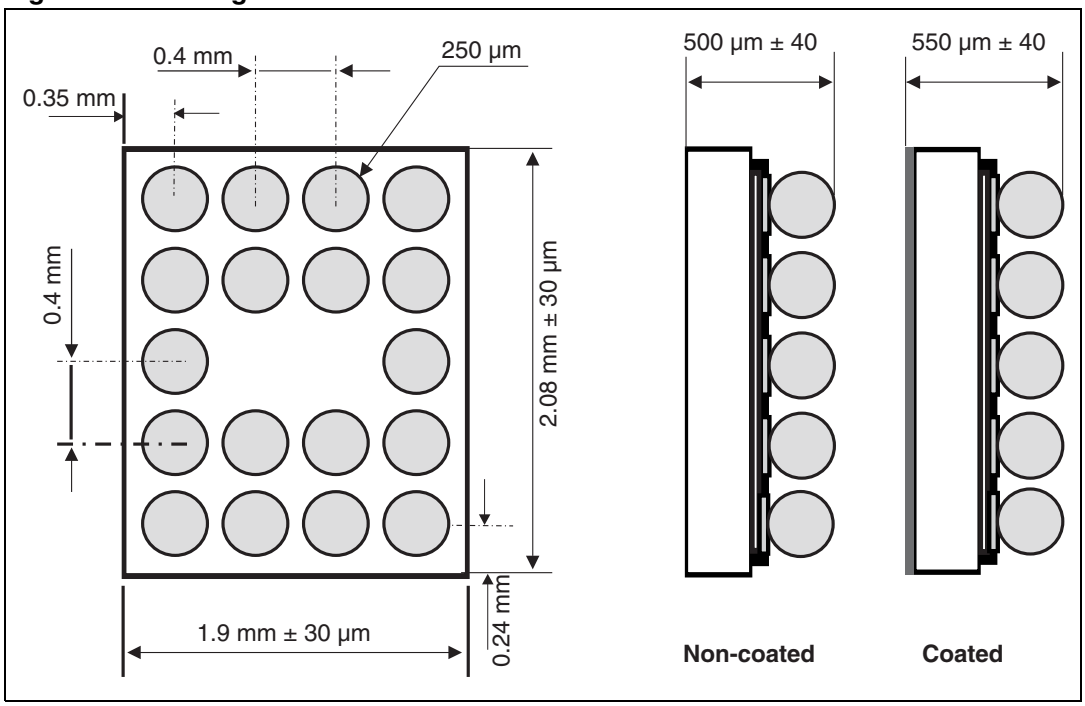

Figure 12. Footprint

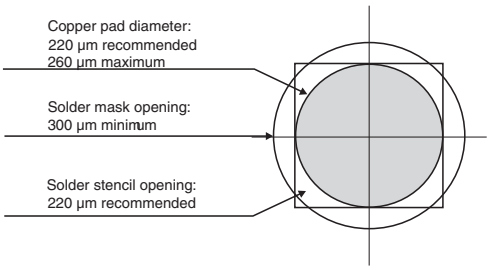

Figure 13. Marking

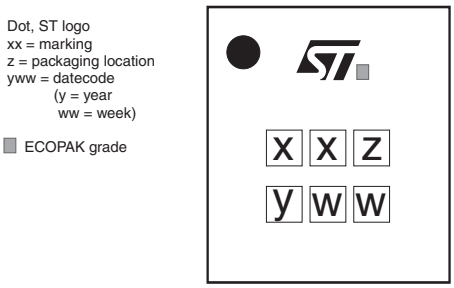

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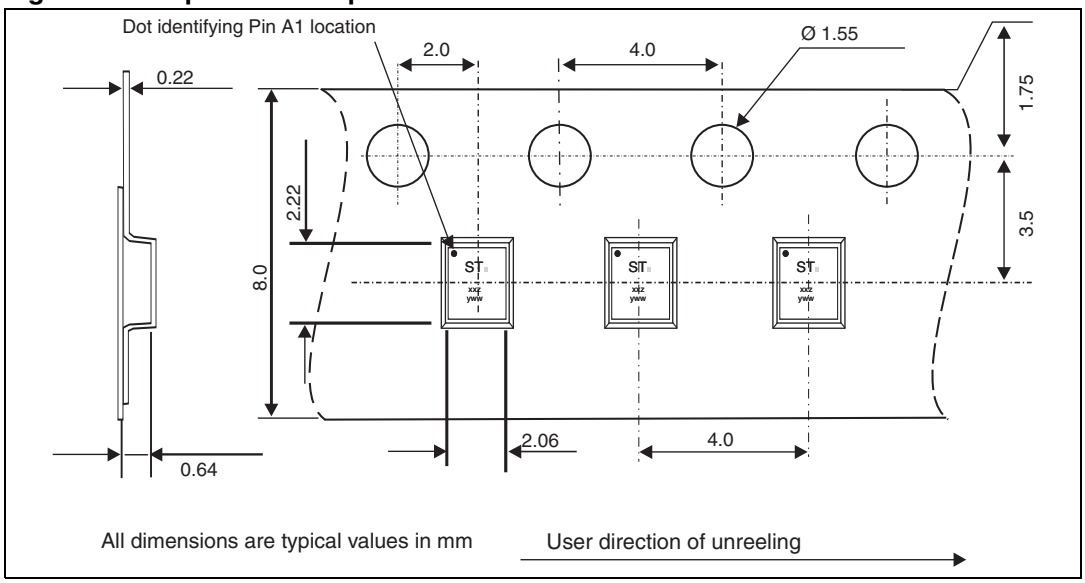
Figure 14. Tape and reel specification



10 Ordering information

Table 18. Ordering information

Order code	RFFE	Marking	Package	Weight	Base qty	Delivery mode
STHVDAC-304MF3	with triggers	PF	Flip Chip	3.8 mg	5000	Tape and reel
STHVDAC-304MC3	with triggers	PG	Coated Flip Chip	4 mg	5000	Tape and reel

Note: More information is available in the STMicroelectronics Application note: AN2348: "400 µm Flip Chip: Package description and recommendations for use"

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11 Revision history

Table 19. Document revision history

Date	Revision	Changes
10-Apr-2012	1	Initial release.
05-Nov-2012	2	Updated document status.

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