STL52N25M5

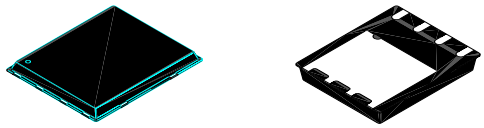
N-channel 250 V, 0.064 Ω, 28 A, PowerFLAT™ (5x6) MDmesh™ V Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max.	I_D(1)
STL52N25M5	250 V	< 0.076 Ω	28 A

1. This value is rated according $R_{thj\text{-}case}$.

- Amongst the best $R_{DS(on)}$* area
- Very low profile package (1 mm max.)
- Excellent switching performance
- High dv/dt capability
- 100% avalanche tested



PowerFLAT™ (5x6)

Application

Switching applications

Description

This device is N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Figure 1. Internal schematic diagram

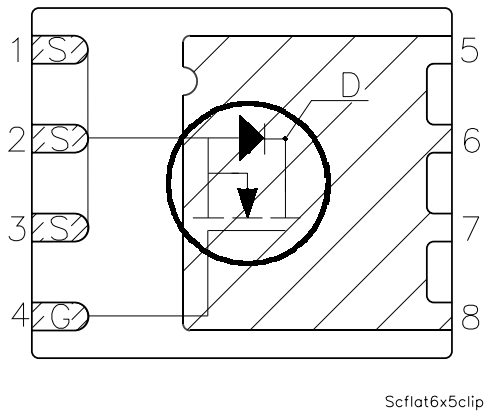


Table 1. Device summary

Order code	Marking	Package	Packaging
STL52N25M5	52N25M5	PowerFLAT™ (5x6)	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	28	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	18	A
I_{DM} (1),(2)	Drain current (pulsed)	112	A
I_D (3)	Drain current (continuous) at T_C = 25 °C	4.2	A
I_D (3)	Drain current (continuous) at T_C = 100 °C	2.6	A
I_{DM} (2),(3)	Drain current (pulsed)	16.8	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	110	W
P_{TOT} (3)	Total dissipation at T_C = 25 °C	2.5	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	230	mJ
dv/dt(4)	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	°C

1. This value is rated according $R_{thj\text{-}case}$.
2. Pulse width limited by safe operating area.
3. This value is rated according $R_{thj\text{-}a}$.
4. $I_{SD} \leq 28$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 150 V, $V_{Peak} < V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj\text{-}a}$ (1)	Thermal resistance junction-amb max	50	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	250			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C				1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 13 A		0.064	0.076	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	1770 110 17	-	pF pF pF
$C_{o(er)}$(1)	Equivalent output capacitance energy related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	93	-	pF
$C_{o(tr)}$(2)	Equivalent output capacitance time related	V_{GS} = 0, V_{DS} = 0 to 80% $V_{(BR)DSS}$	-	178	-	pF
R_g	Gate input resistance	f=1 MHz open drain	-	2.5	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 200 V, I_D = 28 A, V_{GS} = 10 V *(see Figure 14)*	-	47 10 24	-	nC nC nC

1. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
2. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	V_{DD} = 125 V, I_D = 14 A,		40		ns
$t_{r(V)}$	Voltage rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	18	-	ns
$t_{f(i)}$	Current fall time	*(see Figure 13)*		64		ns
$t_{c(off)}$	Crossing time	*(see Figure 18)*		82		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		28	A
I_{SDM} (1)	Source-drain current (pulsed)				112	A
V_{SD} (2)	Forward on voltage	I_{SD} = 28 A, V_{GS} = 0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/µs		168		ns
Q_{rr}	Reverse recovery charge	V_{DD}= 60 V, T_J = 25 °C	-	1.2		µC
I_{RRM}	Reverse recovery current	*(see Figure 15)*		14.5		A
t_{rr}	Reverse recovery time	I_{SD} = 28 A, di/dt = 100 A/µs		196		ns
Q_{rr}	Reverse recovery charge	V_{DD}= 60 V T_J = 150 °C	-	1.7		µC
I_{RRM}	Reverse recovery current	*(see Figure 15)*		17		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

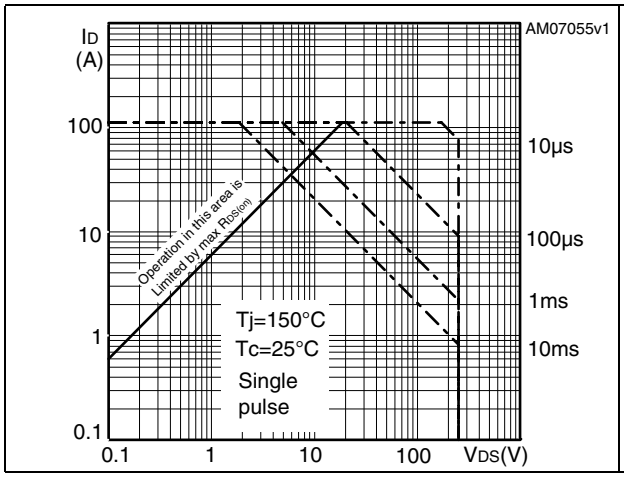


Figure 3. Thermal impedance

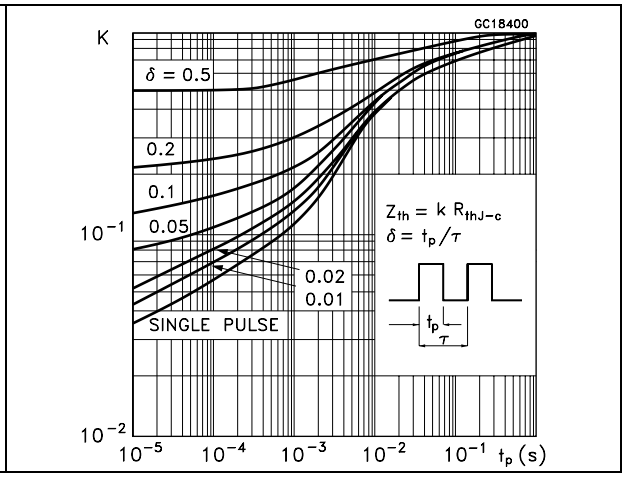


Figure 4. Output characteristics

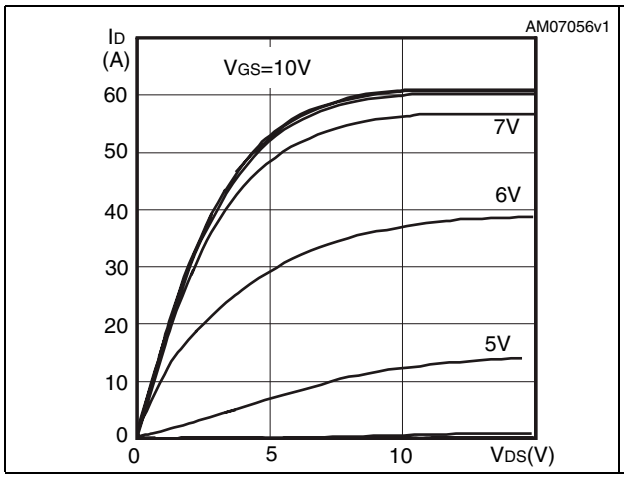


Figure 5. Transfer characteristics

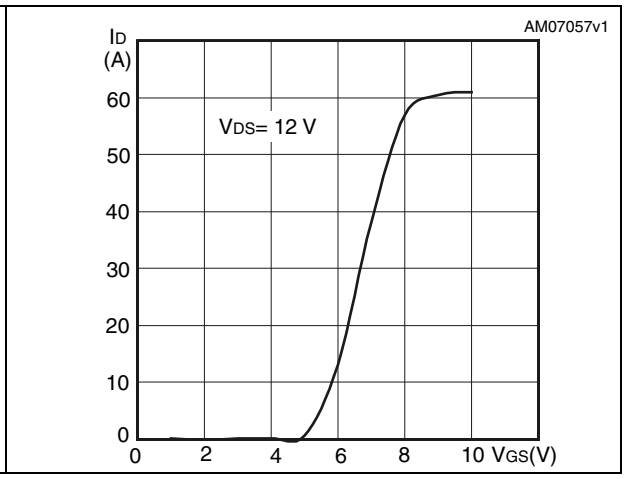


Figure 6. Gate charge vs gate-source voltage

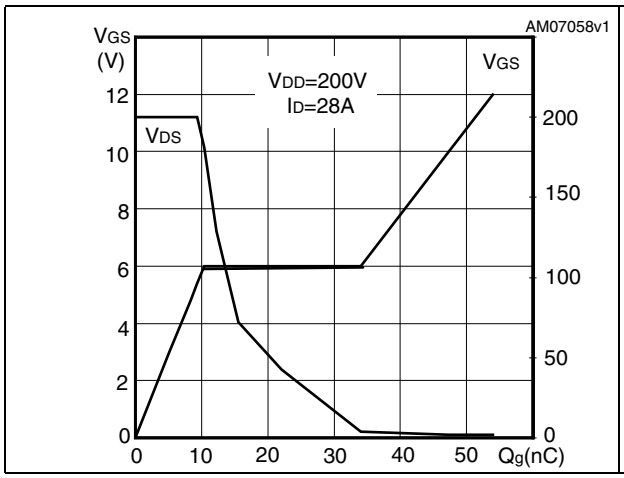


Figure 7. Static drain-source on resistance

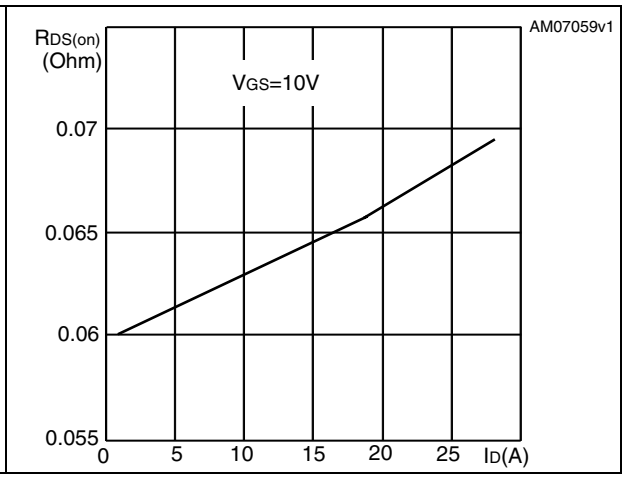


Figure 8. Capacitance variations

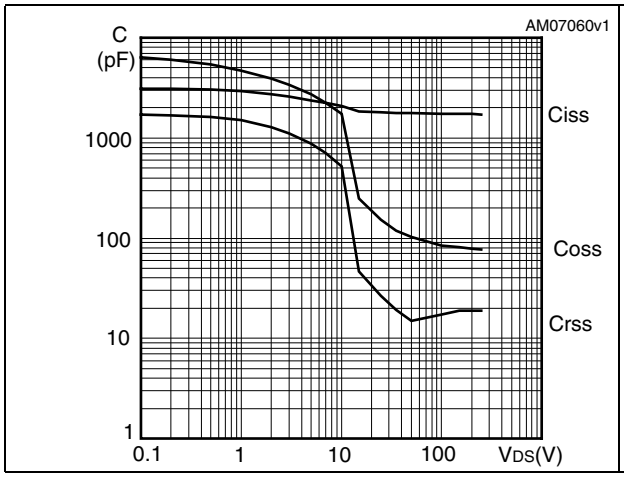


Figure 9. Output capacitance stored energy

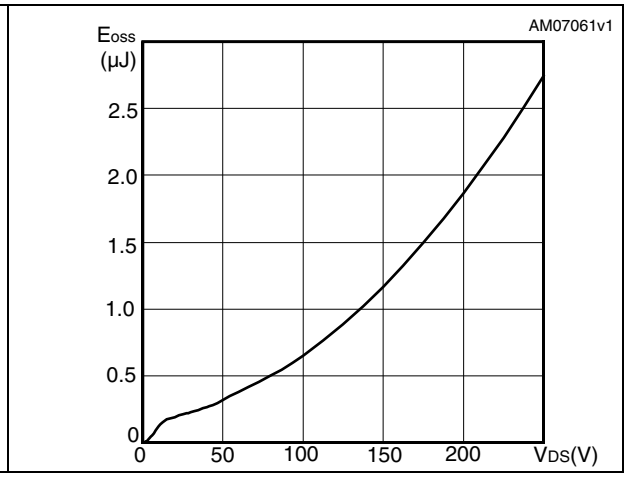


Figure 10. Normalized gate threshold voltage vs temperature

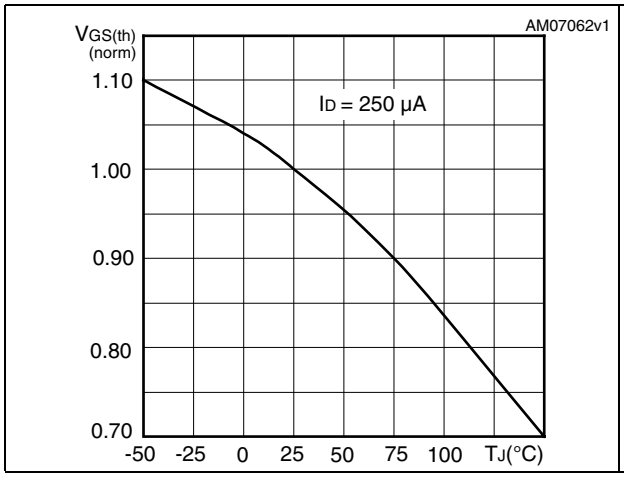


Figure 11. Normalized on resistance vs temperature

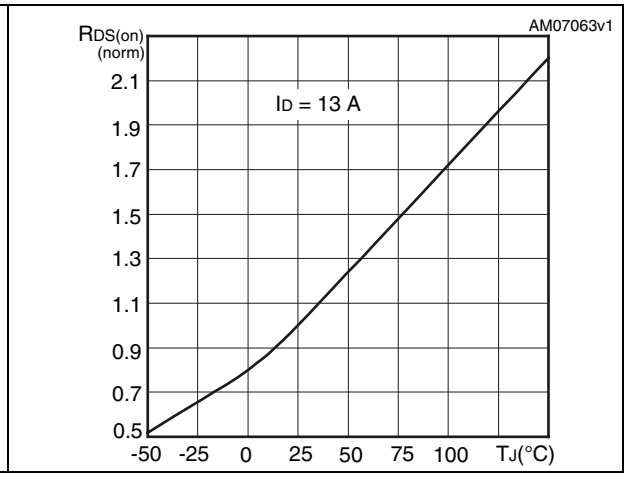
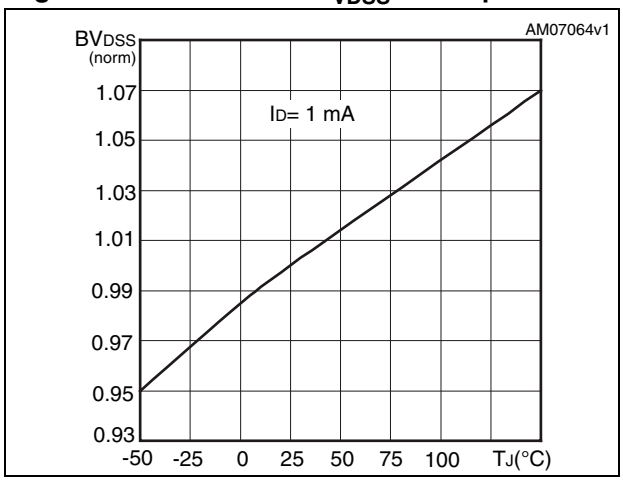


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

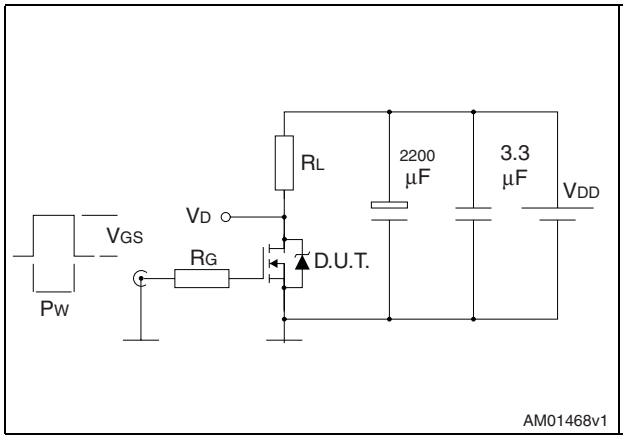


Figure 14. Gate charge test circuit

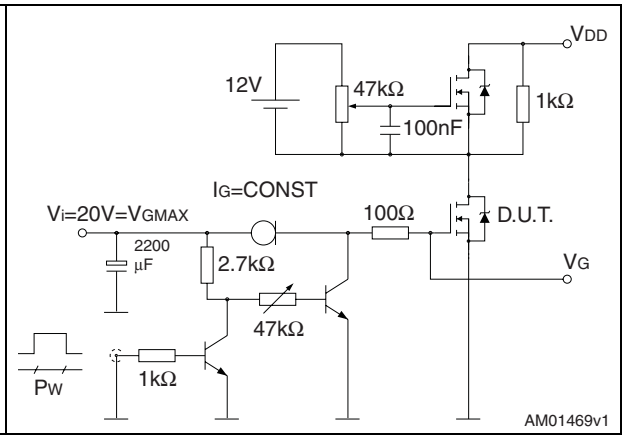


Figure 15. Test circuit for inductive load switching and diode recovery times

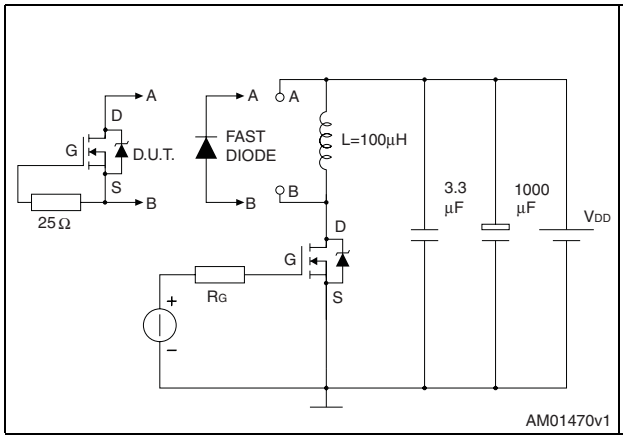


Figure 16. Unclamped inductive load test circuit

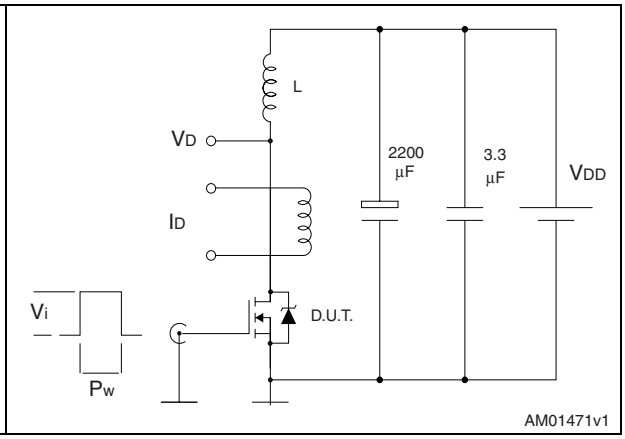


Figure 17. Unclamped inductive waveform

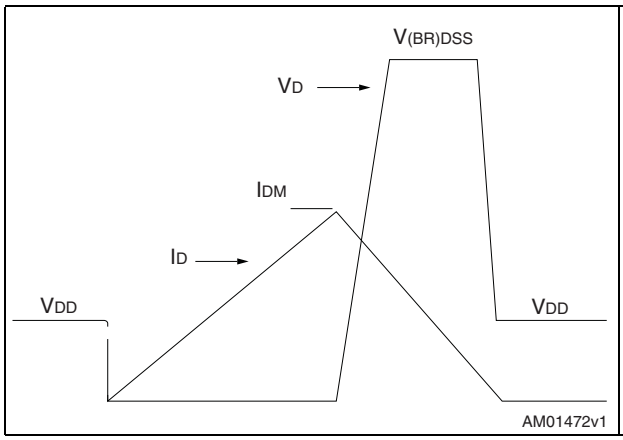
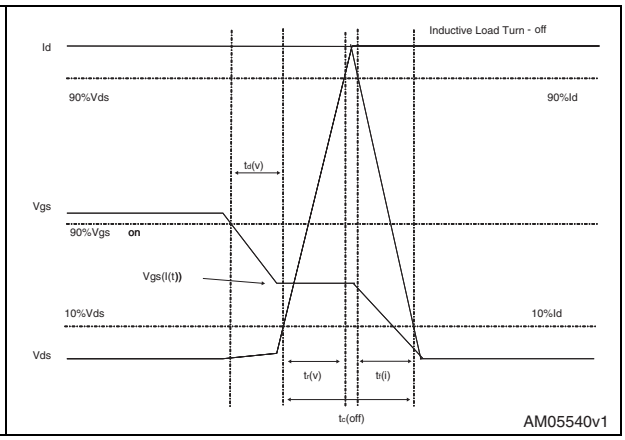


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ (5x6) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.93
A1		0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
E		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e		1.27	
L	0.70	0.80	0.90

Figure 19. PowerFLAT™ (5x6) drawing

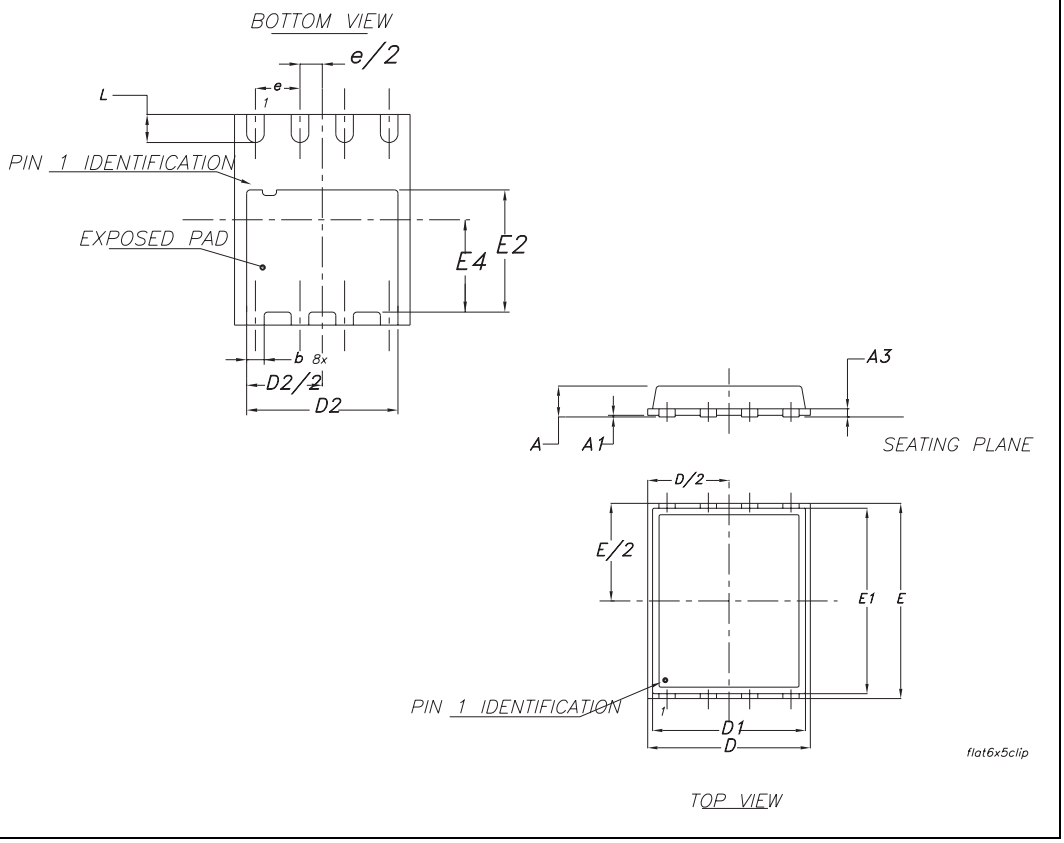
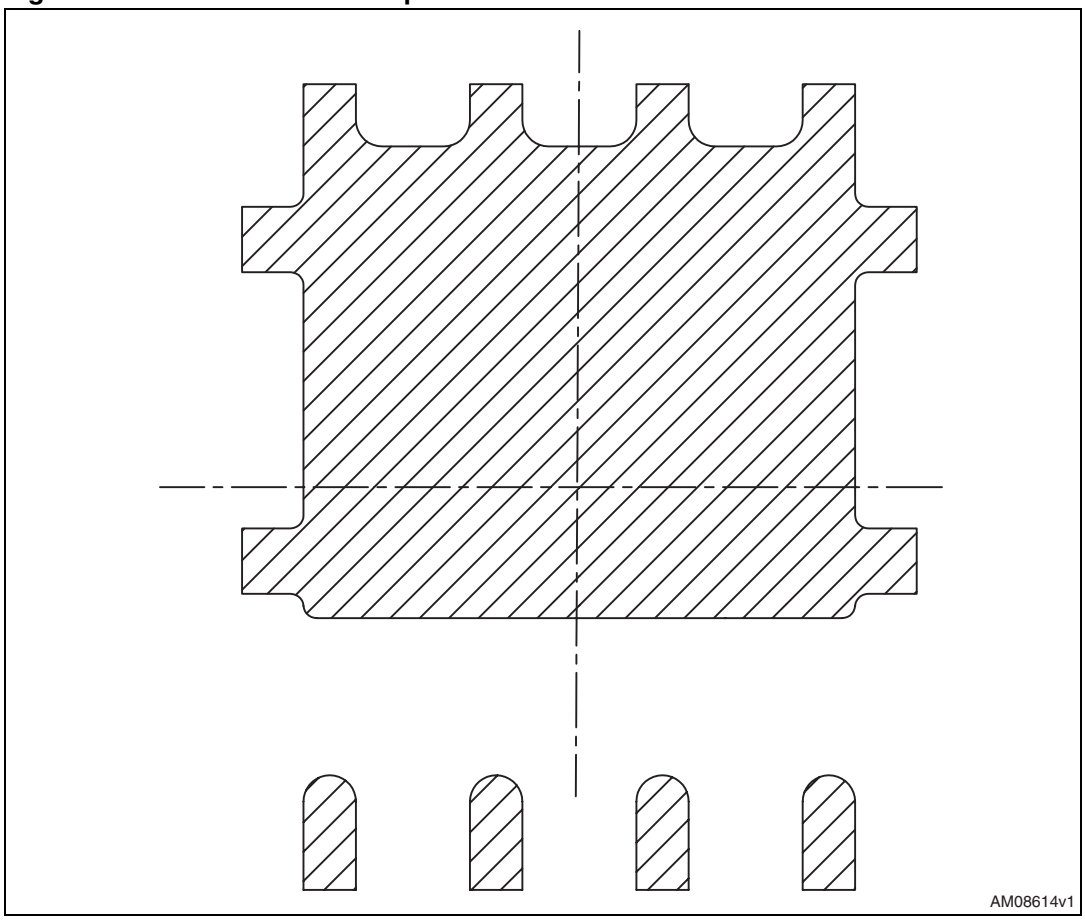


Figure 20. Recommended footprint



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
02-Aug-2010	1	First release.
26-Apr-2011	2	Updated $R_{DS(on)}$ value, and figures *2*, *5*, *7*, *10*, *11* and *12*. Updated *Section 4*.

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