



# STL80N3LLH6

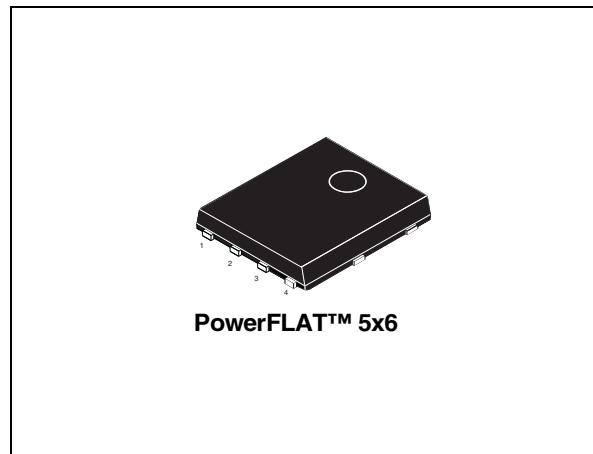
N-channel 30 V, 0.0046  $\Omega$ , 21 A PowerFLAT™ 5x6  
STripFET™ VI DeepGATE™ Power MOSFET

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>
STL80N3LLH6	30 V	0.0052 $\Omega$	21 A <sup>(1)</sup>

1. The value is rated according R<sub>thj-pcb</sub>

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge



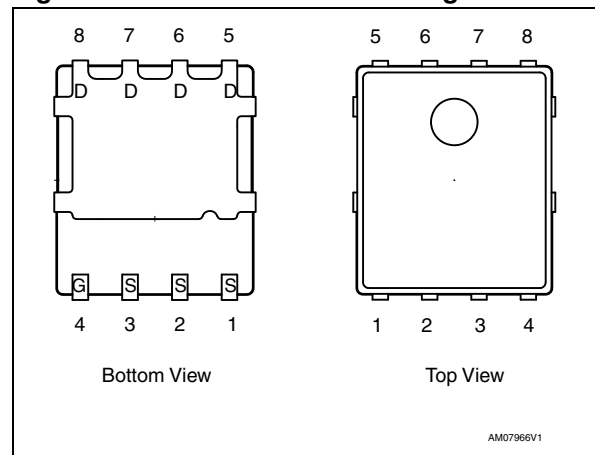
## Applications

- Switching applications

## Description

This device is an N-channel Power MOSFET developed using the 6<sup>th</sup> generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest R<sub>DS(on)</sub> in all packages.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL80N3LLH6	80N3LLH6	PowerFLAT™ 5x6	Tape and reel

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 70\text{ }^\circ\text{C}$	60	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	51	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	21	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=70\text{ }^\circ\text{C}$	15.7	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$	13.1	A
$I_{DM}^{(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. The value is rated according to  $R_{thj-c}$ .
2. The value is rated according to  $R_{thj-pcb}$ .
3. Pulse width limited by safe operating area.

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain, steady state)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10$  sec.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 30\text{ V}$ , $V_{DS} = 30\text{ V}$ at $T_C = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 10.5\text{ A}$		0.0046 0.0067	0.0052 0.0076	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	1350	1690	2030	pF
$C_{oss}$	Output capacitance		230	290	350	pF
$C_{rss}$	Reverse transfer capacitance		140	176	210	pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 21\text{ A}$ $V_{GS} = 4.5\text{ V}$ (see Figure 14)		17		nC
$Q_{gs}$	Gate-source charge			8		nC
$Q_{gd}$	Gate-drain charge			6		nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	1.25	1.7	2	$\Omega$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$ , $I_D=10.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ (see Figure 13)		9.5		ns	
$t_r$	Rise time			30		ns	
$t_{d(off)}$	Turn-off delay time				37		ns
$t_f$	Fall time				12		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit	
$I_{SD}$	Source-drain current		-		21	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=21\text{ A}$ , $V_{GS}=0$	-		1.1	V	
$t_{rr}$	Reverse recovery time	$I_{SD}=10.5\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=25\text{ V}$		24		ns	
$Q_{rr}$	Reverse recovery charge			-	16.8		nC
$I_{RRM}$	Reverse recovery current				1.4		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

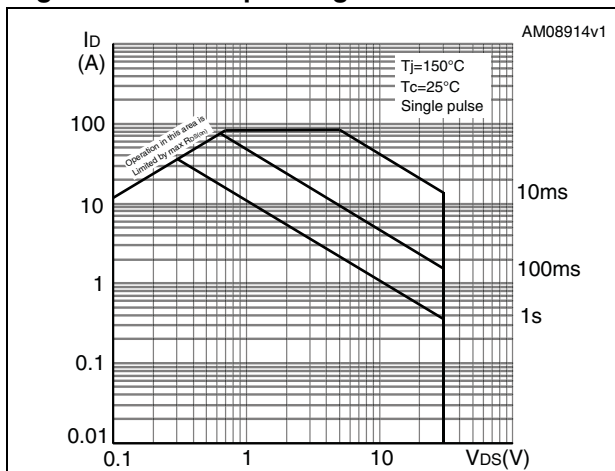


Figure 3. Thermal impedance

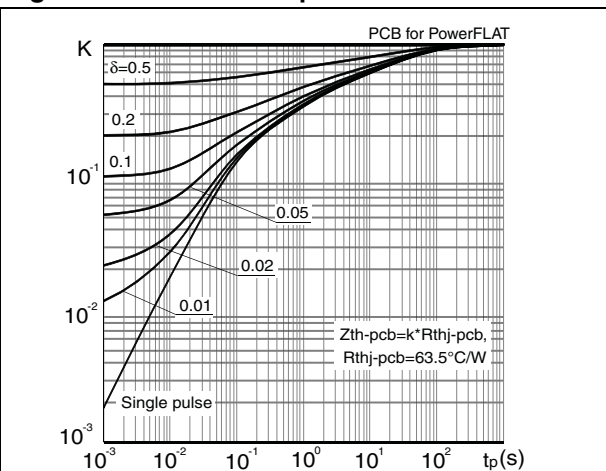


Figure 4. Output characteristics

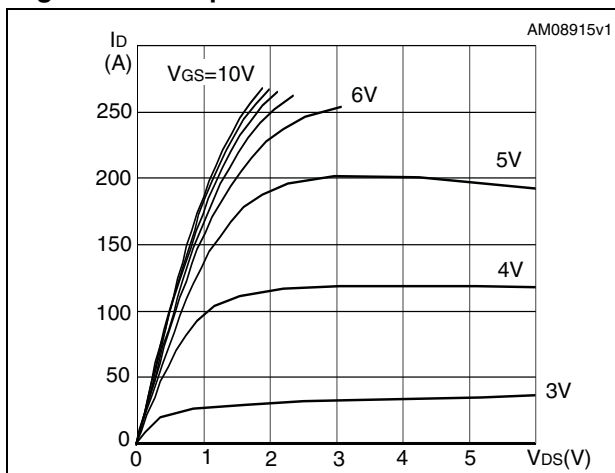


Figure 5. Transfer characteristics

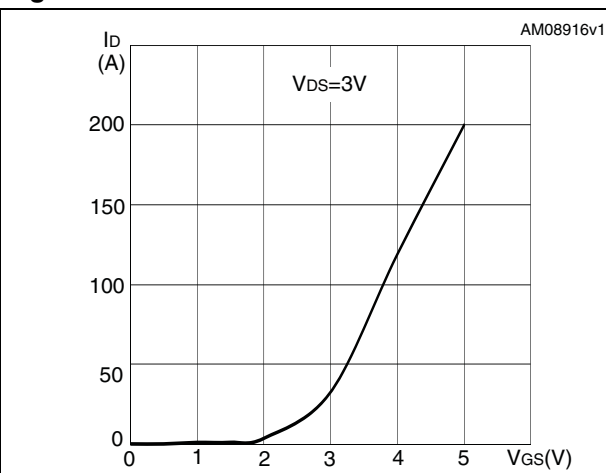


Figure 6. Normalized  $B_{V_{DSS}}$  vs temperature

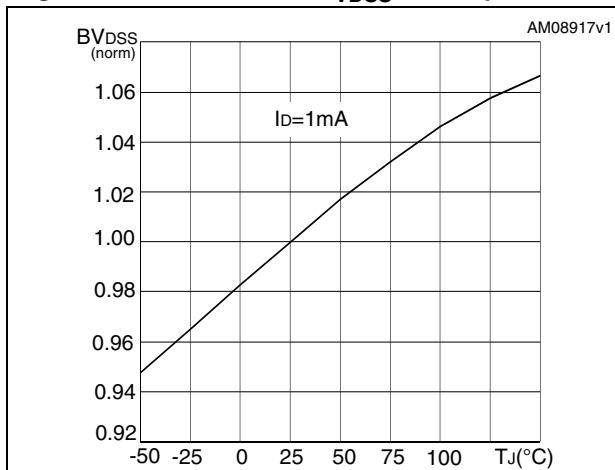


Figure 7. Static drain-source on resistance

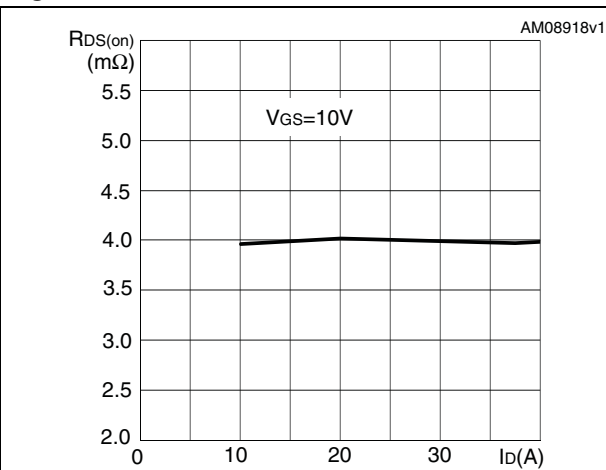


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

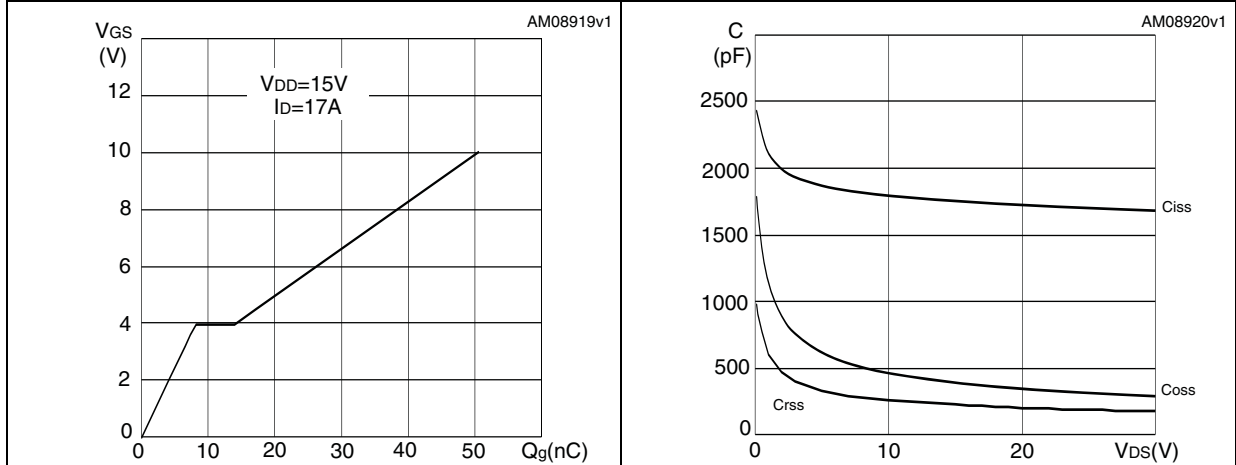


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

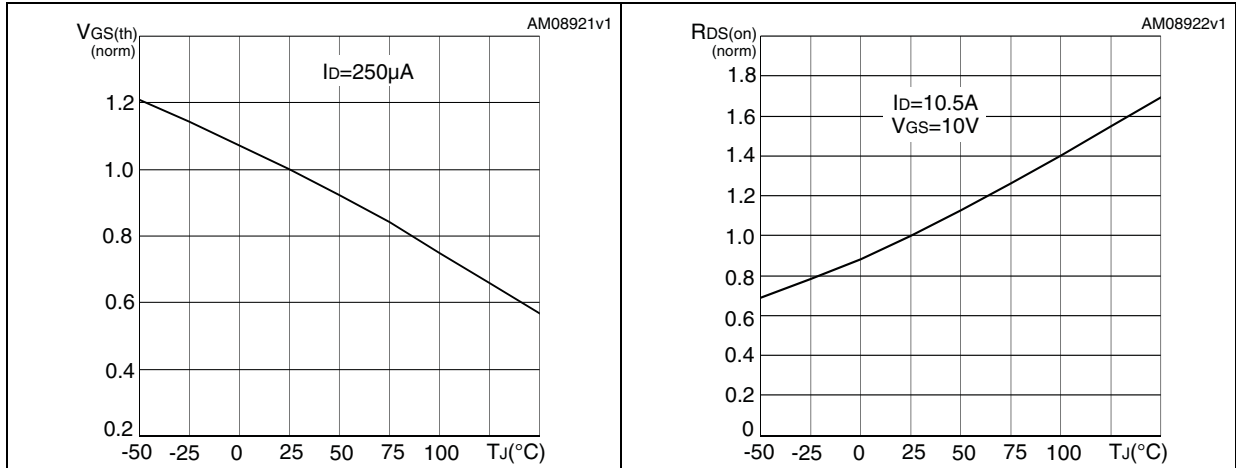
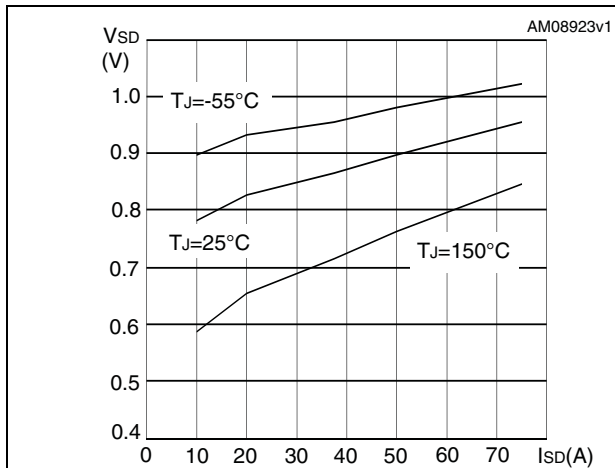
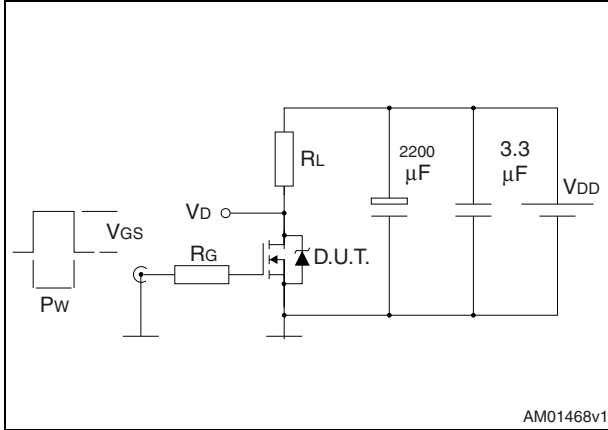


Figure 12. Source-drain diode forward characteristics

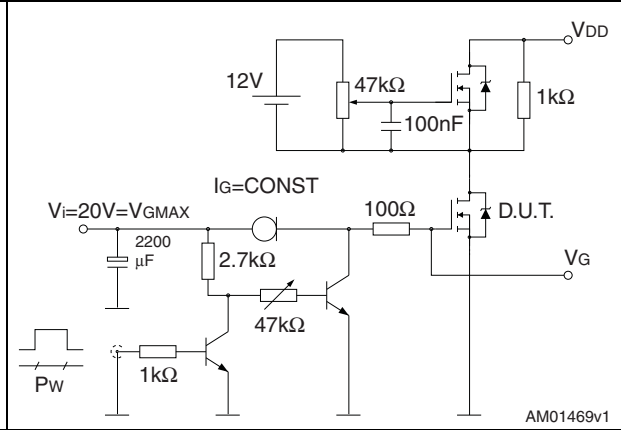


### 3 Test circuits

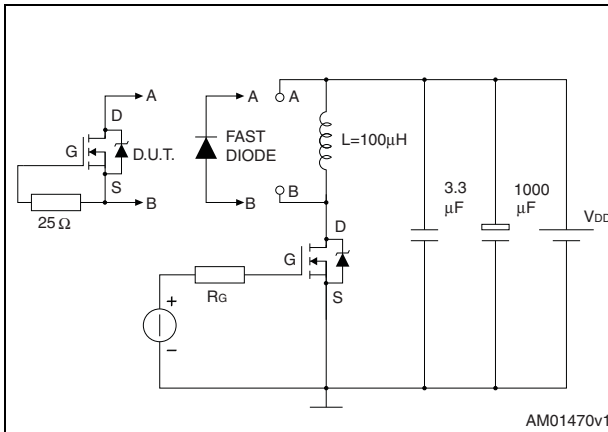
**Figure 13. Switching times test circuit for resistive load**



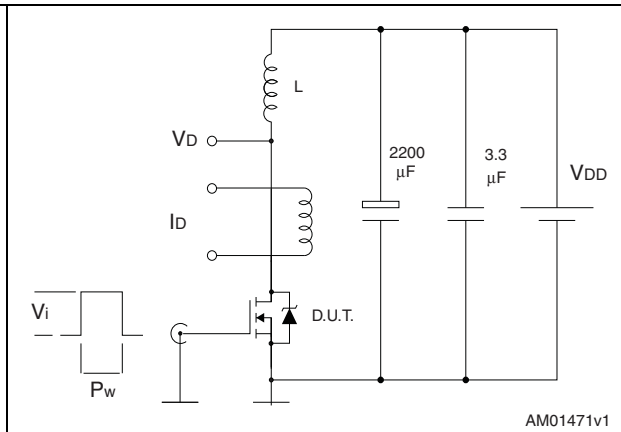
**Figure 14. Gate charge test circuit**



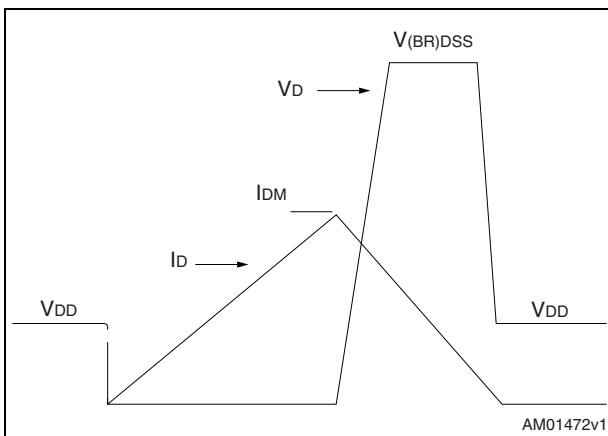
**Figure 15. Test circuit for inductive load switching and diode recovery times**



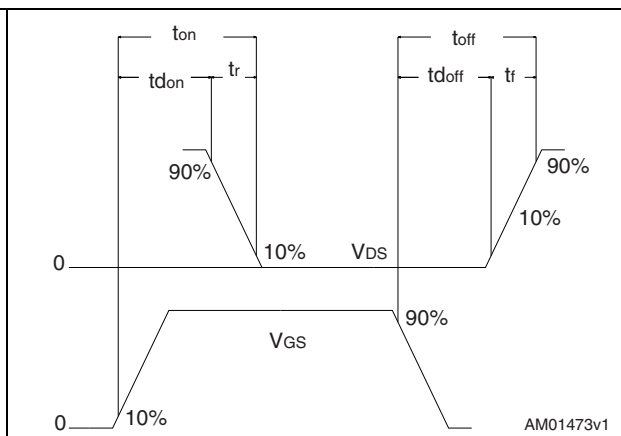
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 19. PowerFLAT 5x6 type S-R drawing

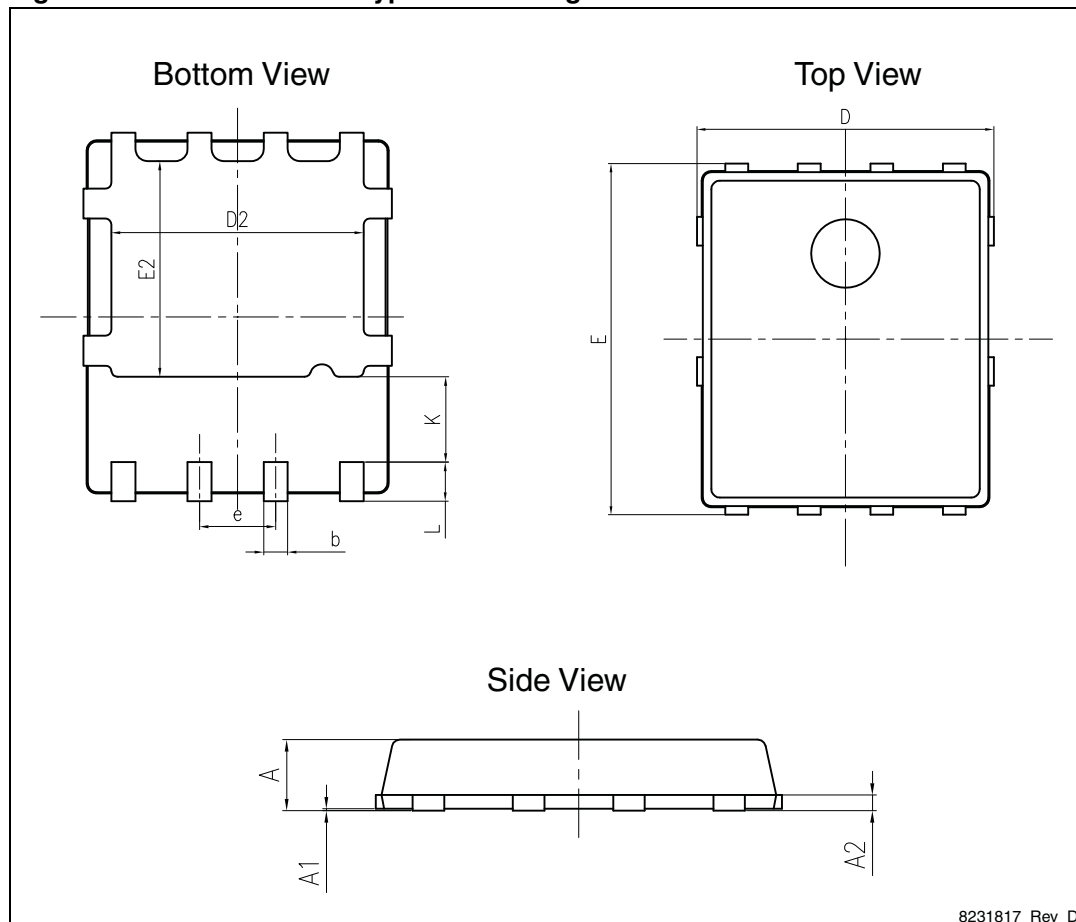
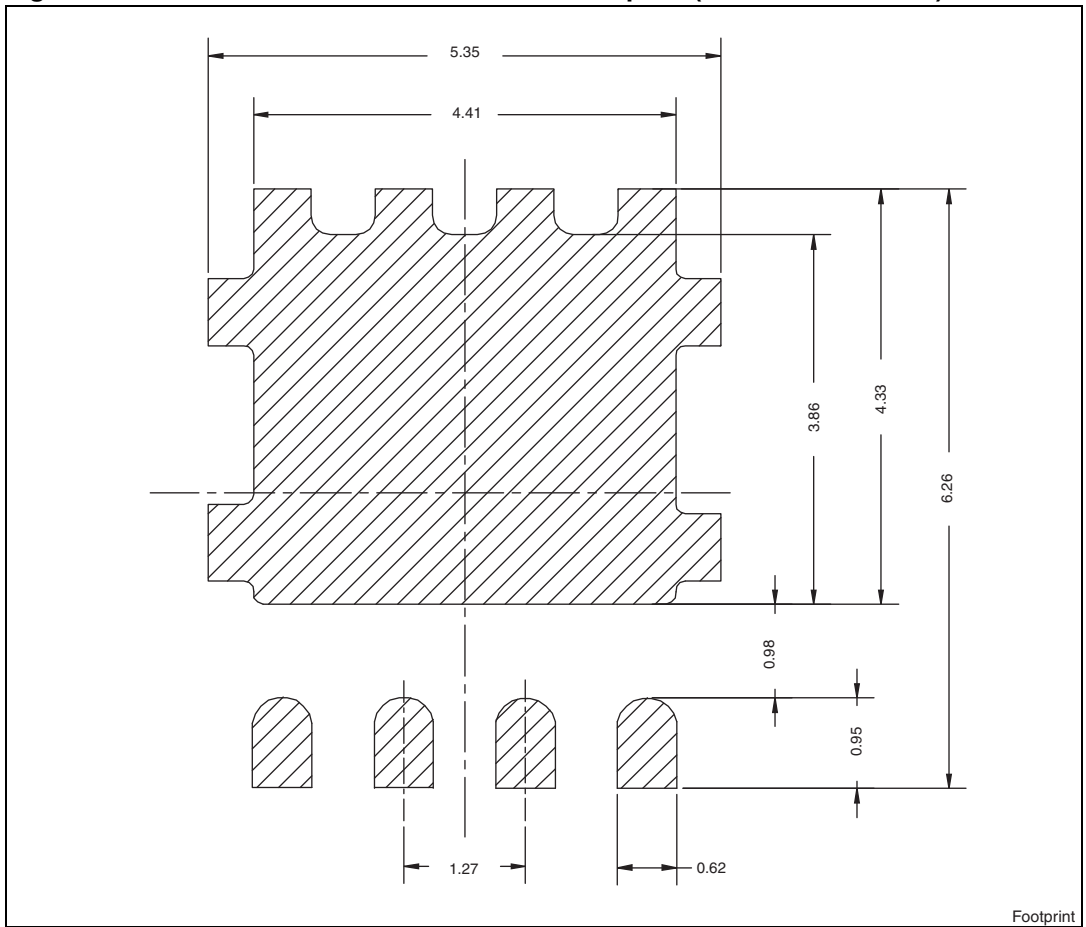


Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
12-Nov-2009	1	First release.
30-Mar-2010	2	$R_{DS(on)}$ values changed in <a href="#">Table 4: On/off states</a>
26-Sep-2011	3	<ul style="list-style-type: none"><li>– Document status promoted from preliminary data to datasheet;</li><li>– Inserted <math>I_D</math> value @ 70 °C, in <a href="#">Table 2: Absolute maximum ratings</a>.</li></ul>
02-Dec-2011	4	<a href="#">Section 4: Package mechanical data</a> has been updated. Minor text changes.

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