STL80N75F6

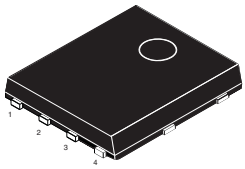
N-channel 75 V, 0.0051 Ω, 18 A, PowerFLAT™ 5x6 STripFET™ VI DeepGATE™ Power MOSFET

Preliminary data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STL80N75F6	75 V	< 0.0063 Ω	18 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness



PowerFLAT™ 5x6

Application

Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Figure 1. Internal schematic diagram

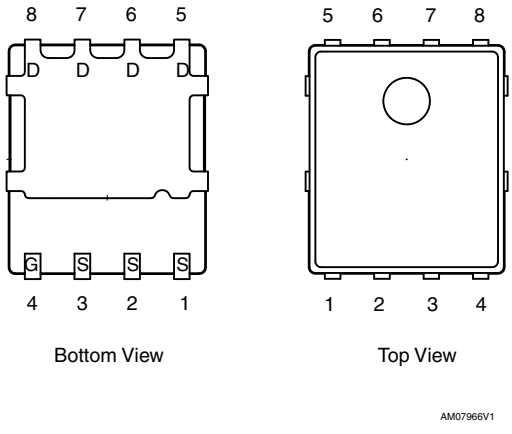


Table 1. Device summary

Order code	Marking	Package	Packaging
STL80N75F6	80N75F6	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	18	A
I_D (2)	Drain current (continuous) at T_{pcb}=100 °C	11	A
I_{DM} (3)	Drain current (pulsed)	74	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	80	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4	W
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Operating junction temperature		

1. The value is rated according to $R_{thj\text{-}c}$
2. The value is rated according to $R_{thj\text{-}pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb max	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case (drain, steady state) max.	1.56	°C/W

1. When mounted on FR-4 board of 1 inch², 2 oz Cu, t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AS}, V_{DD} = 50 V)	TBD	mJ

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	75			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 75 V, V_{DS} = 75 V, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 9 A		0.0051	0.0063	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f = 1 MHz, V_{GS} = 0	-	7120 540 300	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 37 V, I_D = 19 A V_{GS} =10 V (see *Figure 3*)	-	100 TBD TBD	-	nC nC nC
R_g	Gate input resistance	f=1 MHz Gate DC Bias=0 test signal level=20 mV open drain	-	TBD	-	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}= 37 V, I_D= 10 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 2*)	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		19	A
I_{SDM}(1)	Source-drain current (pulsed)		-		80	A
V_{SD}(2)	Forward on voltage	I_{SD} = 19 A, V_{GS} = 0	-		1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 19 A, di/dt = 100 A/µs, V_{DD}= 120 V, T_J = 150 °C (see *Figure 4*)	-	TBD TBD TBD		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

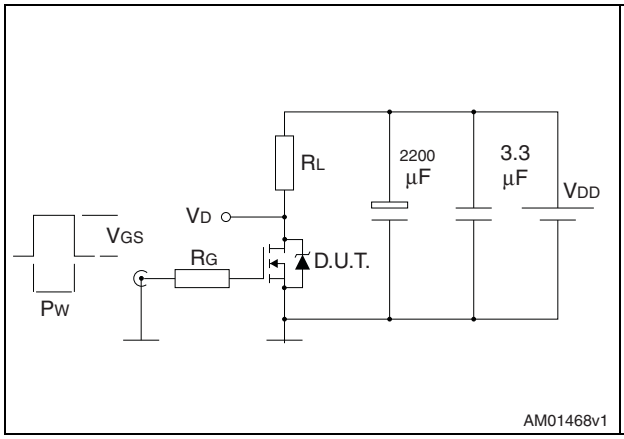


Figure 3. Gate charge test circuit

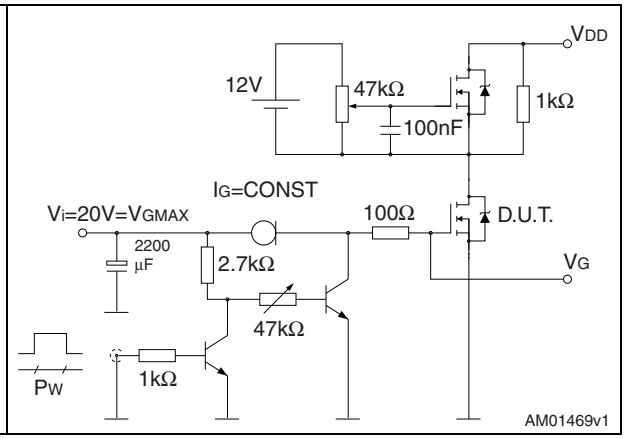


Figure 4. Test circuit for inductive load switching and diode recovery times

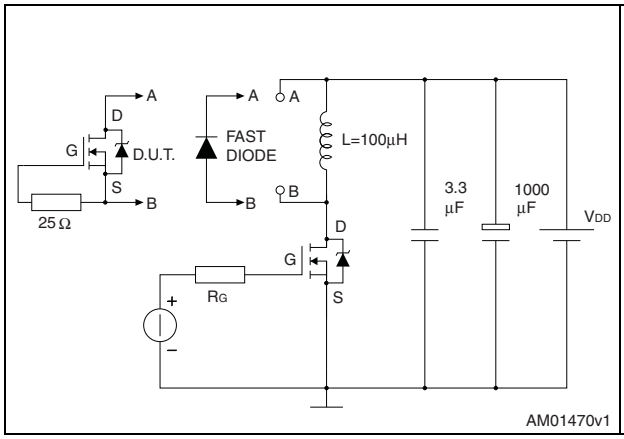


Figure 5. Unclamped inductive load test circuit

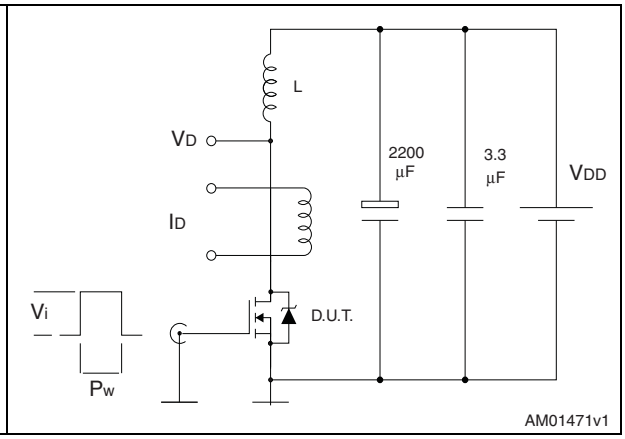


Figure 6. Unclamped inductive waveform

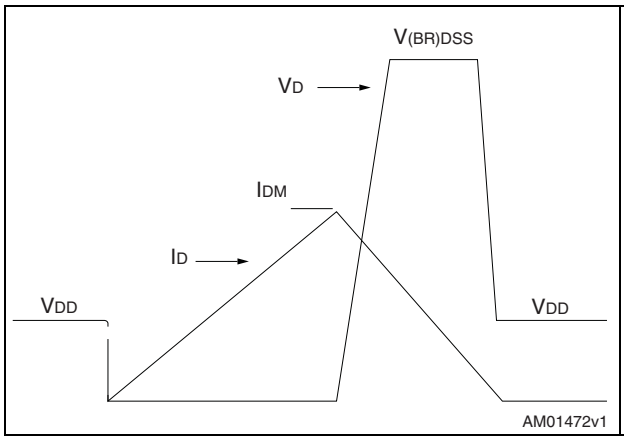
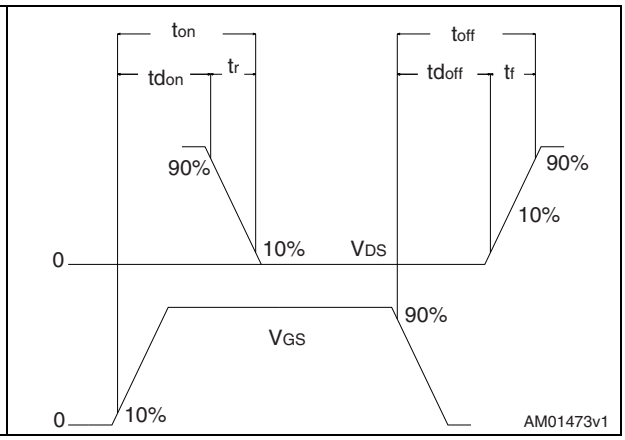


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. PowerFLAT™ 5x6 type C-B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.93
A1	0	0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
E		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e		1.27	
L	0.70	0.80	0.90

Figure 8. PowerFLAT™ 5x6 type C-B drawing

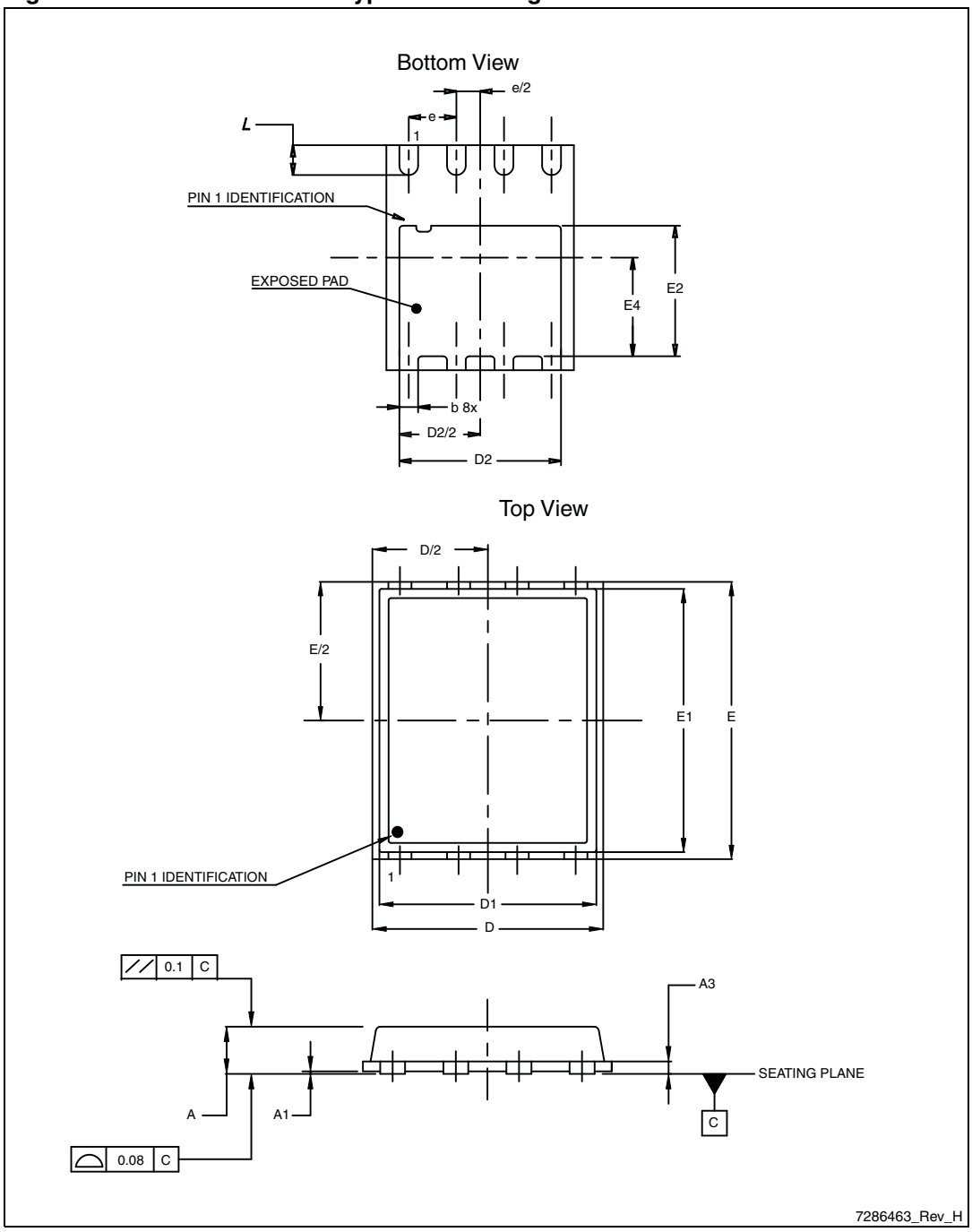


Table 10. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 9. PowerFLAT™ 5x6 type S-C mechanical data

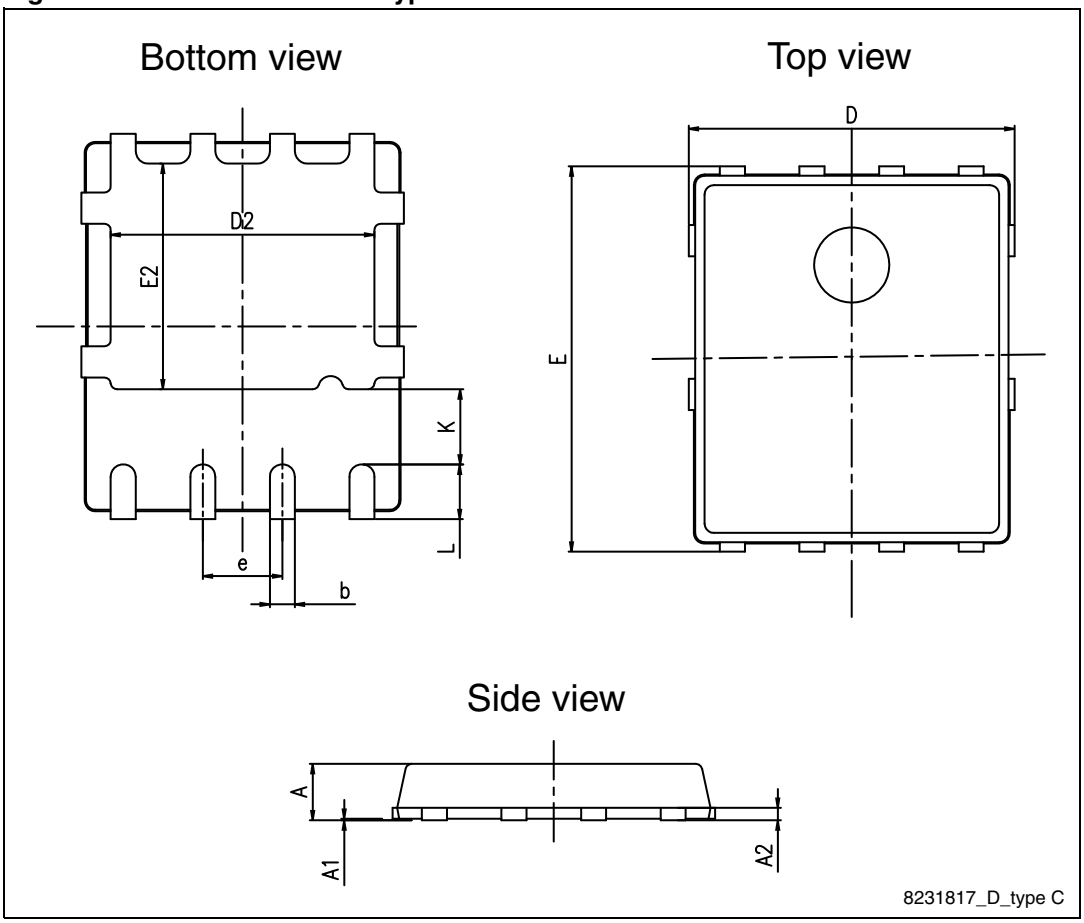
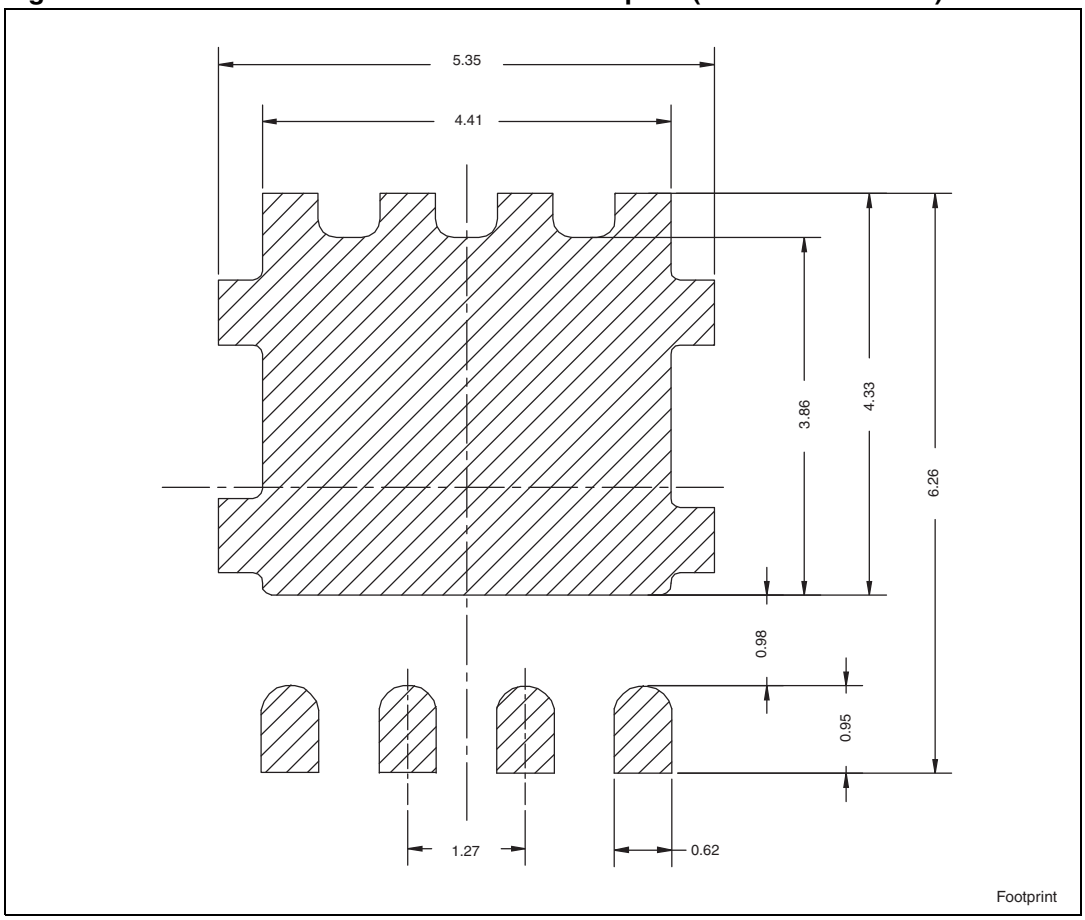


Figure 10. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Apr-2011	1	First release.
10-Nov-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.

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