# STM32F101xC STM32F101xD STM32F101xE

## Access line, ARM-based 32-bit MCU with up to 512 KB Flash, nine 16-bit timers, 1 ADC and 10 communication interfaces

Preliminary Data

## Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 36 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 256 to 512 Kbytes of Flash memory
  - up to 48 Kbytes of SRAM
  - Flexible static memory controller with 4 Chip Select. Supports Compact Flash, SRAM, PSRAM, NOR and NAND memories
  - LCD parallel interface, 8080/6800 modes
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4-to-16 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration capability
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - $V_{BAT}$ supply for RTC and backup registers
- 1 x 12-bit, 1 µs A/D converters (up to 16 channels)
  - Conversion range: 0 to 3.6 V
  - Temperature sensor
- 2-channel, 12-bit D/A converter
- DMA
  - 12-channel DMA controller
  - Peripherals supported: timers, ADC, DAC, SPIs, I²Cs and USARTs
- Up to 112 fast I/O ports

LQFP100
14 x 14 mm

LQFP144
20 x 20 mm

LQFP64
10 x 10 mm

- 51/80/112 I/Os, all mappable on 16 external interrupt vectors, all 5 V-tolerant except for analog inputs
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™
- Up to 9 timers
  - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
  - 2 x watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- Up to 10 communication interfaces
  - Up to 2 x I²C interfaces (SMBus/PMBus)
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 3 SPIs (18 Mbit/s)
- CRC calculation unit, 96-bit unique ID
- ECOPACK® packages

**Table 1.     Device summary**

| Reference | Part number |
|---|---|
| STM32F101xC | STM32F101RC STM32F101VC STM32F101ZC |
| STM32F101xD | STM32F101RD STM32F101VD STM32F101ZD |
| STM32F101xE | STM32F101RE STM32F101ZE STM32F101VE |

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# 1    Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F101xC, STM32F101xD and STM32F101xE High-density access line microcontrollers. For more details on the whole STMicroelectronics STM32F101xx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The High-density STM32F101xx datasheet should be read in conjunction with the Medium- and High-density STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

# 2    Description

The STM32F101xC, STM32F101xD and STM32F101xE access line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 36 MHz frequency, high-speed embedded memories (Flash memory up to 512 Kbytes and SRAM up to 48 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer one 12-bit ADC, four general purpose 16-bit timers, as well as standard and advanced communication interfaces: up to two I²Cs, three SPIs and five USARTs.

The STM32F101xx High-density access line family operates in the –40 to +85 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F101xx High-density access line family offers devices in 3 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F101xx High-density access line microcontroller family suitable for a wide range of applications:

● Medical and handheld equipment
● PC peripherals gaming and GPS platforms
● Industrial applications: PLC, printers, and scanners
● Alarm systems and Video intercom

*Figure 1* shows the general block diagram of the device family.

## 2.1      Device overview

**Table 2.      STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts**

| Peripherals | | STM32F101Rx | | | STM32F101Vx | | | STM32F101Zx | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 256 | 384 | 512 | 256 | 384 | 512 | 256 | 384 | 512 |
| SRAM in Kbytes | | 32 | 48 | | 32 | 48 | | 32 | 48 | |
| FSMC | | No | | | Yes | | | Yes | | |
| Timers | General-purpose | 4 | | | | | | | | |
| | Basic | 2 | | | | | | | | |
| Comm | SPI | 3 | | | | | | | | |
| | I$^2$C | 2 | | | | | | | | |
| | USART | 5 | | | | | | | | |
| GPIOs | | 51 | | | 80 | | | 112 | | |
| 12-bit ADC<br>Number of channels | | 1<br>16 | | | 1<br>16 | | | 1<br>16 | | |
| 12-bit DAC<br>Number of channels | | 1<br>2 | | | | | | | | |
| CPU frequency | | 36 MHz | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | |
| Operating temperatures | | Ambient temperature: –40 to +85 °C (see *Table 9*)<br>Junction temperature: –40 to +105 °C (see *Table 9*) | | | | | | | | |
| Package | | LQFP64 | | | LQFP100[1] | | | LQFP144 | | |

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR Flash memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.

## 2.2 Full compatibility throughout the family

The STM32F101xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F101x6, STM32F101x8 and STM32F101xB are referred to as Medium-density devices, while the STM32F101xC, STM32F101xD and STM32F101xE are referred to as High-density devices. High-density devices are an extension of the STM32F101x6/8/B devices specified in the STM32F101xx datasheet.
They feature higher Flash memory and RAM densities, and additional peripherals like FSMC and DAC, while remaining fully compatible with the other members of the family.

The STM32F101xC, STM32F101xD and STM32F101xE are a drop-in replacement for the STM32F101x6/8/B devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

**Table 3.  STM32F101xx family**

| Pinout | Memory size | | | | | |
| | Medium-density STM32F101xx devices | | | High-density STM32F101xx devices | | |
| | 32 KB Flash | 64 KB Flash | 128 KB Flash | 256 KB Flash | 384 KB Flash | 512 KB Flash |
| | 6 KB RAM | 10 KB RAM | 16 KB RAM | 32 KB RAM | 48 KB RAM | 48 KB RAM |
| 144 | | | | 5 × USARTs 4 × 16-bit timers, 2 × basic timers 3 × SPIs, 2 × I$^2$Cs, 1 × ADC, 1 × DAC FSMC (100 and 144 pins) | | |
| 100 | | 3 × USARTs | | | | |
| 64 | 2 × USARTs | 3 × 16-bit timers, 2 × SPIs 2 × I2Cs, 1 × ADC | | | | |
| 48 | 3 × 16-bit timers 1 × SPI, 1 × I$^2$C | | | | | |
| 36 | 1 × ADC | | | | | |

## 2.3 Overview

### ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F101xC, STM32F101xD and STM32F101xE access line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

### Embedded Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data.

### CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

### Embedded SRAM

Up to 48 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line family. It has four Chip Select outputs supporting the following modes: RAM, PSRAM, NOR and NAND.

Functionality overview:

● The three FSMC interrupt lines are ORed in order to be connected to the NVIC

● No read FIFO

● Code execution from external memory except for

● No boot capability

● The targeted frequency is SYSCLK/2, so external access is at 18 MHz when the system is at 36 MHz

### LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

### Nested vectored interrupt controller (NVIC)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

● Closely coupled NVIC gives low-latency interrupt processing

● Interrupt entry vector table address passed directly to the core

● Closely coupled NVIC core interface

● Allows early processing of interrupts

● Processing of *late arriving* higher priority interrupts

● Support for tail-chaining

● Processor state automatically saved

● Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

### Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers are used to configure the AHB frequency, the high-speed APB (APB2) domain and the low-speed APB (APB1) domain. The maximum frequency of the AHB and APB domains is 36 MHz. See *Figure 2* for details on the clock tree.

### Boot modes

At startup, boot pins are used to select one of three boot options:

● Boot from User Flash
● Boot from System Memory
● Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

### Power supply schemes

● $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.

● $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to $V_{DDA}$ is 2.4 V when the ADC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.

● $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

### Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}$ drops below the $V_{PVD}$ and/or when $V_{DD}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 11: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

● MR is used in the nominal regulation mode (Run)

● LPR is used in the Stop modes.

● Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

### Low-power modes

The STM32F101xC, STM32F101xD and STM32F101xE access line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

● **Sleep** mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

● **Stop** mode

Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.
The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output or the RTC alarm.

● **Standby** mode

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

*Note:*     *The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I$^2$C, USART, general-purpose and basic timers TIMx, DAC and ADC.

### RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the High Speed External clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

### Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

### SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

● A 24-bit down counter

● Autoreload capability

● Maskable system interrupt generation when the counter reaches 0.

● Programmable clock source

### General-purpose timers (TIMx)

There are up to 4 synchronizable standard timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F101xC, STM32F101xD and STM32F101xE access line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages. They can work together with the advanced control timer via the Timer Link feature for synchronization or event chaining.
The counter can be frozen in debug mode.
Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

### Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

### I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.
They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.
They can be served by DMA and they support SMBus 2.0/PMBus.

### Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F101xC, STM32F101xD and STM32F101xE access line embeds three universal synchronous asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The five interfaces are able to communicate at speeds of up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

### Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

### GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

### ADC (analog to digital converter)

A 12-bit analog-to-digital converter is embedded into STM32F101xC, STM32F101xD and STM32F101xE access line devices. It has up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

### DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference $V_{REF+}$

Seven DAC trigger inputs are used in the STM32F101xC, STM32F101xD and STM32F101xE access line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

### Temperature sensor

The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between 2 V < $V_{DDA}$ < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

### Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

**Figure 1.    STM32F101xC, STM32F101xD and STM32F101xE access line block diagram**
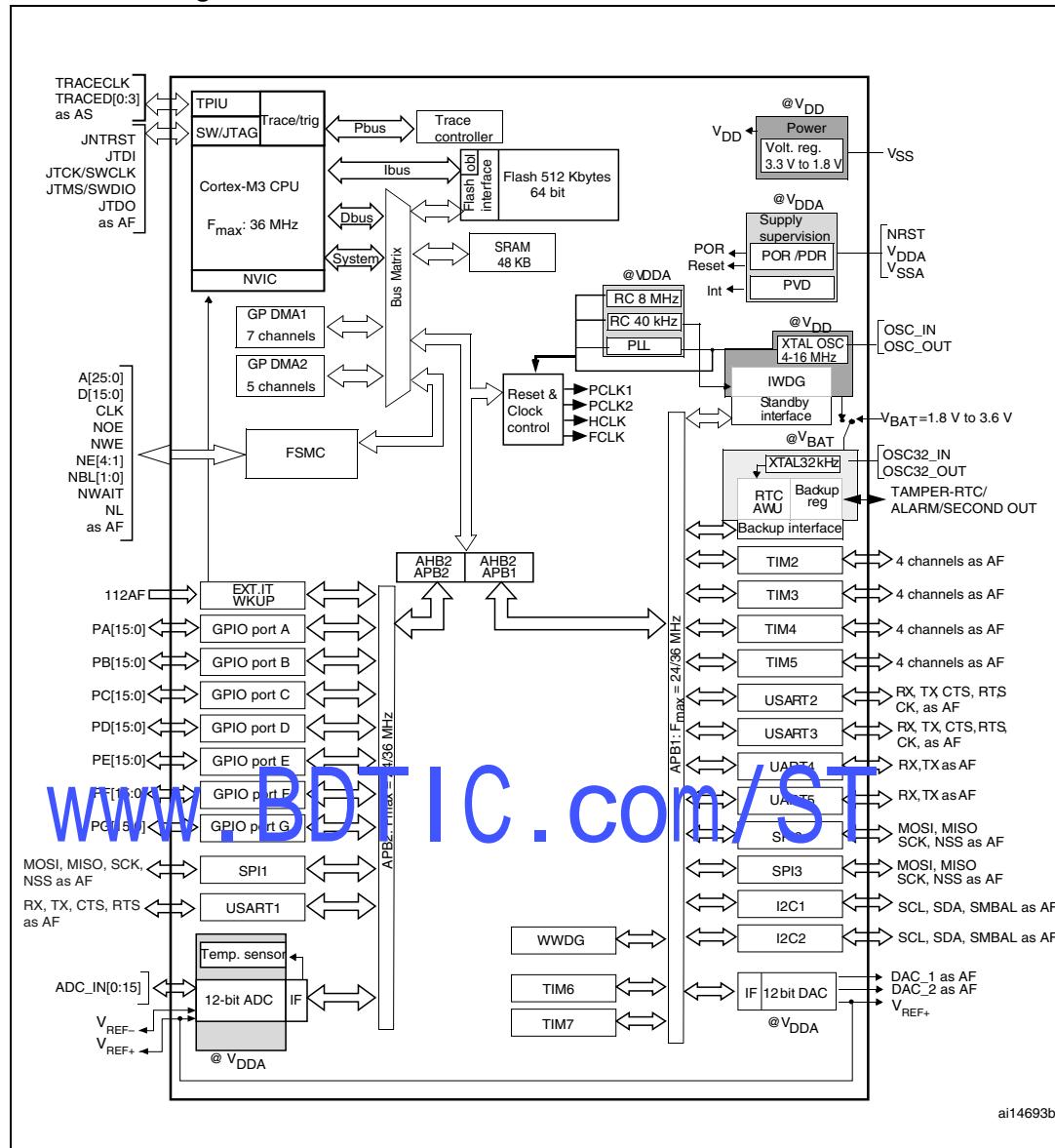


1.  $T_A = -40$ °C to +85 °C (junction temperature up to 105 °C).

2.  AF = alternate function on I/O port pin.

**Figure 2.     Clock tree**
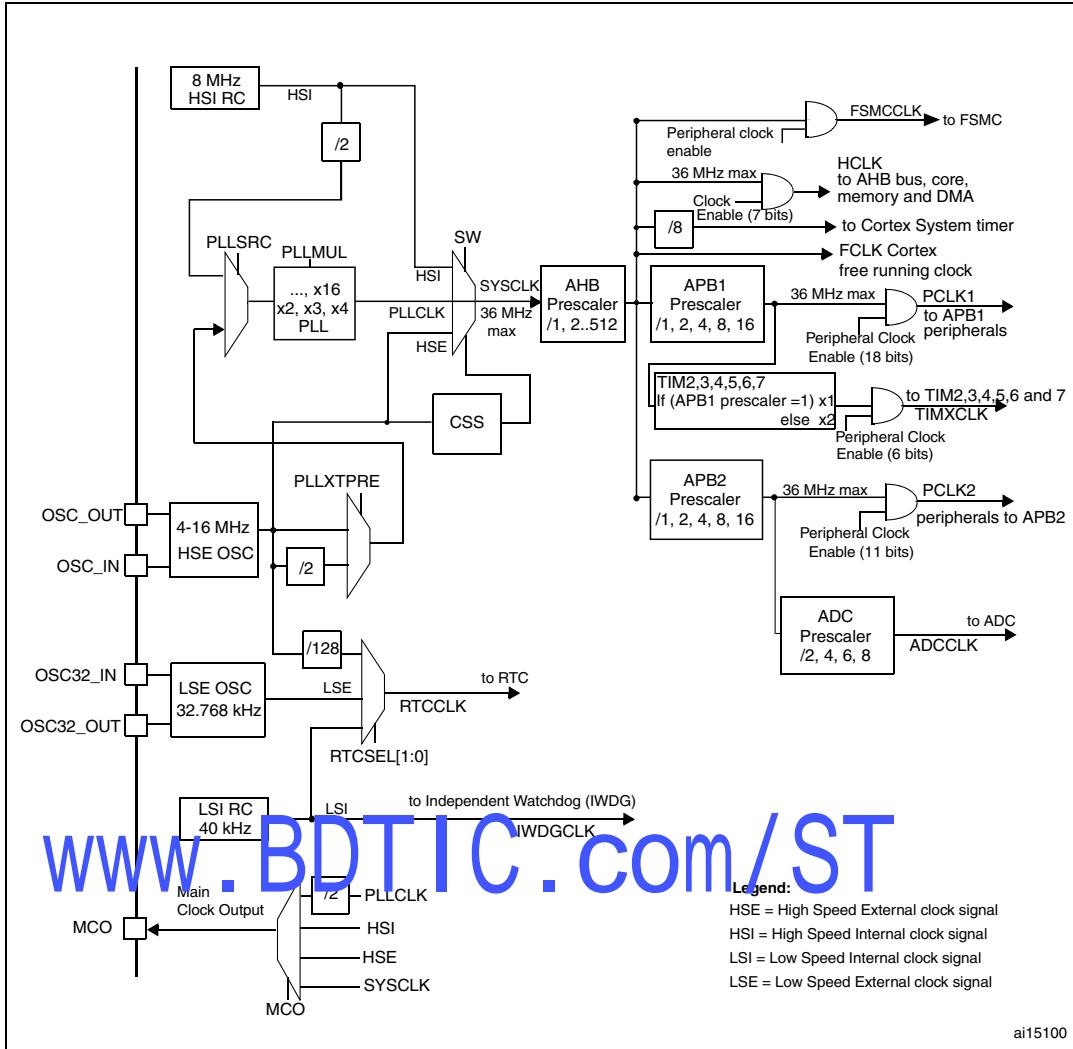


1.  When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 36 MHz.

2.  To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz or 28 MHz.

# 3        Pin descriptions

**Figure 3.     STM32F101xC, STM32F101xD and STM32F101xE access line LQFP144 pinout**
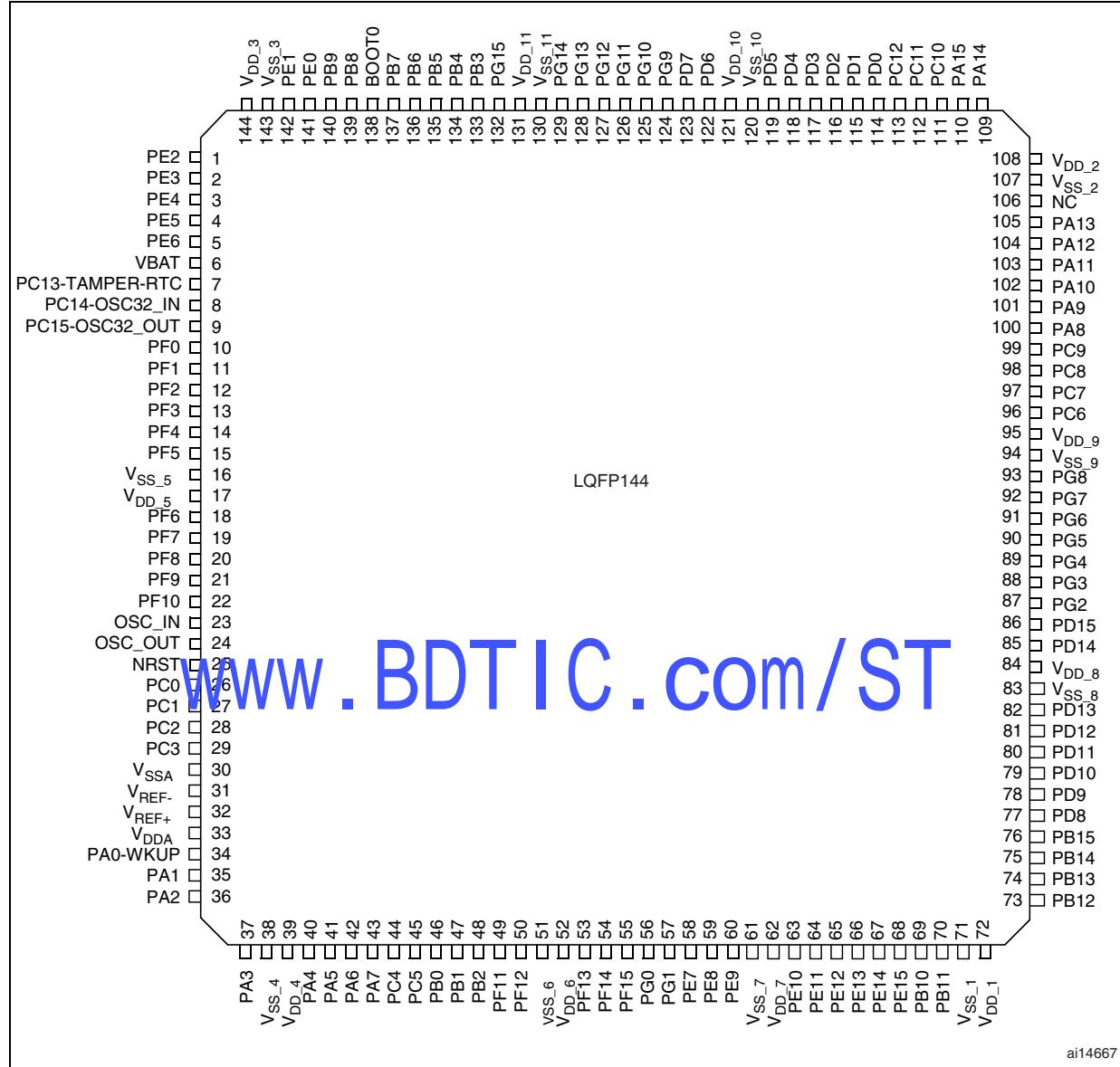
**Figure 4.    STM32F101xC, STM32F101xD and STM32F101xE access line LQFP100 pinout**
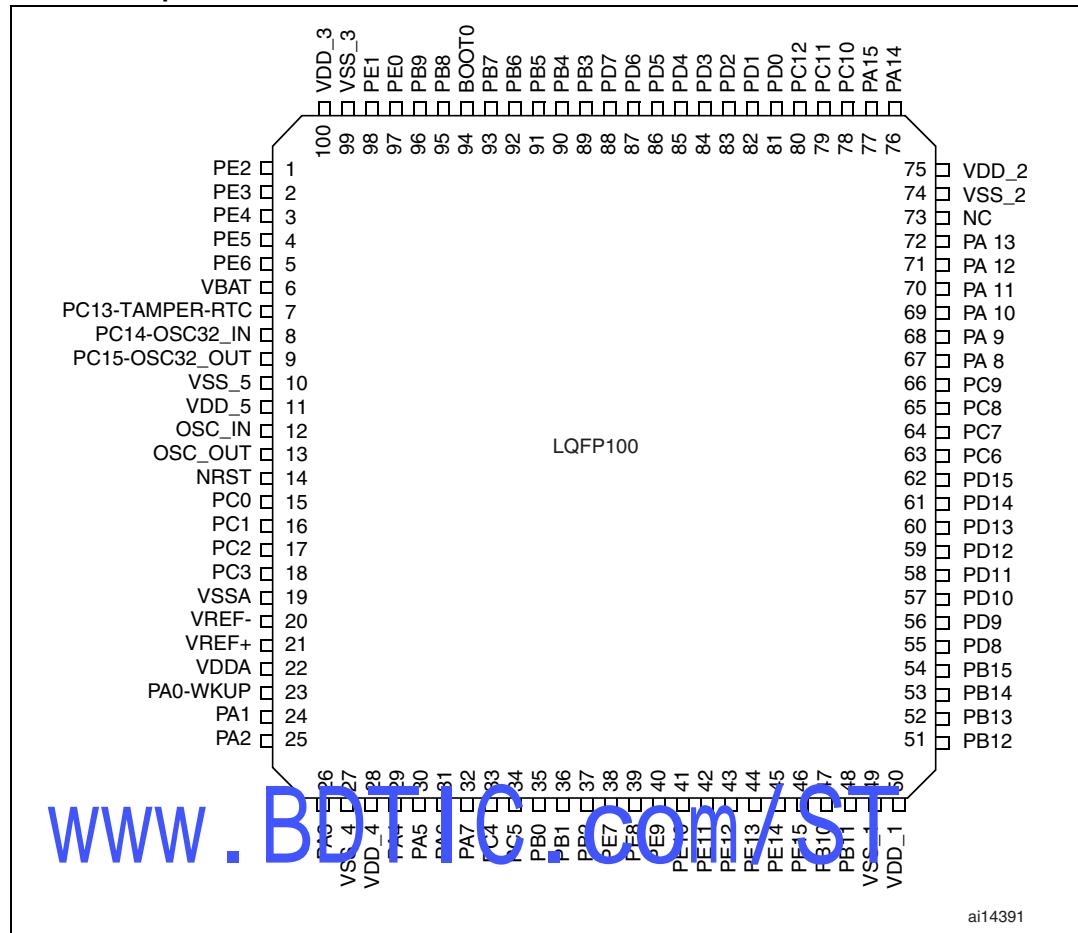
**Figure 5.    STM32F101xC, STM32F101xD and STM32F101xE access line access line LQFP64 pinout**



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**Table 4.        Pin definitions**

| Pins | | | Pin name | Type[(1)] | I / O Level[(2)] | Main function[(3)] (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| - | 1 | 1 | PE2 | I/O | FT | PE2 | TRACECLK/ FSMC_A23 | |
| - | 2 | 2 | PE3 | I/O | FT | PE3 | TRACED0/FSMC_A19 | |
| - | 3 | 3 | PE4 | I/O | FT | PE4 | TRACED1/FSMC_A20 | |
| - | 4 | 4 | PE5 | I/O | FT | PE5 | TRACED2/FSMC_A21 | |
| - | 5 | 5 | PE6 | I/O | FT | PE6 | TRACED3/FSMC_A22 | |
| 1 | 6 | 6 | $V_{BAT}$ | S | | $V_{BAT}$ | | |
| 2 | 7 | 7 | PC13-TAMPER-RTC[(4)] | I/O | | PC13[(5)] | TAMPER-RTC | |
| 3 | 8 | 8 | PC14-OSC32_IN[(4)] | I/O | | PC14[(5)] | OSC32_IN | |
| 4 | 9 | 9 | PC15-OSC32_OUT[(4)] | I/O | | PC15[(5)] | OSC32_OUT | |
| - | - | 10 | PF0 | I/O | FT | PF0 | FSMC_A0 | |
| - | - | 11 | PF1 | I/O | FT | PF1 | FSMC_A1 | |
| - | - | 12 | PF2 | I/O | FT | PF2 | FSMC_A2 | |
| - | - | 13 | PF3 | I/O | FT | PF3 | FSMC_A3 | |
| - | - | 14 | PF4 | I/O | FT | PF4 | FSMC_A4 | |
| - | - | 15 | PF5 | I/O | FT | PF5 | FSMC_A5 | |
| - | 10 | 16 | $V_{SS\_5}$ | S | | $V_{SS\_5}$ | | |

**Table 4.    Pin definitions (continued)**

| Pins | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| - | 11 | 17 | $V_{DD\_5}$ | S | | $V_{DD\_5}$ | | |
| - | - | 18 | PF6 | I/O | | PF6 | FSMC_NIORD | |
| - | - | 19 | PF7 | I/O | | PF7 | FSMC_NREG | |
| - | - | 20 | PF8 | I/O | | PF8 | FSMC_NIOWR | |
| - | - | 21 | PF9 | I/O | | PF9 | FSMC_CD | |
| - | - | 22 | PF10 | I/O | | PF10 | FSMC_INTR | |
| 5 | 12 | 23 | OSC_IN | I | | OSC_IN | | |
| 6 | 13 | 24 | OSC_OUT | O | | OSC_OUT | | |
| 7 | 14 | 25 | NRST | I/O | | NRST | | |
| 8 | 15 | 26 | PC0 | I/O | | PC0 | ADC_IN10 | |
| 9 | 16 | 27 | PC1 | I/O | | PC1 | ADC_IN11 | |
| 10 | 17 | 28 | PC2 | I/O | | PC2 | ADC_IN12 | |
| 11 | 18 | 29 | PC3 | I/O | | PC3 | ADC_IN13 | |
| 12 | 19 | 30 | $V_{SSA}$ | S | | $V_{SSA}$ | | |
| - | 20 | 31 | $V_{REF-}$ | S | | $V_{REF-}$ | | |
| - | 21 | 32 | $V_{REF+}$ | S | | $V_{REF+}$ | | |
| 13 | 22 | 33 | $V_{DDA}$ | S | | $V_{DDA}$ | | |
| 14 | 23 | 34 | PA0-WKUP | I/O | | PA0 | WKUP/ USART2_CTS[6]/ ADC_IN0/TIM5_CH1/ TIM2_CH1_ETR[6] | |
| 15 | 24 | 35 | PA1 | I/O | | PA1 | USART2_RTS[6]/ ADC_IN1/TIM5_CH2 TIM2_CH2[6] | |
| 16 | 25 | 36 | PA2 | I/O | | PA2 | USART2_TX[6]/ TIM5_CH3/ADC_IN2/ TIM2_CH3[6] | |
| 17 | 26 | 37 | PA3 | I/O | | PA3 | USART2_RX[6]/ TIM5_CH4/ ADC_IN3/ TIM2_CH4[6] | |
| 18 | 27 | 38 | $V_{SS\_4}$ | S | | $V_{SS\_4}$ | | |
| 19 | 28 | 39 | $V_{DD\_4}$ | S | | $V_{DD\_4}$ | | |
| 20 | 29 | 40 | PA4 | I/O | | PA4 | SPI1_NSS/ DAC_OUT1//ADC_IN4 USART2_CK[6] | |
| 21 | 30 | 41 | PA5 | I/O | | PA5 | SPI1_SCK/ DAC_OUT2 ADC_IN5 | |

**Table 4.     Pin definitions  (continued)**

| Pins | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| 22 | 31 | 42 | PA6 | I/O | | PA6 | SPI1_MISO/ ADC_IN6/ TIM3_CH1[6] | |
| 23 | 32 | 43 | PA7 | I/O | | PA7 | SPI1_MOSI/ ADC_IN7/ TIM3_CH2[6] | |
| 24 | 33 | 44 | PC4 | I/O | | PC4 | ADC_IN14 | |
| 25 | 34 | 45 | PC5 | I/O | | PC5 | ADC_IN15 | |
| 26 | 35 | 46 | PB0 | I/O | | PB0 | ADC_IN8/ TIM3_CH3[6] | |
| 27 | 36 | 47 | PB1 | I/O | | PB1 | ADC_IN9/TIM3_CH4[6] | |
| 28 | 37 | 48 | PB2/BOOT1 | I/O | FT | PB2/BOOT1 | | |
| - | - | 49 | PF11 | I/O | | | FSMC_NIOS16 | |
| - | - | 50 | PF12 | I/O | | | FSMC_A6 | |
| - | - | 51 | $V_{SS\_6}$ | S | | | | |
| - | - | 52 | $V_{DD\_6}$ | S | | | | |
| - | - | 53 | PF13 | I/O | | | FSMC_A7 | |
| - | - | 54 | PF14 | I/O | | | FSMC_A8 | |
| - | - | 55 | PF15 | I/O | | | FSMC_A9 | |
| - | - | 56 | PG0 | I/O | | | FSMC_A10 | |
| - | - | 57 | PG1 | I/O | | | FSMC_A11 | |
| - | 38 | 58 | PE7 | I/O | FT | PE7 | FSMC_D4 | |
| - | 39 | 59 | PE8 | I/O | FT | PE8 | FSMC_D5 | |
| - | 40 | 60 | PE9 | I/O | FT | PE9 | FSMC_D6 | |
| - | - | 61 | $V_{SS\_7}$ | S | | | | |
| - | - | 62 | $V_{DD\_7}$ | S | | | | |
| - | 41 | 63 | PE10 | I/O | FT | PE10 | FSMC_D7 | |
| - | 42 | 64 | PE11 | I/O | FT | PE11 | FSMC_D8 | |
| - | 43 | 65 | PE12 | I/O | FT | PE12 | FSMC_D9 | |
| - | 44 | 66 | PE13 | I/O | FT | PE13 | FSMC_D10 | |
| - | 45 | 67 | PE14 | I/O | FT | PE14 | FSMC_D11 | |
| - | 46 | 68 | PE15 | I/O | FT | PE15 | FSMC_D12 | |
| 29 | 47 | 69 | PB10 | I/O | FT | PB10 | I2C2_SCL/ USART3_TX[6] | TIM2_CH3 |

**Table 4.     Pin definitions  (continued)**

| LQFP64 | LQFP100 | LQFP144 | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Default | Remap |
|---|---|---|---|---|---|---|---|---|
| 30 | 48 | 70 | PB11 | I/O | FT | PB11 | I2C2_SDA/ USART3_RX[6] | TIM2_CH4 |
| 31 | 49 | 71 | $V_{SS\_1}$ | S | | $V_{SS\_1}$ | | |
| 32 | 50 | 72 | $V_{DD\_1}$ | S | | $V_{DD\_1}$ | | |
| 33 | 51 | 73 | PB12 | I/O | FT | PB12 | SPI2_NSS[6]/ I2C2_SMBAI/ USART3_CK[6] | |
| 34 | 52 | 74 | PB13 | I/O | FT | PB13 | SPI2_SCK[6]/ USART3_CTS[6] | |
| 35 | 53 | 75 | PB14 | I/O | FT | PB14 | SPI2_MISO[6]/ USART3_RTS[6] | |
| 36 | 54 | 76 | PB15 | I/O | FT | PB15 | SPI2_MOSI[6] | |
| - | 55 | 77 | PD8 | I/O | FT | PD8 | FSMC_D13 | USART3_TX |
| - | 56 | 78 | PD9 | I/O | FT | PD9 | FSMC_D14 | USART3_RX |
| - | 57 | 79 | PD10 | I/O | FT | PD10 | FSMC_D15 | USART3_CK |
| - | 58 | 80 | PD11 | I/O | FT | PD11 | FSMC_A16 | USART3_CTS |
| - | 59 | 81 | PD12 | I/O | FT | PD12 | FSMC_A17 | TIM4_CH1 / USART3_RTS |
| - | 60 | 82 | PD13 | I/O | FT | PD13 | FSMC_A18 | TIM4_CH2 |
| - | - | 83 | $V_{SS\_8}$ | S | | | | |
| - | - | 84 | $V_{DD\_8}$ | S | | | | |
| - | 61 | 85 | PD14 | I/O | FT | PD14 | FSMC_D0 | TIM4_CH3 |
| - | 62 | 86 | PD15 | I/O | FT | PD15 | FSMC_D1 | TIM4_CH4 |
| - | - | 87 | PG2 | I/O | FT | | FSMC_A12 | |
| - | - | 88 | PG3 | I/O | FT | | FSMC_A13 | |
| - | - | 89 | PG4 | I/O | FT | | FSMC_A14 | |
| - | - | 90 | PG5 | I/O | FT | | FSMC_A15 | |
| - | - | 91 | PG6 | I/O | FT | | FSMC_INT2 | |
| - | - | 92 | PG7 | I/O | FT | | FSMC_INT3 | |
| - | - | 93 | PG8 | I/O | FT | | | |
| - | - | 94 | $V_{SS\_9}$ | S | | | | |
| - | - | 95 | $V_{DD\_9}$ | S | | | | |
| 37 | 63 | 96 | PC6 | I/O | FT | PC6 | | TIM3_CH1 |
| 38 | 64 | 97 | PC7 | I/O | FT | PC7 | | TIM3_CH2 |
| 39 | 65 | 98 | PC8 | I/O | FT | PC8 | | TIM3_CH3 |

**Table 4.     Pin definitions  (continued)**

| Pins | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions | |
|------|------|------|----------|---------|----------------|--------------------------------|---------------------|---|
| LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| 40 | 66 | 99 | PC9 | I/O | FT | PC9 | | TIM3_CH4 |
| 41 | 67 | 100 | PA8 | I/O | FT | PA8 | USART1_CK/ MCO | |
| 42 | 68 | 101 | PA9 | I/O | FT | PA9 | USART1_TX[6] | |
| 43 | 69 | 102 | PA10 | I/O | FT | PA10 | USART1_RX[6] | |
| 44 | 70 | 103 | PA11 | I/O | FT | PA11 | USART1_CTS | |
| 45 | 71 | 104 | PA12 | I/O | FT | PA12 | USART1_RTS | |
| 46 | 72 | 105 | PA13/JTMS-SWDIO | I/O | FT | JTMS-SWDIO | PA13 | |
| - | 73 | 106 | Not connected | | | | | |
| 47 | 74 | 107 | $V_{SS\_2}$ | S | | $V_{SS\_2}$ | | |
| 48 | 75 | 108 | $V_{DD\_2}$ | S | | $V_{DD\_2}$ | | |
| 49 | 76 | 109 | PA14/JTCK-SWCLK | I/O | FT | JTCK-SWCLK | PA14 | |
| 50 | 77 | 110 | PA15/JTDI | I/O | FT | JTDI | PA15/SPI3_NSS | TIM2_CH1_ETR / SPI1_NSS |
| 51 | 78 | 111 | PC10 | I/O | FT | PC10 | UART4_TX | USART3_TX |
| 52 | 79 | 112 | PC11 | I/O | FT | PC11 | UART4_RX | USART3_RX |
| 53 | 80 | 113 | PC12 | I/O | FT | PC12 | UART5_TX | USART3_CK |
| 5 | 81 | 114 | PD0 | I/O | FT | OSC_IN[7] | FSMC_D2 | |
| 6 | 82 | 115 | PD1 | I/O | FT | OSC_OUT[7] | FSMC_D3 | |
| 54 | 83 | 116 | PD2 | I/O | FT | PD2 | TIM3_ETR/UART5_RX | |
| - | 84 | 117 | PD3 | I/O | FT | PD3 | FSMC_CLK | USART2_CTS |
| - | 85 | 118 | PD4 | I/O | FT | PD4 | FSMC_NOE | USART2_RTS |
| - | 86 | 119 | PD5 | I/O | FT | PD5 | FSMC_NWE | USART2_TX |
| - | - | 120 | $V_{SS\_10}$ | S | | | | |
| - | - | 121 | $V_{DD\_10}$ | S | | | | |
| - | 87 | 122 | PD6 | I/O | FT | PD6 | FSMC_NWAIT | USART2_RX |
| - | 88 | 123 | PD7 | I/O | FT | PD7 | FSMC_NE1/ FSMC_NCE2 | USART2_CK |
| - | - | 124 | PG9 | I/O | FT | | FSMC_NE2/ FSMC_NCE3 | |
| - | - | 125 | PG10 | I/O | FT | | FSMC_NE3/ FSMC_NCE4_1 | |
| - | - | 126 | PG11 | I/O | FT | | FSMC_NCE4_2 | |
| - | - | 127 | PG12 | I/O | FT | | FSMC_NE4 | |
| - | - | 128 | PG13 | I/O | FT | | FSMC_A24 | |

**Table 4.    Pin definitions  (continued)**

| Pins | | | Pin name | Type[1] | I / O Level[2] | Main function[3] (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|
| LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| - | - | 129 | PG14 | I/O | FT | | FSMC_A25 | |
| - | - | 130 | $V_{SS\_11}$ | S | | | | |
| - | - | 131 | $V_{DD\_11}$ | S | | | | |
| - | - | 132 | PG15 | I/O | | | | |
| 55 | 89 | 133 | PB3/JTDO | I/O | FT | JTDO | PB3/TRACESWO/ JTDO/ SPI3_SCK | TIM2_CH2 / SPI1_SCK |
| 56 | 90 | 134 | PB4/JNTRST | I/O | FT | JNTRST | PB4/SPI3_MISO | TIM3_CH1 / SPI1_MISO |
| 57 | 91 | 135 | PB5 | I/O | | PB5 | I2C1_SMBAI/ SPI3_MOSI | TIM3_CH2 / SPI1_MOSI |
| 58 | 92 | 136 | PB6 | I/O | FT | PB6 | I2C1_SCL/ TIM4_CH1[6] | USART1_TX |
| 59 | 93 | 137 | PB7 | I/O | FT | PB7 | I2C1_SDA/FSMC_NADV / TIM4_CH2[6] | USART1_RX |
| 60 | 94 | 138 | BOOT0 | I | | BOOT0 | | |
| 61 | 95 | 139 | PB8 | I/O | FT | PB8 | TIM4_CH3 [6] | I2C1_SCL |
| 62 | 96 | 140 | PB9 | I/O | FT | PB9 | TIM4_CH4[6] | I2C1_SDA |
| - | 97 | 141 | PE0 | I/O | FT | PE0 | TIM4_ETR[6]/ FSMC_NBL0 | |
| - | 98 | 142 | PE1 | I/O | FT | PE1 | FSMC_NBL1 | |
| 63 | 99 | 143 | $V_{SS\_3}$ | S | | $V_{SS\_3}$ | | |
| 64 | 100 | 144 | $V_{DD\_3}$ | S | | $V_{DD\_3}$ | | |

1. I = input, O = output, S = supply, HiZ = high impedance.

2. FT = 5 V tolerant.

3. Function availability depends on the chosen device.

4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.

5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual

**Table 5.     FSMC pin definition**

| Pins | FSMC | | | | | LQFP100 BGA100[1] |
|------|------|-----|----------|--------------|-------------|---------|
|      | **CF** | **CF/IDE** | **NOR/PSRAM** | **NOR/SRAM Mux** | **NAND 16 bit** | |
| PE2  |      |      | A23 | A23 |     | Yes |
| PE3  |      |      | A19 | A19 |     | Yes |
| PE4  |      |      | A20 | A20 |     | Yes |
| PE5  |      |      | A21 | A21 |     | Yes |
| PE6  |      |      | A22 | A22 |     | Yes |
| PF0  | A0   | A0   | A0  |     |     | - |
| PF1  | A1   | A1   | A1  |     |     | - |
| PF2  | A2   | A2   | A2  |     |     | - |
| PF3  | A3   |      | A3  |     |     | - |
| PF4  | A4   |      | A4  |     |     | - |
| PF5  | A5   |      | A5  |     |     | - |
| PF6  | NIORD | NIORD |   |     |     | - |
| PF7  | NREG | NREG |    |     |     | - |
| PF8  | NIOWR | NIOWR |   |     |     | - |
| PF9  | CD   | CD   |     |     |     | - |
| PF10 | INTR | INTR |     |     |     | - |
| PF11 | NIOS16 | NIOS16 |  |    |     | - |
| PF12 | A6   |      | A6  |     |     | - |
| PF13 | A7   |      | A7  |     |     | - |
| PF14 | A8   |      | A8  |     |     | - |
| PF15 | A9   |      | A9  |     |     | - |
| PG0  | A10  |      | A10 |     |     | - |
| PG1  |      |      | A11 |     |     | - |
| PE7  | D4   | D4   | D4  | DA4 | D4  | Yes |
| PE8  | D5   | D5   | D5  | DA5 | D5  | Yes |
| PE9  | D6   | D6   | D6  | DA6 | D6  | Yes |
| PE10 | D7   | D7   | D7  | DA7 | D7  | Yes |
| PE11 | D8   | D8   | D8  | DA8 | D8  | Yes |
| PE12 | D9   | D9   | D9  | DA9 | D9  | Yes |
| PE13 | D10  | D10  | D10 | DA10 | D10 | Yes |
| PE14 | D11  | D11  | D11 | DA11 | D11 | Yes |
| PE15 | D12  | D12  | D12 | DA12 | D12 | Yes |
| PD8  | D13  | D13  | D13 | DA13 | D13 | Yes |

**Table 5.    FSMC pin definition (continued)**

| Pins | FSMC | | | | | LQFP100 BGA100[1] |
|------|------|------|-----------|--------------|-------------|-------------------|
|      | CF | CF/IDE | NOR/PSRAM | NOR/SRAM Mux | NAND 16 bit | |
| PD9 | D14 | D14 | D14 | DA14 | D14 | Yes |
| PD10 | D15 | D15 | D15 | DA15 | D15 | Yes |
| PD11 | | | A16 | A16 | CLE | Yes |
| PD12 | | | A17 | A17 | ALE | Yes |
| PD13 | | | A18 | A18 | | Yes |
| PD14 | D0 | D0 | D0 | DA0 | D0 | Yes |
| PD15 | D1 | D1 | D1 | DA1 | D1 | Yes |
| PG2 | | | A12 | | | - |
| PG3 | | | A13 | | | - |
| PG4 | | | A14 | | | - |
| PG5 | | | A15 | | | - |
| PG6 | | | | | INT2 | - |
| PG7 | | | | | INT3 | - |
| PD0 | D2 | D2 | D2 | DA2 | D2 | Yes |
| PD1 | D3 | D3 | D3 | DA3 | D3 | Yes |
| PD3 | | | CLK | CLK | | Yes |
| PD4 | NOE | NOE | NOE | NOE | NOE | Yes |
| PD5 | NWE | NWE | NWE | NWE | NWE | Yes |
| PD6 | NWAIT | NWAIT | NWAIT | NWAIT | NWAIT | Yes |
| PD7 | | | NE1 | NE1 | NCE2 | Yes |
| PG9 | | | NE2 | NE2 | NCE3 | - |
| PG10 | NCE4_1 | NCE4_1 | NE3 | NE3 | | - |
| PG11 | NCE4_2 | NCE4_2 | | | | - |
| PG12 | | | NE4 | NE4 | | - |
| PG13 | | | A24 | A24 | | - |
| PG14 | | | A25 | A25 | | Yes |
| PB7 | | | NADV | NADV | | Yes |
| PE0 | | | NBL0 | NBL0 | | Yes |
| PE1 | | | NBL1 | NBL1 | | Yes |

1. Ports F and G are not available in devices delivered in 100-pin packages.

# 4    Memory mapping

The memory map is shown in *Figure 6*.

**Figure 6.    Memory map**

| | Address range |
|---|---|
| Reserved | 0xA000 1000 - 0xBFFF FFFF |
| FSMC register | 0xA000 0000 - 0xA000 0FFF |
| FSMC bank 4 PCCARD | 0x9000 0000 - 0x9FFF FFFF |
| FSMC bank 3 NAND (NAND2) | 0x8000 0000 - 0x8FFF FFFF |
| FSMC bank 2 NAND (NAND1) | 0x7000 0000 - 0x7FFF FFFF |
| FSMC bank 1 NOR/PSRAM 4 | 0x6C00 0000 - 0x6FFF FFFF |
| FSMC bank 1 NOR/PSRAM 3 | 0x6800 0000 - 0x6BFF FFFF |
| FSMC bank 1 NOR/PSRAM 2 | 0x6400 0000 - 0x67FF FFFF |
| FSMC bank 1 NOR/PSRAM 1 | 0x6000 0000 - 0x63FF FFFF |
| Reserved | 0x4002 3400 - 0x5FFF FFFF |
| CRC | 0x4002 3000 - 0x4002 33FF |
| Reserved | 0x4002 2400 - 0x4002 2FFF |
| Flash interface | 0x4002 2000 - 0x4002 23FF |
| Reserved | 0x4002 1400 - 0x4002 1FFF |
| RCC | 0x4002 1000 - 0x4002 13FF |
| Reserved | 0x4002 0400 - 0x4002 0FFF |
| DMA2 | 0x4002 0400 - 0x4002 07FF |
| DMA1 | 0x4002 0000 - 0x4002 03FF |
| Reserved | 0x4001 8400 - 0x4001 FFFF |
| Reserved | 0x4001 8000 - 0x4001 83FF |
| Reserved | 0x4001 3C00 - 0x4001 7FFF |
| USART1 | 0x4001 3800 - 0x4001 3BFF |
| Reserved | 0x4001 3400 - 0x4001 37FF |
| SPI1 | 0x4001 3000 - 0x4001 33FF |
| Reserved | 0x4001 2800 - 0x4001 2FFF |
| ADC1 | 0x4001 2400 - 0x4001 27FF |
| Port G | 0x4001 2000 - 0x4001 23FF |
| Port F | 0x4001 1C00 - 0x4001 1FFF |
| Port E | 0x4001 1800 - 0x4001 1BFF |
| Port D | 0x4001 1400 - 0x4001 17FF |
| Port C | 0x4001 1000 - 0x4001 13FF |
| Port B | 0x4001 0C00 - 0x4001 0FFF |
| Port A | 0x4001 0800 - 0x4001 0BFF |
| EXTI | 0x4001 0400 - 0x4001 07FF |
| AFIO | 0x4001 0000 - 0x4001 03FF |
| Reserved | 0x4000 7800 - 0x4000 FFFF |
| DAC | 0x4000 7400 - 0x4000 77FF |
| PWR | 0x4000 7000 - 0x4000 73FF |
| BKP | 0x4000 6C00 - 0x4000 6FFF |
| Reserved | 0x4000 5C00 - 0x4000 6BFF |
| I2C2 | 0x4000 5800 - 0x4000 5BFF |
| I2C1 | 0x4000 5400 - 0x4000 57FF |
| UART5 | 0x4000 5000 - 0x4000 53FF |
| UART4 | 0x4000 4C00 - 0x4000 4FFF |
| USART3 | 0x4000 4800 - 0x4000 4BFF |
| USART2 | 0x4000 4400 - 0x4000 47FF |
| Reserved | 0x4000 4000 - 0x4000 43FF |
| SPI3 | 0x4000 3C00 - 0x4000 3FFF |
| SPI2 | 0x4000 3800 - 0x4000 3BFF |
| Reserved | 0x4000 3400 - 0x4000 37FF |
| IWDG | 0x4000 3000 - 0x4000 33FF |
| WWDG | 0x4000 2C00 - 0x4000 2FFF |
| RTC | 0x4000 2800 - 0x4000 2BFF |
| Reserved | 0x4000 1800 - 0x4000 27FF |
| TIM7 | 0x4000 1400 - 0x4000 17FF |
| TIM6 | 0x4000 1000 - 0x4000 13FF |
| TIM5 | 0x4000 0C00 - 0x4000 0FFF |
| TIM4 | 0x4000 0800 - 0x4000 0BFF |
| TIM3 | 0x4000 0400 - 0x4000 07FF |
| TIM2 | 0x4000 0000 - 0x4000 03FF |

| Address | Block |
|---|---|
| 0xFFFF FFFF | 512-Mbyte block 7 Cortex-M3's internal peripherals |
| 0xE000 0000 0xDFFF FFFF | |
| | 512-Mbyte block 6 Not used |
| 0xC000 0000 0xBFFF FFFF | |
| | 512-Mbyte block 5 FSMC register |
| 0xA000 0000 0x9FFF FFFF | |
| | 512-Mbyte block 4 FSMC bank3 & bank4 |
| 0x8000 0000 0x7FFF FFFF | |
| | 512-Mbyte block 3 FSMC bank1 & bank2 |
| 0x6000 0000 0x5FFF FFFF | |
| | 512-Mbyte block 2 Peripherals |
| 0x4000 0000 0x3FFF FFFF | |
| | 512-Mbyte block 1 SRAM |
| 0x2000 0000 0x1FFF FFFF | |
| | 512-Mbyte block 0 Code |
| 0x0000 0000 | |

| | Address |
|---|---|
| Reserved | 0x3FFF FFFF 0x2000 C000 |
| SRAM (48 KB aliased by bit-banding) | 0x2000 BFFF 0x2000 0000 |
| Option Bytes | 0x1FFF F800 - 0x1FFF F80F |
| System memory | 0x1FFF F000- 0x1FFF F7FF |
| Reserved | 0x1FFF EFFF 0x0808 0000 |
| Flash | 0x0807 FFFF 0x0800 0000 |
| Reserved | 0x07FF FFFF 0x0008 0000 |
| Aliased to Flash, system memory or SRAM depending on BOOT pins | 0x0007 FFFF 0x0000 0000 |

ai14811b

# 5 Electrical characteristics

## 5.1 Test conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\ °C$ and $T_A = T_A max$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

### 5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\ °C$, $V_{DD} = 3.3\ V$ (for the $2\ V \leq V_{DD} \leq 3.6\ V$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

**Figure 7.    Pin loading conditions**     **Figure 8.    Pin input voltage**
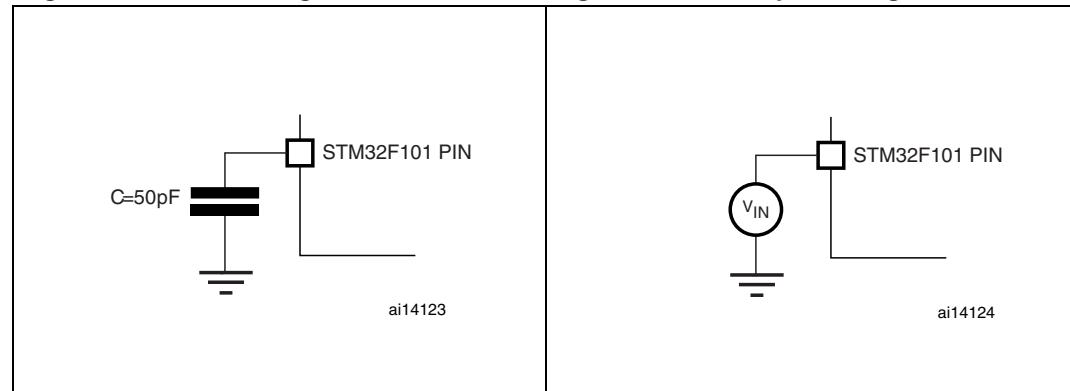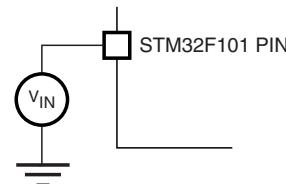


### 5.1.6 Power supply scheme

**Figure 9.    Power supply scheme**
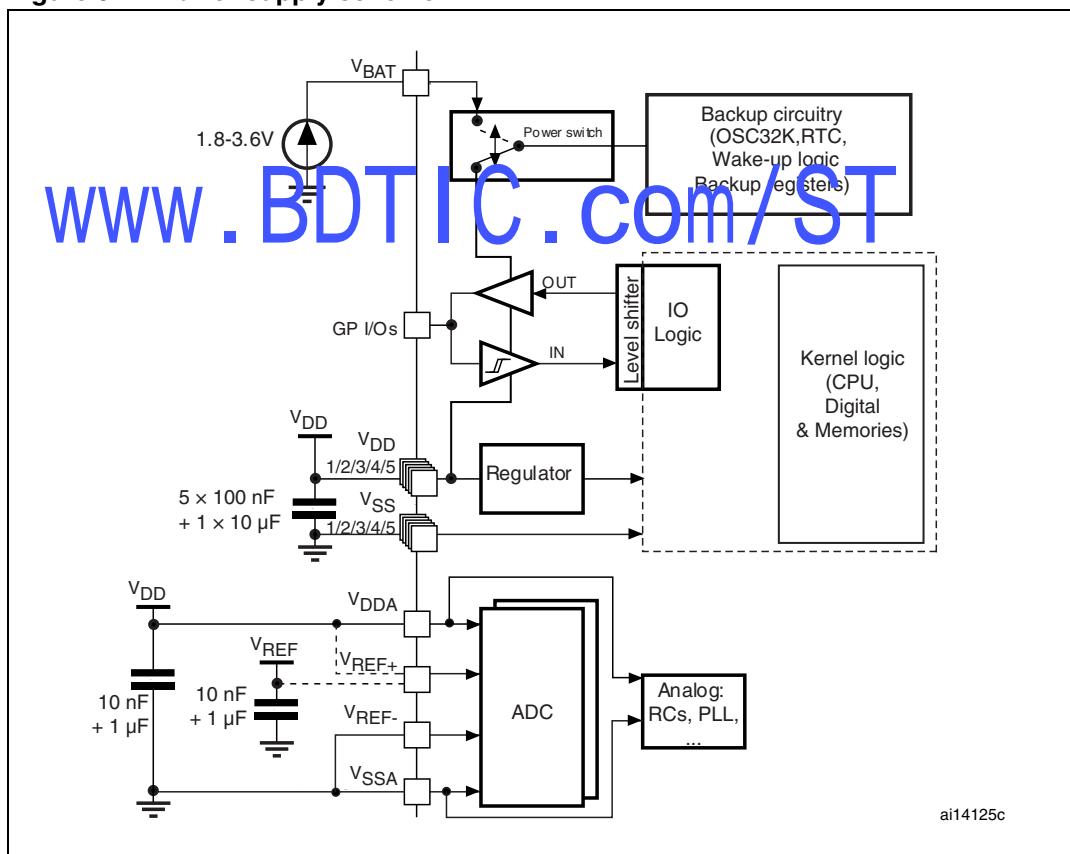
### 5.1.7    Current consumption measurement

**Figure 10.   Current consumption measurement scheme**



ai14126
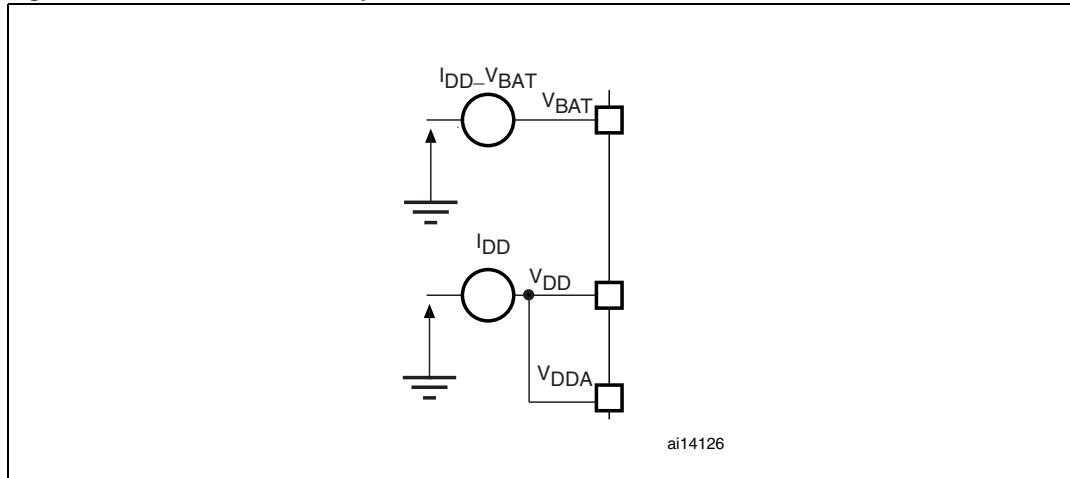
## 5.2    Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 6.   Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|--------|---------|-----|-----|------|
| $V_{DD} - V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD})$[1] | −0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on five volt tolerant pin[2] | $V_{SS}$ −0.3 | +5.5 | |
| | Input voltage on any other pin[2] | $V_{SS}$ −0.3 | $V_{DD}$+0.3 | |
| $\|\Delta V_{DDx}\|$ | Variations between different power pins | 50 | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between all the different ground pins | 50 | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see *Section 5.3.12: Absolute maximum ratings (electrical sensitivity)* | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

**Table 7.    Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power lines (source)[1] | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)[1] | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | −25 | |
| $I_{INJ(PIN)}$ [2][3] | Injected current on NRST pin | ± 5 | |
| | Injected current on High-speed external OSC_IN and Low-speed external OSC_IN pins | ± 5 | |
| | Injected current on any other pin[4] | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ [2] | Total injected current (sum of all I/O and control pins)[4] | ± 25 | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if $V_{IN}$ maximum is respected. If $V_{IN}$ maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.17: 12-bit ADC characteristics*.

4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

**Table 8.    Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | −65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 5.3        Operating conditions

## 5.3.1      General operating conditions

**Table 9.        General operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 36 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 36 | |
| $V_{DD}$ | Standard operating voltage | | 2 | 3.6 | V |
| $V_{BAT}$ | Backup operating voltage | | 1.8 | 3.6 | V |
| $P_D$ | Power dissipation at $T_A =$ 85 °C[1] | LQFP144 | | 444 | mW |
| | | LQFP100 | | 434 | |
| | | LQFP64 | | 444 | |
| $T_A$ | Ambient temperature | Maximum power dissipation | −40 | 85 | °C |
| | | Low power dissipation[2] | −40 | 105 | °C |
| $T_J$ | Junction temperature range | | −40 | 105 | °C |

1. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 99*).

2. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_J$max (see *Table 6.2: Thermal characteristics on page 99*).

## 5.3.2      Operating conditions at power-up / power-down

The parameters given in *Table 10* are derived from tests performed under the ambient temperature condition summarized in *Table 9*.

**Table 10.      Operating conditions at power-up / power-down**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 11. Embedded reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.1 | 2.18 | 2.26 | V |
| | | PLS[2:0]=000 (falling edge) | 2 | 2.08 | 2.16 | V |
| | | PLS[2:0]=001 (rising edge) | 2.19 | 2.28 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.09 | 2.18 | 2.27 | V |
| | | PLS[2:0]=010 (rising edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=010 (falling edge) | 2.18 | 2.28 | 2.38 | V |
| | | PLS[2:0]=011 (rising edge) | 2.38 | 2.48 | 2.58 | V |
| | | PLS[2:0]=011 (falling edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=100 (rising edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=100 (falling edge) | 2.37 | 2.48 | 2.59 | V |
| | | PLS[2:0]=101 (rising edge) | 2.57 | 2.68 | 2.79 | V |
| | | PLS[2:0]=101 (falling edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=110 (rising edge) | 2.66 | 2.78 | 2.9 | V |
| | | PLS[2:0]=110 (falling edge) | 2.56 | 2.68 | 2.8 | V |
| | | PLS[2:0]=111 (rising edge) | 2.76 | 2.88 | 3 | V |
| | | PLS[2:0]=111 (falling edge) | 2.66 | 2.78 | 2.9 | V |
| $V_{PVDhyst}$[2] | PVD hysteresis | | | 100 | | mV |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1.8[1] | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | | 40 | | mV |
| $t_{RSTTEMPO}$[2] | Reset temporization | | 1.5 | 2.5 | 3.5 | ms |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 12. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{REFINT}$ | Internal reference voltage | $-40\ °C < T_A < +85\ °C$ | 1.16 | 1.20 | 1.24 | V |
| $T_{S\_vrefint}$[1] | ADC sampling time when reading the internal reference voltage | | | 5.1 | 17.1 | µs |

1. Shortest sampling time can be determined in the application by multiple iterations.

### 5.3.5 Supply current characteristics

The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.

**Maximum current consumption**

The MCU is placed under the following conditions:

● All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

● All peripherals are disabled except if it is explicitly mentioned

● The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)

● Prefetch in on (reminder: this bit must be set before clock setting and bus prescaling)

● When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 13. Maximum current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max[1] $T_A = 85\ °C$ | Unit |
|--------|-----------|------------|-----------|------------------------|------|
| $I_{DD}$ | Supply current in Run mode | External clock [2], all peripherals enabled | 36 MHz | 39 | mA |
| | | | 24 MHz | 27 | |
| | | | 16 MHz | 20 | |
| | | | 8 MHz | 11 | |
| | | External clock [2], all peripherals Disabled | 36 MHz | 22 | |
| | | | 24 MHz | 16.5 | |
| | | | 16 MHz | 12.5 | |
| | | | 8 MHz | 8 | |

1. Data based on characterization results, not tested in production.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz; external clock is 9 MHz for $f_{HCLK} = 36$ MHz.

**Table 14.** **Maximum current consumption in Run mode, code with data processing running from RAM**

| Symbol | Parameter | Conditions | f$_{HCLK}$ | Max | Unit |
|---|---|---|---|---|---|
| | | | | T$_A$ = 85 °C | |
| I$_{DD}$ | Supply current in Run mode | External clock [1], all peripherals enabled | 36 MHz[2] | 34 | mA |
| | | | 24 MHz[2] | 24 | |
| | | | 16 MHz[2] | 17 | |
| | | | 8 MHz[2] | 10 | |
| | | External clock[1] all peripherals disabled[2] | 36 MHz | 18 | |
| | | | 24 MHz | 13 | |
| | | | 16 MHz | 10 | |
| | | | 8 MHz | 6 | |

1. External clock is 8 MHz and PLL is on when f$_{HCLK}$ > 8 MHz; external clock is 9 MHz for f$_{HCLK}$ = 36 MHz.

2. Based on characterization, not tested in production.

**Figure 11.** **Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled**
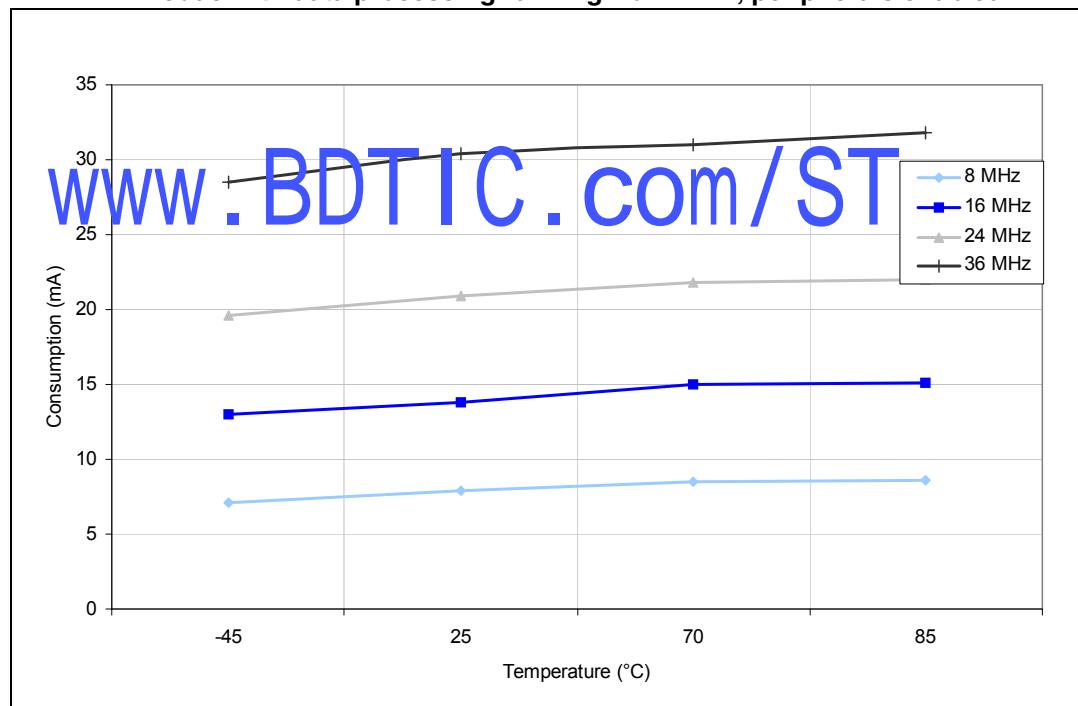
**Figure 12.** **Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled**
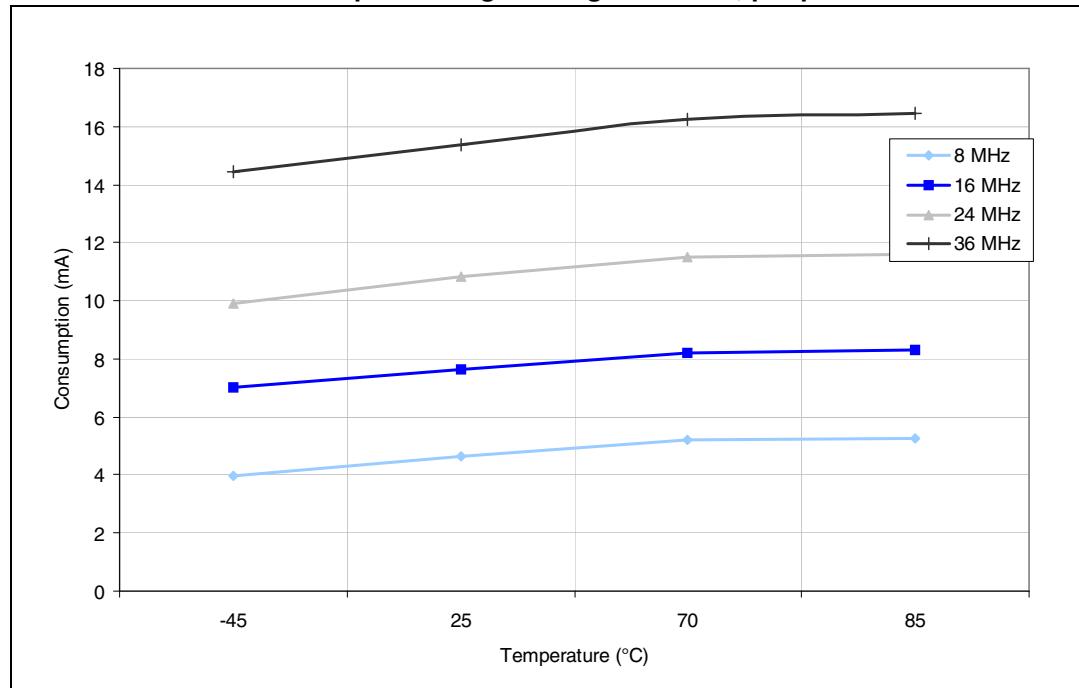


**Table 15.** **Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max $T_A = 85\ °C$ | Unit |
|--------|-----------|------------|------------|------------------|------|
| $I_{DD}$ | Supply current in Sleep mode | External clock[1] all peripherals enabled | 36 MHz[2] | 24 | mA |
| | | | 24 MHz[2] | 17 | |
| | | | 16 MHz[2] | 12.5 | |
| | | | 8 MHz[2] | 8 | |
| | | External clock[1], all peripherals disabled[2] | 36 MHz | 6 | |
| | | | 24 MHz | 5 | |
| | | | 16 MHz | 4.5 | |
| | | | 8 MHz | 4 | |

1. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz; external clock is 9 MHz for $f_{HCLK}$ = 36 MHz.

2. Based on characterization, not tested in production.

**Table 16.     Typical and maximum current consumptions in Stop and Standby modes**

| Symbol | Parameter | Conditions | Typ[1] | | Max | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$ = 2.4 V | $V_{DD}/V_{BAT}$ = 3.3 V | $T_A$ = 85 °C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 34.5 | 35 | TBD[2] | µA |
| | | Regulator in Low Power mode, Low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 24.5 | 25 | TBD[2] | |
| | Supply current in Standby mode[3] | Low-speed internal RC oscillator and independent watchdog ON | 3 | 3.8 | TBD | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | 2.8 | 3.6 | TBD | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | 2.8 | 3.6 | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 1.8 | 2.1 | 5[4] | |
| $I_{DD\_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON | TBD | TBD | TBD[4] | |

1. Typical values are measured at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V, unless otherwise specified.

2. Data based on characterization results, tested in production at $V_{DD}$ max and $f_{HCLK}$ max.

3. To have the Standby consumption with RTC ON, add $I_{DD\_VBAT}$ (Low-speed oscillator and RTC ON) to $I_{DD}$ Standby (when $V_{DD}$ is present the Backup Domain is powered by $V_{DD}$ supply).

4. Data based on characterization results, not tested in production.

**Figure 13.   Current consumption in Stop mode with regulator in main mode versus temperature at different $V_{DD}$ values**
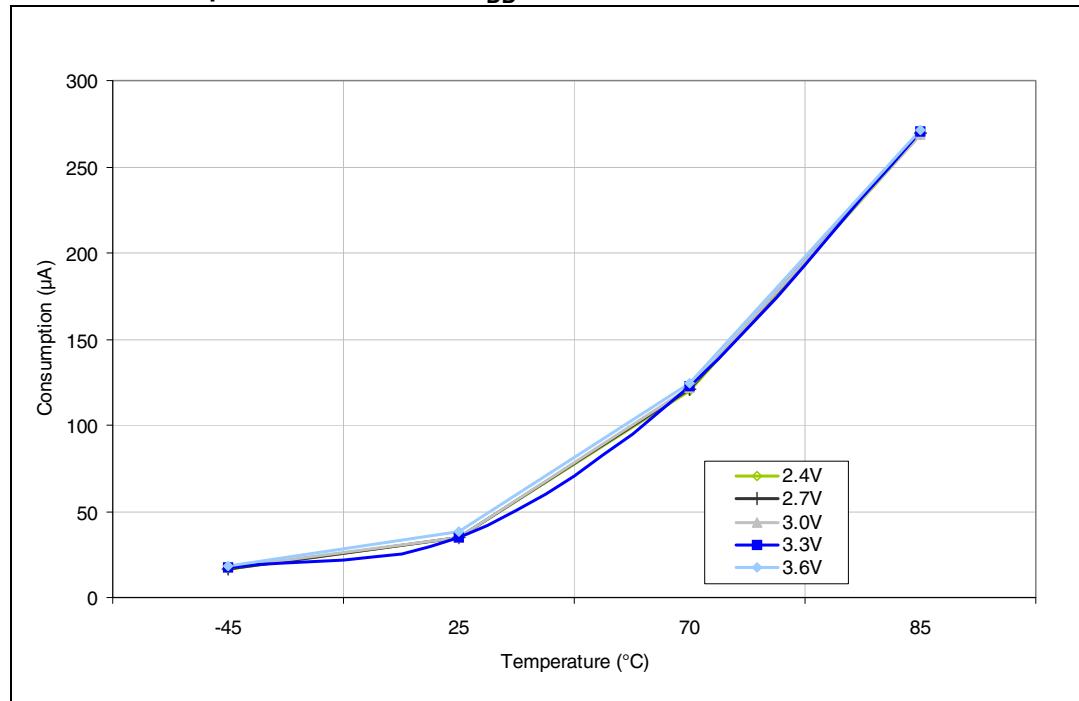


**Figure 14.   Current consumption in Stop mode with regulator in low-power mode versus temperature at different $V_{DD}$ values**
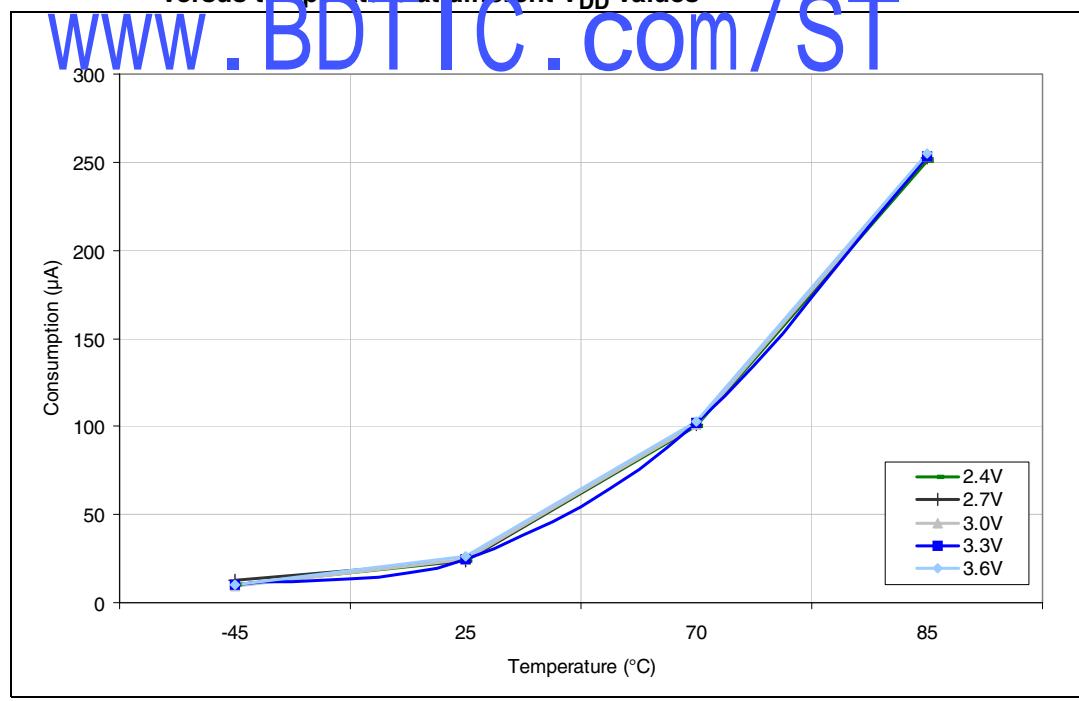
**Figure 15.    Current consumption in Standby mode versus temperature at different V$_{DD}$ values**
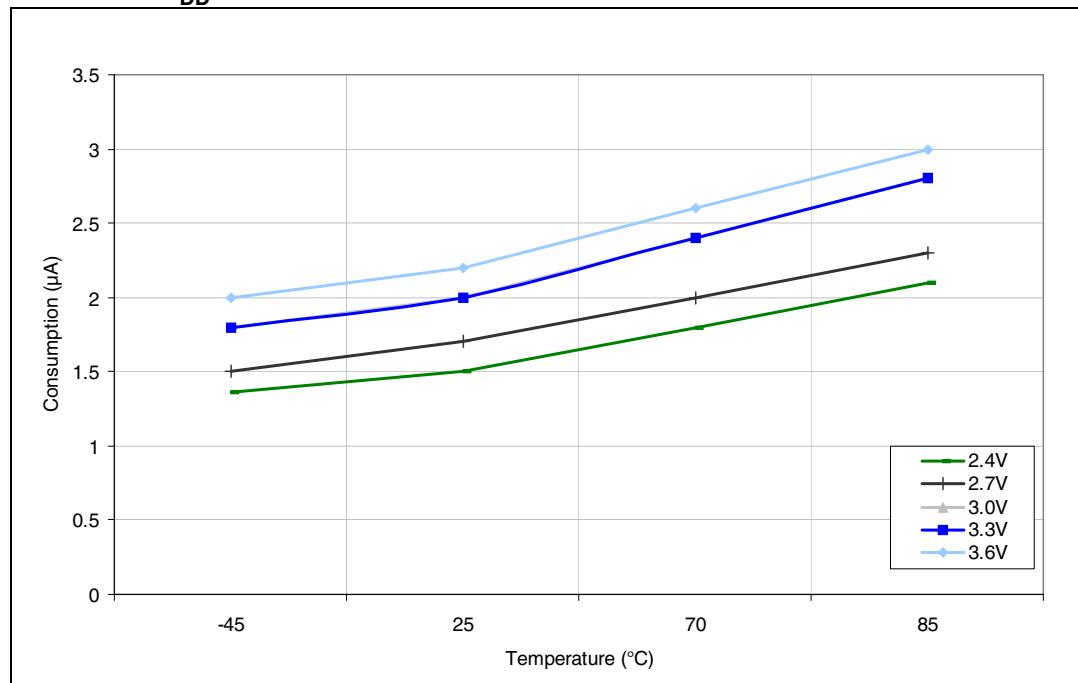
### Typical current consumption

The MCU is placed under the following conditions:

● All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

● All peripherals are disabled except if it is explicitly mentioned

● The Flash access time is adjusted to $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 36 MHz)

● Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling)

● When the peripherals are enabled $f_{PCLK1} = f_{HCLK/4}$, $f_{PCLK2} = f_{HCLK/2}$, $f_{ADCCLK} = f_{PCLK2}/4$

The parameters given in *Table 17* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 17.    Typical current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ[1] All peripherals enabled[2] | Typ[1] All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode | External clock[3] | 36 MHz | 26.6 | 16.2 | mA |
| | | | 24 MHz | 18.5 | 11.4 | |
| | | | 16 MHz | 12.8 | 8.2 | |
| | | | 8 MHz | 7.2 | 5 | |
| | | | 4 MHz | 4.2 | 3.1 | |
| | | | 2 MHz | 2.7 | 2.1 | |
| | | | 1 MHz | 2 | 1.7 | |
| | | | 500 kHz | 1.6 | 1.4 | |
| | | | 125 kHz | 1.3 | 1.2 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 26 | 15.6 | |
| | | | 24 MHz | 17.9 | 10.8 | |
| | | | 16 MHz | 12.2 | 7.6 | |
| | | | 8 MHz | 6.6 | 4.4 | |
| | | | 4 MHz | 3.6 | 2.5 | |
| | | | 2 MHz | 2.1 | 1.5 | |
| | | | 1 MHz | 1.4 | 1.1 | |
| | | | 500 kHz | 1 | 0.8 | |
| | | | 125 kHz | 0.7 | 0.6 | |

1.  Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.

2.  Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3.  External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

**Table 18. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ[1] All peripherals enabled[2] | Typ[1] All peripherals disabled | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Sleep mode | External clock[3] | 36 MHz | 15.1 | 3.6 | mA |
| | | | 24 MHz | 10.4 | 2.6 | |
| | | | 16 MHz | 7.2 | 2 | |
| | | | 8 MHz | 3.9 | 1.3 | |
| | | | 4 MHz | 2.6 | 1.2 | |
| | | | 2 MHz | 1.85 | 1.15 | |
| | | | 1 MHz | 1.5 | 1.1 | |
| | | | 500 kHz | 1.3 | 1.05 | |
| | | | 125 kHz | 1.2 | 1.05 | |
| | | Running on High Speed Internal RC (HSI), AHB prescaler used to reduce the frequency | 36 MHz | 14.5 | 3 | |
| | | | 24 MHz | 9.8 | 2 | |
| | | | 16 MHz | 6.6 | 1.4 | |
| | | | 8 MHz | 3.3 | 0.7 | |
| | | | 4 MHz | 2 | 0.6 | |
| | | | 2 MHz | 1.25 | 0.55 | |
| | | | 1 MHz | 0.9 | 0.5 | |
| | | | 500 kHz | 0.7 | 0.45 | |
| | | | 125 kHz | 0.6 | 0.45 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**On-chip peripheral current consumption**

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

● all I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)

● all peripherals are disabled unless otherwise mentioned

● the given value is calculated by measuring the current consumption

  – with all peripherals clocked off

  – with only one peripheral clocked on

● ambient operating temperature and $V_{DD}$ supply voltage conditions summarized in *Table 6*.

**Table 19.    Peripheral current consumption**

| Peripheral | | Typical consumption at 25 °C[1] | Unit |
|---|---|---|---|
| APB1 | TIM2 | 0.6 | mA |
| | TIM3 | 0.6 | |
| | TIM4 | 0.6 | |
| | TIM5 | 0.6 | |
| | TIM6 | 0.2 | |
| | TIM7 | 0.2 | |
| | SPI2 | 0.15 | |
| | SPI3 | 0.15 | |
| | USART2 | 0.25 | |
| | USART3 | 0.25 | |
| | UART4 | 0.3 | |
| | UART5 | 0.3 | |
| | I2C1 | 0.22 | |
| | I2C2 | 0.22 | |
| | DAC | 0.72 | |
| APB2 | GPIOA | 0.3 | |
| | GPIOB | 0.4 | |
| | GPIOC | 0.4 | |
| | GPIOD | 0.3 | |
| | GPIOE | 0.5 | |
| | GPIOF | 0.4 | |
| | GPIOG | 0.5 | |
| | ADC[2] | 1.4 | |
| | SPI1 | 0.3 | |
| | USART1 | 0.6 | |

1. $f_{HCLK}$ = 36 MHz, $f_{APB1}$ = $f_{HCLK/2}$, $f_{APB2}$ = $f_{HCLK}$, default prescaler value for each peripheral.

2. Specific conditions for ADC: $f_{HCLK}$ = 28 MHz, $f_{APB1}$ = $f_{HCLK/2}$, $f_{APB2}$ = $f_{HCLK}$, $f_{ADCCLK}$ = $f_{APB2/2}$, ADON bit in the ADC_CR2 register is set to 1.

### 5.3.6    External clock source characteristics

**High-speed user external clock**

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 20.    High-speed user external (HSE) clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $f_{HSE\_ext}$ | User external clock source frequency[1] | | | 8 | 25 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time[1] | | 16 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time[1] | | | | 5 | |
| $I_L$ | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ±1 | μA |

1.   Value based on design simulation and/or technology characteristics. It is not tested in production.

**Low-speed user external clock**

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

**Table 21.    Low-speed user external clock characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $f_{LSE\_ext}$ | User external clock source frequency[1] | | | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | | $V_{SS}$ | | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time[1] | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time[1] | | | | 5 | |
| $I_L$ | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ±1 | μA |

1.   Value based on design simulation and/or technology characteristics. It is not tested in production.

**Figure 16.    High-speed external clock source AC timing diagram**
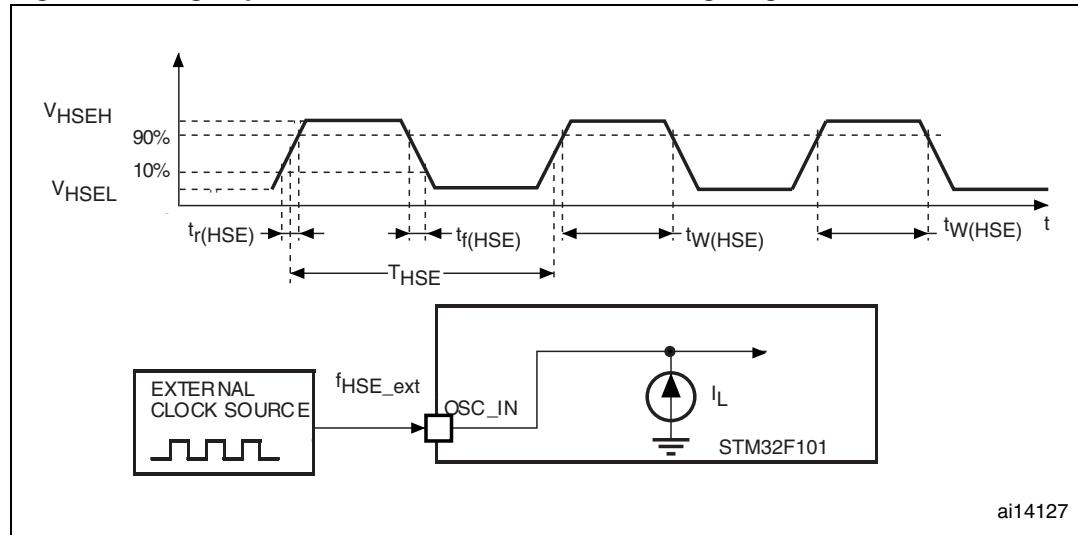


**Figure 17.    Low-speed external clock source AC timing diagram**
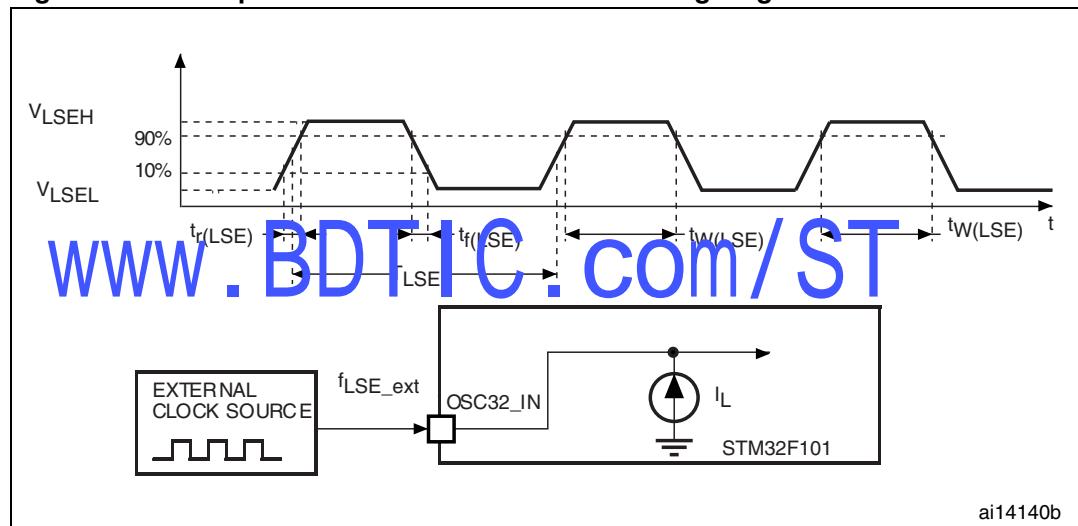
### High-speed external clock

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 22.    HSE 4-16 MHz oscillator characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------|-----|-----|-----|------|
| $f_{OSC\_IN}$ | Oscillator frequency | | 4 | 8 | 16 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | k$\Omega$ |
| $C_{L1}$ $C_{L2}$[2] | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)[3] | $R_S = 30\ \Omega$ | | 30 | | pF |
| $i_2$ | HSE driving current | $V_{DD} = 3.3$ V $V_{IN} = V_{SS}$ with 30 pF load | | | 1 | mA |
| $g_m$[4] | Oscillator transconductance | Startup | 25 | | | mA/V |
| $t_{SU(HSE)}$[5] | Startup time | $V_{DD}$ is stabilized | | 2 | | ms |

1.  Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2.  For $C_{L1}$ and $C_{L2}$ it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included when sizing $C_{L1}$ and $C_{L2}$ (10 pF can be used as a rough estimate of the combined pin and board capacitance).

3.  The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.

4.  Based on characterization results, not tested in production.

5.  $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 18.    Typical application with an 8 MHz crystal**
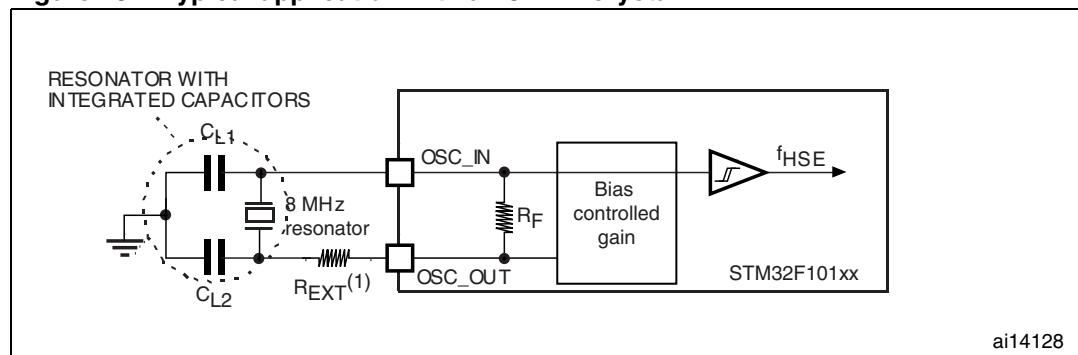


1.  $R_{EXT}$ value depends on the crystal characteristics. Typical value is in the range of 5 to 6$R_S$.

**Low-speed external clock**

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 23.    LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $R_F$ | Feedback resistor | | | 5 | | MΩ |
| $C_{L1}$ $C_{L2}$ | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)[1] | $R_S$ = 30 KΩ | | | 15 | pF |
| $I_2$ | LSE driving current | $V_{DD}$ = 3.3 V $V_{IN} = V_{SS}$ | | | 1.4 | µA |
| $g_m$ | Oscillator transconductance | | 5 | | | µA/V |
| $t_{SU(LSE)}$[2] | Startup time | $V_{DD}$ is stabilized | | 3 | | s |

1.  The oscillator selection can be optimized in terms of supply current using an high quality resonator with small $R_S$ value for example MSIV-TIN32.768 kHz. Refer to crystal manufacturer for more details

2.  $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

**Figure 19.    Typical application with a 32.768 kHz crystal**
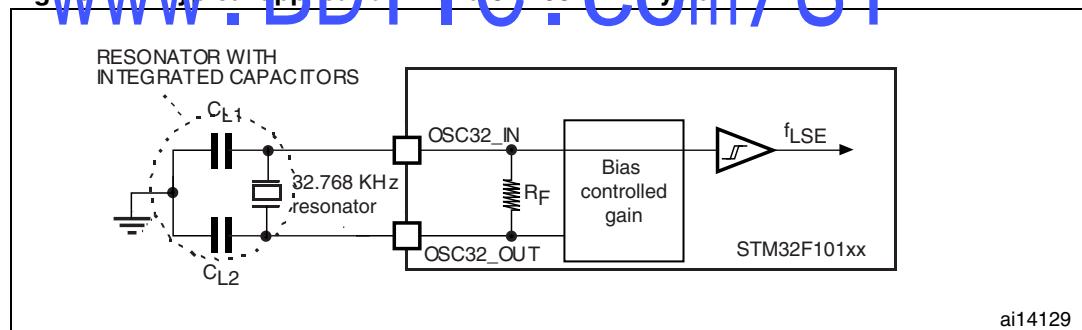
### 5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**High-speed internal (HSI) RC oscillator**

**Table 24.    HSI oscillator characteristics[1]**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | | | 8 | | MHz |
| $ACC_{HSI}$ | Accuracy of HSI oscillator | $T_A = -40$ to $85\ ^\circ$C[2] | | | $\pm 3$ | % |
| | | at $T_A = 25\ ^\circ$C | | $\pm 1$ | $\pm 2$ | % |
| $t_{su(HSI)}$ | HSI oscillator startup time | | 1 | | 2 | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100 | µA |

1. $V_{DD} = 3.3$ V, $T_A = -40$ to $85\ ^\circ$C unless otherwise specified.

2. Values based on device characterization, not tested in production.

**LSI low speed internal RC oscillator**

**Table 25.    LSI oscillator characteristics [1]**

| Symbol | Parameter | Conditions | Min[2] | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$ | LSI oscillator startup time | | | | 85 | µs |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 0.65 | 1.2 | µA |

1. $V_{DD} = 3$ V, $T_A = -40$ to $85\ ^\circ$C unless otherwise specified.

2. Value based on device characterization, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

● Stop or Standby mode: the clock source is the RC oscillator

● Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 26.       Low-power mode wakeup timings**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $t_{WUSLEEP}$[1] | Wakeup from Sleep mode | Wakeup on HSI RC clock | 1.8 | µs |
| $t_{WUSTOP}$[1] | Wakeup from Stop mode (regulator in run mode) | HSI RC wakeup time = 2 µs | 3.6 | µs |
| | Wakeup from Stop mode (regulator in low-power mode) | HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs | 5.4 | |
| $t_{WUSTDBY}$[1] | Wakeup from Standby mode | HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs | 50 | µs |

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

### 5.3.8      PLL characteristics

The parameters given in *Table 27* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 27.       PLL characteristics**

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max[1] | |
| $f_{PLL\_IN}$ | PLL input clock | | | 8.0 | | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock | | 16 | | 36 | MHz |
| $t_{LOCK}$ | PLL lock time | | | | 200 | µs |

1. Data based on device characterization, not tested in production.

### 5.3.9 Memory characteristics

**Flash memory**

The characteristics are given at $T_A$ = -40 to 85 °C unless otherwise specified.

**Table 28.    Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word programming time | $T_A$ = -40 to +85 °C | 40 | 52.5 | 70 | µs |
| $t_{ERASE}$ | Page (2 KB) erase time | $T_A$ = -40 to +85 °C | 20 | | 40 | ms |
| $t_{ME}$ | Mass erase time | $T_A$ = -40 to +85 °C | 20 | | 40 | ms |
| $I_{DD}$ | Supply current | Read mode $f_{HCLK}$ = 36MHz with 2 wait states, $V_{DD}$ = 3.3 V | | | 28 | mA |
| | | Write mode $f_{HCLK}$ = 36 MHz, $V_{DD}$ = 3.3 V | | | 7 | mA |
| | | Erase mode $f_{HCLK}$ = 36 MHz, $V_{DD}$ = 3.3 V | | | 5 | mA |
| | | Power-down mode / Halt, $V_{DD}$ = 3.0 to 3.6 V | | | 50 | µA |
| $V_{prog}$ | Programming voltage | | 2 | | 3.6 | V |

1. Values based on characterization and not tested in production.

**Table 29.    Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min[1] | Typ | Max | |
| $N_{END}$ | Endurance | | TBD[2] | | | kcycles |
| $t_{RET}$ | Data retention | $T_A$ = 85 °C, 1000 cycles | 30 | | | Years |

1. Values based on characterization not tested in production.

2. TBD = to be determined.

## 5.3.10 FSMC characteristics

### Flexible static memory controller (FSMC) timings

All the timing characteristics are relative to the FSMC_CLK signal for synchronous SRAM/NOR Flash memory accesses.

**Figure 20. Asynchronous non-multiplexed SRAM/NOR write timings**


$t_{w(NE)}$
FSMC_NEx
FSMC_NOE
$t_{v(NWE\_NE)}$
$t_{w(NWE)}$
$t_{h(NE\_NWE)}$
FSMC_NWE
$t_{v(A\_NE)}$
$t_{h(A\_NWE)}$
FSMC_A[25:0]
Address
$t_{v(BL\_NE)}$
$t_{h(BL\_NWE)}$
FSMC_NBL[3:0]
NBL
$t_{v(Data\_NE)}$
$t_{h(Data\_NWE)}$
FSMC_D[15:0]
Data
$t_{v(NADV\_NE)}$
$t_{w(NADV)}$
FSMC_NADV(1)
ai14990

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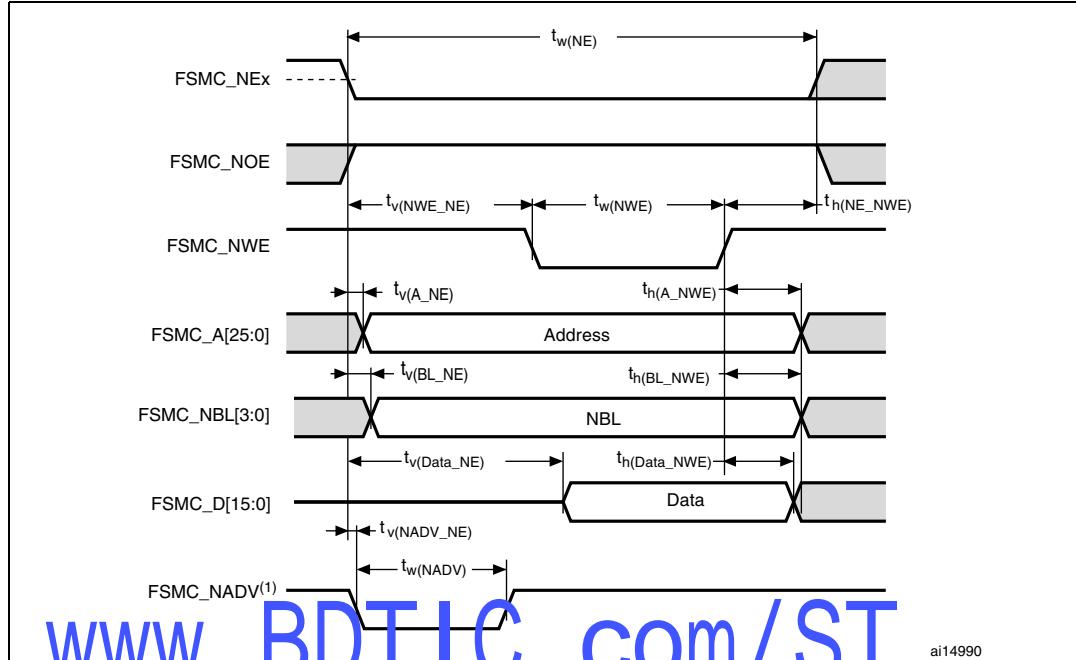
1. Modes 2/B, C and D only.

**Table 30. Asynchronous non-multiplexed SRAM/NOR write timings(1)**

| $V_{DD\_IO}$ = V and $C_L$ = 15 pF | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_{w(NE)}$ | FSMC_NE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{v(WEN\_NE)}$ | FSMC_NEx low to FSMC_NWE low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | TBD | | $t_{CK}$/ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | | TBD | ns |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | TBD | | $t_{CK}$/ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | | TBD | ns |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | TBD | | $t_{CK}$/ns |
| $t_{v(Data\_NE)}$ | FSMC_NEx low to Data valid | | TBD | $t_{CK}$/ns |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | TBD | | $t_{CK}$/ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | | TBD | $t_{CK}$/ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | | TBD | $t_{CK}$/ns |

1. TBD = to be determined.

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**Figure 21.   Asynchronous non-multiplexed SRAM/NOR read timings**
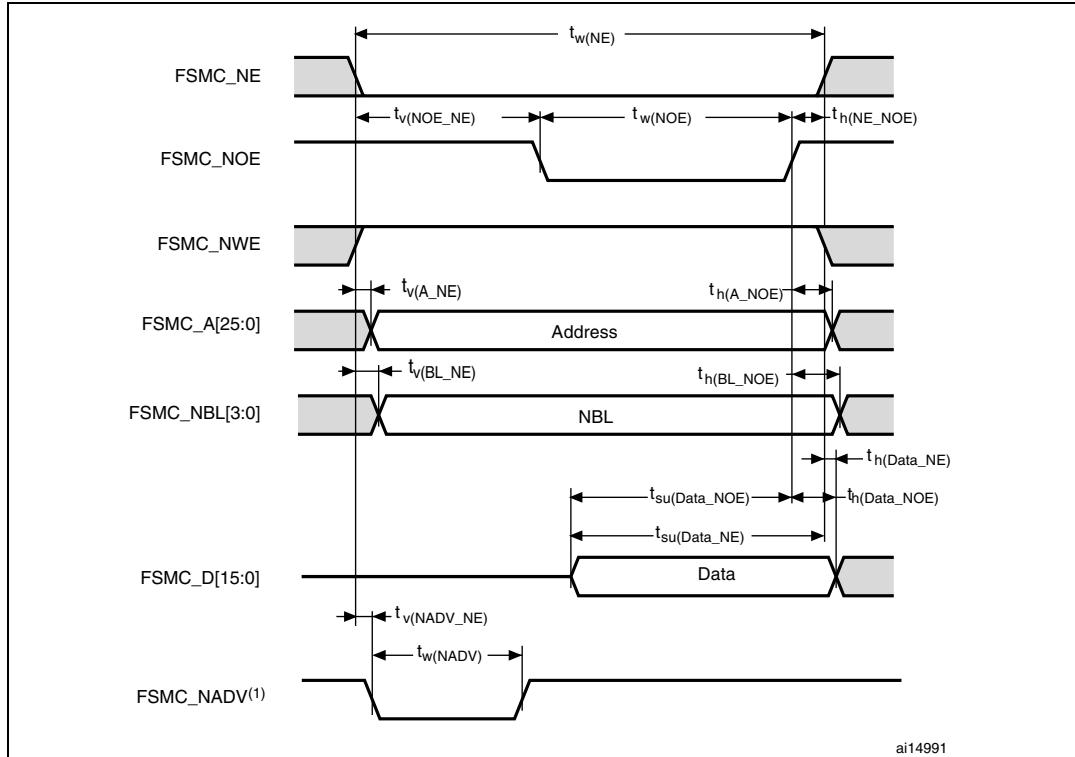


1.   Modes 2/B, C and D only.

**Table 31.   Asynchronous non-multiplexed SRAM/NOR read timings[1]**

$V_{DD\_IO}$ = V and $C_L$ = 15 pF

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | TBD | | $t_{CK}$/ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | | TBD | ns |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | TBD | | $t_{CK}$/ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | | TBD | ns |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | TBD | | $t_{CK}$/ns |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | TBD | | $t_{CK}$/ns |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOEx high setup time | TBD | | $t_{CK}$/ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | TBD | | $t_{CK}$/ns |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | TBD | | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | | TBD | $t_{CK}$/ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | | TBD | $t_{CK}$/ns |

1.   TBD = to be determined.

**Figure 22.    Asynchronous multiplexed SRAM/NOR write timings**



ai14891
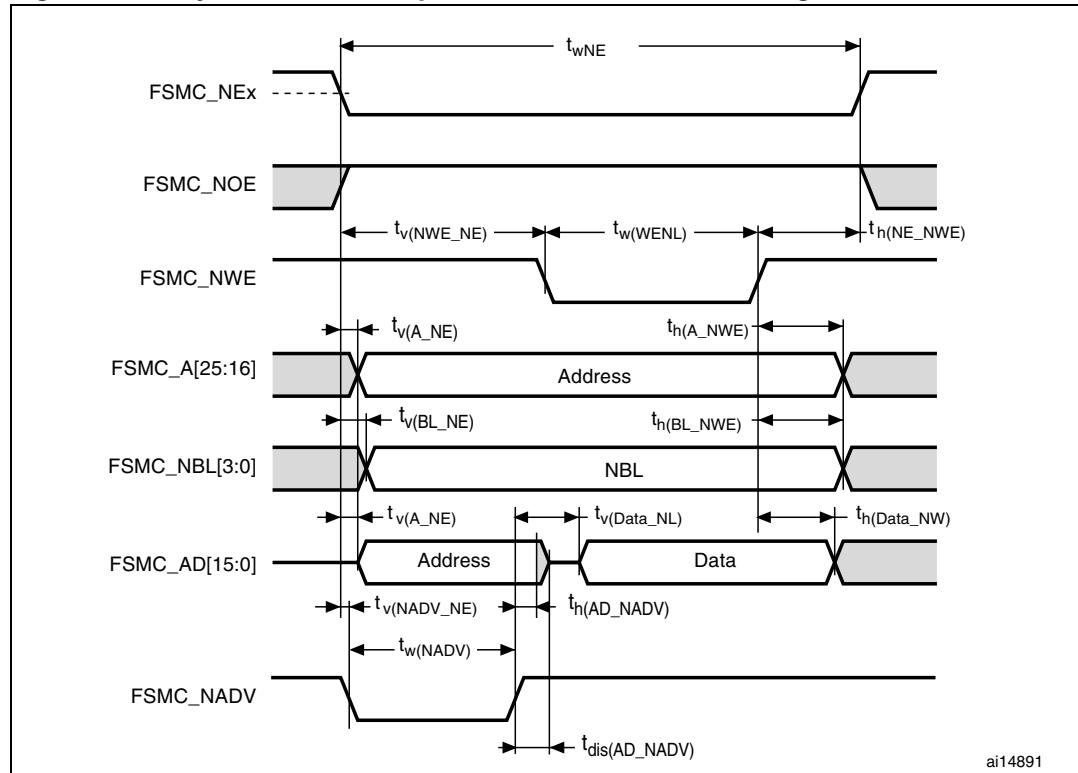
**Table 32.    Asynchronous multiplexed SRAM/NOR write timings[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | TBD |  | $t_{CK}$/ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid |  | TBD | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | TBD |  | $t_{CK}$/ns |
| $t_{dis(AD\_NADV)}$ | FSMC_AD (address) disable time after FSMC_NADV high |  | TBD | $t_{CK}$/ns |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | TBD |  | $t_{CK}$/ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid |  | TBD | ns |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | TBD |  | $t_{CK}$/ns |
| $t_{v(Data\_NADV)}$ | FSMC_NADV high to Data valid | TBD |  | $t_{CK}$/ns |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | TBD |  | $t_{CK}$/ns |

1.   TBD = to be determined.

**Figure 23.    Asynchronous multiplexed SRAM/NOR read timings**
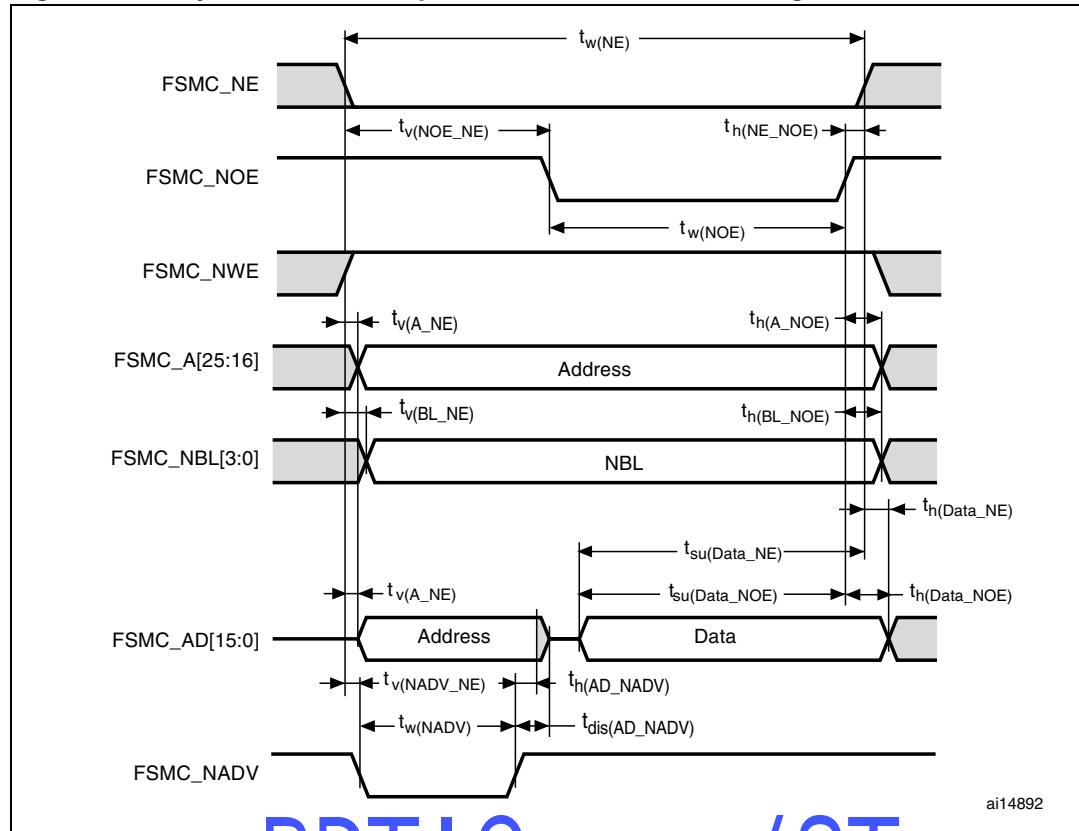
**Table 33. Asynchronous multiplexed SRAM/NOR read timings[1]**

| $V_{DD\_IO}$ = V and $C_L$ = 15 pF | | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_{w(NE)}$ | FSMC_NE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(NE\_WEN)}$ | FSMC_WEN high to FSMC_NE high hold time | TBD | | $t_{CK}$/ns |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | TBD | | $t_{CK}$/ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | | TBD | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | TBD | TBD | $t_{CK}$/ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | TBD | TBD | $t_{CK}$/ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | TBD | | $t_{CK}$/ns |
| $t_{dis(AD\_NADV)}$ | FSMC_AD (address) disable time after FSMC_NADV high | | TBD | $t_{CK}$/ns |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | TBD | | $t_{CK}$/ns |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | TBD | | $t_{CK}$/ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | | TBD | ns |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | TBD | | $t_{CK}$/ns |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOE high setup time | TBD | | $t_{CK}$/ns |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | TBD | | ns |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | TBD | | ns |

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1. TBD = to be determined.

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**Figure 24.    Synchronous multiplexed NOR/PSRAM read timings**
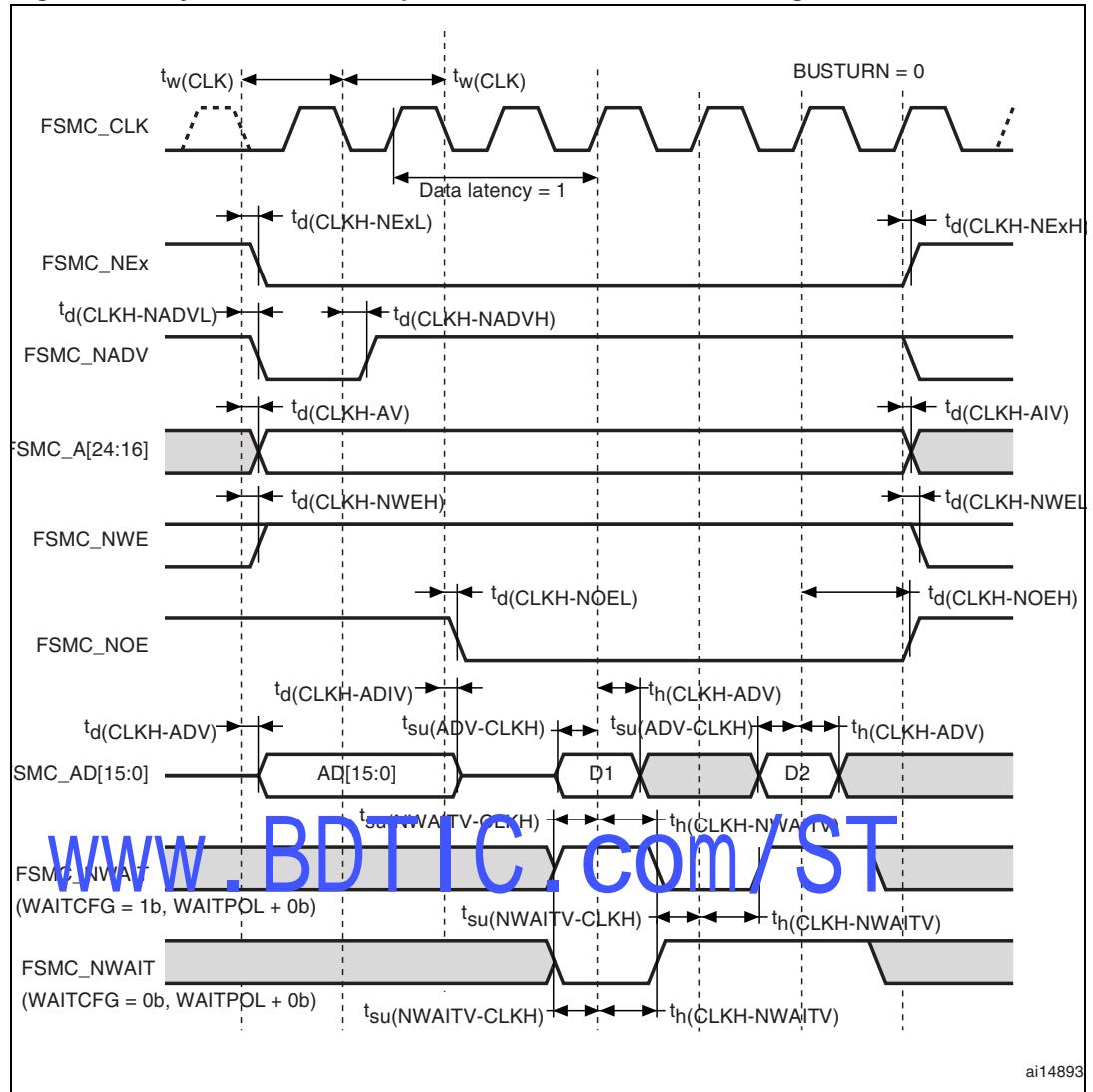
**Table 34.    Synchronous multiplexed NOR/PSRAM read timings[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | TBD | - | ns |
| $t_{d(CLKH-NExL)}$ | FSMC_CLK high to FSMC_NEx low (x = 0...2) | - | TBD | ns |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | TBD | - | ns |
| $t_{d(CLKH-NADVL)}$ | FSMC_CLK high to FSMC_NADV low | - | TBD | ns |
| $t_{d(CLKH-NADVH)}$ | FSMC_CLK high to FSMC_NADV high | TBD | - | ns |
| $t_{d(CLKH-AV)}$ | FSMC_CLK high to FSMC_Ax valid (x = 16...25) | - | TBD | ns |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16...25) | TBD | - | ns |
| $t_{d(CLKH-NWEL)}$ | FSMC_CLK high to FSMC_NWE low | - | TBD | ns |
| $t_{d(CLKH-NWEH)}$ | FSMC_CLK high to FSMC_NWE high | TBD | - | ns |
| $t_{d(CLKH-NOEL)}$ | FSMC_CLK high to FSMC_NOE low | - | TBD | ns |
| $t_{d(CLKH-NOEH)}$ | FSMC_CLK high to FSMC_NOE high | TBD | - | ns |
| $t_{d(CLKH-ADV)}$ | FSMC_CLK high to FSMC_AD[15:0] valid | - | TBD | ns |
| $t_{d(CLKH-ADIV)}$ | FSMC_CLK high to FSMC_AD[15:0] invalid | TBD | - | ns |
| $t_{su(ADV-CLKH)}$ | FSMC_A/D[15:0] valid data before FSMC_CLK high | TBD | - | ns |
| $t_{h(CLKH-ADV)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | TBD | - | ns |
| $t_{su(NWAITV-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | TBD | - | ns |
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | TBD | - | ns |

**$V_{DD\_IO}$ = V and $C_L$ = 15 pF**

1.   TBD = to be determined.

**Figure 25. Synchronous multiplexed PSRAM write timings**
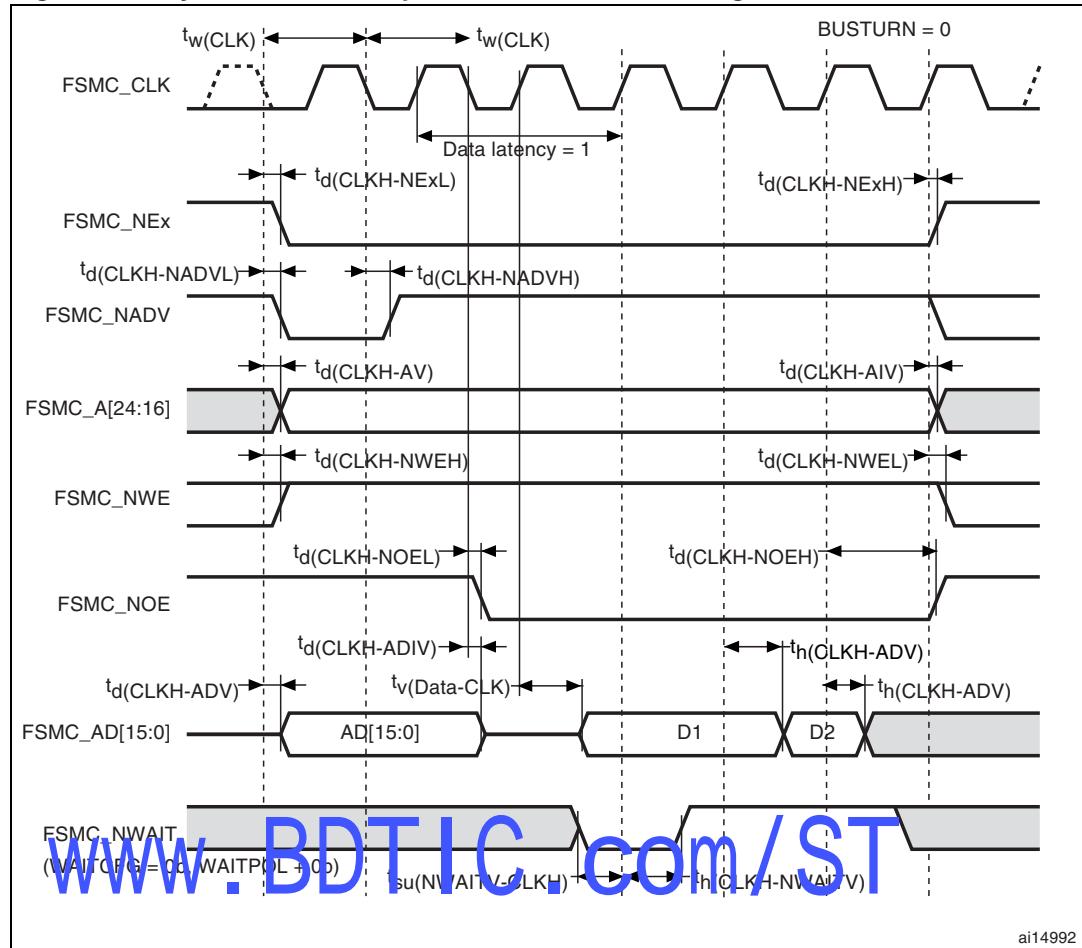
**Table 35.    Synchronous multiplexed PSRAM write timings[1]**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | TBD | - | ns |
| $t_{d(CLKH-NExL)}$ | FSMC_CLK high to FSMC_NEx low (x = 0...2) | - | TBD | ns |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | TBD | - | ns |
| $t_{d(CLKH-NADVL)}$ | FSMC_CLK high to FSMC_NADV low | - | TBD | ns |
| $t_{d(CLKH-NADVH)}$ | FSMC_CLK high to FSMC_NADV high | TBD | - | ns |
| $t_{d(CLKH-AV)}$ | FSMC_CLK high to FSMC_Ax valid (x = 16...25) | - | TBD | ns |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16...25) | TBD | - | ns |
| $t_{d(CLKH-NWEL)}$ | FSMC_CLK high to FSMC_NWE low | - | TBD | ns |
| $t_{d(CLKH-NWEH)}$ | FSMC_CLK high to FSMC_NWE high | TBD | - | ns |
| $t_{d(CLKH-NOEL)}$ | FSMC_CLK high to FSMC_NOE low | - | TBD | ns |
| $t_{d(CLKH-NOEH)}$ | FSMC_CLK high to FSMC_NOE high | TBD | - | ns |
| $t_{d(CLKH-ADV)}$ | FSMC_CLK high to FSMC_AD[15:0] valid | - | TBD | ns |
| $t_{d(CLKH-ADIV)}$ | FSMC_CLK high to FSMC_AD[15:0] invalid | TBD | - | ns |
| $t_{h(CLKH-ADV)}$ | FSMC_A/D[15:0] valid data after FSMC_CLK high | TBD | - | ns |
| $t_{su(NWAITV-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | TBD | - | ns |
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | TBD | - | ns |
| $t_{v(Data-CLK)}$ | FSMC_CLK high to FSMC_CLK valid | TBD | - | ns |

1.   TBD = to be determined.

**Figure 26.   Synchronous non-multiplexed NOR/PSRAM read timings**
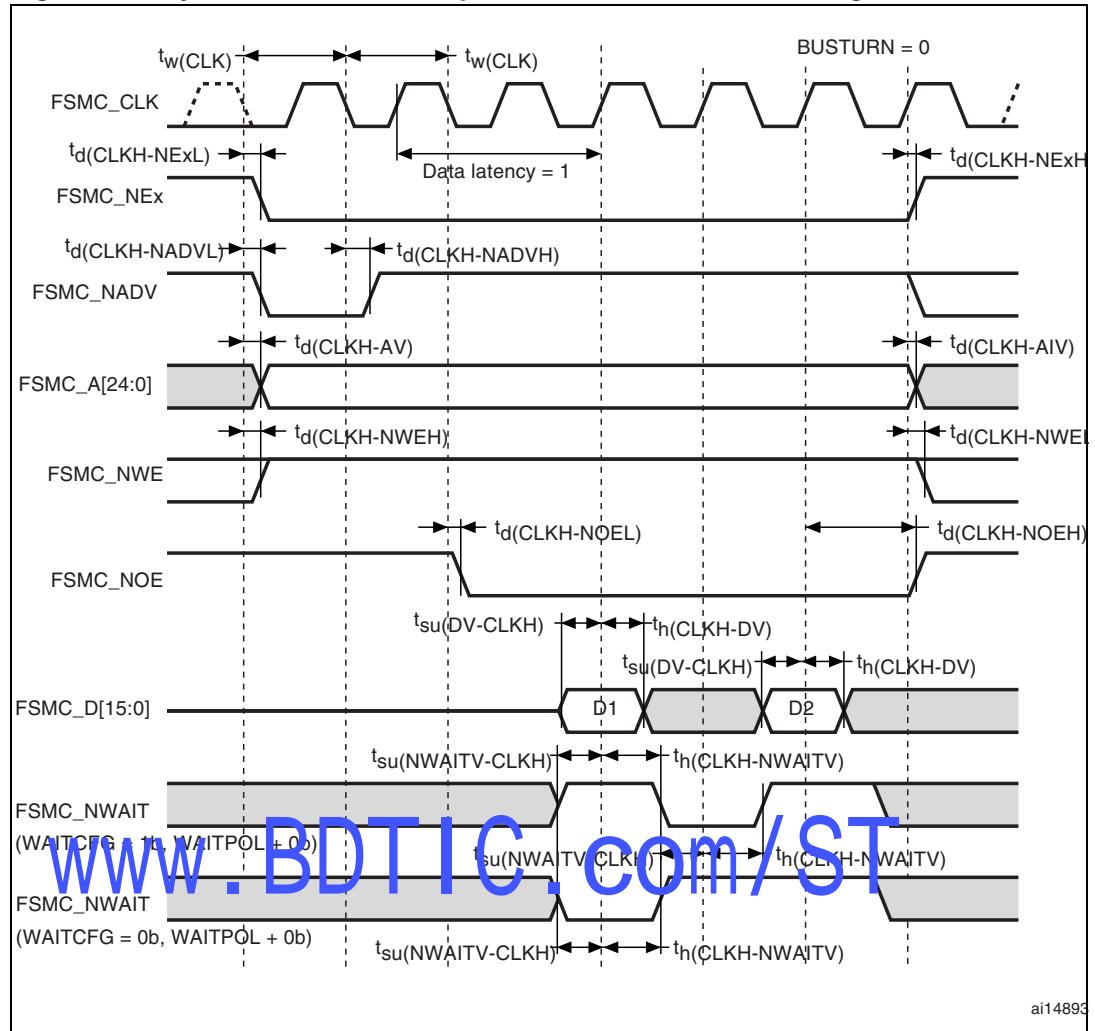
**Table 36.     Synchronous non-multiplexed NOR/PSRAM read timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | TBD | - | ns |
| $t_{d(CLKH\text{-}NExL)}$ | FSMC_CLK high to FSMC_NEx low (x = 0...2) | - | TBD | ns |
| $t_{d(CLKH\text{-}NExH)}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | TBD | - | ns |
| $t_{d(CLKH\text{-}NADVL)}$ | FSMC_CLK high to FSMC_NADV low | - | TBD | ns |
| $t_{d(CLKH\text{-}NADVH)}$ | FSMC_CLK high to FSMC_NADV high | TBD | - | ns |
| $t_{d(CLKH\text{-}AV)}$ | FSMC_CLK high to FSMC_Ax valid (x = 0...25) | - | TBD | ns |
| $t_{d(CLKH\text{-}AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 0...25) | TBD | - | ns |
| $t_{d(CLKH\text{-}NWEL)}$ | FSMC_CLK high to FSMC_NWE low | - | TBD | ns |
| $t_{d(CLKH\text{-}NWEH)}$ | FSMC_CLK high to FSMC_NWE high | TBD | - | ns |
| $t_{d(CLKH\text{-}NOEL)}$ | FSMC_CLK high to FSMC_NOE low | - | TBD | ns |
| $t_{d(CLKH\text{-}NOEH)}$ | FSMC_CLK high to FSMC_NOE high | TBD | - | ns |
| $t_{su(DV\text{-}CLKH)}$ | FSMC_D[15:0] valid data before FSMC_CLK high | TBD | - | ns |
| $t_{h(CLKH\text{-}DV)}$ | FSMC_D[15:0] valid data after FSMC_CLK high | TBD | - | ns |
| $t_{su(NWAITV\text{-}CLKH)}$ | FSMC_NWAIT valid before FSMC_SMCLK high | TBD | - | ns |
| $t_{h(CLKH\text{-}NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | TBD | - | ns |

The table heading row: $V_{DD\_IO}$ = V and $C_L$ = 15 pF

**Figure 27.   Synchronous non-multiplexed PSRAM write timings**
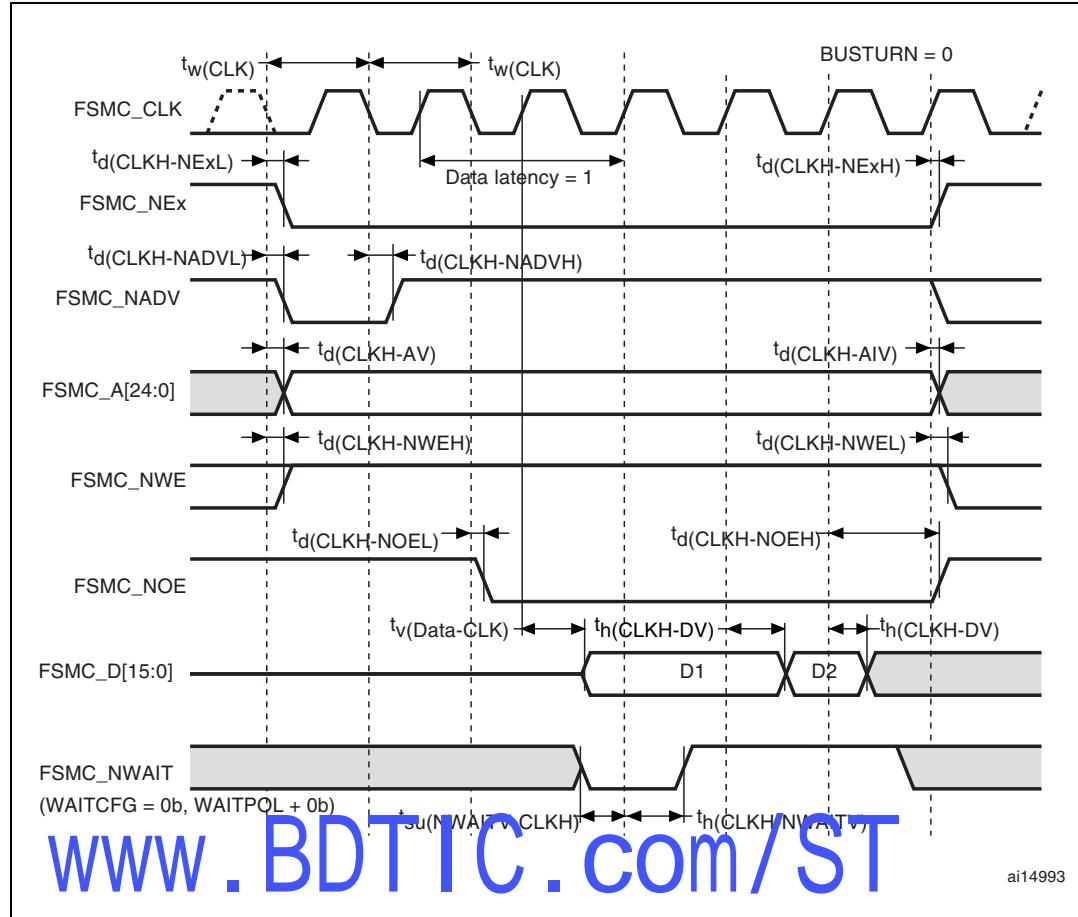
**Table 37.    Synchronous non-multiplexed PSRAM write timings**

| | $V_{DD\_IO}$ = V and $C_L$ = 15 pF | | | |
|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Unit** |
| $t_{w(CLK)}$ | FSMC_CLK period | TBD | - | ns |
| $t_{d(CLKH-NExL)}$ | FSMC_CLK high to FSMC_NEx low (x = 0...2) | - | TBD | ns |
| $t_{d(CLKH-NExH)}$ | FSMC_CLK high to FSMC_NEx high (x = 0...2) | TBD | - | ns |
| $t_{d(CLKH-NADVL)}$ | FSMC_CLK high to FSMC_NADV low | - | TBD | ns |
| $t_{d(CLKH-NADVH)}$ | FSMC_CLK high to FSMC_NADV high | TBD | - | ns |
| $t_{d(CLKH-AV)}$ | FSMC_CLK high to FSMC_Ax valid (x = 16...25) | - | TBD | ns |
| $t_{d(CLKH-AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16...25) | TBD | - | ns |
| $t_{d(CLKH-NWEL)}$ | FSMC_CLK high to FSMC_NWE low | - | TBD | ns |
| $t_{d(CLKH-NWEH)}$ | FSMC_CLK high to FSMC_NWE high | TBD | - | ns |
| $t_{d(CLKH-NOEL)}$ | FSMC_CLK high to FSMC_NOE low | - | TBD | ns |
| $t_{d(CLKH-NOEH)}$ | FSMC_CLK high to FSMC_NOE high | TBD | - | ns |
| $t_{su(DV-CLKH)}$ | FSMC_D[15:0] valid data before FSMC_CLK high | TBD | - | ns |
| $t_{h(CLKH-DV)}$ | FSMC_D[15:0] valid data after FSMC_CLK high | TBD | - | ns |
| $t_{v(Data-CLK)}$ | FSMC_CLK high to FSMC_CLK valid | TBD | - | ns |
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | TBD | - | ns |

**Figure 28. PC-card controller timing for common memory read access**
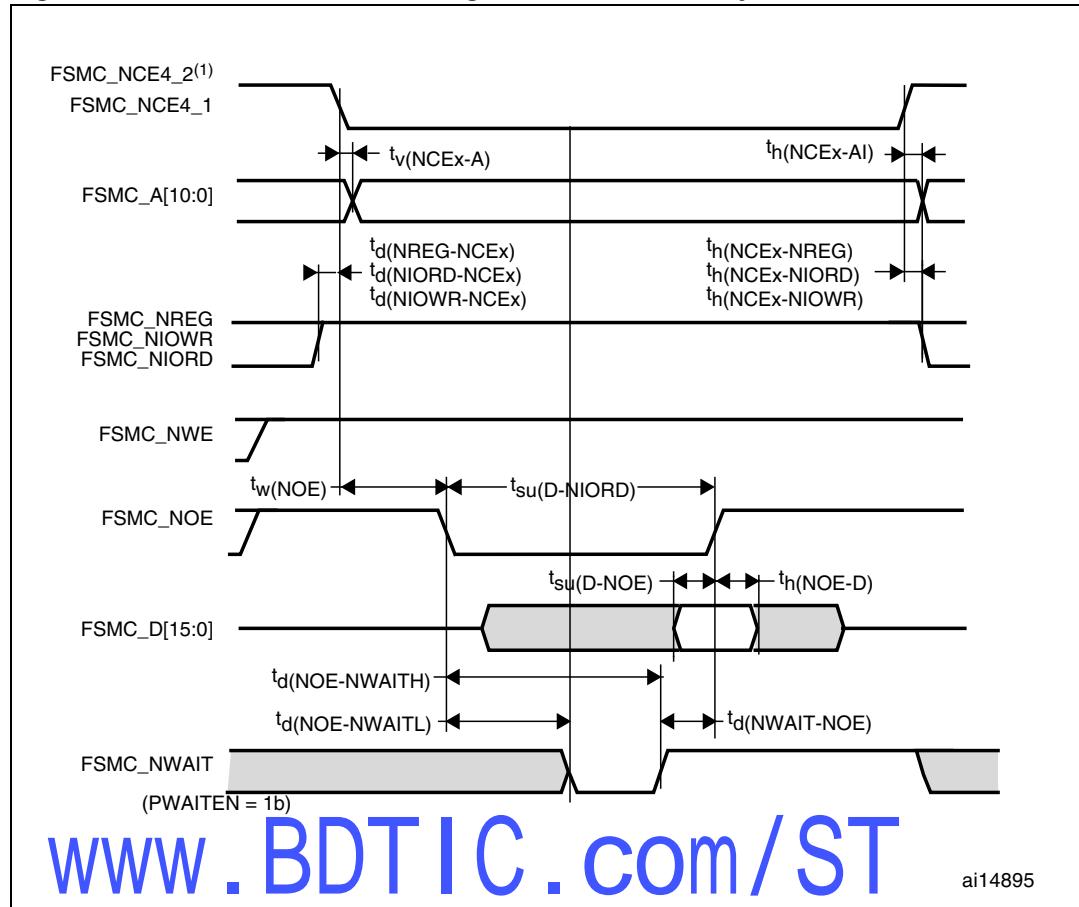


1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

**Figure 29.    PC-card controller timing for common memory write access**



1.    FSMC_NCE4_2 remains high (inactive during 8-bit access.
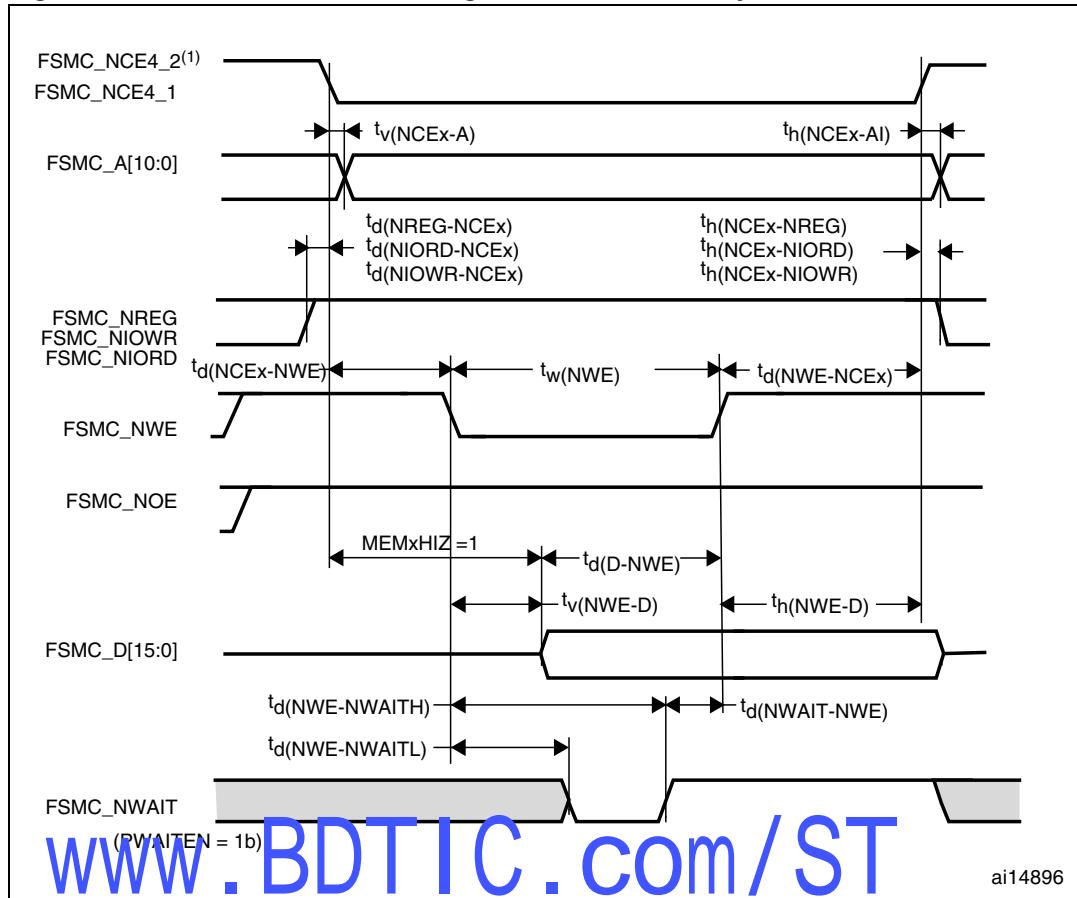
**Figure 30. PC-card controller timing for attribute memory read access**
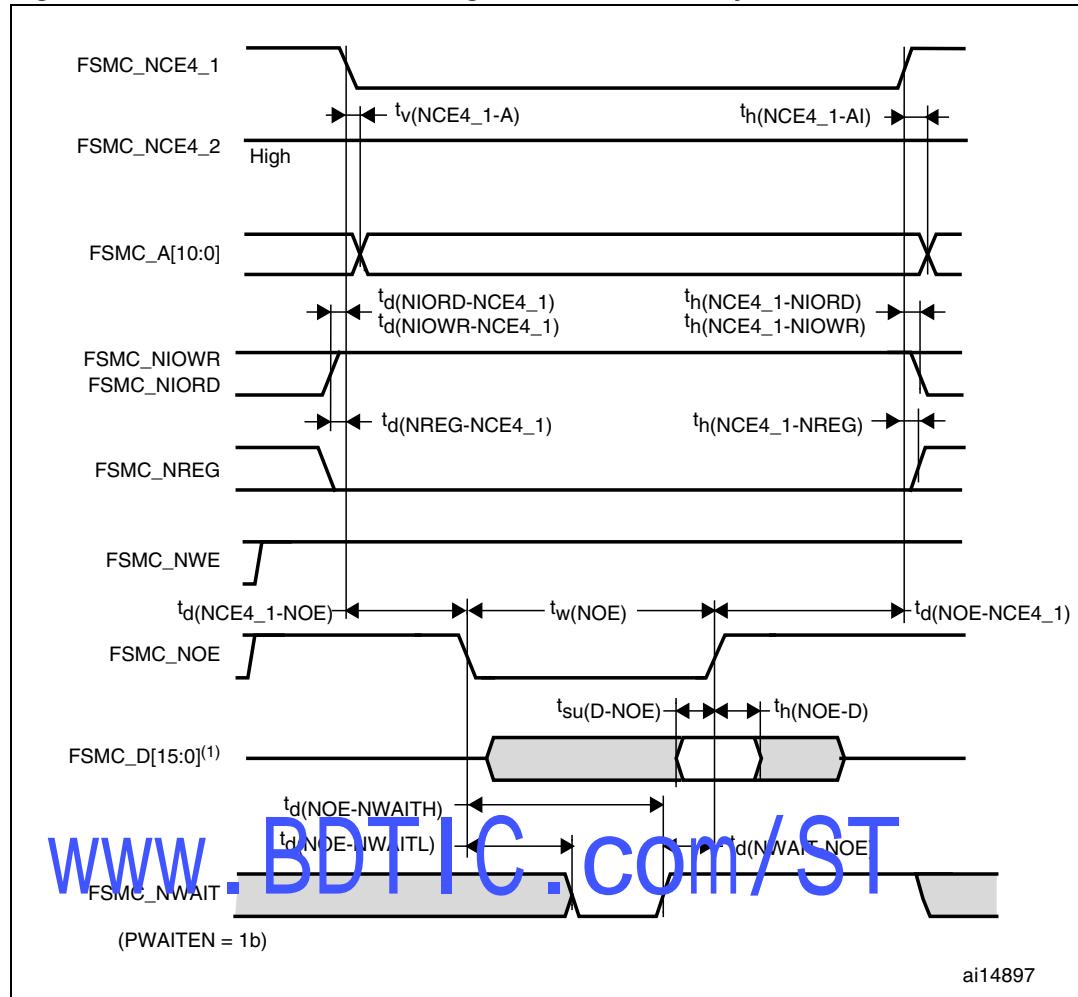


1. Only data bits 0...7 are read (bits 8...15 are disregarded).

**Figure 31.    PC-card controller timing for attribute memory write access**
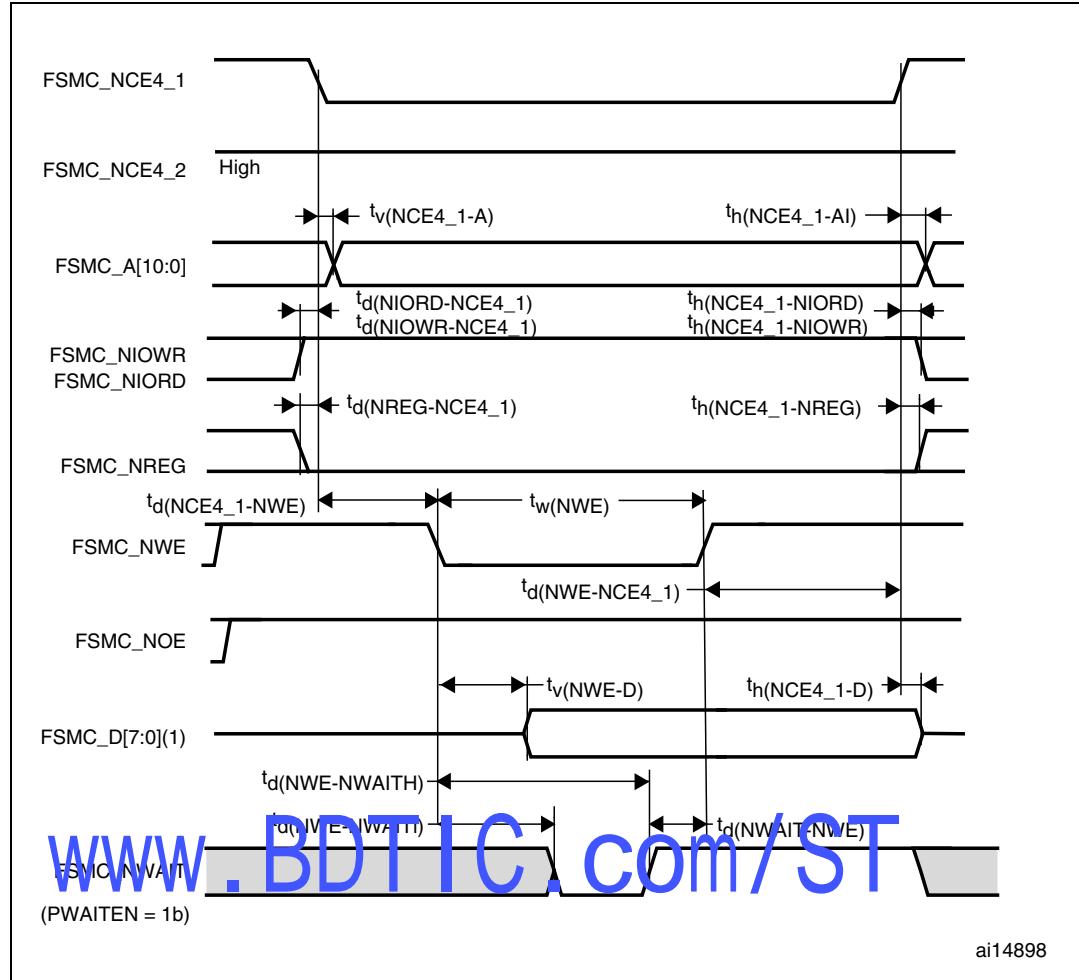


1.    Only data bits 0...7 are driven (bits 8...15 remains HiZ).

**Figure 32.    PC-card controller timing for I/O space read access**
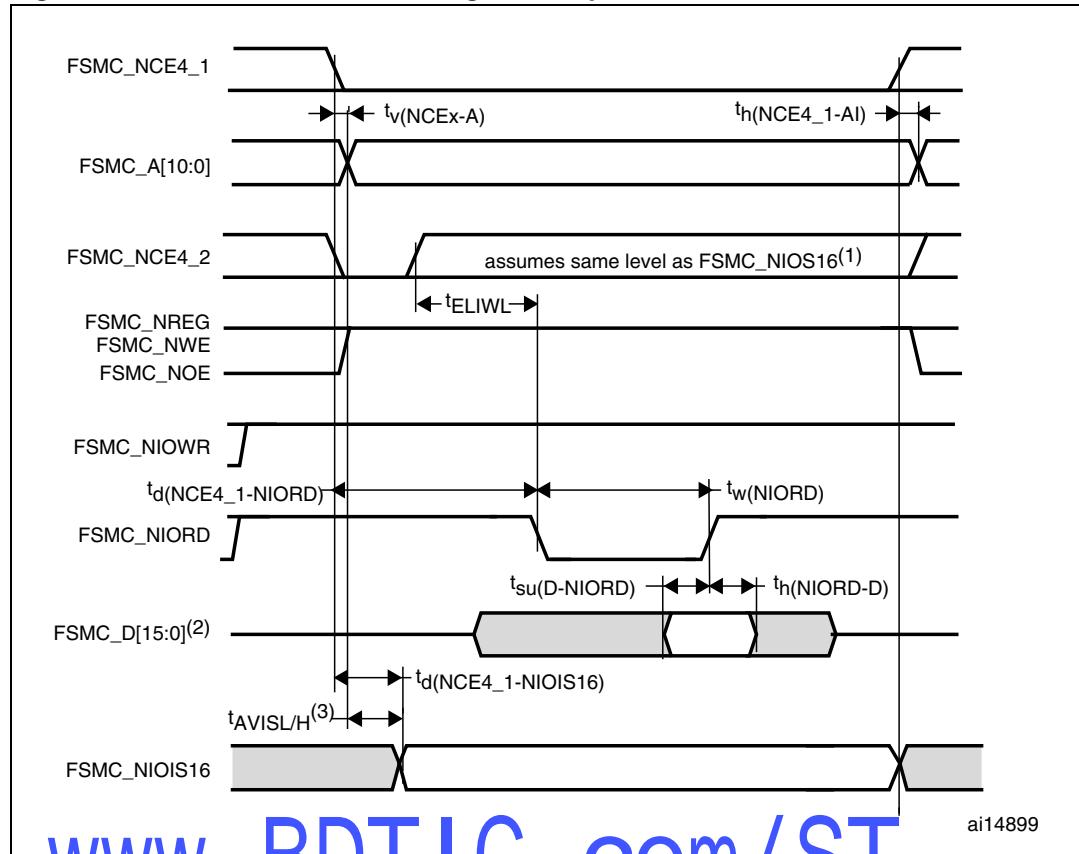


1.  FSMC_NCE4_2 is high independently of FSMC_NIOIS16 if the AHB transfer is for one byte.

2.  Only data bits 0...7 are read (bits 8...15 are disregarded) if FSMC_NIOIS16 is high.

3.  The CF card asserts FSMC_NIOIS16 after $t_{AVISL/H}$.

4.  FSMC_NWAIT not shown but behaves as in the previous figures.

**Figure 33.   PC-card controller timing for I/O space write access**
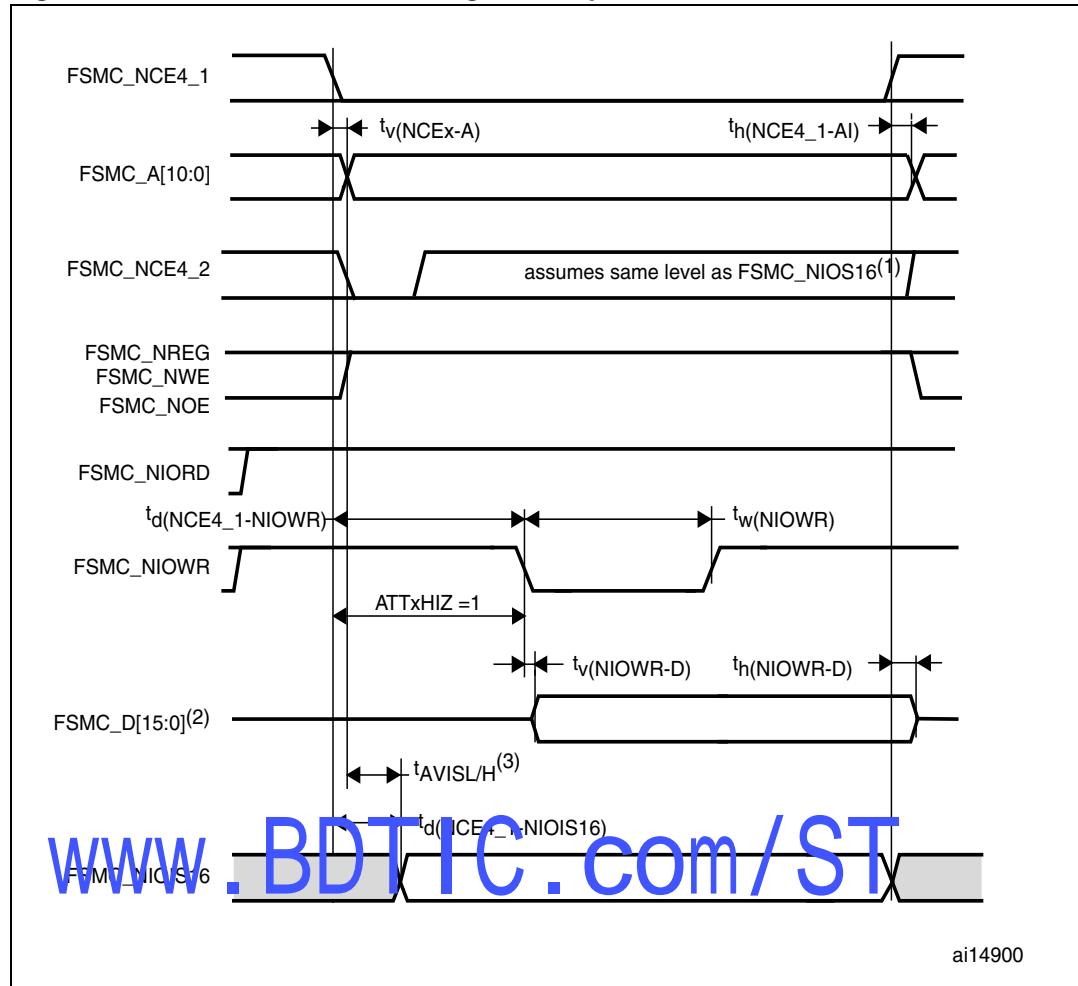


1.  FSMC_NCE4_2 is high independently of FSMC_NIOIS16 if the AHB transfer is for one byte.

2.  Only data bits 0...7 are driven (bits 8...15 remains HiZ) if FSMC_NIOIS16 is high.

3.  The CF card asserts FSMC_NIOIS16 after $t_{AVISL/H}$.

4.  FSMC_NWAIT not shown but behaves as in the previous figures.

**Table 38.     Switching characteristics for CF read and write cycles**[1]

| Symbol | Parameter | Timing | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{v(NCEx-A)}$ $t_{v(NCE4\_1-A)}$ | FSMC_NCEx low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) FSMC_NCE4_1 low (x = 4_1/4_2) to FSMC_Ay valid (y = 0...10) | - | TBD | ns |
| $t_{h(NCEx-AI)}$ $t_{h(NCE4\_1-AI)}$ | FSMC_NCEx high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) FSMC_NCE4_1 high (x = 4_1/4_2) to FSMC_Ax invalid (x = 0...10) | TBD | - | ns |
| $t_{d(NREG-NCEx)}$ $t_{d(NREG-NCE4\_1)}$ | FSMC_NCEx low to FSMC_NREG valid FSMC_NCE4_1 low to FSMC_NREG valid | - | TBD | ns |
| $t_{h(NCEx-NREG)}$ $t_{h(NCE4\_1-NREG)}$ | FSMC_NCEx high to FSMC_NREG invalid FSMC_NCE4_1 high to FSMC_NREG invalid | TBD | - | ns |
| $t_{d(NIORD-NCEx)}$ $t_{d(NIORD-NCE4\_1)}$ | FSMC_NCEx low to FSMC_NIORD valid FSMC_NCE4_1 low to FSMC_NIORD valid | - | TBD | ns |
| $t_{h(NCEx-NIORD)}$ $t_{h(NCE4\_1-NIORD)}$ | FSMC_NCEx high to FSMC_NIORD invalid FSMC_NCE4_1 high to FSMC_NIORD invalid | TBD | - | ns |
| $t_{d(NIOWR-NCEx)}$ $t_{d(NIOWR-NCE4\_1)}$ | FSMC_NIOWR valid to FSMC_NCEx low FSMC_NIOWR valid to FSMC_NCE4_1 low | | | |
| $t_{h(NCEx-NIOWR)}$ $t_{h(NCE4\_1-NIOWR)}$ | FSMC_NCEx high to FSMC_NIOWR invalid FSMC_NCE4_1 high to FSMC_NIOWR invalid | | | |
| $t_{su(D-NIORD)}$ | FSMC_D[15:0] valid before FSMC_NIORD high | TBD | - | ns |
| $t_{d(NIORD-D)}$ | FSMC_D[15:0] valid after FSMC_NIORD high | TBD | - | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | TBD | - | ns |
| $t_{d(NCE4\_1-NIOWR)}$ | FSMC_NCE4_1 low to FSMC_NIOWR valid | - | TBD | ns |
| $t_{w(NIOWR)}$ | FSMC_NIOWR low width | TBD | - | ns |
| $t_{v(NIOWR-D)}$ | FSMC_NIOWR low to FSMC_D[15:0] valid | - | TBD | ns |
| $t_{h(NIOWR-D)}$ | FSMC_NIOWR high to FSMC_D[15:0] invalid | TBD | - | ns |
| $t_{d(NCE4\_1-NIOIS16)}$ | FSMC_NIOS16 valid after FSMC_NCE4_1 low | - | TBD | ns |
| $t_{d(NCE4\_1-NOE)}$ | FSMC_NCE4_1 low to FSMC_NOE low | - | 4 | ns |
| $t_{w(NOE)}$ | FSMC_NOE low width | TBD | TBD | cycles/ns |
| $t_{d(NOE-NCEx)}$ $t_{d(NOE-NCE4\_1)}$ | FSMC_NOE high to FSMC_NCEx high FSMC_NOE high to FSMC_NCE4_1 high | TBD | | |
| $t_{d(NOE-NWAITL)}$ | FSMC_NWAIT low after FSMC_NOE low[2] | | TBD | |
| $t_{d(NOE-NWAITH)}$ | FSMC_NWAIT high after FSMC_NOE low[2] | TBD | | |
| $t_{d(NWAIT-NOE)}$ | FSMC_NOE high after FSMC_NWAIT high | TBD | - | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | TBD | - | ns |

**Table 38.    Switching characteristics for CF read and write cycles[1] (continued)**

| Symbol | Parameter | Timing | | Unit |
|--------|-----------|--------|--------|------|
| | | Min | Max | |
| $t_{h(NOE-D)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | TBD | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | TBD | ns |
| $t_{w(NWE)}$ | FSMC_NWE low width | TBD | TBD | cycles/ns |
| $t_{d(NWE-NCEx)}$ $t_{d(NWE-NCE4\_1)}$ | FSMC_NWE high to FSMC_NCEx high FSMC_NWE high to FSMC_NCE4_1 high | TBD | | ns |
| $t_{d(NCE4\_1-NWE)}$ | FSMC_NCE4_1 low to FSMC_NWE low | | | ns |
| $t_{d(NWE-NWAITL)}$ | FSMC_NWAIT low after FSMC_NWE low[2] | | TBD | ns |
| $t_{d(NWE-NWAITH)}$ | FSMC_NWAIT high after FSMC_NWE low[2] | TBD | | ns |
| $t_{d(NWAIT-NWE)}$ | FSMC_NWE high after FSMC_NWAIT high | TBD | - | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | - | TBD | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | TBD | - | ns |
| $t_{h(NCE4\_1-D)}$ | FSMC_NCE4_1 high to FSMC_D[15:0] invalid | | | ns |
| $t_{w(NIORD)}$ | FSMC_NIORD low width | | | ns |
| $t_{ELIWL}$ | FSMC_NCEx setup before FSMC_NWE low | | | ns |
| $t_{AVISL/H}$ | Address valid to FSMC_NIOIS16 valid | | TBD | ns |

1.  TBD = to be determined.

2.  When one or more wait states are inserted. If no wait state needs inserted, NWAIT should be kept high or the wait feature should be disabled (WAITEN=0) in the control register.

**Figure 34.   NAND controller timing for read access**
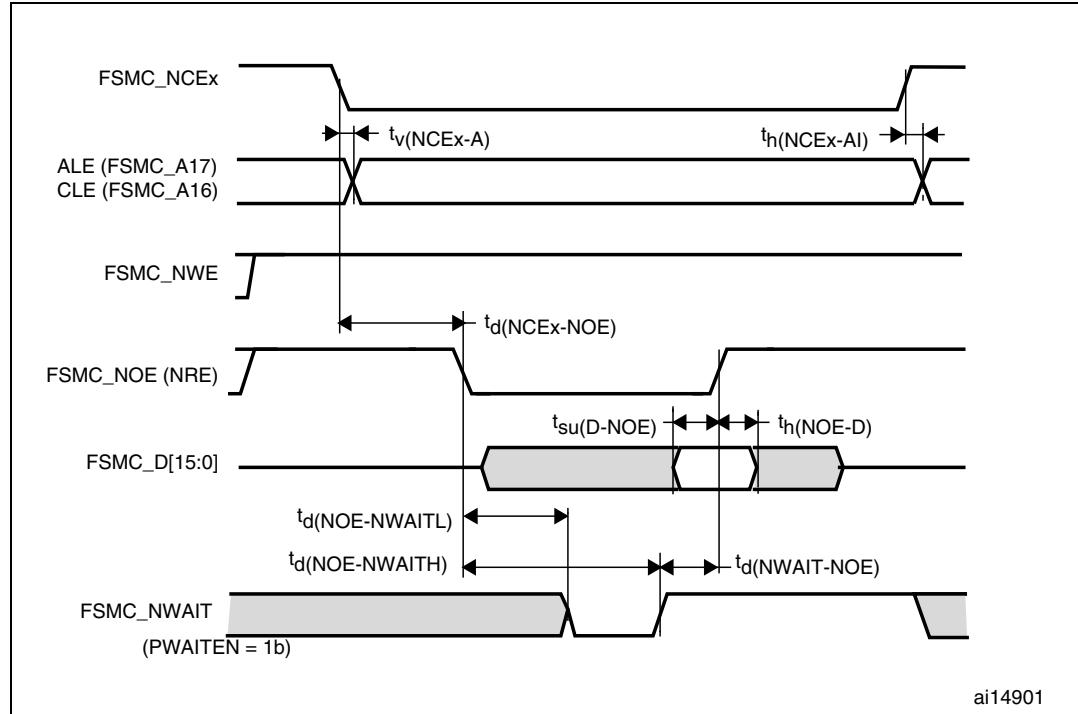


**Figure 35.   NAND controller timing for write access**
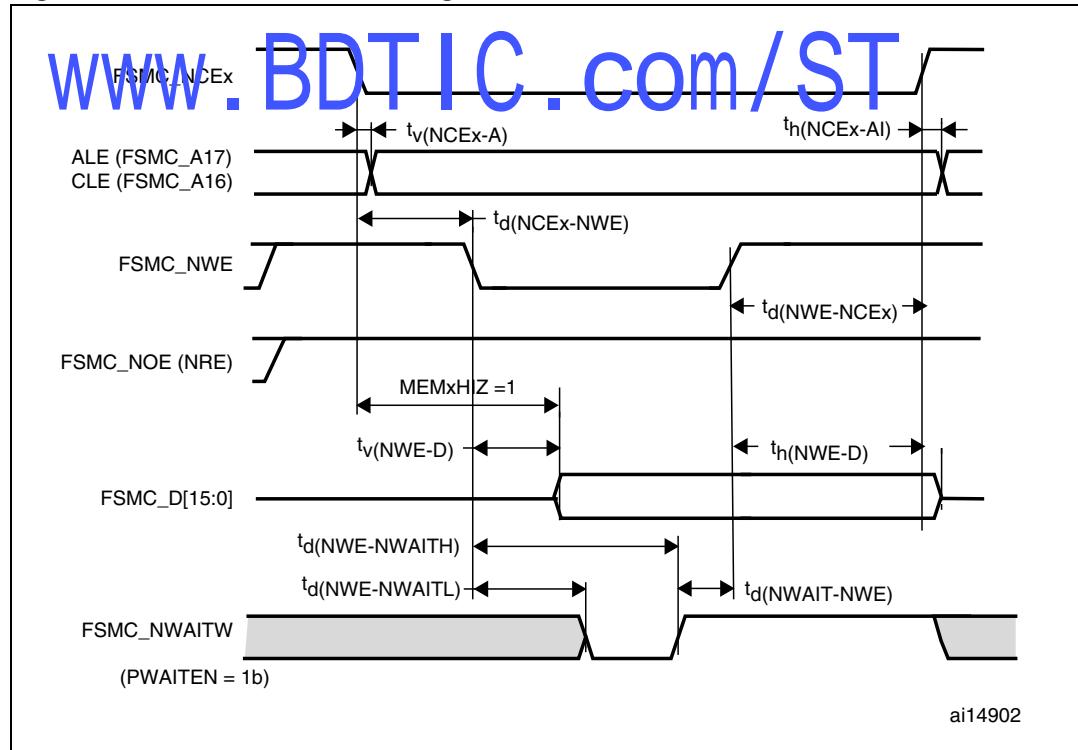
**Figure 36.    NAND controller timing for common memory read access**
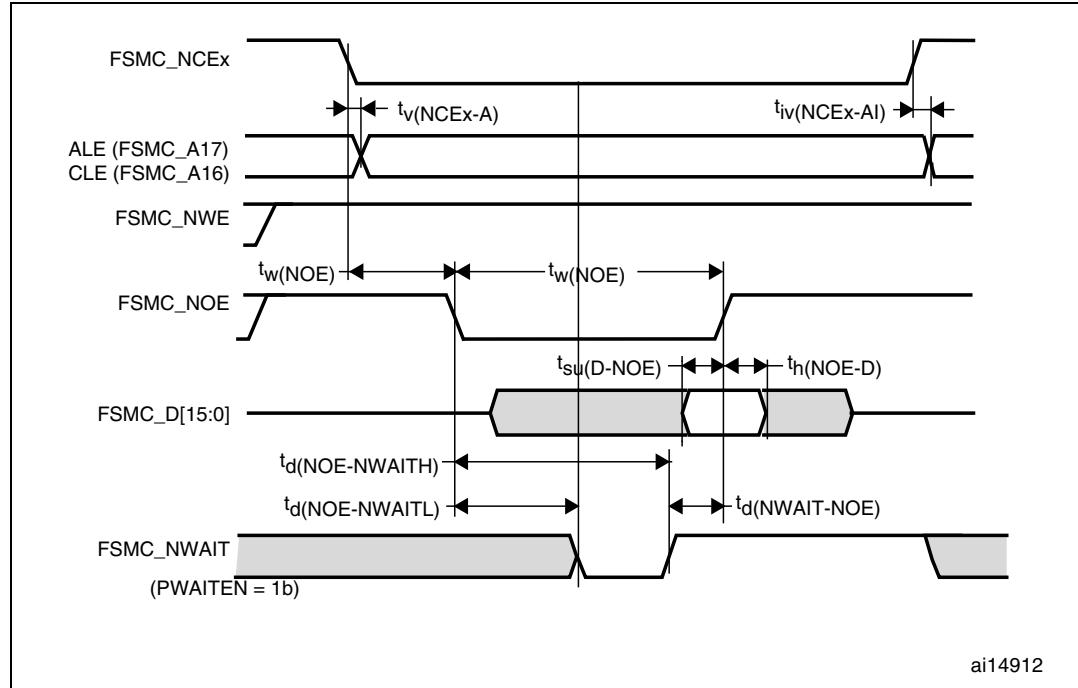


**Figure 37.    NAND controller timing for common memory write access**
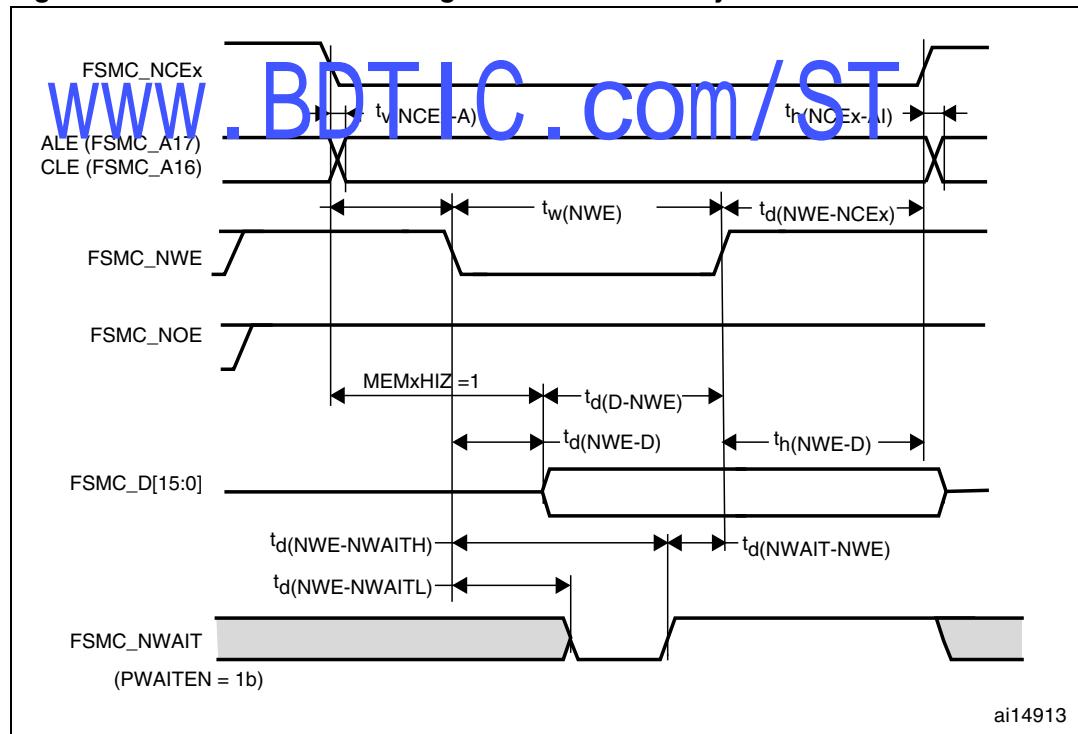
**Table 39. Switching characteristics for NAND Flash read and write cycles[1]**

| Symbol | Parameter | Timing | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{v(NCEx-A)}$ | FSMC_NCEx low (x = 2/3) to FSMC_Ay valid (y = 16/17) | - | TBD | ns |
| $t_{h(NCEx-AI)}$ | FSMC_NCEx high (x = 2/3) to FSMC_Ax invalid (x = 16/17) | TBD | - | ns |
| $t_{d(D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | TBD | - | ns |
| $t_{d(NWE-D)}$ | FSMC_D[15:0] valid after FSMC_NWE high | TBD | - | ns |
| $t_{d(NCEx-NOE)}$ | FSMC_NCEx low to FSMC_NOE low | - | TBD | ns |
| $t_{w(NOE)}$ | FSMC_NOE low width | TBD | TBD | cycles/ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | | | ns |
| $t_{d(NOE-NWAITL)}$ | FSMC_NWAIT low after FSMC_NOE low[2] | | TBD | |
| $t_{d(NOE-NWAITH)}$ | FSMC_NWAIT high after FSMC_NOE low[2] | TBD | | |
| $t_{d(NWAIT-NOE)}$ | FSMC_NOE high after FSMC_NWAIT high | TBD | - | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | TBD | - | ns |
| $t_{h(NOE-D)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | TBD | - | ns |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | TBD | ns |
| $t_{w(NWE)}$ | FSMC_NWE low width | TBD | TBD | cycles/ns |
| $t_{d(NWE-NCEx)}$ | FSMC_NWE high to FSMC_NCEx high | TBD | | ns |
| $t_{d(NWE-NWAITL)}$ | FSMC_NWAIT low after FSMC_NWE low[2] | | TBD | ns |
| $t_{d(NWE-NWAITH)}$ | FSMC_NWAIT high after FSMC_NWE low[2] | TBD | | ns |
| $t_{d(NWAIT-NWE)}$ | FSMC_NWE high after FSMC_NWAIT high | TBD | - | ns |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | - | TBD | ns |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | TBD | - | ns |

1. TBD = to be determined.

2. When one or more wait states are inserted. If no wait state needs inserted, NWAIT should be kept high or the wait feature should be disabled (WAITEN=0) in the control register.

### 5.3.11  EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

#### Functional EMS (Electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

● **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.

● **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 40. They are based on the EMS levels and classes defined in application note AN1709.

**Table 40.    EMS characteristics**

| Symbol | Parameter | Conditions | Level/Class |
|--------|-----------|------------|-------------|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$=48 MHz conforms to IEC 1000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 48 MHz conforms to IEC 1000-4-4 | 4A |

#### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and pre qualification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

● Corrupted program counter
● Unexpected reset
● Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second. To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

**Table 41. EMI characteristics[1]**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{HCLK}$] 8/36 MHz | Unit |
|--------|-----------|------------|--------------------------|------|------|
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25 °C, LQFP100 package compliant with SAE J 1752/3 | 0.1 MHz to 30 MHz | TBD | dBµV |
| | | | 30 MHz to 130 MHz | TBD | |
| | | | 130 MHz to 1GHz | TBD | |
| | | | SAE EMI Level | TBD | - |

1. TBD = to be determined.

## 5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1 supply pins). This test conforms to the JESD22-A114/C101 standard.

**Table 42. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Class | Maximum value[1] | Unit |
|--------|---------|------------|-------|------------------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to JESD22-C101 | II | 500 | |

1. Values based on characterization results, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

● A supply overvoltage is applied to each power supply pin
● A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78 IC latch-up standard.

**Table 43.    Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|--------|-----------|------------|-------|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

### 5.3.13    I/O port characteristics

#### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 44* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 44.    I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
| $V_{IL}$ | Input low level voltage[1] | | −0.5 | | 0.8 | V |
| $V_{IH}$ | Standard IO input high level voltage[1] | TTL ports | 2 | | $V_{DD}$+0.5 | |
| | IO FT[2] input high level voltage[1] | | 2 | | 5.5V | |
| $V_{IL}$ | Input low level voltage[1] | CMOS ports | −0.5 | | 0.35 $V_{DD}$ | V |
| $V_{IH}$ | Input high level voltage[1] | | 0.65 $V_{DD}$ | | $V_{DD}$+0.5 | |
| $V_{hys}$ | Standard IO Schmitt trigger voltage hysteresis[3] | | 200 | | | mV |
| | IO FT Schmitt trigger voltage hysteresis[3] | | 5% $V_{DD}$[4] | | | mV |
| $I_{lkg}$ | Input leakage current [4] | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | | | ±1 | µA |
| | | $V_{IN}$ = 5 V I/O FT | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor[5] | $V_{IN}$ = $V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor[6] | $V_{IN}$ = $V_{DD}$ | 30 | 40 | 50 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

1. Values based on characterization results, and not tested in production.

2. FT = Five-volt tolerant.

3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.

4. With a minimum of 100 mV.

5. Leakage could be higher than max. if negative current is injected on adjacent pins.

6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

### Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed $V_{OL}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

● The sum of the currents sourced by all the I/Os on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD}$ (see *Table 7*).

● The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $I_{VSS}$ (see *Table 7*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 45* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

**Table 45.    Output voltage characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$[1] | Output Low level voltage for an I/O pin when 8 pins are sunk at the same time | TTL port, $I_{IO}$ = +8 mA, 2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$[2] | Output High level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | | |
| $V_{OL}$[1] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | CMOS port, $I_{IO}$ = +8 mA 2.7 V < $V_{DD}$ < 3.6 V | | 0.4 | V |
| $V_{OH}$[2] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | 2.4 | | |
| $V_{OL}$[1] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +20 mA[3] 2.7 V < $V_{DD}$ < 3.6 V | | 1.3 | V |
| $V_{OH}$[2] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–1.3 | | |
| $V_{OL}$[1] | Output low level voltage for an I/O pin when 8 pins are sunk at the same time | $I_{IO}$ = +6 mA[3] 2 V < $V_{DD}$ < 2.7 V | | 0.4 | V |
| $V_{OH}$[2] | Output high level voltage for an I/O pin when 8 pins are sourced at the same time | | $V_{DD}$–0.4 | | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

3. Based on characterization data, not tested in production.

### Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 38* and *Table 46*, respectively.

Unless otherwise specified, the parameters given in *Table 46* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 46.    I/O AC characteristics[1]**

| MODEx [1:0] bit value[1] | Symbol | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|---|
| 10 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 125[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | 125[3] | |
| 01 | $f_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 3.6 V | 25[3] | ns |
| | $t_{r(IO)out}$ | Output low to high level rise time | | 25[3] | |
| 11 | $F_{max(IO)out}$ | Maximum frequency[2] | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 50 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 30 | MHz |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 20 | MHz |
| | $t_{f(IO)out}$ | Output high to low level fall time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 5[3] | ns |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 12[3] | |
| | $t_{r(IO)out}$ | Output low to high level rise time | $C_L$ = 30 pF, $V_{DD}$ = 2.7 V to 3.6 V | 5[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2.7 V to 3.6 V | 8[3] | |
| | | | $C_L$ = 50 pF, $V_{DD}$ = 2 V to 2.7 V | 12[3] | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10x reference manual for a description of GPIO Port configuration register.

2. The maximum frequency is defined in *Figure 38*.

3. Values based on design simulation and validated on silicon, not tested in production.

**Figure 38.   I/O AC characteristics definition**
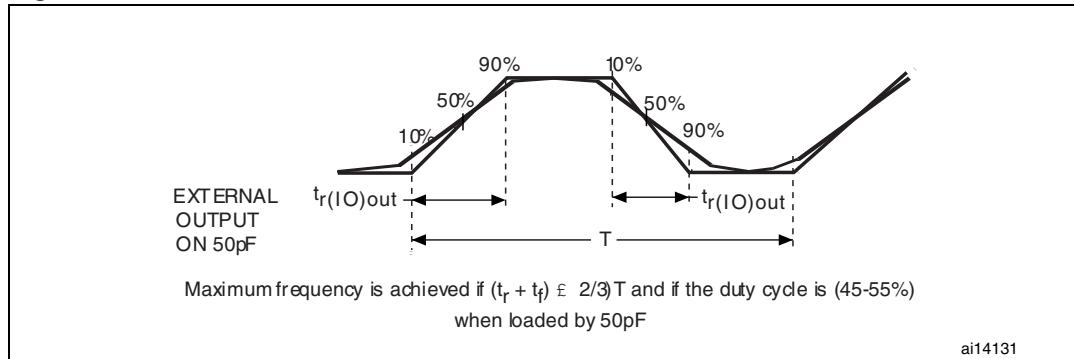


**5.3.14   NRST pin characteristics**

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 44*).

Unless otherwise specified, the parameters given in *Table 47* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

**Table 47.     NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST Input low level voltage | | −0.5 | | 0.8 | V |
| $V_{IH(NRST)}$ | NRST Input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 200 | | |
| $R_{PU}$ | Weak pull-up equivalent resistor[1] | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$ | NRST Input filtered pulse[2] | | | | 100 | ns |
| $V_{NF(NRST)}$ | NRST Input not filtered pulse[2] | | 300 | | | ns |

1.  The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2.  Values guaranteed by design, not tested in production.

**Figure 39.   Recommended NRST pin protection**
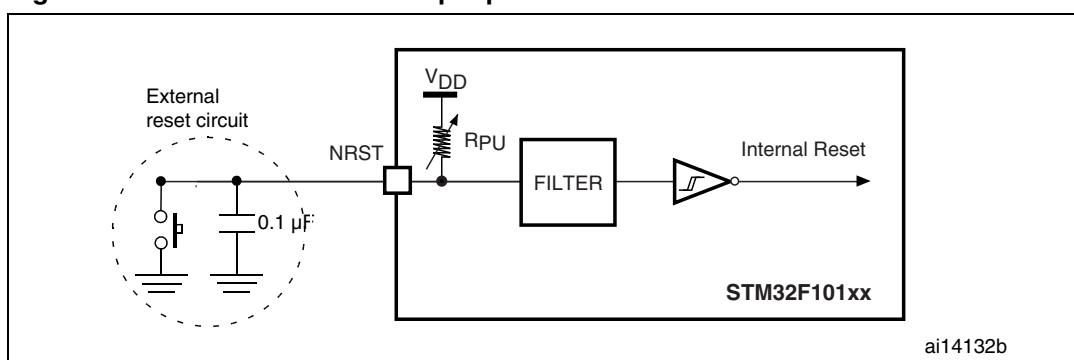


1.  The reset network protects the device against parasitic resets.

2.  The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 47*. Otherwise the reset will not be taken into account by the device.

### 5.3.15     TIM timer characteristics

The parameters given in *Table 48* are guaranteed by fabrication.

Refer to *Section 5.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 48.     TIMx[1] characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|-----------|-----|-----|------|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | 27.8 | | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK}$ = 36 MHz | 0 | 18 | MHz |
| $Res_{TIM}$ | Timer resolution | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | 0.0278 | 1820 | µs |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65536 × 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 36 MHz | | 119.2 | s |

1.   TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

### 5.3.16     Communications interfaces

**I$^2$C interface characteristics**

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.

The STM32F101xC, STM32F101xD and STM32F101xE access line I$^2$C interface meets the requirements of the standard I$^2$C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I$^2$C characteristics are described in *Table 49*. Refer also to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 49.** I²C characteristics

| Symbol | Parameter | Standard mode I²C[1] | | Fast mode I²C[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | **Min** | **Max** | **Min** | **Max** | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0[3] | | 0[4] | 900[3] | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20+0.1C_b$ | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | $20+0.1C_b$ | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | µs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Values based on standard I²C protocol requirement, not tested in production.

2. $f_{PCLK1}$ must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.

3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

**Figure 40.   I$^2$C bus AC waveforms and measurement circuit[1]**
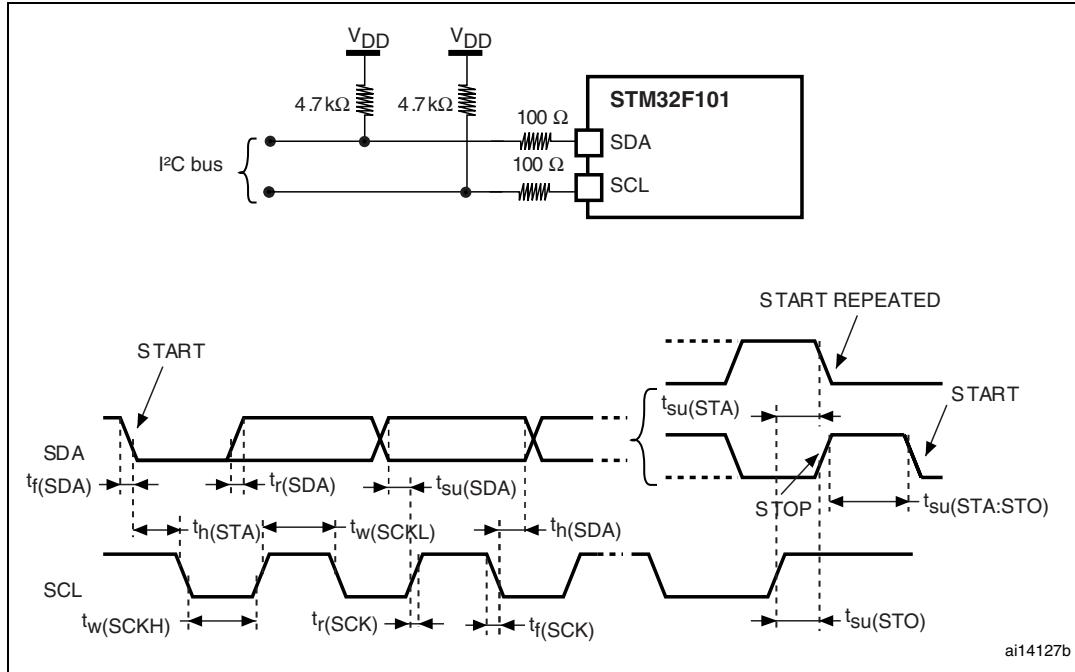


1.   Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Table 50.     SCL frequency (f$_{PCLK1}$= 36 MHz, V$_{DD}$ = 3.3 V)[1][2][3]**

| f$_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | R$_P$ = 4.7 kΩ |
| 400 | TBD |
| 300 | TBD |
| 200 | TBD |
| 100 | TBD |
| 50 | TBD |
| 20 | TBD |

1.   TBD = to be determined.

2.   R$_P$ = External pull-up resistance, f$_{SCL}$ = I$^2$C speed,

3.   For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 9*.
Refer to *Section 5.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 51.　SPI characteristics[1] [2]**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | 0 | 18 | MHz |
| | | Slave mode | 0 | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| $t_{su(NSS)}$[3] | NSS setup time | Slave mode | $t_{C(SCK)}$ | | |
| $t_{h(NSS)}$[3] | NSS hold time | Slave mode | $0.5t_{C(SCK)}$ | | |
| $t_{w(SCKH)}$[3] $t_{w(SCKL)}$[3] | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$[3] $t_{su(SI)}$[3] | Data input setup time | Master mode | 10 | | |
| | | Slave mode | 5 | | |
| $t_{h(MI)}$[3] $t_{h(SI)}$[3] | Data input hold time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 15 | | |
| | | Slave mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 5 | | |
| | | Master mode, $f_{PCLK}$ = TBD | TBD[4] | | |
| | | Slave mode, $f_{PCLK}$ = TBD | TBD[4] | | |
| $t_{a(SO)}$[3][5] | Data output access time | Slave mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 0 | 60 | |
| | | Slave mode, $f_{PCLK}$ = TBD | 0 | TBD | |
| $t_{dis(SO)}$[3][6] | Data output disable time | Slave mode | 5 | TBD | |
| $t_{v(SO)}$[3][1] | Data output valid time | Slave mode (after enable edge), $f_{PCLK}$ = 36 MHz, presc = 4 | | 30 | |
| | | $f_{PCLK}$ = TBD | | TBD | |
| $t_{v(MO)}$[3][1] | Data output valid time | Master mode (after enable edge), $f_{PCLK}$ = 36 MHz, presc = 4 | | 10 | |
| | | $f_{PCLK}$ = TBD | TBD | TBD | |
| $t_{h(SO)}$[3] | Data output hold time | Slave mode (after enable edge) | 30 | | |
| $t_{h(MO)}$[3] | | Master mode (after enable edge) | 10 | | |

1.　TBD = to be determined.

2.　Remapped SPI1 characteristics to be determined.

3.　Values based on design simulation and/or characterization results, and not tested in production.

4.　Depends on $f_{PCLK}$. For example, if $f_{PCLK}$= 8MHz, then $t_{PCLK}$ = $1/f_{PLCLK}$ =125 ns and $t_{v(MO)}$ = 255 ns.

5.　Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.

6.　Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 41.   SPI timing diagram - slave mode and CPHA=0**
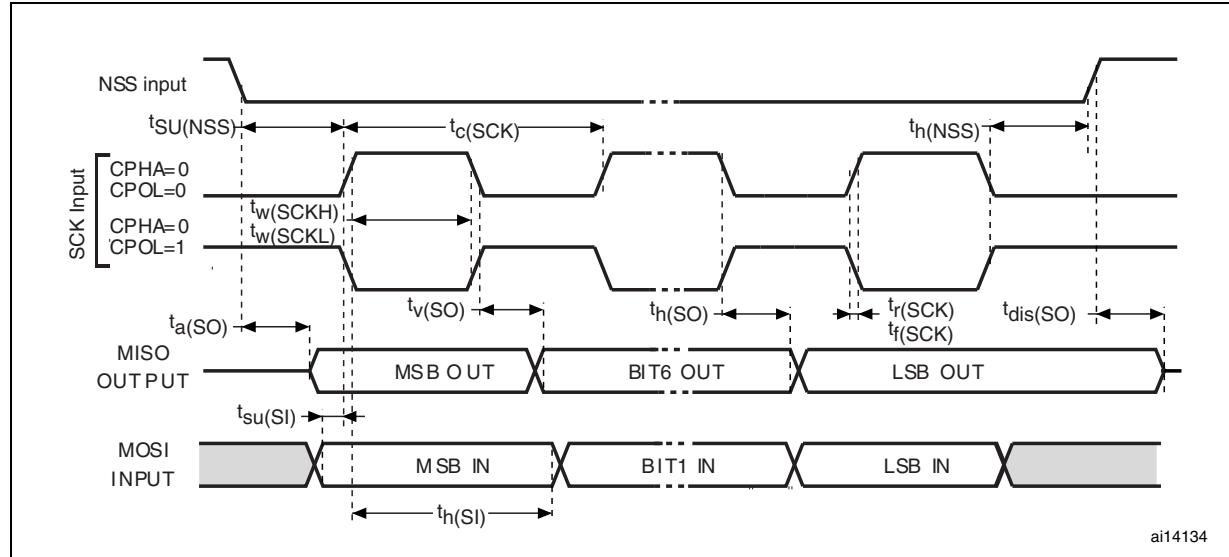


**Figure 42.   SPI timing diagram - slave mode and CPHA=1[1]**
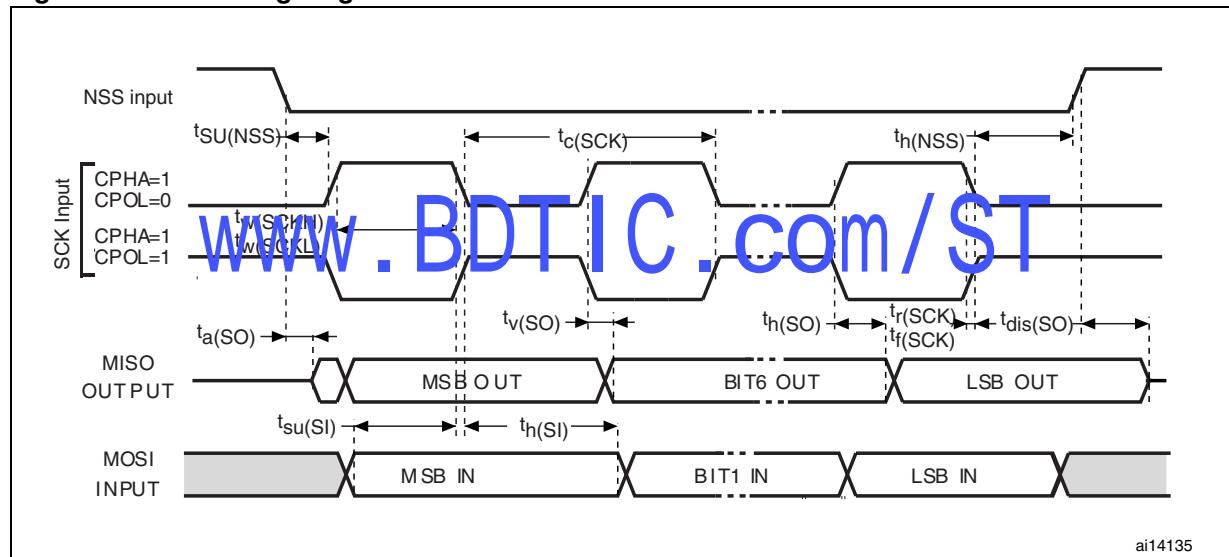


1.   Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 43.　SPI timing diagram - master mode[1]**
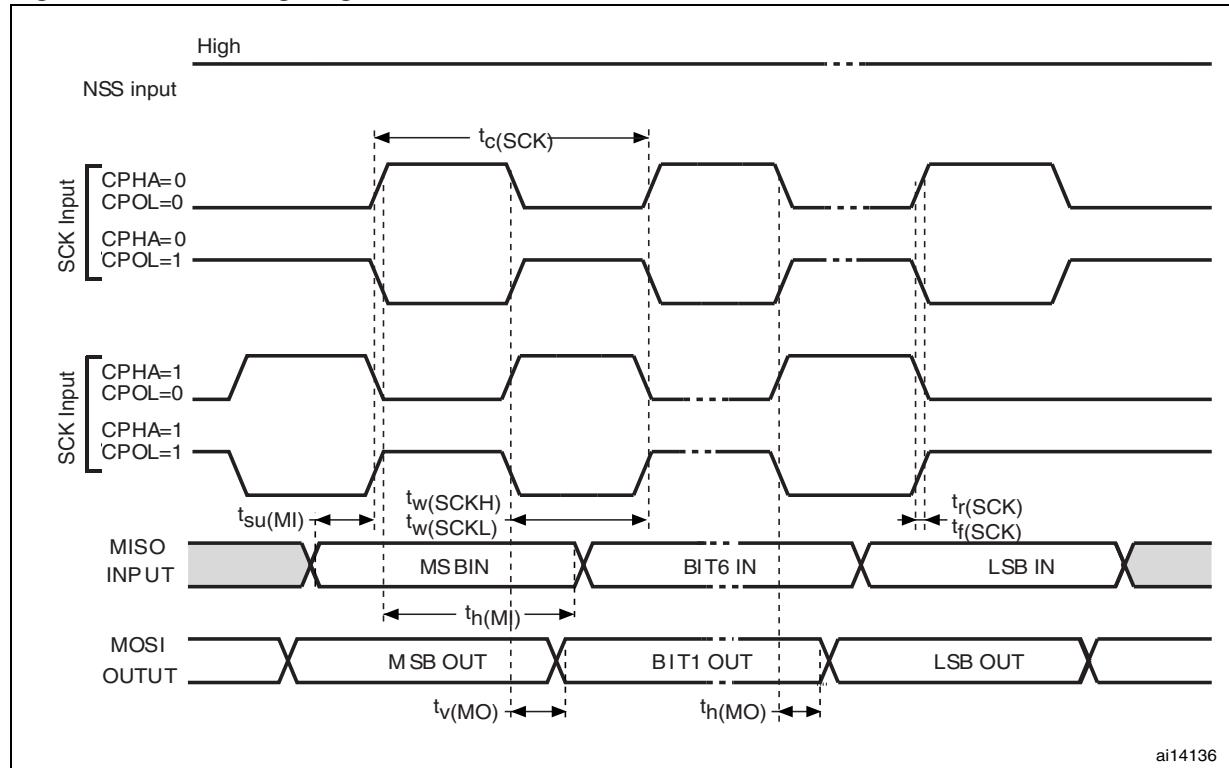


1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## 5.3.17　12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 9*.

*Note:　　It is recommended to perform a calibration after each power-up.*

**Table 52.**    **ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | ADC power supply | | 2.4 | | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 2.4 | | $V_{DDA}$ | V |
| $f_{ADC}$ | ADC clock frequency | | 0.6 | | 14 | MHz |
| $f_S$[1] | Sampling rate | | 0.05 | | 1 | MHz |
| $f_{TRIG}$[1] | External trigger frequency | $f_{ADC}$ = 14 MHz | | | 823 | kHz |
| | | | | | 17 | $1/f_{ADC}$ |
| $V_{AIN}$ | Conversion voltage range[2] | | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | | $V_{REF+}$ | V |
| $R_{AIN}$[1] | External input impedance | | See *Equation 1* and *Table 53* | | | kΩ |
| $R_{ADC}$[1] | Sampling switch resistance | | | | 1 | kΩ |
| $C_{ADC}$[1] | Internal sample and hold capacitor | | | | 5 | pF |
| $t_{CAL}$[1] | Calibration time | $f_{ADC}$ = 14 MHz | 5.9 | | | μs |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$[1] | Injection trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.214 | μs |
| | | | | | 3[3] | $1/f_{ADC}$ |
| $t_{latr}$[1] | Regular trigger conversion latency | $f_{ADC}$ = 14 MHz | | | 0.143 | μs |
| | | | | | 2[3] | $1/f_{ADC}$ |
| $t_S$[1] | Sampling time | $f_{ADC}$ = 14 MHz | 0.107 | | 17.1 | μs |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$[1] | Power-up time | | 0 | 0 | 1 | μs |
| $t_{CONV}$[1] | Total conversion time (including sampling time) | $f_{ADC}$ = 14 MHz | 1 | | 18 | μs |
| | | | 14 to 252 ($t_S$ for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Guaranteed by design, not tested in production.

2. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 3: Pin descriptions* for further details.

3. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 52*.

**Equation 1: $R_{AIN}$ max formula:**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 53.    $R_{AIN}$ max for $f_{ADC}$ = 14 MHz[1]**

| $T_S$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 1.2 |
| 7.5 | 0.54 | 10 |
| 13.5 | 0.96 | 19 |
| 28.5 | 2.04 | 41 |
| 41.5 | 2.96 | 60 |
| 55.5 | 3.96 | 80 |
| 71.5 | 5.11 | 104 |
| 239.5 | 17.1 | 350 |

1. Data guaranteed by design, not tested in production.

**Table 54.    ADC accuracy - limited test conditions[1]**

| Symbol | Parameter | Test conditions | Typ | Max[2] | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error[3] | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V, $T_A$ = 25 °C Measurements made after ADC calibration $V_{REF+}$ = $V_{DDA}$ | ±1.3 | ±2 | LSB |
| EO | Offset error[3] | | ±1 | ±1.5 | |
| EG | Gain error[3] | | ±0.5 | ±1.5 | |
| ED | Differential linearity error[3] | | ±0.7 | ±1 | |
| EL | Integral linearity error[3] | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.

2. Data based on characterization, not tested in production.

3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.

**Table 55.    ADC accuracy[1] [2]**

| Symbol | Parameter | Test conditions | Typ | Max[3] | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error[4] | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error[3] | | ±1.5 | ±25 | |
| EG | Gain error[3] | | ±1.5 | ±3 | |
| ED | Differential linearity error[3] | | ±1 | ±2 | |
| EL | Integral linearity error[3] | | ±1.5 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted $V_{DD}$, frequency, $V_{REF}$ and temperature ranges.

3. Data based on characterization, not tested in production.

4. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.13* does not affect the ADC accuracy.

**Figure 44.    ADC accuracy characteristics**



$$\left[1LSB_{IDEAL} = \frac{V_{REF+}}{4096} \left(or \frac{V_{DDA}}{4096} \text{ depending on package}\right)\right]$$

(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

$E_T$=Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
$E_O$=Offset Error: deviation between the first actual transition and the first ideal one.
$E_G$=Gain Error: deviation between the last ideal transition and the last actual one.
$E_D$=Differential Linearity Error: maximum deviation between actual steps and the ideal one.
$E_L$=Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 45.    Typical connection diagram using the ADC**
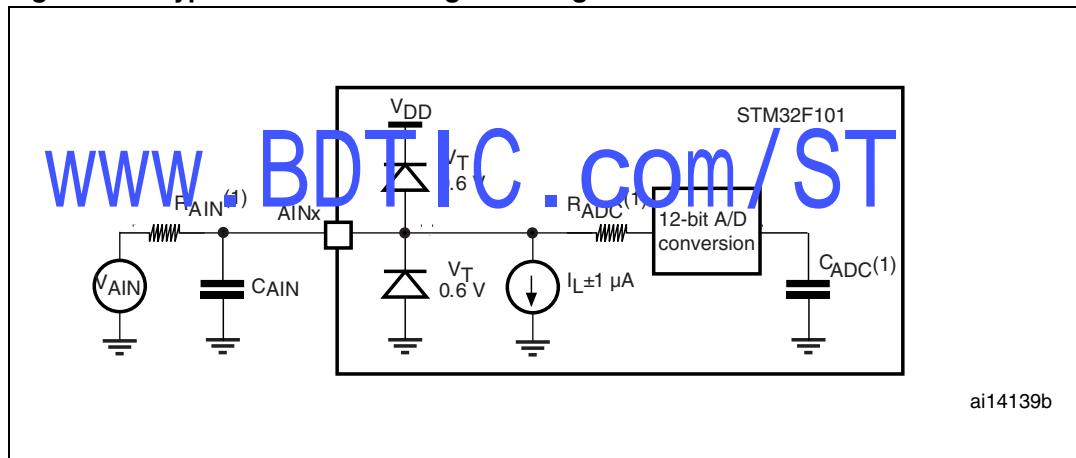


1.  Refer to *Table 52* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.

2.  $C_{PARASITIC}$ must be added to $C_{AIN}$. It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 46.   Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**
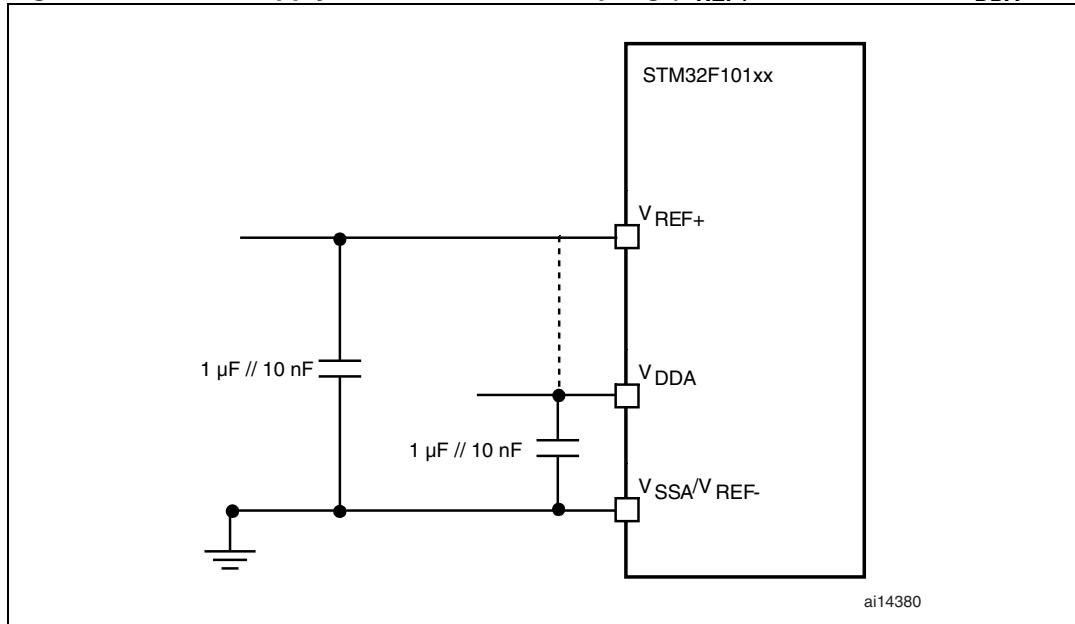


1.   $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

**Figure 47.   Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**
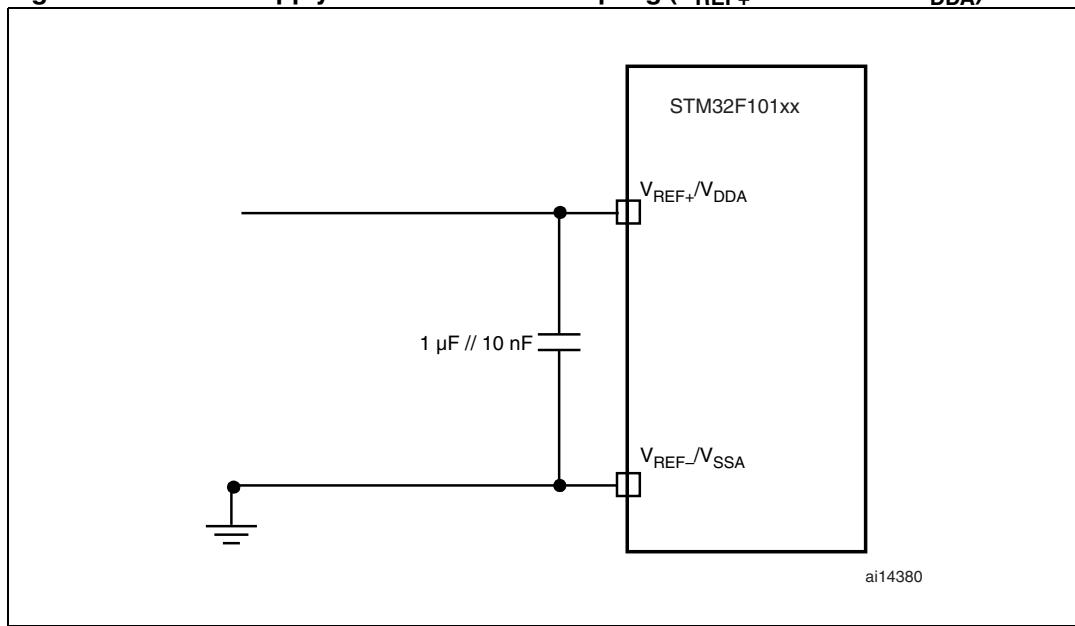


1.   $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

### 5.3.18 DAC electrical specifications

**Table 56. DAC characteristics**

| Symbol | Parameter | Min | Typ | Max[1] | Unit | Comments |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Analog supply voltage | 2.4 | | 3.6 | V | |
| $V_{DD18D}$ | Digital supply voltage | 1.6 | 1.8 | 2 | V | |
| $V_{REF+}$ | Reference supply voltage | 2.4 | | 3.6 | V | $V_{REF+}$ must always be below $V_{DD33A}$ |
| $V_{SSA}$ | Ground | 0 | | 0 | V | |
| $R_L$ | Resistive load with buffer ON | 5 | | | kΩ | Minimum resistive load between DAC_OUT and $V_{SSA}$ |
| $C_L$ | Capacitive load | | | 50 | pF | Maximum capacitive load at DAC_OUT pin. |
| DAC_OUTmin | Lower DAC_OUT voltage with buffer ON | 0.2 | | | V | It gives the maximum output excursion of the DAC |
| DAC_OUTmax | Higher DAC_OUT voltage with buffer ON | | | $V_{REF+}$– 0.2 V | V | it corresponds to 12-bit input code (0E0)h to (F1C)h @ $V_{REF+}$ = 3.6 V and (155)h and (EAB)h @ $V_{REF+}$ = 2.4 V |
| $I_{DD}$ | DAC DC current consumption in quiescent mode (Standby mode) (in $V_{DD18D}+V_{DD33A}+V_{REF+}$) | | 425 | 600 | µA | With no load, middle code (800)H on the inputs |
| | | | 500 | 700 | µA | With no load, worst code (F1C)H @ $V_{REF+}$ = 3.6 V in terms of DC consumption on the inputs |
| $I_{DDQ}$ | DAC DC current consumption in Power Down mode (in $V_{DD18D}+V_{DD33A}+V_{REF+}$) | | 5 | 350 | nA | With no load. |
| | DAC DC current consumption in Power Down mode (in $V_{DD33A}+V_{REF+}$) | | 5 | 200 | | |
| DNL | Differential non linearity (Difference between two consecutive code-1LSB) | | ±0.5 | | LSB | Given for the DAC in 10-bit configuration (B1=B0=0 always) |
| INL | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | | ±1 | | LSB | Given for the DAC in 10-bit configuration (B1=B0=0 always) |
| Offset | Offset error (difference between measured value at Code (800)H and the ideal value = $V_{REF+}/2$ | | ±10 | | mV | Given for the DAC in 10-bit configuration (B1=B0=0 always) |
| | | | ±3 | | LSB | Given for the DAC in 10-bit @ $V_{REF+}$ = 3.6 V |

**Table 56.    DAC characteristics (continued)**

| Symbol | Parameter | Min | Typ | Max[1] | Unit | Comments |
|---|---|---|---|---|---|---|
| Gain error | Gain error | | ±0.5 | | % | Given for the DAC in 10-bit configuration (B1=B0=0 always) |
| Amplifier gain | Gain of the amplifier in open loop | 80 | 85 | | dB | with a 5 kΩ load (worst case) |
| $t_{SETTLING}$ | Settling time (full scale: for an 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB | | 3 | 4 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| Update rate | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | | | 1 | MS/s | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ |
| $t_{WAKEUP}$ | Wakeup time from off state (PDV18 from 1 to 0) | | 6.5 | 10 | µs | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones. |
| PSRR+ | Power supply rejection ratio (to $V_{DD33A}$) (static DC measurement | | −67 | −40 | dB | No $R_{LOAD}$, $C_{LOAD} = 50$ pF |

1. Guaranteed by characterization, not tested in production.

### 5.3.19    Temperature sensor characteristics

**Table 57.    TS characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$[1] | $V_{SENSE}$ linearity with temperature | | ±1 | ±2 | °C |
| Avg_Slope[1] | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| $V_{25}$[1] | Voltage at 25°C | 1.34 | 1.43 | 1.52 | V |
| $t_{START}$[2] | Startup time | 4 | | 10 | µs |
| $T_{S\_temp}$[3][2] | ADC sampling time when reading the temperature | | 2.2 | 17.1 | µs |

1. Guaranteed by characterization, not tested in production.

2. Data guaranteed by design, not tested in production.

3. Shortest sampling time can be determined in the application by multiple iterations.

# 6        Package characteristics

## 6.1       Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK®
packages. These packages have a Lead-free second-level interconnect. The category of
second-level interconnect is marked on the package and on the inner box label, in
compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

**Figure 48. LQFP144, 20 x 20 mm, 144-pin thin quad flat package outline[1]**
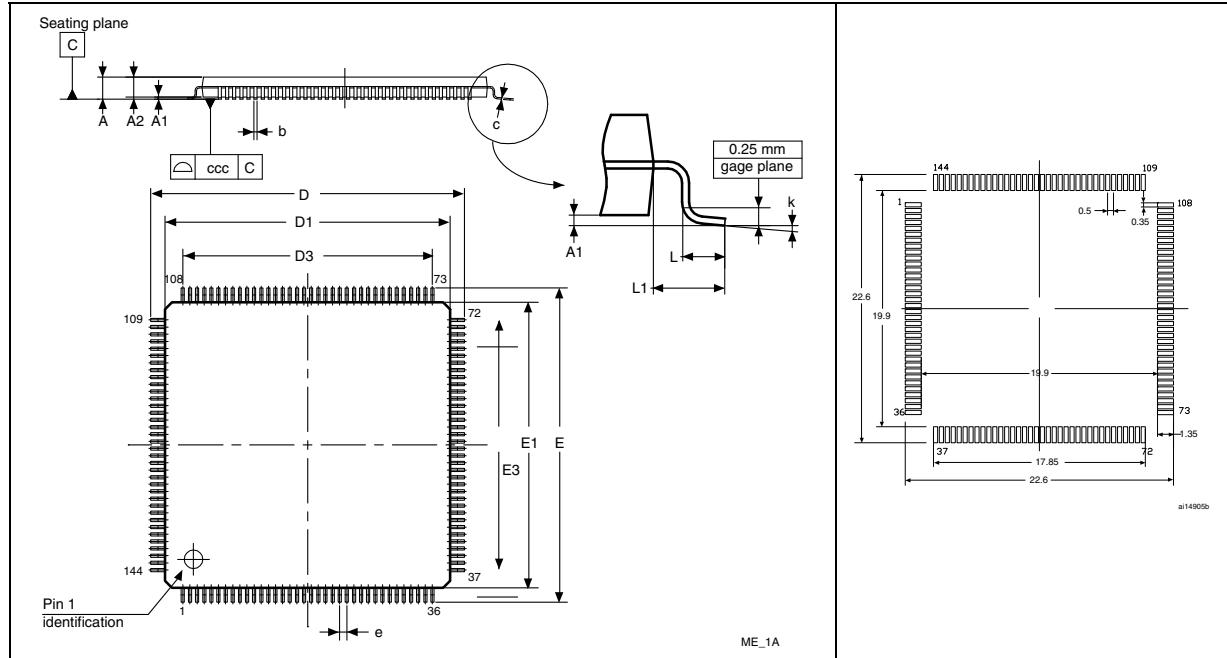


**Figure 49. Recommended footprint[1][2]**



1. Drawing is not to scale.

2. Dimensions are in millimeters.
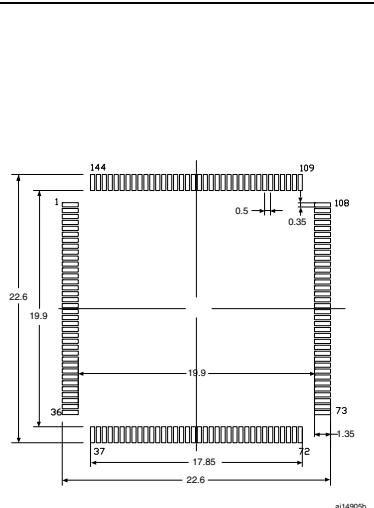
**Table 58. LQFP144, 20 x 20 mm, 144-pin thin quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.60 | | | 0.063 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.0059 |
| A2 | 1.40 | 1.35 | 1.45 | 0.0551 | 0.0531 | 0.0571 |
| b | 0.22 | 0.17 | 0.27 | 0.0087 | 0.0067 | 0.0106 |
| c | | 0.09 | 0.20 | | 0.0035 | 0.0079 |
| D | 22.00 | 21.80 | 22.20 | 0.8661 | 0.8583 | 0.874 |
| D1 | 20.00 | 19.80 | 20.20 | 0.7874 | 0.7795 | 0.7953 |
| D3 | 17.50 | | | 0.689 | | |
| E | 22.00 | 21.80 | 22.20 | 0.8661 | 0.8583 | 0.874 |
| E1 | 20.00 | 19.80 | 20.20 | 0.7874 | 0.7795 | 0.7953 |
| E3 | 17.50 | | | 0.689 | | |
| e | 0.50 | | | 0.0197 | | |
| L | 0.60 | 0.45 | 0.75 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.00 | | | 0.0394 | | |
| k | 3.5° | 0° | 7° | 3.5° | 0° | 7° |
| ccc | | 0.08 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 50.    LQFP100, 100-pin low-profile quad flat package outline[1]**
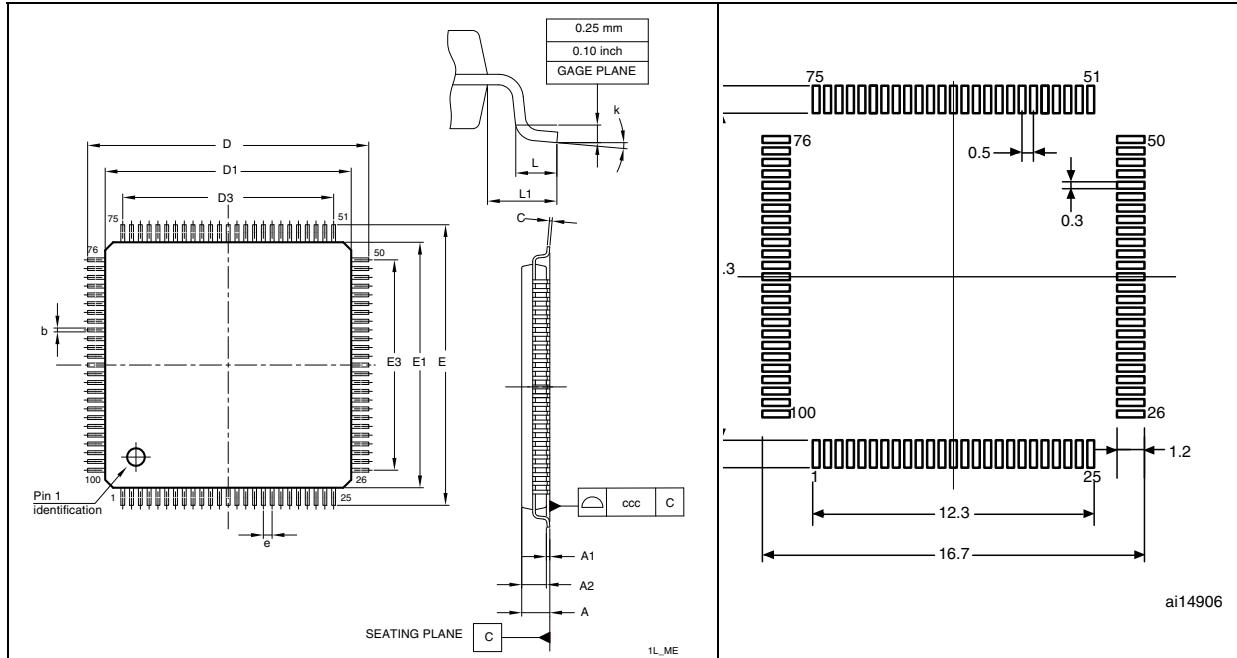
**Figure 51.    Recommended footprint[1][2]**



1.  Drawing is not to scale.

2.  Dimensions are in millimeters.
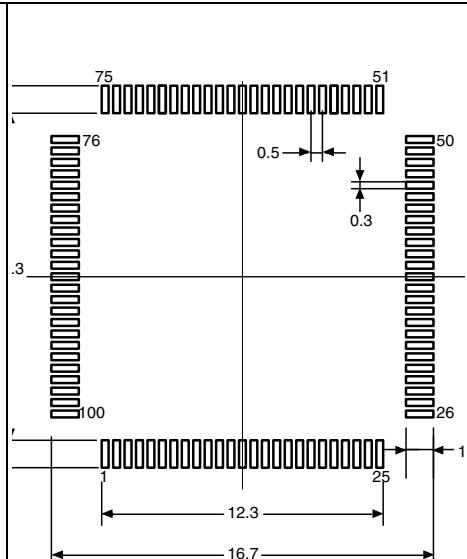
**Table 59.    LQPF100 – 100-pin low profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
|  | Typ | Min | Max | Typ | Min | Max |
| A |  |  | 1.60 |  |  | 0.063 |
| A1 |  | 0.05 | 0.15 |  | 0.002 | 0.0059 |
| A2 | 1.40 | 1.35 | 1.45 | 0.0551 | 0.0531 | 0.0571 |
| b | 0.22 | 0.17 | 0.27 | 0.0087 | 0.0067 | 0.0106 |
| c |  | 0.09 | 0.20 |  | 0.0035 | 0.0079 |
| D | 16.00 | 15.80 | 16.20 | 0.6299 | 0.622 | 0.6378 |
| D1 | 14.00 | 13.80 | 14.20 | 0.5512 | 0.5433 | 0.5591 |
| D3 | 12.00 |  |  | 0.4724 |  |  |
| E | 16.00 | 15.80 | 16.20 | 0.6299 | 0.622 | 0.6378 |
| E1 | 14.00 | 13.80 | 14.20 | 0.5512 | 0.5433 | 0.5591 |
| E3 | 12.00 |  |  | 0.4724 |  |  |
| e | 0.50 |  |  | 0.0197 |  |  |
| L | 0.60 | 0.45 | 0.75 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1.00 |  |  | 0.0394 |  |  |
| k | 3.5° | 0° | 7° | 3.5° | 0° | 7° |
| ccc |  | 0.08 |  |  | 0.0031 |  |

1.  Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 52. LQFP64 – 64 pin low-profile quad flat package outline[1]**
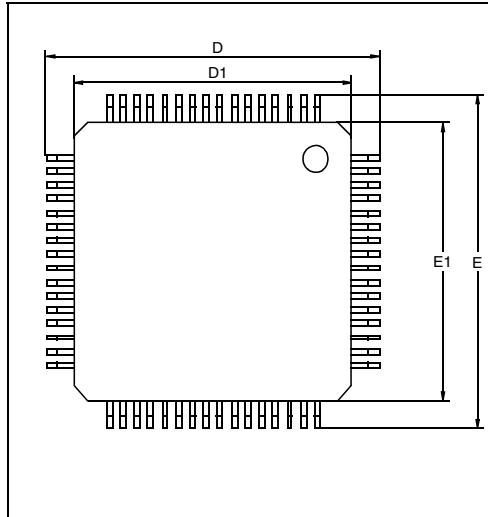


**Figure 53. Recommended footprint[1][2]**
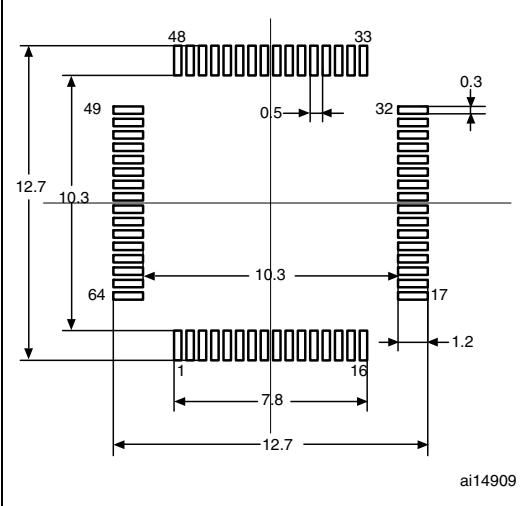


1. Drawing is not to scale.

2. Dimensions are in millimeters.

**Table 60. LQFP64 – 64 pin low-profile quad flat package mechanical data**

| Dim. | mm | | | inches[1] | | |
|------|-----|-----|-----|-----|-----|-----|
|      | Min | Typ | Max | Min | Typ | Max |
| A    |     |     | 1.60 |     |     | 0.0630 |
| A1   | 0.05 |    | 0.15 | 0.0020 |  | 0.0059 |
| A2   | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b    | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c    | 0.09 |     | 0.20 | 0.0035 |     | 0.0079 |
| D    |     | 12.00 |    |     | 0.4724 |     |
| D1   |     | 10.00 |    |     | 0.3937 |     |
| E    |     | 12.00 |    |     | 0.4724 |     |
| E1   |     | 10.00 |    |     | 0.3937 |     |
| e    |     | 0.50 |     |     | 0.0197 |     |
| θ    | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L    | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1   |     | 1.00 |     |     | 0.0394 |     |
| **Number of pins** | | | | | | |
| N    | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.2　Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 9: General operating conditions on page 35*.

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

● $T_A$ max is the maximum ambient temperature in °C,

● $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,

● $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),

● $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL} \times I_{OL}$) + $\Sigma$(($V_{DD} - V_{OH}$) $\times I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 61.　Thermal characteristics**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $\Theta_{JA}$ | **Thermal resistance junction-ambient**<br>LQFP144 - 20 x 20 mm / 0.5 mm pitch | TBD | °C/W |
| | **Thermal resistance junction-ambient**<br>LQFP100 - 14 x 14 mm / 0.5 mm pitch | 46 | |
| | **Thermal resistance junction-ambient**<br>LQFP64 - 10 x 10 mm / 0.5 mm pitch | 45 | |

### 6.2.1　Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

### 6.2.2 Evaluating the maximum junction temperature for an application

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 62: Ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature. Here, only temperature range 6 is available (–40 to 85 °C).

The following example shows how to calculate the temperature range needed for a given application, making it possible to check whether the required temperature range is compatible with the STM32F10xxx junction temperature range.

#### Example: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82$ °C (measured according to JESD51-2), $I_{DDmax} = 50$ mA, $V_{DD} = 3.5$ V, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8$ mA, $V_{OL} = 0.4$ V and maximum 8 I/Os used at the same time in output mode at low level with $I_{OL} = 20$ mA, $V_{OL} = 1.3$ V

$P_{INTmax} = 50$ mA $\times$ 3.5 V= 175 mW

$P_{IOmax} = 20 \times 8$ mA $\times 0.4$ V $+ 8 \times 20$ mA $\times 1.3$ V $= 272$ mW

This gives: $P_{INTmax} = 175$ mW and $P_{IOmax} = 272$ mW

$P_{Dmax} = 175 + 272 = 447$ mW

Thus: $P_{Dmax} = 464$ mW

Using the values obtained in *Table 62* $T_{Jmax}$ is calculated as follows:

– For LQFP64, 45 °C/W

$T_{Jmax} = 82$ °C $+ (45$ °C/W $\times 447$ mW) $= 82$ °C $+ 20.1$ °C $= 102.1$ °C

This is within the junction temperature range of the STM32F10xxx (–40 < $T_J$ < 105 °C).

**Figure 54. LQFP64 $P_D$ max vs. $T_A$**
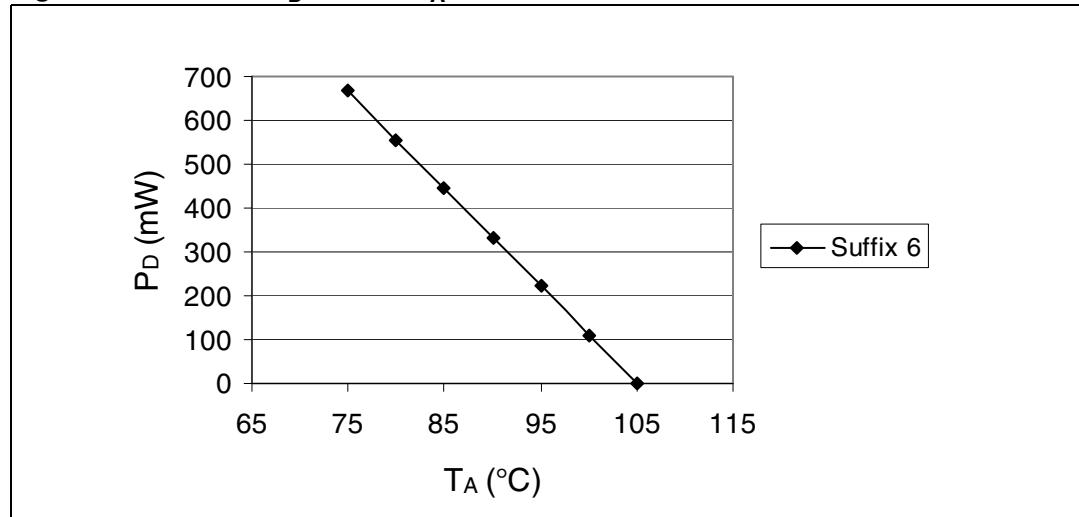
# 7        Part numbering

**Table 62.        Ordering information scheme**

Example:                                    STM32  F 101 R  C    T  6  xxx

**Device family**

STM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

101 = access line

**Pin count**

R = 64 pins

V = 100 pins

Z = 144 pins

**Flash memory size**

C = 256 Kbytes of Flash memory

D = 384 Kbytes of Flash memory

E = 512 Kbytes of Flash memory

**Package**

T = LQFP

**Temperature range**

6 = Industrial temperature range, –40 to 85 °C.

**Options**

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 8    Revision history

**Table 63.    Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-Apr-2008 | 1 | Initial release. |
| 22-May-2008 | 2 | Document status promoted from Target Specification to Preliminary Data.<br><br>*Section 1: Introduction* and *Section 2.2: Full compatibility throughout the family* modified. Small text changes.<br><br>*Note 1* added in *Table 2: STM32F101xC, STM32F101xD and STM32F101xE features and peripheral counts on page 9*.<br><br>LQPF100/BGA100 column added to *Table 5: FSMC pin definition on page 28*.<br><br>Values added to *Maximum current consumption on page 37* (see *Table 13*, *Table 14*, *Table 15* and *Table 16*).<br><br>Values added to *Typical current consumption on page 43* (see *Table 17*, *Table 18* and *Table 19* and see *Figure 11*, *Figure 12*, *Figure 13*, *Figure 14* and *Figure 15*). *Table 19: Typical current consumption in Standby mode* removed.<br><br>*Figure 49: Recommended footprint(1) on page 96* corrected.<br><br>*Equation 1* corrected. *Section 6.2.2: Evaluating the maximum junction temperature for an application on page 100* added. |

**Please Read Carefully:**

www.bdtic.com/ST