

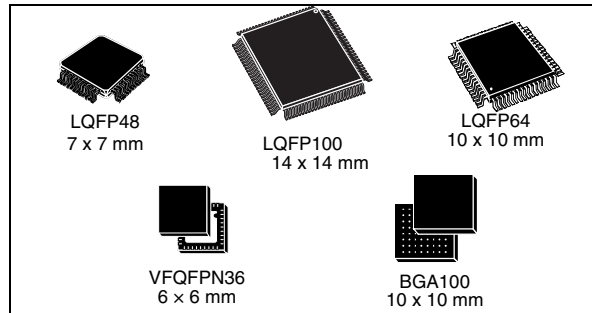


STM32F103x6 STM32F103x8 STM32F103xB

Performance line, ARM-based 32-bit MCU with up to 128 KB Flash, USB, CAN, seven 16-bit timers, 2 ADCs & 9 communication interfaces

Features

- Core: ARM 32-bit Cortex™-M3 CPU
 - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
 - Single-cycle multiplication and hardware division
- Memories
 - 32 to 128 Kbytes of Flash memory
 - 6 to 20 Kbytes of SRAM
- Clock, reset and supply management
 - 2.0 to 3.6 V application supply and I/Os
 - POR, PDR, and programmable voltage detector (PVD)
 - 4-to-16 MHz crystal oscillator
 - Internal 8 MHz factory-trimmed FC
 - Internal 40 kHz FC
 - PLL for CPU clock
 - 32 kHz oscillator for RTC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC and backup registers
- 2 x 12-bit, 1 μs A/D converters (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Dual-sample and hold capability
 - Temperature sensor
- DMA
 - 7-channel DMA controller
 - Peripherals supported: timers, ADC, SPIs, I²Cs and USARTs
- Up to 80 fast I/O ports
 - 26/37/51/80 I/Os, all mappable on 16 external interrupt vectors, all 5 V-tolerant except for analog inputs
- Debug mode



- Serial wire debug (SWD) & JTAG interfaces
- Up to 7 timers
 - Up to three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter
 - 16-bit, 6-channel advanced control timer: up to 6 channels for PWM output, dead-time generation and emergency stop
 - 2 watchdog timers (Independent and Window)
 - System timer: a 24-bit downcounter
- Up to 9 communication interfaces
 - Up to 2 x I²C interfaces (SMBus/PMBus)
 - Up to 3 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
 - Up to 2 SPIs (18 Mbit/s)
 - CAN interface (2.0B Active)
 - USB 2.0 full speed interface
- CRC calculation unit, 96-bit unique ID
- Packages are ECOPACK®

Table 1. Device summary

| Reference | Root part number |
|-------------|--|
| STM32F103x6 | STM32F103C6, STM32F103R6, STM32F103T6 |
| STM32F103x8 | STM32F103C8, STM32F103R8, STM32F103V8, STM32F103T8 |
| STM32F103xB | STM32F103RB, STM32F103VB, STM32F103CB |

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103x6, STM32F103xB and STM32F103x8 Medium-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xx family, please refer to [Section 2.2: Full compatibility throughout the family](#).

The Medium-density STM32F103xx datasheet should be read in conjunction with the Medium- and High-density STM32F10xxx reference manual.

The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: <http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/>.

2 Description

The STM32F103x6, STM32F103xB and STM32F103x8 performance line family incorporates the high-performance ARM Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 128Kbytes and SRAM up to 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs, a USB and a CAN.

The STM32F103xx Medium-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the -40 to +85 °C temperature range and the -40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The complete STM32F103xx Medium-density performance line family includes devices in 5 different package types: from 36 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx Medium-density performance line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- PC peripherals gaming and GPS platforms
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC

[Figure 1](#) shows the general block diagram of the device family.

2.1 Device overview

Table 2. Device features and peripheral counts (STM32F103xx Medium-density performance line)

| Peripheral | | STM32F103Tx | | STM32F103Cx | | | STM32F103Rx | | | STM32F103Vx | |
|-------------------------|------------------|--|----|-------------|----|-----|-------------|----|-----|--------------------|-----|
| Flash - Kbytes | | 32 | 64 | 32 | 64 | 128 | 32 | 64 | 128 | 64 | 128 |
| SRAM - Kbytes | | 10 | 20 | 10 | 20 | 20 | 10 | 20 | | 20 | |
| Timers | General purpose | 2 | 3 | 2 | 3 | 3 | 2 | 3 | | 3 | |
| | Advanced control | 1 | | 1 | | | 1 | | | 1 | |
| Communication | SPI | 1 | 1 | 1 | 2 | 2 | 1 | 2 | | 2 | |
| | I ² C | 1 | 1 | 1 | 2 | 2 | 1 | 2 | | 2 | |
| | USART | 2 | 2 | 2 | 3 | 3 | 2 | 3 | | 3 | |
| | USB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 1 | |
| | CAN | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 1 | |
| GPIOs | | 26 | | 37 | | | 51 | | | 80 | |
| 12-bit synchronized ADC | | 2 | | 2 | | | 2 | | | | |
| Number of channels | | 10 channels | | 10 channels | | | 16 channels | | | | |
| CPU frequency | | 72 MHz | | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | | |
| Operating temperatures | | Ambient temperatures: -40 to +85 °C / -40 to +105 °C (see Table 8) Junction temperature: -40 to +125 °C (see Table 8) | | | | | | | | | |
| Packages | | VFQFPN36 | | LQFP48 | | | LQFP64 | | | LQFP100, BGA100 | |



2.2 Full compatibility throughout the family

The STM32F103xx is a complete family whose members are fully pin-to-pin, software and feature compatible. In the reference manual, the STM32F103x6, STM32F103xB and STM32F103x8 are referred to as Medium-density devices, while the STM32F103xC, STM32F103xD and STM32F103xE are referred to as High-density devices.

High-density devices are an extension of the Medium-density STM32F103x6/8/B devices, they are specified in the STM32F103xC/D/E datasheet. High-density STM32F103xx devices feature higher Flash memory and RAM capacities, and additional peripherals like SDIO, FSMC, I²S and DAC, while remaining fully compatible with the other members of the family.

The STM32F103xC, STM32F103xD and STM32F103xE are a drop-in replacement for the STM32F103x6, STM32F103xB and STM32F103x8 devices, allowing the user to try different memory densities and providing a greater degree of freedom during the development cycle.

Table 3. STM32F103xx family

| Pinout | Memory size | | | | | |
|--------|--|--|--------------|--|--------------|--------------|
| | Medium-density STM32F103xx devices | | | High-density STM32F103xx devices | | |
| | 32 KB Flash | 64 KB Flash | 128 KB Flash | 256 KB Flash | 384 KB Flash | 512 KB Flash |
| | 10 KB RAM | 20 KB RAM | 20 KB RAM | 48 KB RAM | 64 KB RAM | 64 KB RAM |
| 144 | | | | 5 × USARTs | | |
| 100 | | | | 4 × 16-bit timers, 2 × basic timers | | |
| 64 | 2 × USARTs | 3 × 16-bit timers | | 3 × SPIs, 2 × I ² Ss, 2 × I ² Cs | | |
| | 2 × 16-bit timers | 2 × SPIs, 2 × I ² Cs, USB, CAN, 1 × PWM timer | | USB, CAN, 2 × PWM timers | | |
| 48 | 1 × SPI, 1 × I ² C, USB, CAN, 1 × PWM timer | 1 × ADC | | 3 × ADCs, 1 × DAC, 1 × SDIO | | |
| 36 | 1 × ADC | | | FSMC (100 and 144 pins) | | |

2.3 Overview

ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

Embedded Flash memory

Up to 128 Kbytes of embedded Flash is available for storing programs and data.

CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

Embedded SRAM

Up to 20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

Nested vectored interrupt controller (NVIC)

The STM32F103xx performance line embeds a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 72 MHz. The maximum allowed frequency of the low-speed APB domain is 36 MHz. See [Figure 2](#) for details on the clock tree.

Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1. For further details please refer to AN2606.

Power supply schemes

- $V_{DD} = 2.0$ to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , $V_{DDA} = 2.0$ to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- $V_{BAT} = 1.8$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 11: Power supply scheme](#).

Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} and/or when V_{DD} is higher than the V_{PVD} threshold. The

interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to [Table 10: Embedded reset and power control block characteristics](#) for the values of $V_{POR/PDR}$ and V_{PVD} .

Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop mode
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

Low-power modes

The STM32F103xx performance line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I²C, USART, general-purpose and advanced-control timers TIMx and ADC.

RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers (ten 16-bit registers) can be used to store data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable and can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

General-purpose timers (TIMx)

There are up to 3 synchronizable standard timers embedded in the STM32F103xx performance line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures / output

compares / PWMs on the largest packages. They can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generation.

Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for

- Input Capture
- Output Compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output
- Complementary PWM outputs with programmable inserted dead-times.

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

I²C bus

Up to two I²C bus interfaces can operate in multi-master and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

Both SPIs can be served by the DMA controller.

Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

ADC (analog to digital converter)

Two 12-bit analog to digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

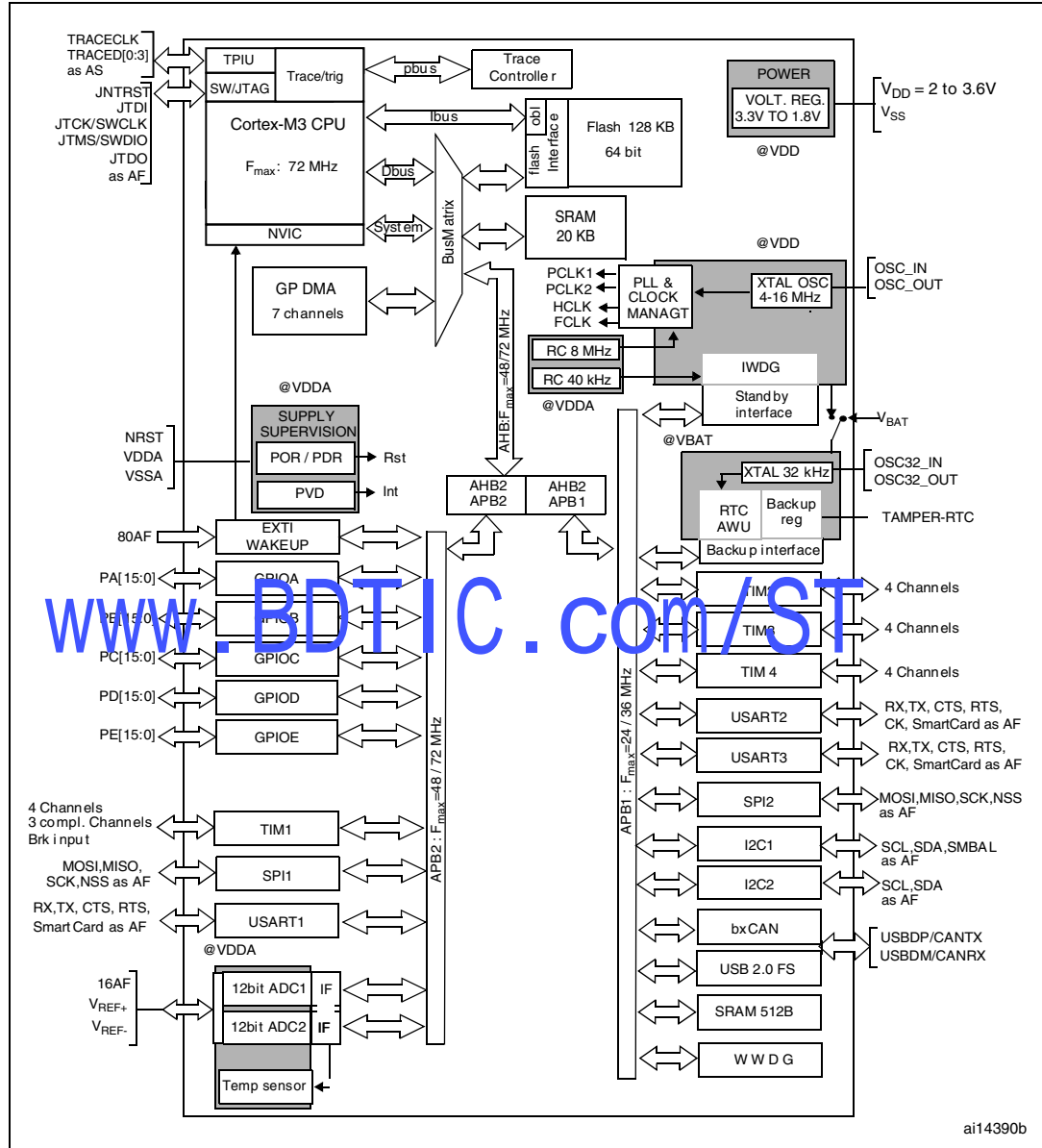
Temperature sensor

The temperature sensor has to generate a linear voltage with any variation in temperature. The conversion range is between $2\text{ V} < V_{\text{DDA}} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

Serial wire JTAG debug port (SWJ-DP)

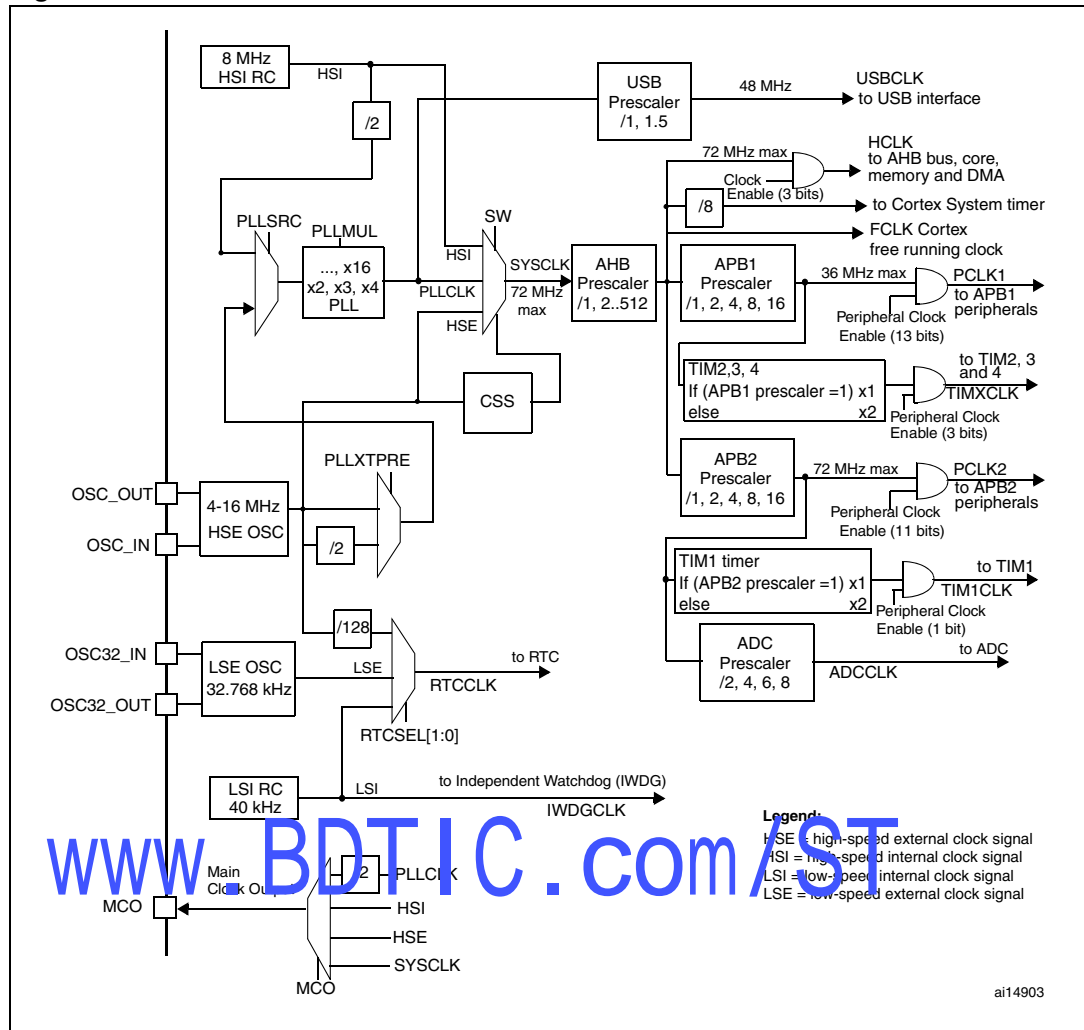
The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

Figure 1. STM32F103xx performance line block diagram



1. $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$ (junction temperature up to $125\text{ }^{\circ}\text{C}$).
2. AF = alternate function on I/O port pin.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the CPU running at either 48 MHz or 72 MHz.
3. To have an ADC conversion time of 1 μ s, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

3 Pin descriptions

Figure 3. STM32F103xx performance line BGA100 ballout

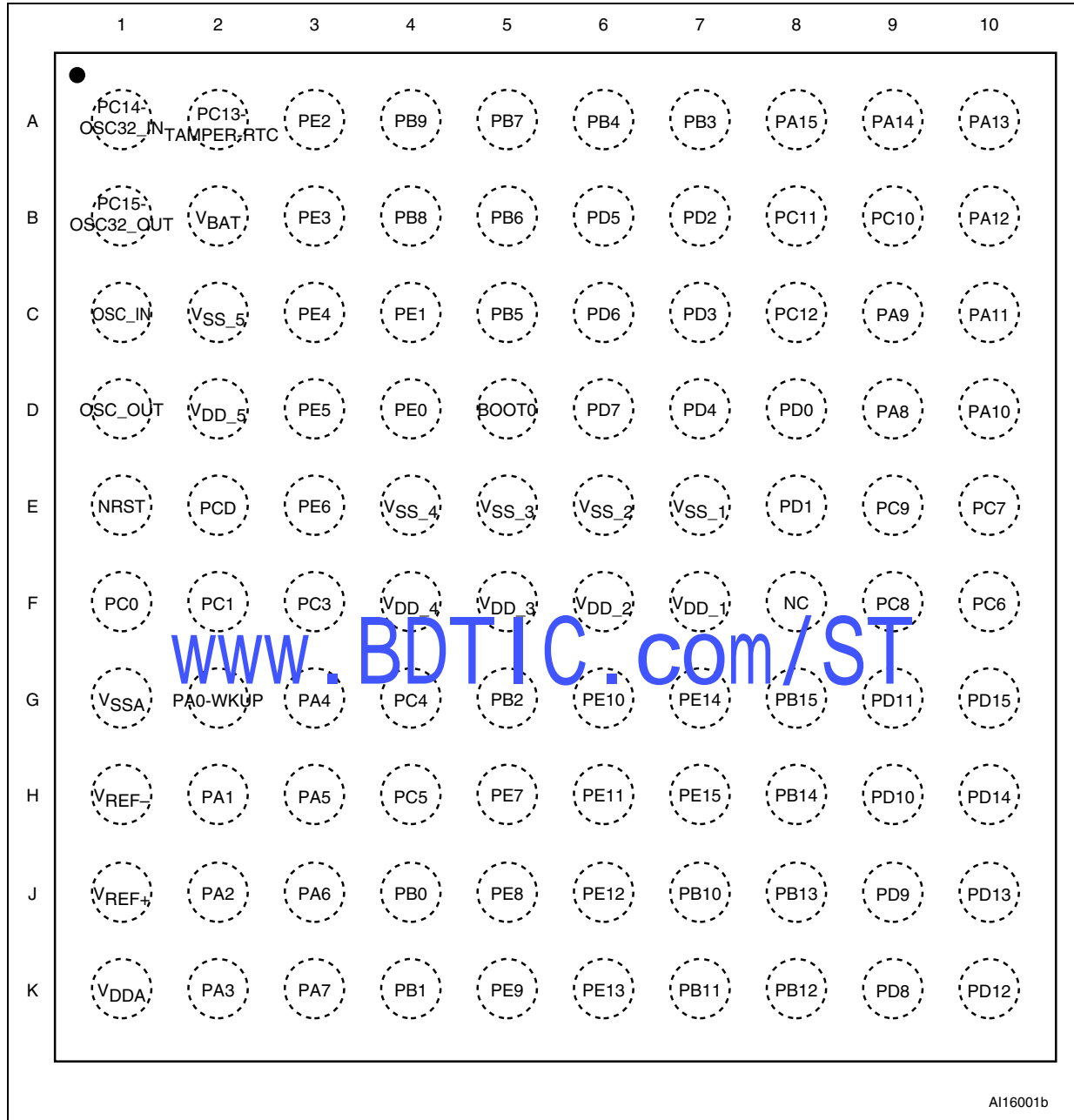
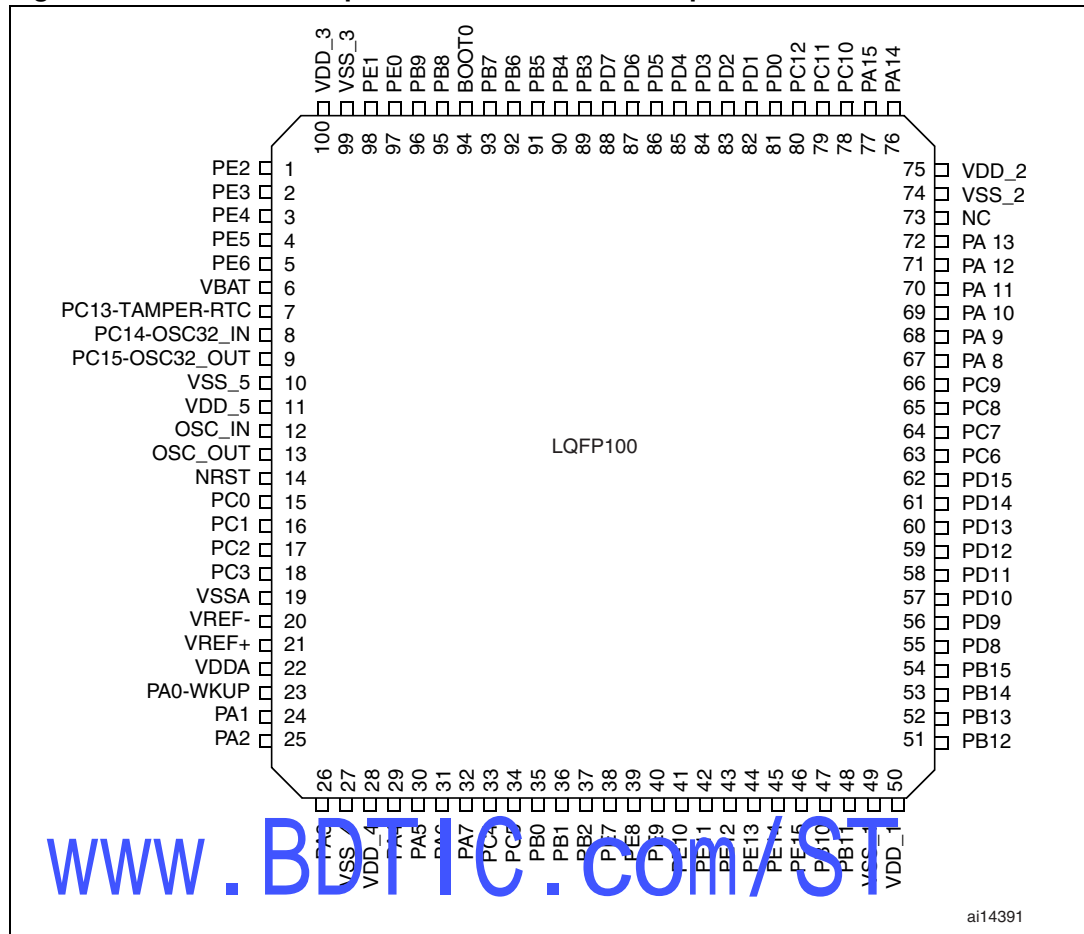
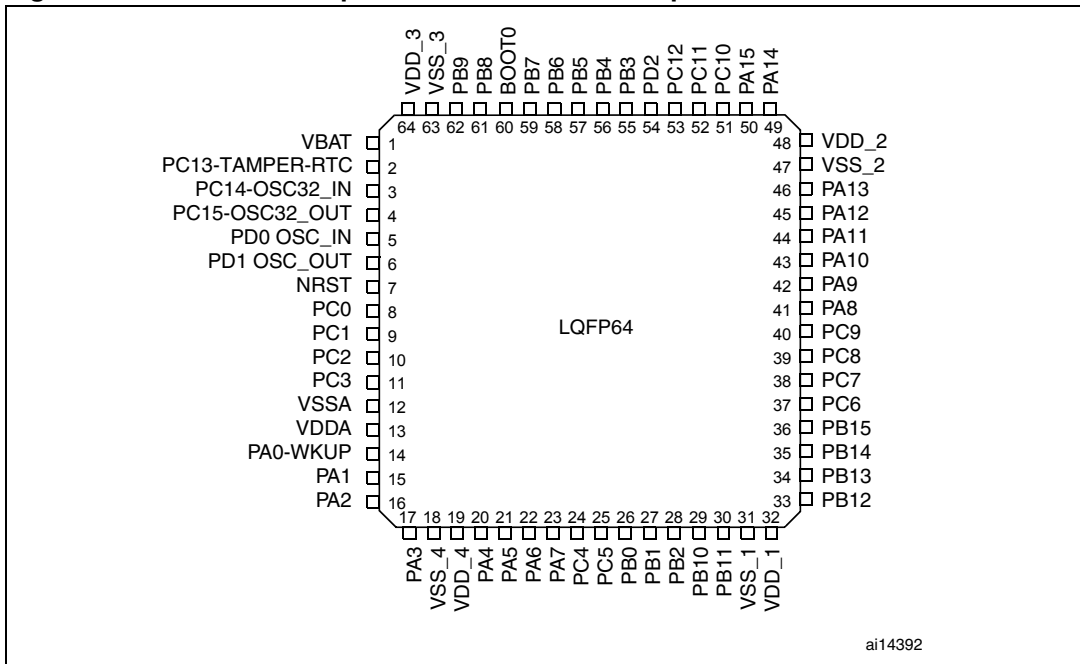


Figure 4. STM32F103xx performance line LQFP100 pinout



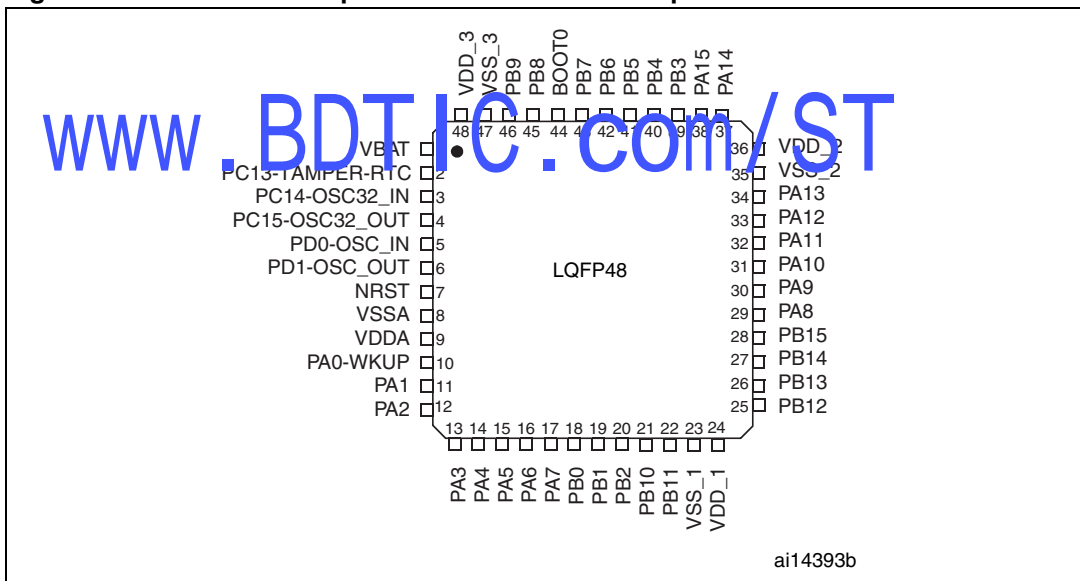
ai14391

Figure 5. STM32F103xx performance line LQFP64 pinout



ai14392

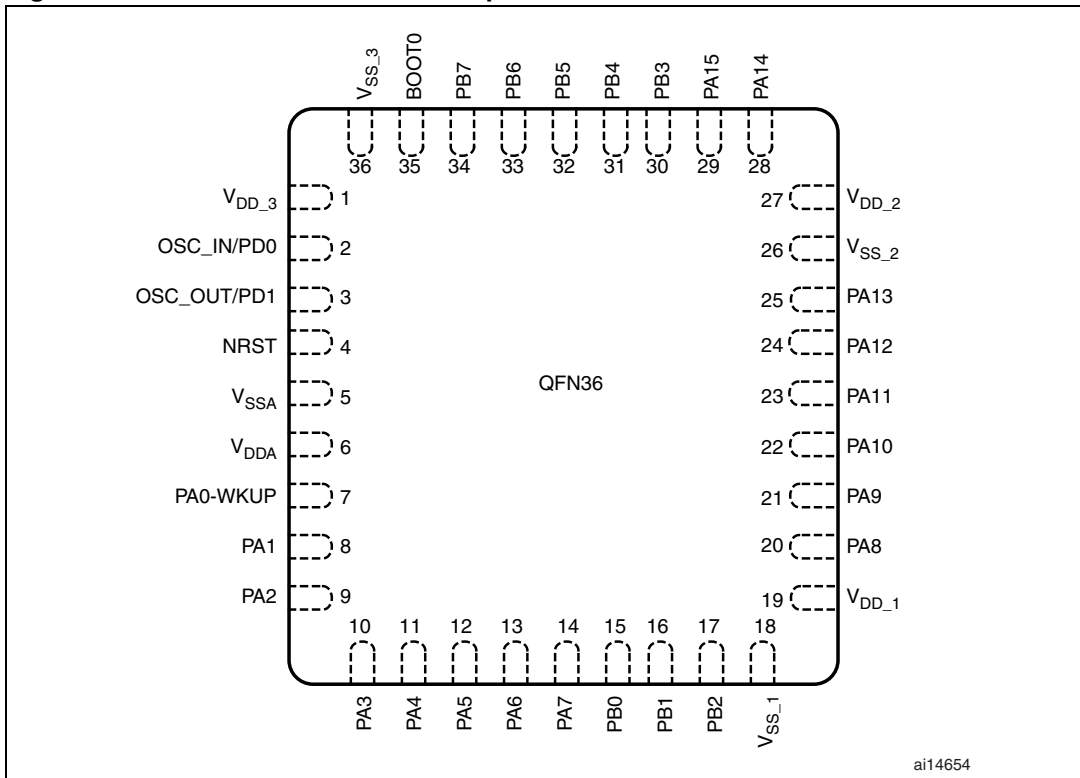
Figure 6. STM32F103xx performance line LQFP48 pinout



ai14393b



Figure 7. STM32F103xx VFQFPN36 pinout



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Table 4. Pin definitions

| Pins | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | |
|--------|--------|--------|---------|----------|--------------------------------|---------------------|--------------------------|---|---|-------|
| BGA100 | LQFP48 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| A3 | - | - | 1 | - | PE2 | I/O | FT | PE2 | TRACECK | |
| B3 | - | - | 2 | - | PE3 | I/O | FT | PE3 | TRACED0 | |
| C3 | - | - | 3 | - | PE4 | I/O | FT | PE4 | TRACED1 | |
| D3 | - | - | 4 | - | PE5 | I/O | FT | PE5 | TRACED2 | |
| E3 | - | - | 5 | - | PE6 | I/O | FT | PE6 | TRACED3 | |
| B2 | 1 | 1 | 6 | - | V _{BAT} | S | | V _{BAT} | | |
| A2 | 2 | 2 | 7 | - | PC13-TAMPER-RTC ⁽⁴⁾ | I/O | | PC13 ⁽⁵⁾ | TAMPER-RTC | |
| A1 | 3 | 3 | 8 | - | PC14-OSC32_IN ⁽⁴⁾ | I/O | | PC14 ⁽⁵⁾ | OSC32_IN | |
| B1 | 4 | 4 | 9 | - | PC15-OSC32_OUT ⁽⁴⁾ | I/O | | PC15 ⁽⁵⁾ | OSC32_OUT | |
| C2 | - | - | 10 | - | V _{SS_5} | S | | V _{SS_5} | | |
| D2 | - | - | 11 | - | V _{DD_5} | S | | V _{DD_5} | | |
| C1 | 5 | 5 | 12 | 2 | OSC_IN | I | | OSC_IN | | |
| D1 | 6 | 6 | 13 | 3 | OSC_OUT | O | | OSC_OUT | | |
| E1 | 7 | 7 | 14 | 4 | NRST | I/O | | NRST | | |
| F1 | - | 8 | 15 | - | PC0 | I/O | | PC0 | ADC12_IN10 | |
| F2 | - | 9 | 16 | - | PC1 | I/O | | PC1 | ADC12_IN11 | |
| E2 | - | 10 | 17 | - | PC2 | I/O | | PC2 | ADC12_IN12 | |
| F3 | - | 11 | 18 | - | PC3 | I/O | | PC3 | ADC12_IN13 | |
| G1 | 8 | 12 | 19 | 5 | V _{SSA} | S | | V _{SSA} | | |
| H1 | - | - | 20 | - | V _{REF-} | S | | V _{REF-} | | |
| J1 | - | - | 21 | - | V _{REF+} | S | | V _{REF+} | | |
| K1 | 9 | 13 | 22 | 6 | V _{DDA} | S | | V _{DDA} | | |
| G2 | 10 | 14 | 23 | 7 | PA0-WKUP | I/O | | PA0 | WKUP/USART2_CTS ⁽⁷⁾ / ADC12_IN0/ TIM2_CH1_ETR ⁽⁷⁾ | |
| H2 | 11 | 15 | 24 | 8 | PA1 | I/O | | PA1 | USART2_RTS ⁽⁷⁾ / ADC12_IN1/ TIM2_CH2 ⁽⁷⁾ | |
| J2 | 12 | 16 | 25 | 9 | PA2 | I/O | | PA2 | USART2_TX ⁽⁷⁾ / ADC12_IN2/ TIM2_CH3 ⁽⁷⁾ | |

Table 4. Pin definitions (continued)

| Pins | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | |
|--------|--------|--------|---------|----------|-------------------|---------------------|--------------------------|---|--|-----------|
| BGA100 | LQFP48 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| K2 | 13 | 17 | 26 | 10 | PA3 | I/O | | PA3 | USART2_RX ⁽⁷⁾ / ADC12_IN3/ TIM2_CH4 ⁽⁷⁾ | |
| E4 | - | 18 | 27 | - | V _{SS_4} | S | | V _{SS_4} | | |
| F4 | - | 19 | 28 | - | V _{DD_4} | S | | V _{DD_4} | | |
| G3 | 14 | 20 | 29 | 11 | PA4 | I/O | | PA4 | SPI1_NSS ⁽⁷⁾ / USART2_CK ⁽⁷⁾ / ADC12_IN4 | |
| H3 | 15 | 21 | 30 | 12 | PA5 | I/O | | PA5 | SPI1_SCK ⁽⁷⁾ / ADC12_IN5 | |
| J3 | 16 | 22 | 31 | 13 | PA6 | I/O | | PA6 | SPI1_MISO ⁽⁷⁾ / ADC12_IN6/ TIM3_CH1 ⁽⁷⁾ | TIM1_BKIN |
| K3 | 17 | 23 | 32 | 14 | PA7 | I/O | | PA7 | SPI1_MOSI ⁽⁷⁾ / ADC12_IN7/ TIM3_CH2 ⁽⁷⁾ | TIM1_CH1N |
| G4 | - | 24 | 33 | | PC4 | I/O | | PC4 | ADC12_IN14 | |
| H4 | - | 25 | 34 | | PC5 | I/O | | PC5 | ADC12_IN15 | |
| J4 | 18 | 26 | 35 | 15 | PB0 | I/O | | PB0 | ADC12_IN8/ TIM3_CH3 ⁽⁷⁾ | TIM1_CH2N |
| K4 | 19 | 27 | 36 | 16 | PB1 | I/O | | PB1 | ADC12_IN9/ TIM3_CH4 ⁽⁷⁾ | TIM1_CH3N |
| G5 | 20 | 28 | 37 | 17 | PB2 / BOOT1 | I/O | FT | PB2/BOOT1 | | |
| H5 | - | - | 38 | - | PE7 | I/O | FT | PE7 | | TIM1_ETR |
| J5 | - | - | 39 | - | PE8 | I/O | FT | PE8 | | TIM1_CH1N |
| K5 | - | - | 40 | - | PE9 | I/O | FT | PE9 | | TIM1_CH1 |
| G6 | - | - | 41 | - | PE10 | I/O | FT | PE10 | | TIM1_CH2N |
| H6 | - | - | 42 | - | PE11 | I/O | FT | PE11 | | TIM1_CH2 |
| J6 | - | - | 43 | - | PE12 | I/O | FT | PE12 | | TIM1_CH3N |
| K6 | - | - | 44 | - | PE13 | I/O | FT | PE13 | | TIM1_CH3 |
| G7 | - | - | 45 | - | PE14 | I/O | FT | PE14 | | TIM1_CH4 |
| H7 | - | - | 46 | - | PE15 | I/O | FT | PE15 | | TIM1_BKIN |
| J7 | 21 | 29 | 47 | - | PB10 | I/O | FT | PB10 | I2C2_SCL/ USART3_TX ⁽⁶⁾⁽⁷⁾ | TIM2_CH3 |
| K7 | 22 | 30 | 48 | - | PB11 | I/O | FT | PB11 | I2C2_SDA/ USART3_RX ⁽⁶⁾⁽⁷⁾ | TIM2_CH4 |
| E7 | 23 | 31 | 49 | 18 | V _{SS_1} | S | | V _{SS_1} | | |



Table 4. Pin definitions (continued)

| Pins | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | |
|--------|--------|--------|---------|----------|-------------------|---------------------|--------------------------|---|--|--------------------------|
| BGA100 | LQFP48 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| F7 | 24 | 32 | 50 | 19 | V _{DD_1} | S | | V _{DD_1} | | |
| K8 | 25 | 33 | 51 | - | PB12 | I/O | FT | PB12 | SPI2_NSS ⁽⁶⁾ / I2C2_SMBA ⁽⁶⁾ / USART3_CK ⁽⁶⁾⁽⁷⁾ / TIM1_BKIN ⁽⁷⁾ | |
| J8 | 26 | 34 | 52 | - | PB13 | I/O | FT | PB13 | SPI2_SCK ⁽⁶⁾ / USART3_CTS ⁽⁶⁾⁽⁷⁾ / TIM1_CH1N ⁽⁷⁾ | |
| H8 | 27 | 35 | 53 | - | PB14 | I/O | FT | PB14 | SPI2_MISO ⁽⁶⁾ / USART3_RTS ⁽⁶⁾⁽⁷⁾ / TIM1_CH2N ⁽⁷⁾ | |
| G8 | 28 | 36 | 54 | - | PB15 | I/O | FT | PB15 | SPI2_MOSI ⁽⁶⁾ / TIM1_CH3N ⁽⁷⁾ | |
| K9 | - | - | 55 | - | PD8 | I/O | FT | PD8 | | USART3_TX |
| J9 | - | - | 56 | - | PD9 | I/O | FT | PD9 | | USART3_RX |
| H9 | - | - | 57 | - | PD10 | I/O | FT | PD10 | | USART3_CK |
| G9 | - | - | 58 | - | PD11 | I/O | FT | PD11 | | USART3_CTS |
| K10 | - | - | 59 | - | PD12 | I/O | FT | PD12 | | TIM4_CH1 / USART3_RTS |
| J10 | - | - | 60 | - | PD13 | I/O | FT | PD13 | | TIM4_CH2 |
| H10 | - | - | 61 | - | PD14 | I/O | FT | PD14 | | TIM4_CH3 |
| G10 | - | - | 62 | - | PD15 | I/O | FT | PD15 | | TIM4_CH4 |
| F10 | - | 37 | 63 | - | PC6 | I/O | FT | PC6 | | TIM3_CH1 |
| E10 | - | 38 | 64 | - | PC7 | I/O | FT | PC7 | | TIM3_CH2 |
| F9 | - | 39 | 65 | - | PC8 | I/O | FT | PC8 | | TIM3_CH3 |
| E9 | - | 40 | 66 | - | PC9 | I/O | FT | PC9 | | TIM3_CH4 |
| D9 | 29 | 41 | 67 | 20 | PA8 | I/O | FT | PA8 | USART1_CK/ TIM1_CH1 ⁽⁷⁾ /MCO | |
| C9 | 30 | 42 | 68 | 21 | PA9 | I/O | FT | PA9 | USART1_TX ⁽⁷⁾ / TIM1_CH2 ⁽⁷⁾ | |
| D10 | 31 | 43 | 69 | 22 | PA10 | I/O | FT | PA10 | USART1_RX ⁽⁷⁾ / TIM1_CH3 ⁽⁷⁾ | |
| C10 | 32 | 44 | 70 | 23 | PA11 | I/O | FT | PA11 | USART1_CTS/ CANRX ⁽⁷⁾ / TIM1_CH4 ⁽⁷⁾ / USBDM | |

Table 4. Pin definitions (continued)

| Pins | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | |
|--------|--------|--------|---------|----------|-------------------|---------------------|--------------------------|---|---|---------------------------|
| BGA100 | LQFP48 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| B10 | 33 | 45 | 71 | 24 | PA12 | I/O | FT | PA12 | USART1_RTS/ CANTX ⁽⁷⁾ / TIM1_ETR ⁽⁷⁾ / USBDP | |
| A10 | 34 | 46 | 72 | 25 | PA13/JTMS/SWDIO | I/O | FT | JTMS/SWDIO | PA13 | |
| F8 | - | - | 73 | - | Not connected | | | | | |
| E6 | 35 | 47 | 74 | 26 | V _{SS_2} | S | | V _{SS_2} | | |
| F6 | 36 | 48 | 75 | 27 | V _{DD_2} | S | | V _{DD_2} | | |
| A9 | 37 | 49 | 76 | 28 | PA14/JTCK/SWCLK | I/O | FT | JTCK/SWCLK | PA14 | |
| A8 | 38 | 50 | 77 | 29 | PA15/JTDI | I/O | FT | JTDI | PA15 | TIM2_CH1_ETR/ SPI1_NSS |
| B9 | - | 51 | 78 | | PC10 | I/O | FT | PC10 | | USART3_TX |
| B8 | - | 52 | 79 | | PC11 | I/O | FT | PC11 | | USART3_RX |
| C8 | - | 53 | 80 | | PC12 | I/O | FT | PC12 | | USART3_CK |
| D8 | 5 | 5 | 81 | 2 | PD0 | I/O | FT | OSC_IN ⁽⁸⁾ | | CANRX |
| E8 | 6 | 6 | 82 | 3 | PD1 | I/O | FT | OSC_OUT ⁽⁸⁾ | | CANTX |
| B7 | | 54 | 83 | | PD2 | I/O | FT | PD2 | TIM3_ETR | |
| C7 | - | - | 84 | - | PD3 | I/O | FT | PD3 | | USART2_CTS |
| D7 | - | - | 85 | - | PD4 | I/O | FT | PD4 | | USART2_RTS |
| B6 | - | - | 86 | - | PD5 | I/O | FT | PD5 | | USART2_TX |
| C6 | - | - | 87 | - | PD6 | I/O | FT | PD6 | | USART2_RX |
| D6 | - | - | 88 | - | PD7 | I/O | FT | PD7 | | USART2_CK |
| A7 | 39 | 55 | 89 | 30 | PB3/JTDO | I/O | FT | JTDO | PB3/TRACESWO | TIM2_CH2 / SPI1_SCK |
| A6 | 40 | 56 | 90 | 31 | PB4/JNTRST | I/O | FT | JNTRST | PB4 | TIM3_CH1 / SPI1_MISO |
| C5 | 41 | 57 | 91 | 32 | PB5 | I/O | | PB5 | I2C1_SMBAL | TIM3_CH2 / SPI1_MOSI |
| B5 | 42 | 58 | 92 | 33 | PB6 | I/O | FT | PB6 | I2C1_SCL ⁽⁷⁾ / TIM4_CH1 ⁽⁶⁾⁽⁷⁾ | USART1_TX |
| A5 | 43 | 59 | 93 | 34 | PB7 | I/O | FT | PB7 | I2C1_SDA ⁽⁷⁾ / TIM4_CH2 ⁽⁶⁾⁽⁷⁾ | USART1_RX |
| D5 | 44 | 60 | 94 | 35 | BOOT0 | I | | BOOT0 | | |
| B4 | 45 | 61 | 95 | - | PB8 | I/O | FT | PB8 | TIM4_CH3 ⁽⁶⁾⁽⁷⁾ | I2C1_SCL / CANRX |

Table 4. Pin definitions (continued)

| Pins | | | | | Pin name | Type ⁽¹⁾ | I/O Level ⁽²⁾ | Main function ⁽³⁾ (after reset) | Alternate functions | |
|--------|--------|--------|---------|----------|-------------------|---------------------|--------------------------|---|-----------------------------|------------------|
| BGA100 | LQFP48 | LQFP64 | LQFP100 | VFQFPN36 | | | | | Default | Remap |
| A4 | 46 | 62 | 96 | - | PB9 | I/O | FT | PB9 | TIM4_CH4 ⁽⁶⁾ (7) | I2C1_SDA / CANTX |
| D4 | - | - | 97 | - | PE0 | I/O | FT | PE0 | TIM4_ETR ⁽⁶⁾ | |
| C4 | - | - | 98 | - | PE1 | I/O | FT | PE1 | | |
| E5 | 47 | 63 | 99 | 36 | V _{SS_3} | S | | V _{SS_3} | | |
| F5 | 48 | 64 | 100 | 1 | V _{DD_3} | S | | V _{DD_3} | | |

1. I = input, O = output, S = supply, HiZ = high impedance.

2. FT = 5 V tolerant.

3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to [Table 2 on page 8](#).

4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.

5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

6. Available only on devices with a Flash memory density equal or higher than 64 Kbytes.

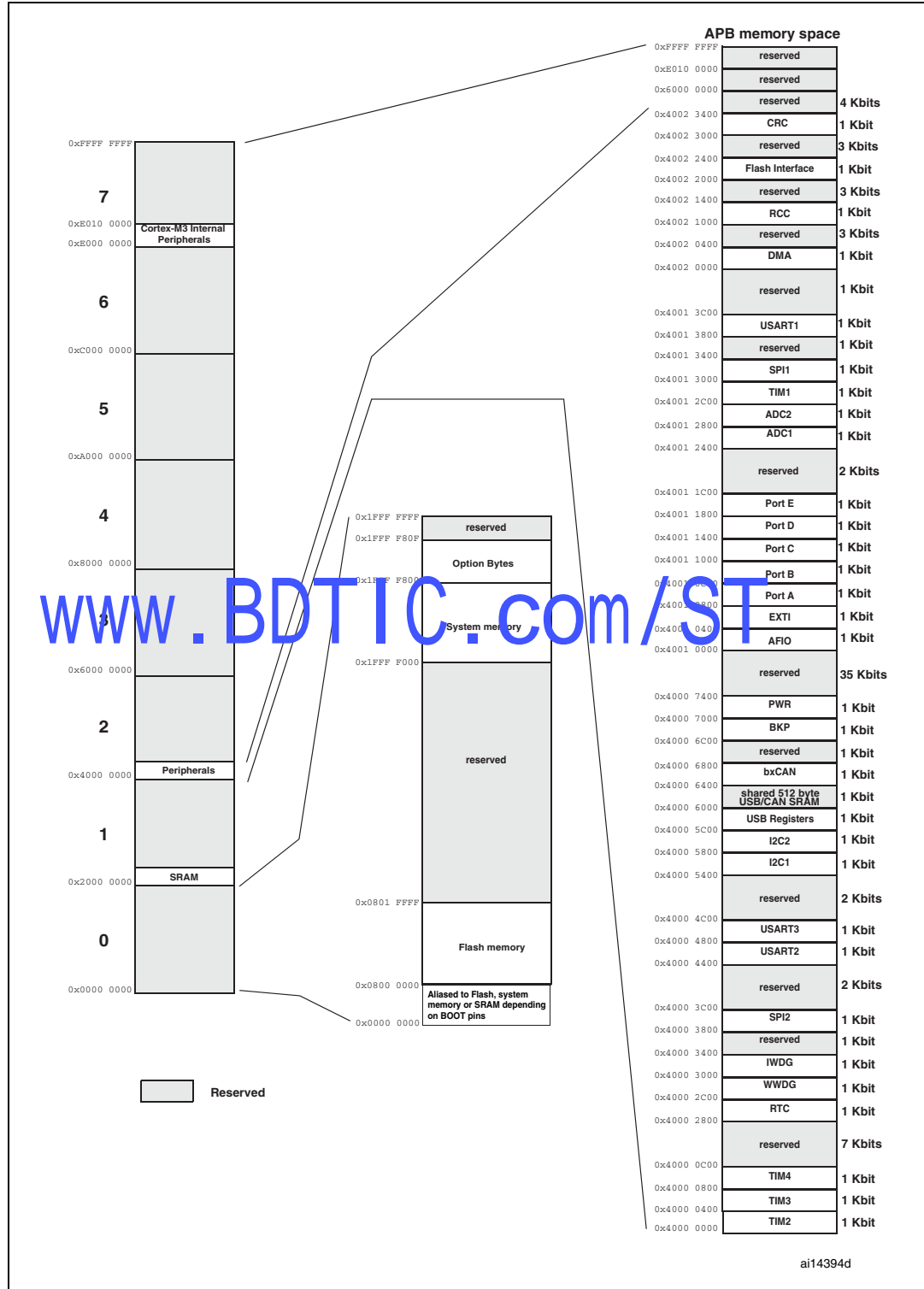
7. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

8. The pins number 2 and 3 in the VFQFPN36 package, and 5 and 6 in the LQFP48 and LQFP64 packages are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 package, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual. The use of PD0 and PD1 in output mode is limited as they can only be used at 50 MHz in output mode.

4 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A=25\text{ °C}$ and $T_A=T_{Amax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation ($\text{mean}\pm 3\Sigma$).

5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ °C}$, $V_{DD} = 3.3\text{ V}$ (for the $2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated ($\text{mean}\pm 2\Sigma$).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 9](#).

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 10](#).

Figure 9. Pin loading conditions

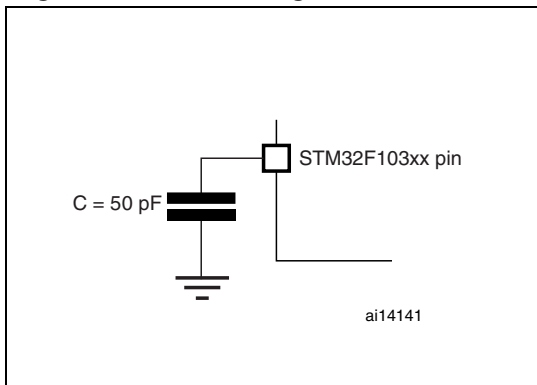
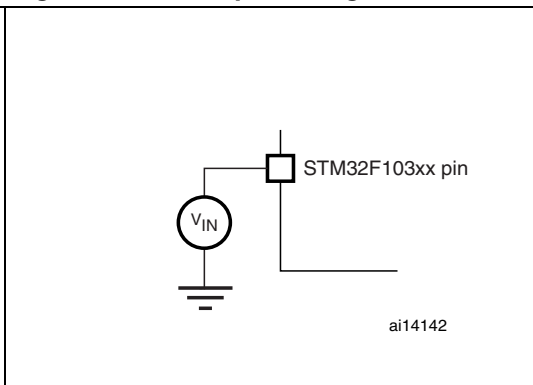
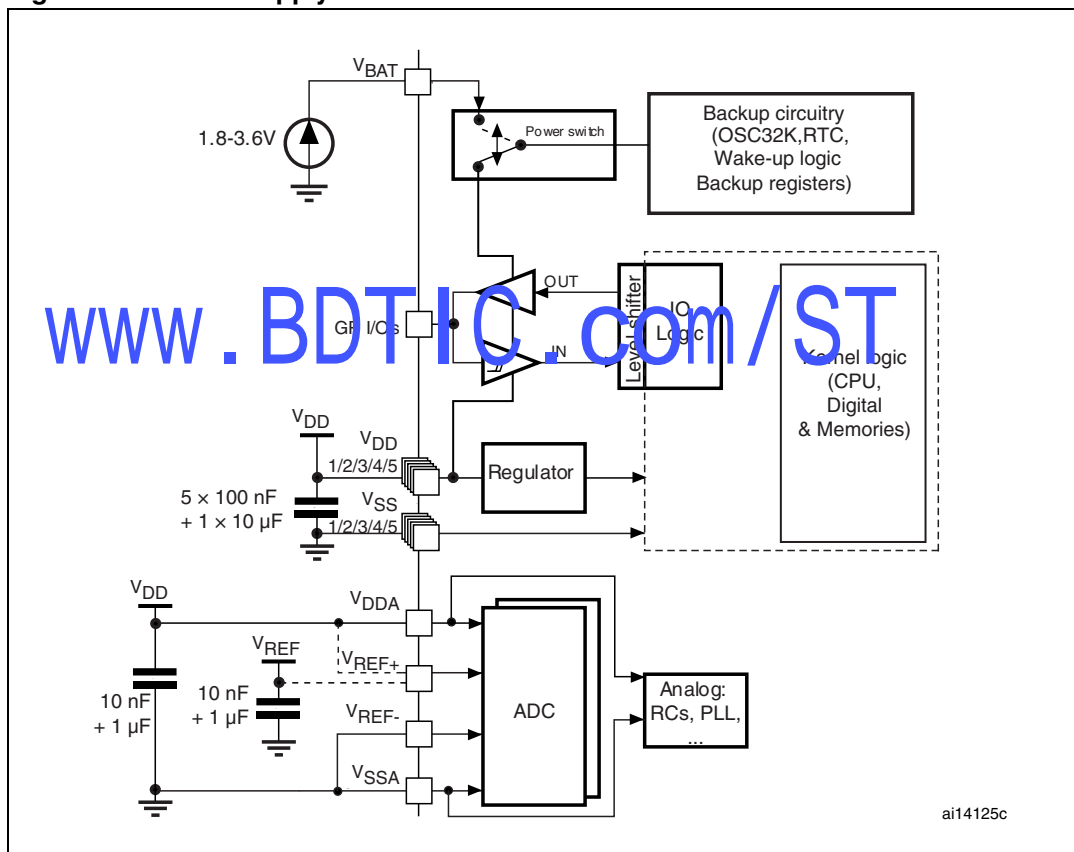


Figure 10. Pin input voltage



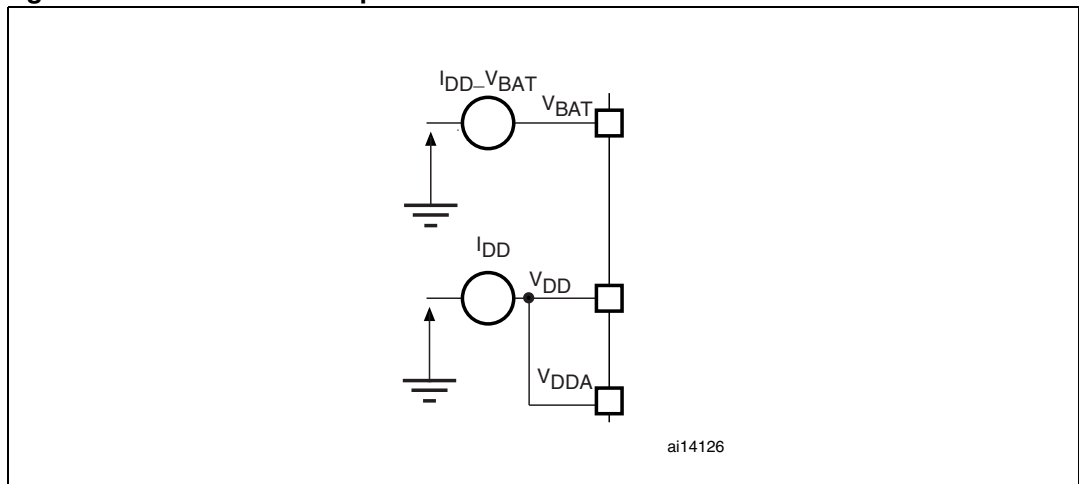
5.1.6 Power supply scheme

Figure 11. Power supply scheme



5.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme



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5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 5: Voltage characteristics](#), [Table 6: Current characteristics](#), and [Table 7: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5. Voltage characteristics

| Symbol | Ratings | Min | Max | Unit |
|--------------------|---|---|--------------|------|
| $V_{DD}-V_{SS}$ | External main supply voltage (including V_{DDA} and V_{DD}) ⁽¹⁾ | -0.3 | 4.0 | V |
| V_{IN} | Input voltage on five volt tolerant pin ⁽²⁾ | $V_{SS}-0.3$ | +5.5 | |
| | Input voltage on any other pin ⁽²⁾ | $V_{SS}-0.3$ | $V_{DD}+0.3$ | |
| $ ΔV_{DDx} $ | Variations between different power pins | 50 | 50 | mV |
| $ V_{SSx}-V_{SS} $ | Variations between all the different ground pins | 50 | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see Section 5.3.11: Absolute maximum ratings (electrical sensitivity) | | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see [Table 6: Current characteristics](#)). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 6. Current characteristics

| Symbol | Ratings | Max. | Unit |
|----------------------------------|---|------|------|
| I_{VDD} | Total current into V_{DD} power lines (source) ⁽¹⁾ | 150 | mA |
| I_{VSS} | Total current out of V_{SS} ground lines (sink) ⁽¹⁾ | 150 | |
| I_{IO} | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/Os and control pin | -25 | |
| $I_{INJ(PIN)}$ ⁽²⁾⁽³⁾ | Injected current on NRST pin | ± 5 | |
| | Injected current on HSE OSC_IN and LSE OSC_IN pins | ± 5 | |
| | Injected current on any other pin ⁽⁴⁾ | ± 5 | |
| $ΣI_{INJ(PIN)}$ ⁽²⁾ | Total injected current (sum of all I/O and control pins) ⁽⁴⁾ | ± 25 | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in [Section 5.3.17: 12-bit ADC characteristics](#).
4. When several inputs are submitted to a current injection, the maximum $ΣI_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $ΣI_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 7. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|------------------------------|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature | 150 | °C |

5.3 Operating conditions

5.3.1 General operating conditions

Table 8. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|---|--------------------------------------|-----|------|------|
| f_{HCLK} | Internal AHB clock frequency | | 0 | 72 | MHz |
| f_{PCLK1} | Internal APB1 clock frequency | | 0 | 36 | |
| f_{PCLK2} | Internal APB2 clock frequency | | 0 | 72 | |
| V_{DD} | Standard operating voltage | | 2 | 3.6 | V |
| V_{BAT} | Backup operating voltage | | 1.8 | 3.6 | V |
| P_D | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 ⁽¹⁾ | LFBGA100 | | 487 | mW |
| | | LQFP100 | | 434 | |
| | | LQFP64 | | 444 | |
| | | LQFP48 | | 363 | |
| | | VQFPN36 | | 1110 | |
| T_A | Ambient temperature for 6 suffix version | Maximum power dissipation | -40 | 85 | °C |
| | | Low power dissipation ⁽²⁾ | -40 | 105 | |
| | Ambient temperature for 7 suffix version | Maximum power dissipation | -40 | 105 | °C |
| | | Low power dissipation ⁽²⁾ | -40 | 125 | |
| T_J | Junction temperature range | 6 suffix version | -40 | 105 | °C |
| | | 7 suffix version | -40 | 125 | |

1. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see [Table 6.2: Thermal characteristics on page 75](#)).

2. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Table 6.2: Thermal characteristics on page 75](#)).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A .

Table 9. Operating conditions at power-up / power-down

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | | 0 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | | 20 | ∞ | |

5.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 10](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 10. Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------|---|-----------------------------|--------------------|------|------|------|
| V_{PVD} | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.1 | 2.18 | 2.26 | V |
| | | PLS[2:0]=000 (falling edge) | 2 | 2.08 | 2.16 | V |
| | | PLS[2:0]=001 (rising edge) | 2.19 | 2.28 | 2.37 | V |
| | | PLS[2:0]=001 (falling edge) | 2.09 | 2.18 | 2.27 | V |
| | | PLS[2:0]=010 (rising edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=010 (falling edge) | 2.18 | 2.28 | 2.38 | V |
| | | PLS[2:0]=011 (rising edge) | 2.38 | 2.48 | 2.58 | V |
| | | PLS[2:0]=011 (falling edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0]=100 (rising edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=100 (falling edge) | 2.37 | 2.48 | 2.59 | V |
| | | PLS[2:0]=101 (rising edge) | 2.57 | 2.68 | 2.79 | V |
| | | PLS[2:0]=101 (falling edge) | 2.47 | 2.58 | 2.69 | V |
| | | PLS[2:0]=110 (rising edge) | 2.66 | 2.78 | 2.9 | V |
| | | PLS[2:0]=110 (falling edge) | 2.56 | 2.68 | 2.8 | V |
| | | PLS[2:0]=111 (rising edge) | 2.76 | 2.88 | 3 | V |
| PLS[2:0]=111 (falling edge) | 2.66 | 2.78 | 2.9 | V | | |
| $V_{PVDhyst}^{(2)}$ | PVD hysteresis | | | 100 | | mV |
| $V_{POR/PDR}$ | Power on/power down reset threshold | Falling edge | 1.8 ⁽¹⁾ | 1.88 | 1.96 | V |
| | | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | | 40 | | mV |
| $T_{RSTTEMPO}^{(2)}$ | Reset temporization | | 1 | 2.5 | 4.5 | mS |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in [Table 11](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 11. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|--|------|------|------|---------------|
| V_{REFINT} | Internal reference voltage | $-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$ | 1.16 | 1.20 | 1.26 | V |
| | | $-40\text{ }^{\circ}\text{C} < T_A < +85\text{ }^{\circ}\text{C}$ | 1.16 | 1.20 | 1.24 | V |
| $T_{S_vrefint}^{(1)}$ | ADC sampling time when reading the internal reference voltage | | | 5.1 | 17.1 | μs |

1. Shortest sampling time can be determined in the application by multiple iterations.

5.3.5 Supply current characteristics

The current consumption is measured as described in [Figure 12: Current consumption measurement scheme](#).

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in [Table 12](#), [Table 13](#) and [Table 14](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 12. Maximum current consumption in Run mode, code with data processing running from Flash

| Symbol | Parameter | Conditions | f _{HCLK} | Max ⁽¹⁾ | | Unit |
|-----------------|----------------------------|--|-------------------|------------------------|-------------------------|------|
| | | | | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Run mode | External clock ⁽²⁾ , all peripherals enabled | 72 MHz | 50 | 50.3 | mA |
| | | | 48 MHz | 36.1 | 36.2 | |
| | | | 36 MHz | 28.6 | 28.7 | |
| | | | 24 MHz | 19.9 | 20.1 | |
| | | | 16 MHz | 14.7 | 14.9 | |
| | | | 8 MHz | 8.6 | 8.9 | |
| | | External clock ⁽²⁾ , all peripherals disabled | 72 MHz | 32.8 | 32.9 | |
| | | | 48 MHz | 24.4 | 24.5 | |
| | | | 36 MHz | 19.8 | 19.9 | |
| | | | 24 MHz | 13.9 | 14.2 | |
| | | | 16 MHz | 10.7 | 11 | |
| | | | 8 MHz | 6.8 | 7.1 | |

1. Data based on characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.

Table 13. Maximum current consumption in Run mode, code with data processing running from RAM

| Symbol | Parameter | Conditions | f _{HCLK} | Max | | Unit |
|-----------------|----------------------------|---|-----------------------|------------------------|-------------------------|------|
| | | | | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Run mode | External clock ⁽¹⁾ , all peripherals enabled | 72 MHz ⁽²⁾ | 48 | 50 | mA |
| | | | 48 MHz ⁽³⁾ | 31.5 | 32 | |
| | | | 36 MHz ⁽²⁾ | 24 | 25.5 | |
| | | | 24 MHz ⁽³⁾ | 17.5 | 18 | |
| | | | 16 MHz ⁽³⁾ | 12.5 | 13 | |
| | | | 8 MHz ⁽³⁾ | 7.5 | 8 | |
| | | External clock ⁽¹⁾ , all peripherals disabled ⁽³⁾ | 72 MHz | 29 | 29.5 | |
| | | | 48 MHz | 20.5 | 21 | |
| | | | 36 MHz | 16 | 16.5 | |
| | | | 24 MHz | 11.5 | 12 | |
| | | | 16 MHz | 8.5 | 9 | |
| | | | 8 MHz | 5.5 | 6 | |

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Data based on characterization results, tested in production at V_{DD max}, f_{HCLK max}. and T_{A max}, and code executed from RAM.
3. Based on characterization, not tested in production.

Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

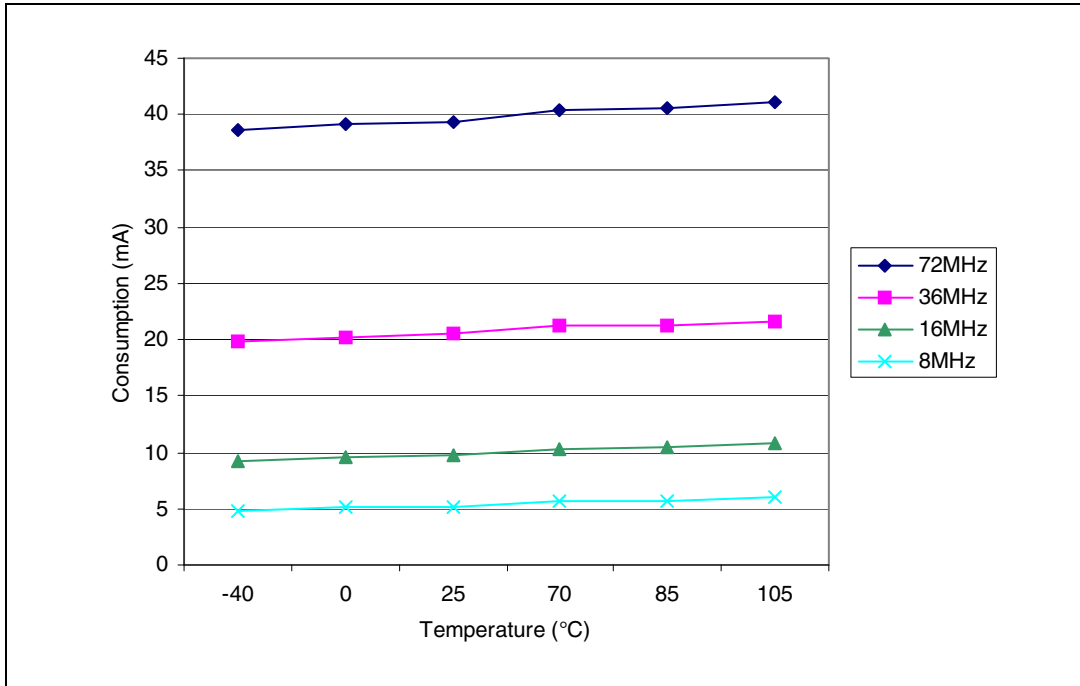


Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

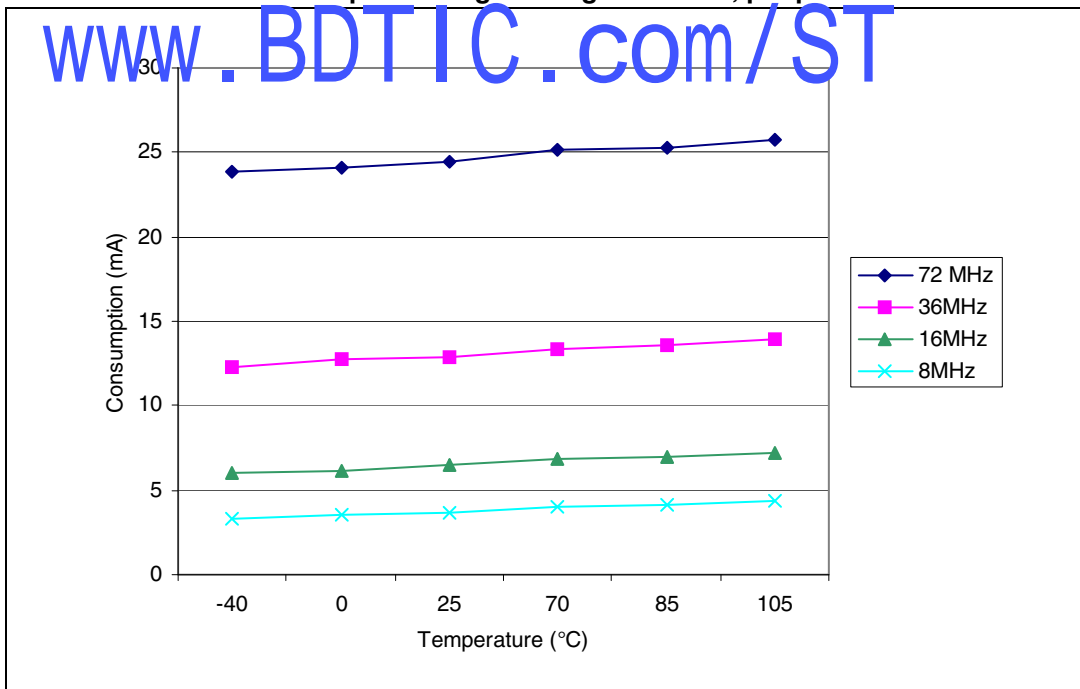


Table 14. Maximum current consumption in Sleep mode, code running from Flash or RAM

| Symbol | Parameter | Conditions | f _{HCLK} | Max | | Unit |
|-----------------|------------------------------|---|-----------------------|------------------------|-------------------------|------|
| | | | | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Sleep mode | External clock ⁽¹⁾ , all peripherals enabled | 72 MHz ⁽²⁾ | 30 | 32 | mA |
| | | | 48 MHz ⁽³⁾ | 20 | 20.5 | |
| | | | 36 MHz ⁽²⁾ | 15.5 | 16 | |
| | | | 24 MHz ⁽²⁾ | 11.5 | 12 | |
| | | | 16 MHz ⁽²⁾ | 8.5 | 9 | |
| | | | 8 MHz ⁽²⁾ | 5.5 | 6 | |
| | | External clock ⁽¹⁾ , all peripherals disabled ⁽²⁾ | 72 MHz | 7.5 | 8 | |
| | | | 48 MHz | 6 | 6.5 | |
| | | | 36 MHz | 5 | 5.5 | |
| | | | 24 MHz | 4.5 | 5 | |
| | | | 16 MHz | 4 | 4.5 | |
| | | | 8 MHz | 3 | 4 | |

1. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz; external clock is 9 MHz for f_{HCLK} = 36 MHz.
2. Data based on characterization results, tested in production at V_{DD max}, f_{HCLK max}. and T_{A max}.
3. Based on characterization, not tested in production.

Table 15. Typical and maximum current consumptions in Stop and Standby modes

| Symbol | Parameter | Conditions | Max | | | | Unit |
|----------------------|---|---|---|---|------------------------|-------------------------|------|
| | | | V _{DD} /V _{BAT} = 2.4 V | V _{DD} /V _{BAT} = 3.3 V | T _A = 85 °C | T _A = 105 °C | |
| I _{DD} | Supply current in Stop mode | Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 23.5 | 24 | 200 ⁽²⁾ | 370 ⁽²⁾ | µA |
| | | Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 13.5 | 14 | 180 ⁽²⁾ | 340 ⁽²⁾ | |
| | Supply current in Standby mode ⁽³⁾ | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 1.7 | 2 | 4 ⁽²⁾ | 5 ⁽²⁾ | |
| I _{DD_VBAT} | Backup domain supply current | Low-speed oscillator and RTC ON | 1.1 | 1.4 | 1.9 ⁽⁴⁾ | 2.2 ⁽⁴⁾ | |

1. Typical values are measured at T_A = 25 °C, V_{DD} = 3.3 V, unless otherwise specified.
2. Data based on characterization results, tested in production at V_{DD max} and f_{HCLK max}.
3. To have the Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator and RTC ON) to I_{DD Standby} (when V_{DD} is present the Backup Domain is powered by V_{DD} supply).
4. Data based on characterization results, not tested in production.

Figure 15. Current consumption in Stop mode with regulator in Run mode versus temperature at $V_{DD} = 3.3\text{ V}$ and 3.6 V

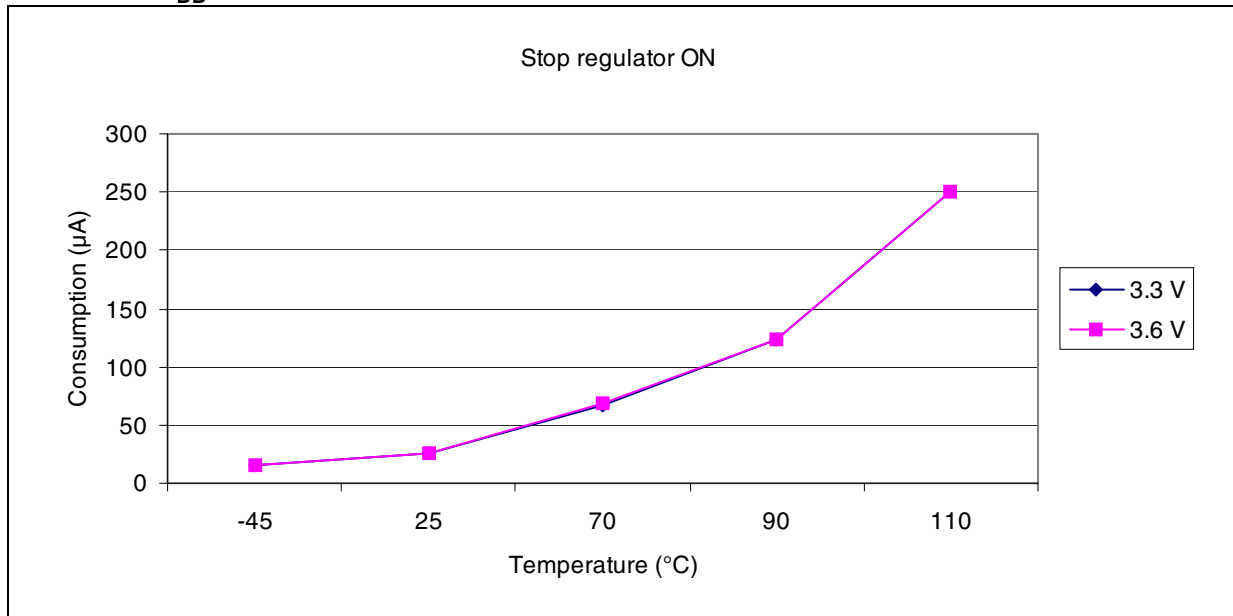


Figure 16. Current consumption in Stop mode with regulator in Low-power mode versus temperature at $V_{DD} = 3.3\text{ V}$ and 3.6 V

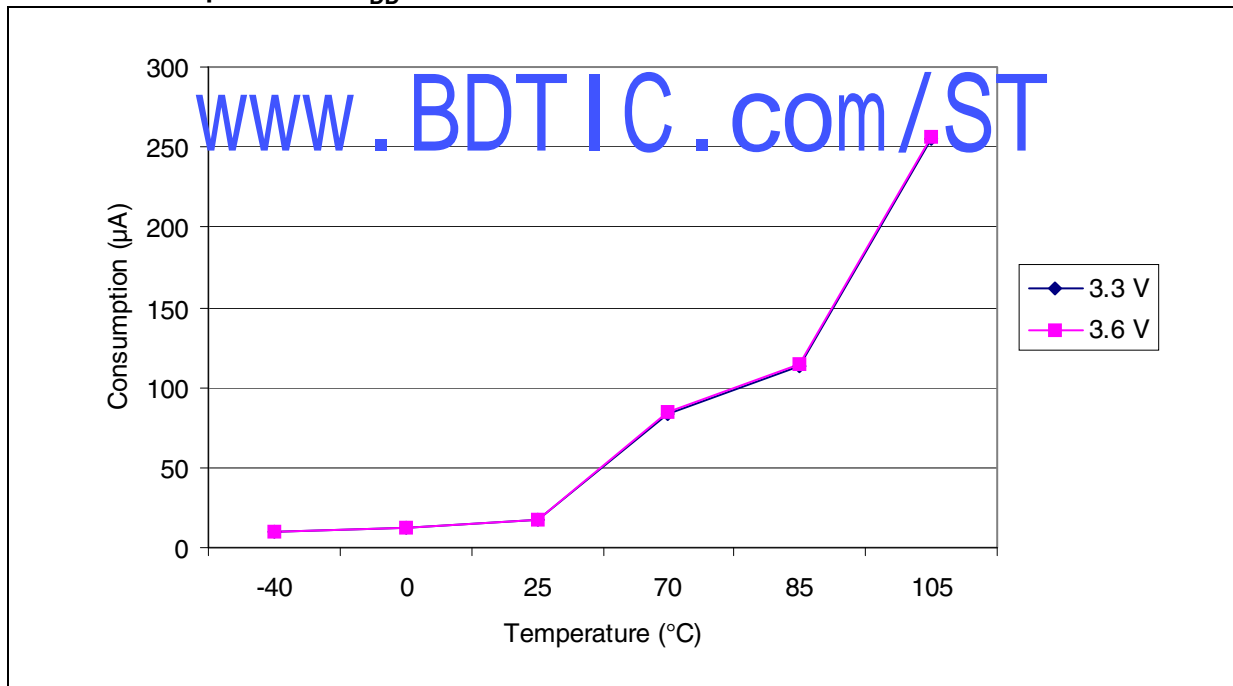
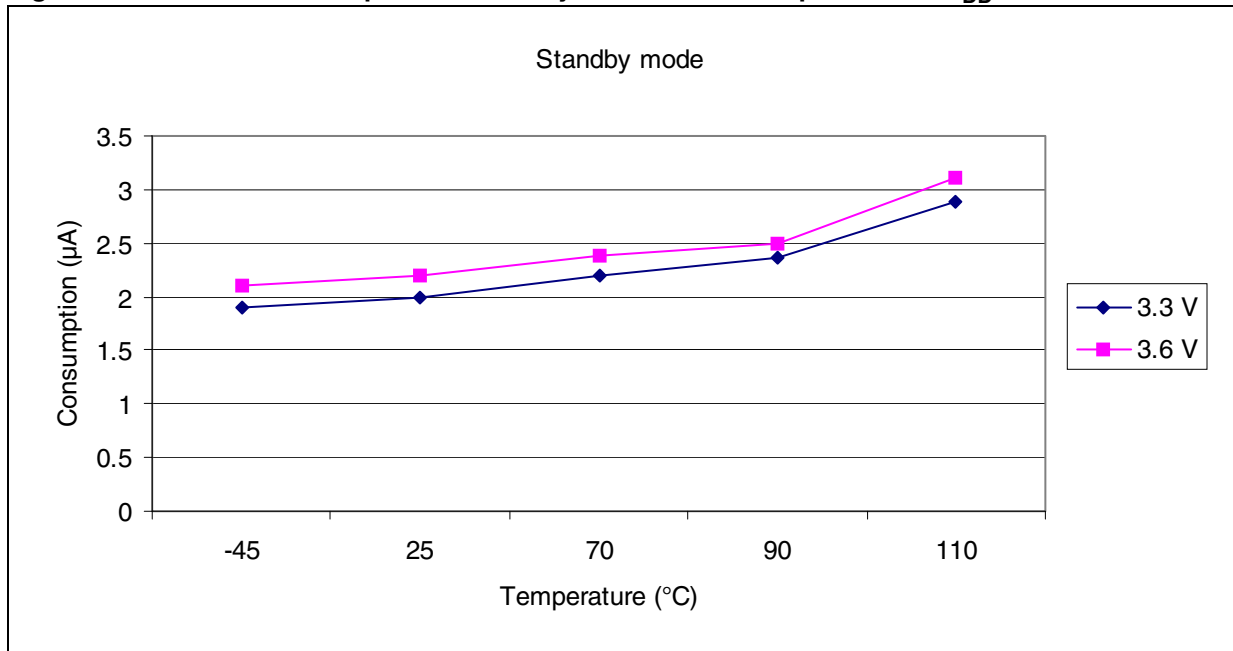


Figure 17. Current consumption in Standby mode versus temperature at $V_{DD} = 3.3\text{ V}$ and 3.6 V



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{PCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 16. Typical current consumption in Run mode, code with data processing running from Flash

| Symbol | Parameter | Conditions | f _{HCLK} | Typ ⁽¹⁾ | | Unit |
|-----------------|----------------------------|---|-------------------|--|--------------------------|------|
| | | | | All peripherals enabled ⁽²⁾ | All peripherals disabled | |
| I _{DD} | Supply current in Run mode | External clock ⁽³⁾ | 72 MHz | 36 | 27 | mA |
| | | | 48 MHz | 24.2 | 18.6 | |
| | | | 36 MHz | 19 | 14.8 | |
| | | | 24 MHz | 12.9 | 10.1 | |
| | | | 16 MHz | 9.3 | 7.4 | |
| | | | 8 MHz | 5.5 | 4.6 | |
| | | | 4 MHz | 3.3 | 2.8 | |
| | | | 2 MHz | 2.2 | 1.9 | |
| | | | 1 MHz | 1.6 | 1.45 | |
| | | | 500 kHz | 1.3 | 1.25 | |
| | | 125 kHz | 1.08 | 1.06 | | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 31.4 | 23.9 | mA |
| | | | 48 MHz | 23.5 | 17.9 | |
| | | | 36 MHz | 18.3 | 14.1 | |
| | | | 24 MHz | 12.2 | 9.5 | |
| | | | 16 MHz | 8.5 | 6.8 | |
| | | | 8 MHz | 4.9 | 4 | |
| | | | 4 MHz | 2.7 | 2.2 | |
| | | | 2 MHz | 1.6 | 1.4 | |
| | | | 1 MHz | 1.02 | 0.9 | |
| 500 kHz | 0.73 | | 0.67 | | | |
| 125 kHz | 0.5 | 0.48 | | | | |

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

| Symbol | Parameter | Conditions | f _{HCLK} | Typ ⁽¹⁾ | | Unit |
|-----------------|------------------------------|---|-------------------|--|--------------------------|------|
| | | | | All peripherals enabled ⁽²⁾ | All peripherals disabled | |
| I _{DD} | Supply current in Sleep mode | External clock ⁽³⁾ | 72 MHz | 14.4 | 5.5 | mA |
| | | | 48 MHz | 9.9 | 3.9 | |
| | | | 36 MHz | 7.6 | 3.1 | |
| | | | 24 MHz | 5.3 | 2.3 | |
| | | | 16 MHz | 3.8 | 1.8 | |
| | | | 8 MHz | 2.1 | 1.2 | |
| | | | 4 MHz | 1.6 | 1.1 | |
| | | | 2 MHz | 1.3 | 1 | |
| | | | 1 MHz | 1.11 | 0.98 | |
| | | | 500 kHz | 1.04 | 0.96 | |
| | | | 125 kHz | 0.98 | 0.95 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 12.3 | 4.4 | |
| | | | 48 MHz | 9.3 | 3.3 | |
| | | | 36 MHz | 7 | 2.5 | |
| | | | 24 MHz | 4.9 | 1.8 | |
| | | | 16 MHz | 3.2 | 1.2 | |
| | | | 8 MHz | 1.6 | 0.6 | |
| | | | 4 MHz | 1 | 0.5 | |
| | | | 2 MHz | 0.72 | 0.47 | |
| | | | 1 MHz | 0.56 | 0.44 | |
| | | | 500 kHz | 0.49 | 0.42 | |
| | | | 125 kHz | 0.43 | 0.41 | |

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Standby mode

| Symbol | Parameter | Conditions | V _{DD} | Typ ⁽¹⁾ | Unit |
|-----------------|---|---|-----------------|--------------------|------|
| I _{DD} | Supply current in Standby mode ⁽²⁾ | Low-speed internal RC oscillator and independent watchdog OFF | 3.3 V | 2 | μA |
| | | | 2.4 V | 1.5 | |
| | | Low-speed internal RC oscillator and independent watchdog ON | 3.3 V | 3.4 | |
| | | | 2.4 V | 2.6 | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | 3.3 V | 3.2 | |
| | | | 2.4 V | 2.4 | |

1. Typical values are measures at T_A = 25 °C.
2. To obtain Standby consumption with RTC ON, add I_{DD_VBAT} (Low-speed oscillator, RTC ON) to I_{DD} Standby.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 19](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in [Table 5](#)

Table 19. Peripheral current consumption⁽¹⁾

| Peripheral | | Typical consumption at 25 °C | Unit |
|------------|--------|------------------------------|------|
| APB1 | TIM2 | 1.2 | mA |
| | TIM3 | 1.2 | |
| | TIM4 | 0.9 | |
| | SPI2 | 0.2 | |
| | USART2 | 0.35 | |
| | USART3 | 0.35 | |
| | I2C1 | 0.39 | |
| | I2C2 | 0.39 | |
| | USB | 0.65 | |
| | CAN | 0.715 | |

Table 19. Peripheral current consumption⁽¹⁾ (continued)

| Peripheral | | Typical consumption at 25 °C | Unit |
|------------|---------------------|------------------------------|------|
| APB2 | GPIO A | 0.47 | mA |
| | GPIO B | 0.47 | |
| | GPIO C | 0.47 | |
| | GPIO D | 0.47 | |
| | GPIO E | 0.47 | |
| | ADC1 ⁽²⁾ | 1.81 | |
| | ADC2 | 1.78 | |
| | TIM1 | 1.6 | |
| | SPI1 | 0.43 | |
| | USART1 | 0.85 | |

- $f_{HCLK} = 72 \text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
- Specific conditions for ADC: $f_{HCLK} = 56 \text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCLK} = f_{APB2}/4$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock

The characteristics given in [Table 20](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 3](#).

Table 20. High-speed external (HSE) user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|-----|-------------|---------|
| f_{HSE_ext} | User external clock source frequency ⁽¹⁾ | | | 8 | 25 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | | $0.7V_{DD}$ | | V_{DD} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | | V_{SS} | | $0.3V_{DD}$ | |
| $t_{w(HSE)}$ $t_{w(HSE)}$ | OSC_IN high or low time ⁽¹⁾ | | 16 | | | ns |
| $t_{r(HSE)}$ $t_{f(HSE)}$ | OSC_IN rise or fall time ⁽¹⁾ | | | | 5 | |
| I_L | OSC_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1 | μA |

- Value based on design simulation and/or technology characteristics. It is not tested in production.

Low-speed external user clock

The characteristics given in [Table 21](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 8](#).

Table 21. Low-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|---|----------------------------------|-------------|--------|-------------|---------|
| f_{LSE_ext} | User External clock source frequency ⁽¹⁾ | | | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | | $0.7V_{DD}$ | | V_{DD} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | | V_{SS} | | $0.3V_{DD}$ | |
| $t_{w(LSE)}$ $t_{w(LSE)}$ | OSC32_IN high or low time ⁽¹⁾ | | 450 | | | ns |
| $t_{r(LSE)}$ $t_{f(LSE)}$ | OSC32_IN rise or fall time ⁽¹⁾ | | | | 5 | |
| I_L | OSC32_IN Input leakage current | $V_{SS} \leq V_{IN} \leq V_{DD}$ | | | ± 1 | μA |

1. Value based on design simulation and/or technology characteristics. It is not tested in production.

Figure 18. High-speed external clock source AC timing diagram

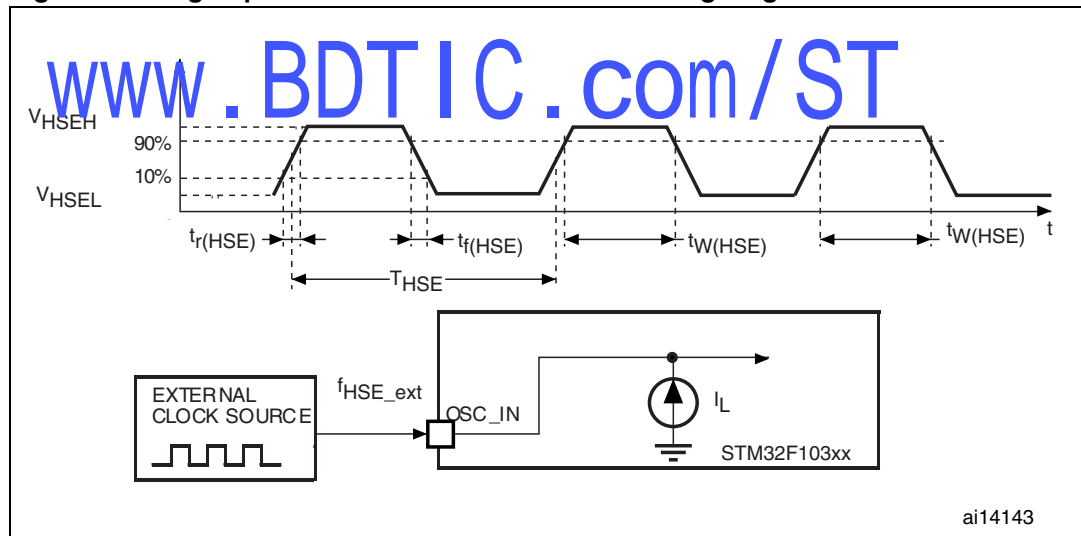
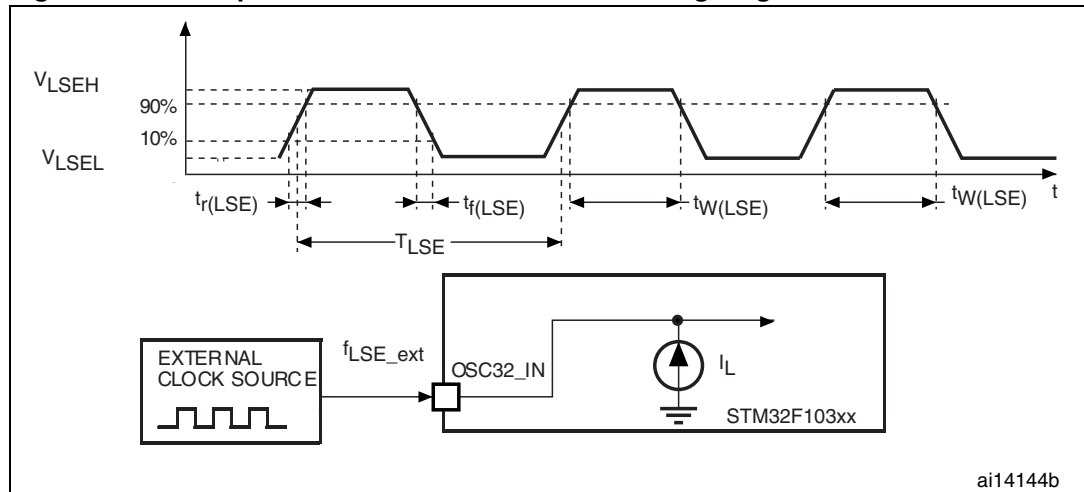


Figure 19. Low-speed external clock source AC timing diagram



High-speed external clock

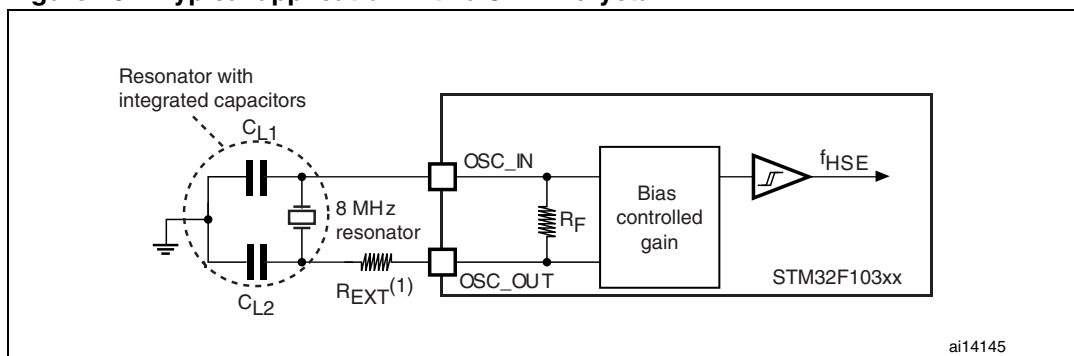
The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 22](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 4-16 MHz oscillator characteristics (1)

| Symbol | Parameter | Conditions | Min. | Typ | Max | Unit |
|----------------------------|--|--|------|-----|-----|------------|
| f_{OSC_IN} | Oscillator frequency | | 4 | 8 | 16 | MHz |
| R_F | Feedback resistor | | | 200 | | k Ω |
| C_{L1} $C_{L2}^{(2)}$ | Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾ | $R_S = 30 \Omega$ | | 30 | | pF |
| i_2 | HSE driving current | $V_{DD} = 3.3 V, V_{IN} = V_{SS}$ with 30 pF load | | | 1 | mA |
| $g_m^{(4)}$ | Oscillator transconductance | Startup | 25 | | | mA/V |
| $t_{SU(HSE)}^{(5)}$ | startup time | V_{DD} is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. Based on characterization results, not tested in production.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 20. Typical application with a 8-MHz crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to $6R_S$.

Low-speed external clock

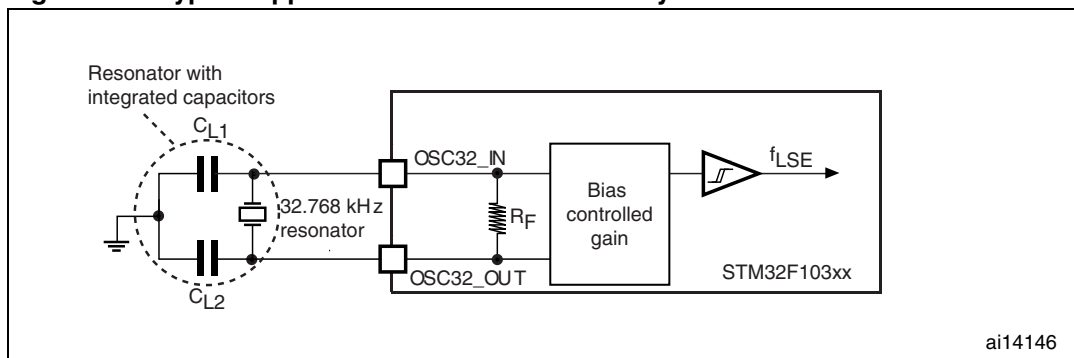
The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 23. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 23. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------|--|-------------------------------------|-----|-----|-----|-----------|
| R_F | Feedback resistor | | | 5 | | $M\Omega$ |
| C_{L1} C_{L2} | Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽¹⁾ | $R_S = 30$ k Ω | | | 15 | pF |
| I_2 | LSE driving current | $V_{DD} = 3.3$ V, $V_{IN} = V_{SS}$ | | | 1.4 | μ A |
| g_m | Oscillator Transconductance | | 5 | | | μ A/V |
| $t_{SU(LSE)}$ ⁽²⁾ | startup time | V_{DD} is stabilized | | 3 | | s |

1. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in [Table 24](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|----------------------------------|-------------------------|-----|---------|-----------|---------|
| f_{HSI} | Frequency | | | 8 | | MHz |
| ACC_{HSI} | Accuracy of HSI oscillator | $T_A = -40$ to 105 °C | | ± 1 | ± 3 | % |
| | | $T_A = -10$ to 85 °C | | ± 1 | ± 2.5 | % |
| | | $T_A = 0$ to 70 °C | | ± 1 | ± 2.2 | % |
| | | at $T_A = 25$ °C | | ± 1 | ± 2 | % |
| $t_{su(HSI)}$ | HSI oscillator start up time | | 1 | | 2 | μs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100 | μA |

1. $V_{DD} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

LSI Low Speed Internal RC Oscillator

Table 25. LSI oscillator characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min ⁽²⁾ | Typ | Max | Unit |
|---------------|----------------------------------|------------|--------------------|------|-----|---------|
| f_{LSI} | Frequency | | 30 | 40 | 60 | kHz |
| $t_{su(LSI)}$ | LSI oscillator startup time | | | | 85 | μs |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 0.65 | 1.2 | μA |

1. $V_{DD} = 3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Value based on device characterization, not tested in production.

Wakeup time from low-power mode

The wakeup times given in [Table 26](#) is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 26. Low-power mode wakeup timings

| Symbol | Parameter | Conditions | Typ | Unit |
|-------------------------------------|---|--|-----|------|
| t _{WUSLEEP} ⁽¹⁾ | Wakeup from Sleep mode | Wakeup on HSI RC clock | 1.8 | μs |
| t _{WUSTOP} ⁽¹⁾ | Wakeup from Stop mode (regulator in run mode) | HSI RC wakeup time = 2 μs | 3.6 | μs |
| | Wakeup from Stop mode (regulator in low power mode) | HSI RC wakeup time = 2 μs, Regulator wakeup from LP mode time = 5 μs | 5.4 | |
| t _{WUSTDBY} ⁽¹⁾ | Wakeup from Standby mode | HSI RC wakeup time = 2 μs, Regulator wakeup from power down time = 38 μs | 50 | μs |

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8

PLL characteristics

The parameters given in [Table 27](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 27. PLL characteristics

| Symbol | Parameter | Test conditions | Value | | | Unit |
|----------------------|-----------------------------|-----------------|-------|-----|--------------------|------|
| | | | Min | Typ | Max ⁽¹⁾ | |
| f _{PLL_IN} | PLL input clock | | | 8.0 | | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| f _{PLL_OUT} | PLL multiplier output clock | | 16 | | 72 | MHz |
| t _{LOCK} | PLL lock time | | | | 200 | μs |

1. Data based on device characterization, not tested in production.



5.3.9 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 28. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max ⁽¹⁾ | Unit |
|-------------|-------------------------|---|-----|------|--------------------|------|
| t_{prog} | 16-bit programming time | $T_A = -40$ to $+105$ °C | 40 | 52.5 | 70 | µs |
| t_{ERASE} | Page (1 KB) erase time | $T_A = -40$ to $+105$ °C | 20 | | 40 | ms |
| t_{ME} | Mass erase time | $T_A = -40$ to $+105$ °C | 20 | | 40 | ms |
| I_{DD} | Supply current | Read mode $f_{HCLK} = 72$ MHz with 2 wait states, $V_{DD} = 3.3$ V | | | 20 | mA |
| | | Write / Erase modes $f_{HCLK} = 72$ MHz, $V_{DD} = 3.3$ V | | | 5 | mA |
| | | Power-down mode / Halt, $V_{DD} = 3.0$ to 3.6 V | | | 50 | µA |
| V_{prog} | Programming voltage | | 2 | | 3.6 | V |

1. Values based on characterization and not tested in production.

Table 29. Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Value | | | Unit |
|-----------|----------------|---|--------------------|-----|-----|---------|
| | | | Min ⁽¹⁾ | Typ | Max | |
| N_{END} | Endurance | $T_A = -40$ to $+85$ °C (6 suffix versions) $T_A = -40$ to $+105$ °C (7 suffix versions) | 10 | | | kcycles |
| t_{RET} | Data retention | $T_A = 85$ °C, 1 kcycle ⁽²⁾ | 30 | | | Years |
| | | $T_A = 105$ °C, 1 kcycle ⁽²⁾ | 10 | | | |
| | | $T_A = 55$ °C, 10 kcycles ⁽²⁾ | 20 | | | |

1. Values based on characterization not tested in production.

2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB: A Burst of Fast Transient voltage** (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 30](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 30. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|------------|---|---|-------------|
| V_{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-2 | 2B |
| V_{ENTB} | Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance | $V_{DD} = 3.3\text{ V}$, $T_A = +25\text{ °C}$, $f_{HCLK} = 48\text{ MHz}$ conforms to IEC 1000-4-4 | 4A |

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 31. EMI characteristics

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [f _{HSE} /f _{HCLK}] | | Unit |
|------------------|------------|--|--------------------------|--|----------|------|
| | | | | 8/48 MHz | 8/72 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.3 V, T _A = 25 °C, LQFP100 package compliant with SAE J 1752/3 | 0.1 to 30 MHz | 12 | 12 | dBµV |
| | | | 30 to 130 MHz | 22 | 19 | |
| | | | 130 MHz to 1GHz | 23 | 29 | |
| | | | SAE EMI Level | 4 | 4 | - |

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Class | Maximum value ⁽¹⁾ | Unit |
|-----------------------|---|---|-------|------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A = +25 °C conforming to JESD22-A114 | 2 | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | T _A = +25 °C conforming to JESD22-C101 | II | 500 | |

1. Values based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 33. Electrical sensitivities

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|--|------------|
| LU | Static latch-up class | T _A = +105 °C conforming to JESD78A | II level A |

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 34](#) are derived from tests performed under the conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

Table 34. I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---|---|-----------------------------|-----|---------------|-----------|
| V_{IL} | Input low level voltage ⁽¹⁾ | TTL ports | -0.5 | | 0.8 | V |
| V_{IH} | Standard IO input high level voltage ⁽¹⁾ | | 2 | | $V_{DD}+0.5$ | |
| | IO FT ⁽²⁾ input high level voltage ⁽¹⁾ | | 2 | | 5.5V | |
| V_{IL} | Input low level voltage ⁽¹⁾ | CMOS ports | -0.5 | | $0.35 V_{DD}$ | V |
| V_{IH} | Input high level voltage ⁽¹⁾ | | $0.65 V_{DD}$ | | $V_{DD}+0.5$ | |
| V_{hys} | Standard IO Schmitt trigger voltage hysteresis ⁽³⁾ | | 200 | | | mV |
| | IO FT Schmitt trigger voltage hysteresis ⁽³⁾ | | $5\% V_{DD}$ ⁽⁴⁾ | | | mV |
| I_{lkg} | Input leakage current ⁽⁵⁾ | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | | | ± 1 | μA |
| | | $V_{IN} = 5 V$ I/O FT | | | 3 | |
| R_{PU} | Weak pull-up equivalent resistor ⁽⁶⁾ | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | $k\Omega$ |
| R_{PD} | Weak pull-down equivalent resistor ⁽⁶⁾ | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | $k\Omega$ |
| C_{IO} | I/O pin capacitance | | | 5 | | pF |

1. Values based on characterization results, and not tested in production.

2. FT = Five-volt tolerant.

3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.

4. With a minimum of 100 mV.

5. Leakage could be higher than max. if negative current is injected on adjacent pins.

6. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 5.2](#):

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating I_{VDD} (see [Table 6](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see [Table 6](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 35](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#). All I/Os are CMOS and TTL compliant.

Table 35. Output voltage characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---|---|--------------|-----|------|
| $V_{OL}^{(1)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | TTL port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | | |
| $V_{OL}^{(1)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | CMOS port $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | 2.4 | | |
| $V_{OL}^{(1)(3)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} < V_{DD} < 3.6 \text{ V}$ | | 1.3 | V |
| $V_{OH}^{(2)(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-1.3$ | | |
| $V_{OL}^{(1)(3)}$ | Output low level voltage for an I/O pin when 8 pins are sunk at same time | $I_{IO} = +6 \text{ mA}$ $2 \text{ V} < V_{DD} < 2.7 \text{ V}$ | | 0.4 | V |
| $V_{OH}^{(2)(3)}$ | Output high level voltage for an I/O pin when 8 pins are sourced at same time | | $V_{DD}-0.4$ | | |

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 6](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 22](#) and [Table 36](#), respectively.

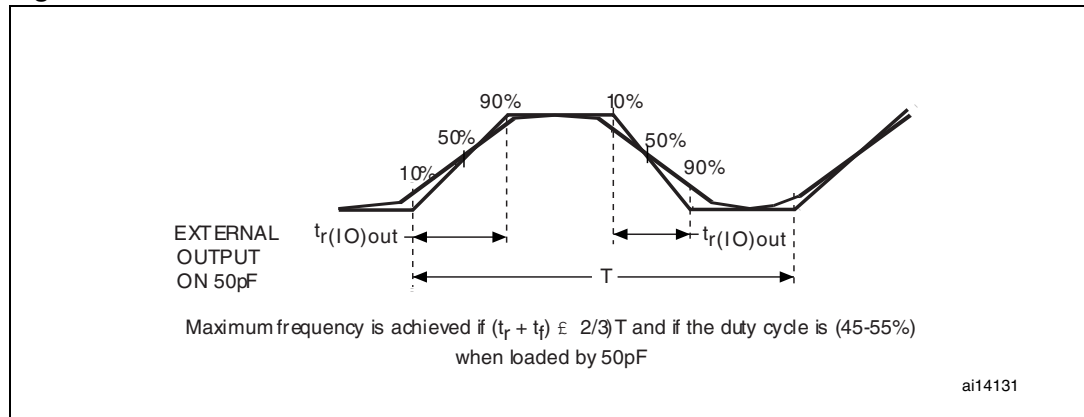
Unless otherwise specified, the parameters given in [Table 36](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 36. I/O AC characteristics⁽¹⁾

| MODEx[1:0] bit value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------------------------|-------------------------|---|--|-----|--------------------|------|
| 10 | f _{max(IO)out} | Maximum frequency ⁽²⁾ | C _L = 50 pF, V _{DD} = 2 V to 3.6 V | | 2 | MHz |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 50 pF, V _{DD} = 2 V to 3.6 V | | 125 ⁽³⁾ | ns |
| | t _{r(IO)out} | Output low to high level rise time | | | 125 ⁽³⁾ | |
| 01 | f _{max(IO)out} | Maximum frequency ⁽²⁾ | C _L = 50 pF, V _{DD} = 2 V to 3.6 V | | 10 | MHz |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 50 pF, V _{DD} = 2 V to 3.6 V | | 25 ⁽³⁾ | ns |
| | t _{r(IO)out} | Output low to high level rise time | | | 25 ⁽³⁾ | |
| 11 | F _{max(IO)out} | Maximum frequency ⁽²⁾ | C _L = 30 pF, V _{DD} = 2.7 V to 3.6 V | | 50 | MHz |
| | | | C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V | | 30 | MHz |
| | | | C _L = 50 pF, V _{DD} = 2 V to 2.7 V | | 20 | MHz |
| | t _{f(IO)out} | Output high to low level fall time | C _L = 30 pF, V _{DD} = 2.7 V to 3.6 V | | 5 ⁽³⁾ | ns |
| | | | C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V | | 8 ⁽³⁾ | |
| | | | C _L = 50 pF, V _{DD} = 2 V to 2.7 V | | 12 ⁽³⁾ | |
| | t _{r(IO)out} | Output low to high level rise time | C _L = 30 pF, V _{DD} = 2.7 V to 3.6 V | | 5 ⁽³⁾ | |
| | | | C _L = 50 pF, V _{DD} = 2.7 V to 3.6 V | | 8 ⁽³⁾ | |
| | | | C _L = 50 pF, V _{DD} = 2 V to 2.7 V | | 12 ⁽³⁾ | |
| - | t _{EXTIpw} | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10x reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in [Figure 22](#).
3. Values based on design simulation and validated on silicon, not tested in production.

Figure 22. I/O AC characteristics definition



5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 34](#)).

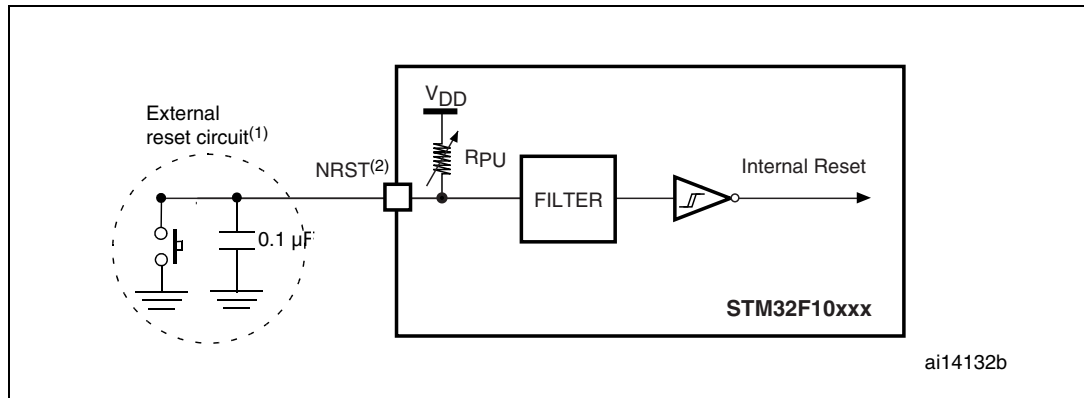
Unless otherwise specified, the parameters given in [Table 37](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 8](#).

Table 37. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|-------------------|------|-----|--------------|-----------|
| $V_{IL(NRST)}$ | NRST Input low level voltage | | -0.5 | | 0.8 | V |
| $V_{IH(NRST)}$ | NRST Input high level voltage | | 2 | | $V_{DD}+0.5$ | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 200 | | |
| R_{PU} | Weak pull-up equivalent resistor ⁽¹⁾ | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | $k\Omega$ |
| $V_{F(NRST)}$ | NRST Input filtered pulse ⁽²⁾ | | | | 100 | ns |
| $V_{NF(NRST)}$ | NRST Input not filtered pulse ⁽²⁾ | | 300 | | | ns |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Values guaranteed by design, not tested in production.

Figure 23. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 37. Otherwise the reset will not be taken into account by the device.

5.3.14 TIM timer characteristics

The parameters given in Table 38 are guaranteed by fabrication.

Refer to Section 5.3.12: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 38. TIMx⁽¹⁾ characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---|--------------------------------|--------|----------------------|---------------|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 72 \text{ MHz}$ | 13.9 | | ns |
| f_{EXT} | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK} = 72 \text{ MHz}$ | 0 | 36 | MHz |
| Res_{TIM} | Timer resolution | | | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 72 \text{ MHz}$ | 0.0139 | 910 | μs |
| t_{MAX_COUNT} | Maximum possible count | | | 65536×65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 72 \text{ MHz}$ | | 59.6 | s |

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.15 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in [Table 39](#) are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in [Table 8](#).

The STM32F103xx performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

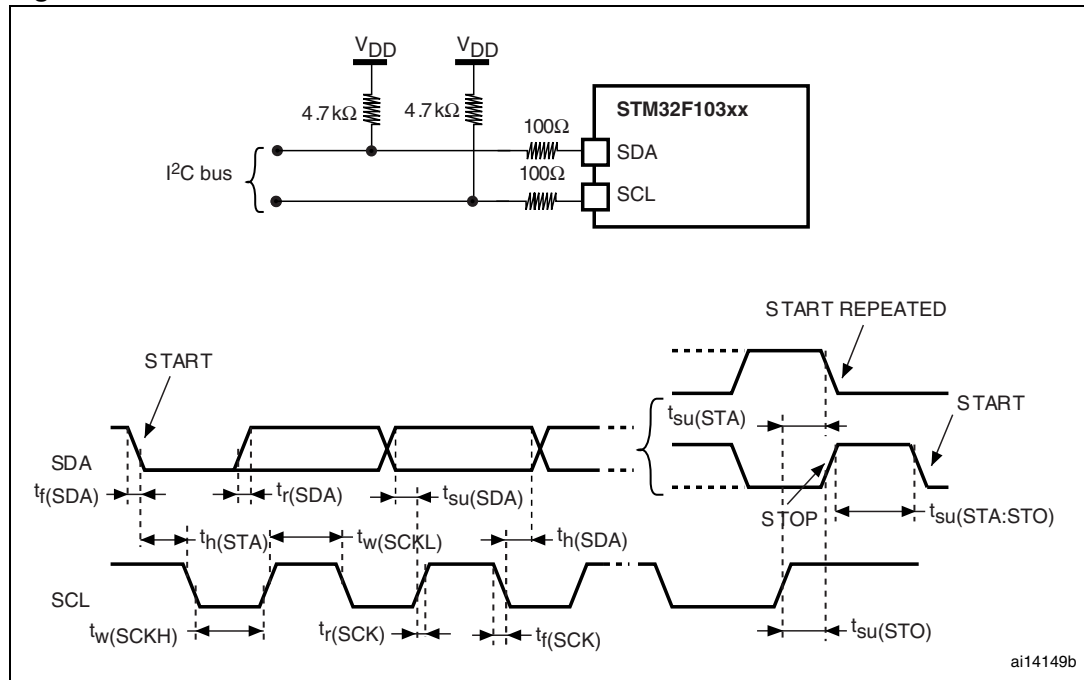
The I²C characteristics are described in [Table 39](#). Refer also to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

Table 39. I²C characteristics

| Symbol | Parameter | Standard mode I ² C ⁽¹⁾ | | Fast mode I ² C ⁽¹⁾⁽²⁾ | | Unit |
|--|---|---|------|--|--------------------|------|
| | | Min | Max | Min | Max | |
| t _{w(SCLL)} | SCL clock low time | 4.7 | | 1.3 | | μs |
| t _{w(SCLH)} | SCL clock high time | 4.0 | | 0.6 | | |
| t _{su(SDA)} | SDA setup time | 250 | | 100 | | ns |
| t _{h(SDA)} | SDA data hold time | 0 ⁽³⁾ | | 0 ⁽⁴⁾ | 900 ⁽³⁾ | |
| t _{r(SDA)} t _{r(SCL)} | SDA and SCL rise time | | 1000 | 20 + 0.1C _b | 300 | |
| t _{f(SDA)} t _{f(SCL)} | SDA and SCL fall time | | 300 | 20 + 0.1C _b | 300 | |
| t _{h(STA)} | Start condition hold time | 4.0 | | 0.6 | | |
| t _{su(STA)} | Repeated Start condition setup time | 4.7 | | 0.6 | | μs |
| t _{su(STO)} | Stop condition setup time | 4.0 | | 0.6 | | μs |
| t _{w(STO:STA)} | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | μs |
| C _b | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Values based on standard I²C protocol requirement, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 24. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 40. SCL frequency ($f_{PCLK1} = 36 \text{ MHz}, V_{DD} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

| $f_{SCL} \text{ (kHz)}$ | I2C_CCR value |
|-------------------------|-----------------------------|
| | $R_p = 4.7 \text{ k}\Omega$ |
| 400 | 0x801E |
| 300 | 0x8028 |
| 200 | 0x803C |
| 100 | 0x00B4 |
| 50 | 0x0168 |
| 20 | 0x0384 |

- R_p = External pull-up resistance, f_{SCL} = I²C speed,
- For speeds around 200 kHz, the tolerance on the achieved speed is of $\pm 5\%$. For other speed ranges, the tolerance on the achieved speed $\pm 2\%$. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 41](#) are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 8](#).

Refer to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 41. SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|--------------------------------------|--|--------------|--------------|------|
| f_{SCK} $1/t_c(SCK)$ | SPI clock frequency | Master mode | 0 | 18 | MHz |
| | | Slave mode | 0 | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | | 8 | ns |
| $t_{su(NSS)}^{(2)}$ | NSS setup time | Slave mode | $4 t_{PCLK}$ | | |
| $t_h(NSS)^{(2)}$ | NSS hold time | Slave mode | 18 | | |
| $t_w(SCKH)^{(2)}$ $t_w(SCKL)^{(2)}$ | SCK high and low time | Master mode, $f_{PCLK} = 36$ MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}^{(2)}$ | Data input setup time Master mode | SPI1 | 1 | | |
| | | SPI2 | 5 | | |
| $t_{su(SI)}^{(2)}$ | Data input setup time Slave mode | | 1 | | |
| $t_{h(MI)}^{(2)}$ | Data input hold time Master mode | SPI1 | 1 | | |
| | | SPI2 | 5 | | |
| $t_h(SI)^{(2)}$ | Data input hold time Slave mode | | 3 | | |
| $t_a(SO)^{(2)(3)}$ | Data output access time | Slave mode, $f_{PCLK} = 36$ MHz, presc = 4 | 0 | 55 | |
| | | Slave mode, $f_{PCLK} = 24$ MHz | 0 | $4 t_{PCLK}$ | |
| $t_{dis(SO)}^{(2)(4)}$ | Data output disable time | Slave mode | 10 | | |
| $t_v(SO)^{(2)(1)}$ | Data output valid time | Slave mode (after enable edge) | | 25 | |
| $t_v(MO)^{(2)(1)}$ | Data output valid time | Master mode (after enable edge) | | 3 | |
| $t_h(SO)^{(2)}$ | Data output hold time | Slave mode (after enable edge) | 25 | | |
| $t_h(MO)^{(2)}$ | | Master mode (after enable edge) | 4 | | |

1. Remapped SPI1 characteristics to be determined.
2. Values based on design simulation and/or characterization results, and not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 25. SPI timing diagram - slave mode and CPHA = 0

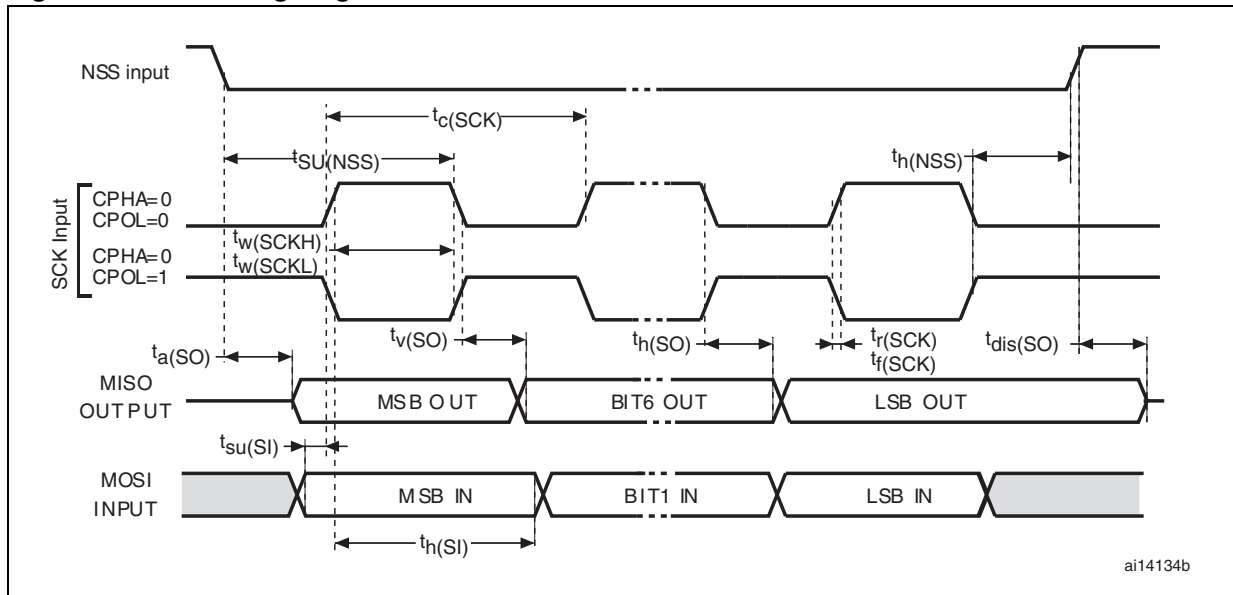
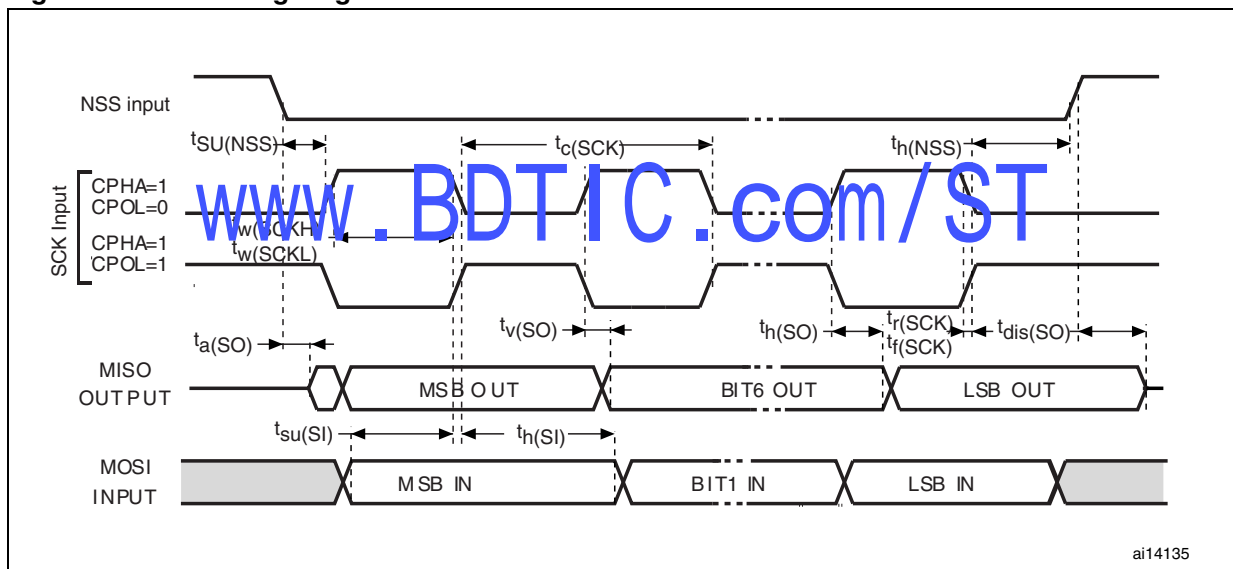
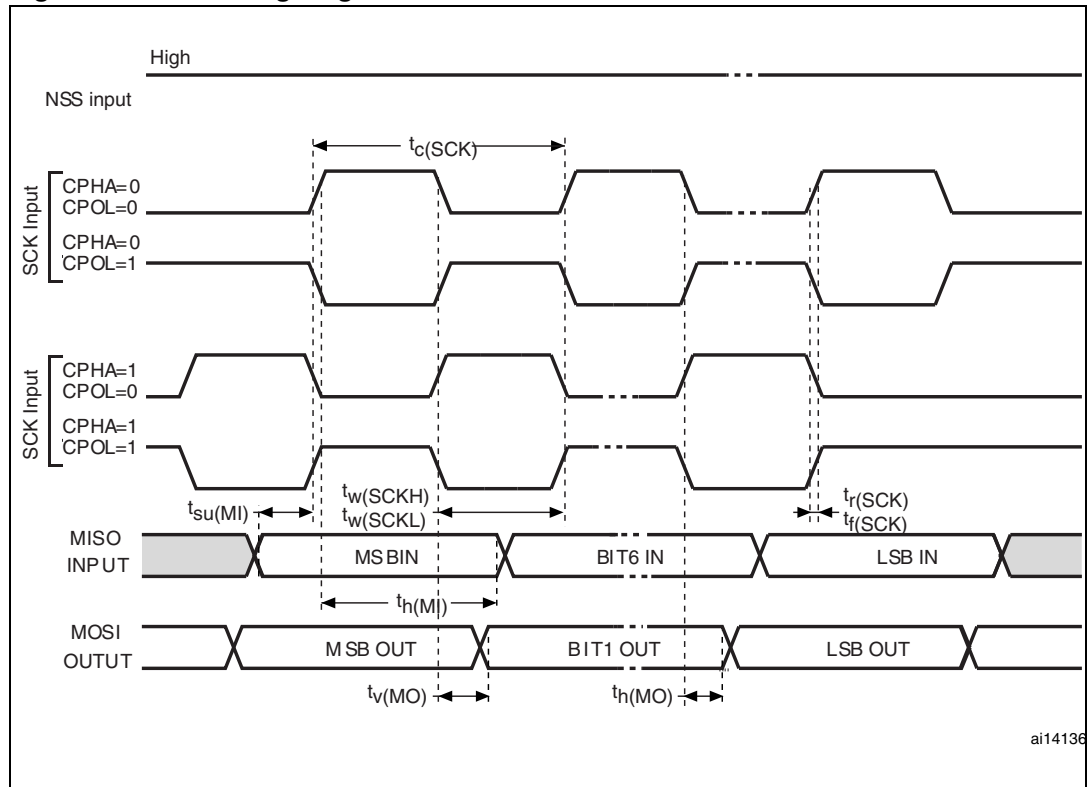


Figure 26. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Figure 27. SPI timing diagram - master mode⁽¹⁾



1. Measurement points are done at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 42. USB startup time

| Symbol | Parameter | Max | Unit |
|----------------------|------------------------------|-----|------|
| t _{STARTUP} | USB transceiver startup time | 1 | μs |

Table 43. USB DC electrical characteristics

| Symbol | Parameter | Conditions | Min. ⁽¹⁾ | Max. ⁽¹⁾ | Unit |
|----------------------|---------------------------------|---|---------------------|---------------------|------|
| Input levels | | | | | |
| V _{USB} | USB voltage ⁽²⁾ | Within V _{DD} voltage range | 3.0 ⁽³⁾ | 3.6 | V |
| V _{DI} | Differential input sensitivity | I(USBDP, USBDM) | 0.2 | | V |
| V _{CM} | Differential common mode range | Includes V _{DI} range | 0.8 | 2.5 | |
| V _{SE} | Single ended receiver threshold | | 1.3 | 2.0 | |
| Output levels | | | | | |
| V _{OL} | Static output level low | R _L of 1.5 kΩ to 3.6 V ⁽⁴⁾ | | 0.3 | V |
| V _{OH} | Static output level high | R _L of 15 kΩ to V _{SS} ⁽⁴⁾ | 2.8 | 3.6 | |

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F103xx USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. R_L is the load connected on the USB drivers

Figure 28. USB timings: definition of data signal rise and fall time

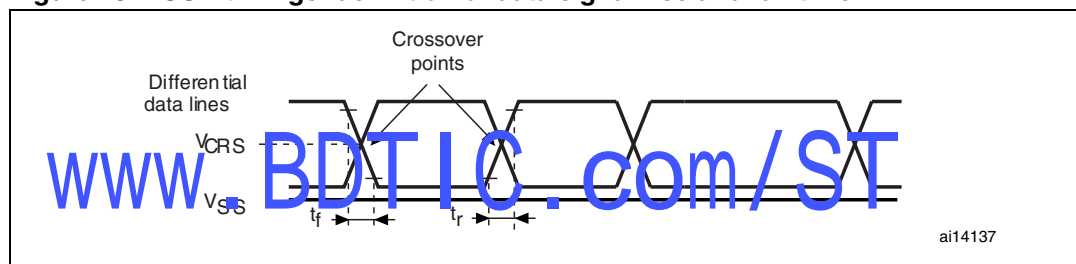


Table 44. USB: Full-speed electrical characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------------------|---------------------------------|--------------------------------|-----|-----|------|
| Driver characteristics | | | | | |
| t _r | Rise time ⁽¹⁾ | C _L = 50 pF | 4 | 20 | ns |
| t _f | Fall time ⁽¹⁾ | C _L = 50 pF | 4 | 20 | ns |
| t _{rfm} | Rise/ fall time matching | t _r /t _f | 90 | 110 | % |
| V _{CRS} | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

5.3.16 CAN (controller area network) interface

Refer to [Section 5.3.12: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 45](#) are derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 8](#).

Note: It is recommended to perform a calibration after each power-up.

Table 45. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|--------------------|--|--------------------|--------------------|-------------|
| V_{DDA} | ADC power supply | | 2.4 | | 3.6 | V |
| V_{REF+} | Positive reference voltage | | 2.4 | | V_{DDA} | V |
| I_{VREF} | Current on the V_{REF} input pin | | | 160 ⁽¹⁾ | 220 ⁽¹⁾ | μ A |
| f_{ADC} | ADC clock frequency | | 0.6 | | 14 | MHz |
| $f_S^{(2)}$ | Sampling rate | | 0.05 | | 1 | MHz |
| $f_{TRIG}^{(2)}$ | External trigger frequency | $f_{ADC} = 14$ MHz | | | 823 | kHz |
| | | | | | 17 | $1/f_{ADC}$ |
| V_{AIN} | Conversion voltage range ⁽³⁾ | | 0 (V_{SSA} or V_{REF-} tied to ground) | | V_{REF+} | V |
| $R_{AIN}^{(2)}$ | External input impedance | | See Equation 1 and Table 46 | | | k Ω |
| $R_{ADC}^{(2)}$ | Sampling switch resistance | | | | 1 | k Ω |
| $C_{ADC}^{(2)}$ | Internal sample and hold capacitor | | | | 5 | pF |
| $t_{CAL}^{(2)}$ | Calibration time | $f_{ADC} = 14$ MHz | 5.9 | | | μ s |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{lat}^{(2)}$ | Injection trigger conversion latency | $f_{ADC} = 14$ MHz | | | 0.214 | μ s |
| | | | | | 3 ⁽⁴⁾ | $1/f_{ADC}$ |
| $t_{latr}^{(2)}$ | Regular trigger conversion latency | $f_{ADC} = 14$ MHz | | | 0.143 | μ s |
| | | | | | 2 ⁽⁴⁾ | $1/f_{ADC}$ |
| $t_S^{(2)}$ | Sampling time | $f_{ADC} = 14$ MHz | 0.107 | | 17.1 | μ s |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}^{(2)}$ | Power-up time | | 0 | 0 | 1 | μ s |
| $t_{CONV}^{(2)}$ | Total conversion time (including sampling time) | $f_{ADC} = 14$ MHz | 1 | | 18 | μ s |
| | | | 14 to 252 (t_S for sampling +12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Data based on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA} , depending on the package. Refer to [Section 3: Pin descriptions](#) for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 45](#).

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 46. R_{AIN} max for f_{ADC} = 14 MHz⁽¹⁾

| T _s (cycles) | t _s (μs) | R _{AIN} max (kΩ) |
|-------------------------|---------------------|---------------------------|
| 1.5 | 0.11 | 1.2 |
| 7.5 | 0.54 | 10 |
| 13.5 | 0.96 | 19 |
| 28.5 | 2.04 | 41 |
| 41.5 | 2.96 | 60 |
| 55.5 | 3.96 | 80 |
| 71.5 | 5.11 | 104 |
| 239.5 | 17.1 | 350 |

1. Data guaranteed by design, not tested in production.

Table 47. ADC accuracy - limited test conditions⁽¹⁾

| Symbol | Parameter | Test conditions | Typ | Max ⁽²⁾ | Unit |
|--------|---|--|------|--------------------|------|
| ET | Total unadjusted error ⁽³⁾ | PCLK2 = 56 MHz, f _{ADC} = 14 MHz, R _{AIN} = 10 kΩ, V _{DDA} = 3 V to 3.6 V T _A = 25 °C Measurements made after ADC calibration V _{REF+} = V _{DDA} | ±1.3 | ±2 | LSB |
| EC | Offset error ⁽³⁾ | | ±1 | ±1.5 | |
| EG | Gain error ⁽³⁾ | | ±0.5 | ±1.5 | |
| ED | Differential linearity error ⁽³⁾ | | ±0.7 | ±1 | |
| EL | Integral linearity error ⁽³⁾ | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. Data based on characterization, not tested in production.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in [Section 5.3.12](#) does not affect the ADC accuracy.

Table 48. ADC accuracy^{(1) (2)}

| Symbol | Parameter | Test conditions | Typ | Max ⁽³⁾ | Unit |
|--------|---|--|-----------|--------------------|------|
| ET | Total unadjusted error ⁽⁴⁾ | $f_{PCLK2} = 56 \text{ MHz}$, $f_{ADC} = 14 \text{ MHz}$, $R_{AIN} < 10 \text{ k}\Omega$ $V_{DDA} = 2.4 \text{ V to } 3.6 \text{ V}$ Measurements made after ADC calibration | ± 2 | ± 5 | LSB |
| EO | Offset error ⁽³⁾ | | ± 1.5 | ± 2.5 | |
| EG | Gain error ⁽³⁾ | | ± 1.5 | ± 3 | |
| ED | Differential linearity error ⁽³⁾ | | ± 1 | ± 2 | |
| EL | Integral linearity error ⁽³⁾ | | ± 1.5 | ± 3 | |

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD} , frequency, V_{REF} and temperature ranges.
3. Data based on characterization, not tested in production.
4. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.

Figure 29. ADC accuracy characteristics

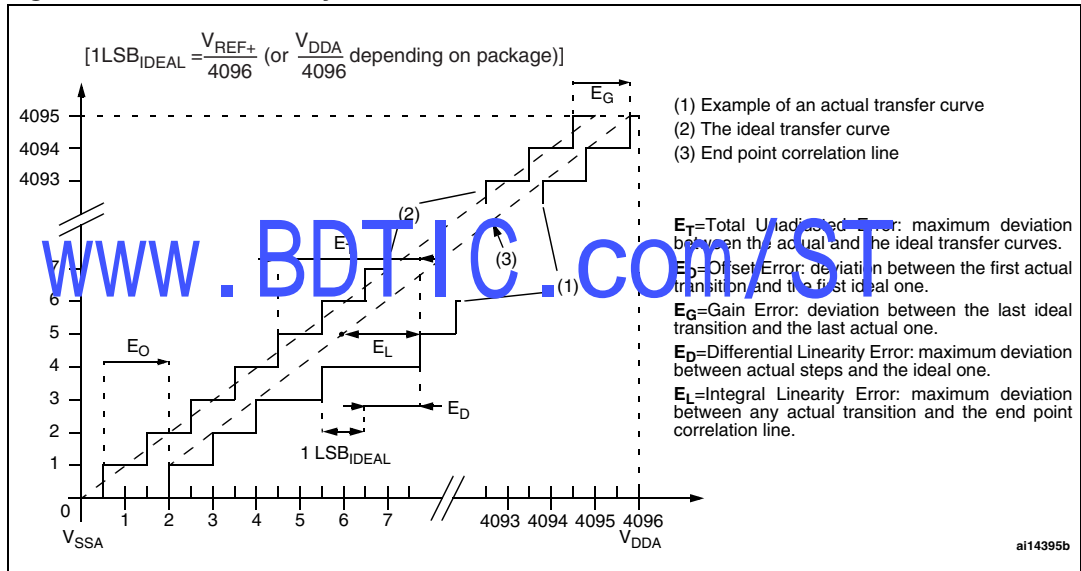
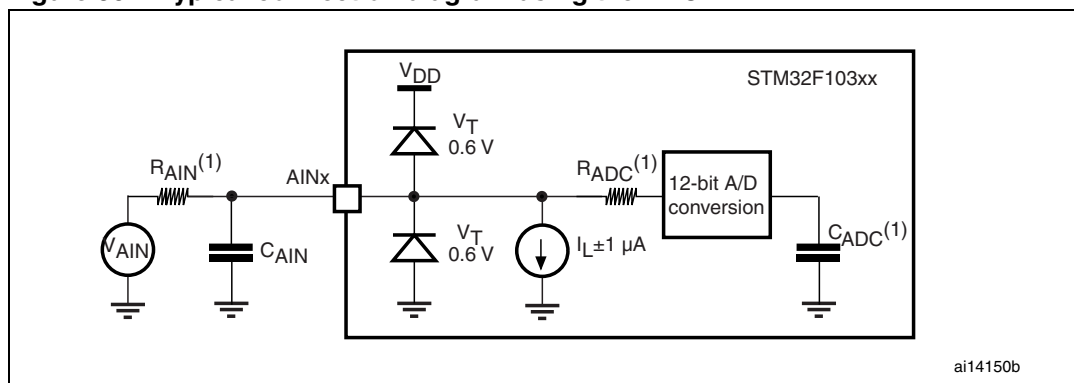


Figure 30. Typical connection diagram using the ADC

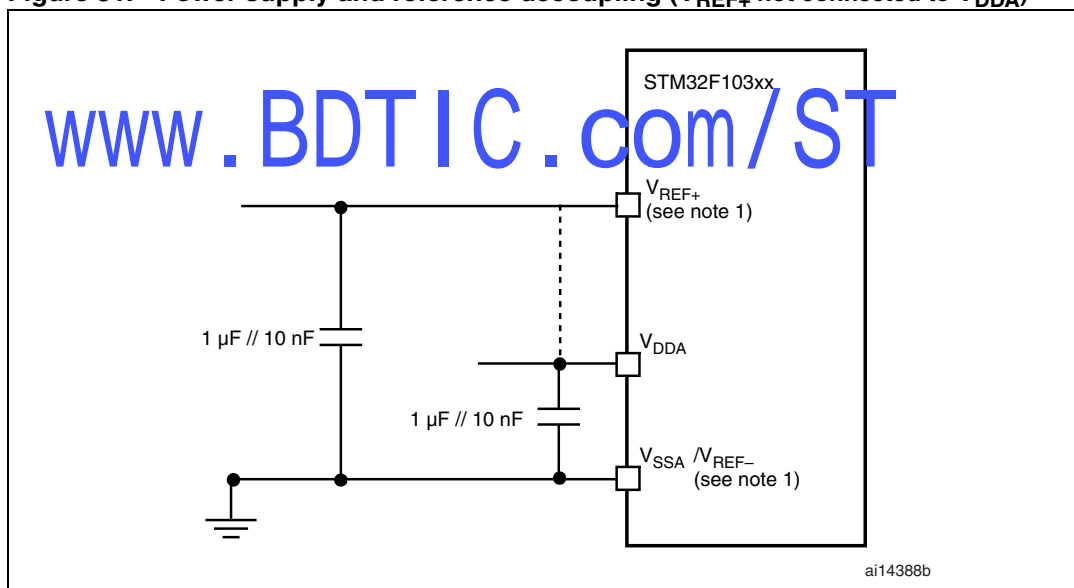


1. Refer to [Table 45](#) for the values of C_{AIN} , R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{PARASITIC}$ must be added to C_{AIN} . It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{PARASITIC}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

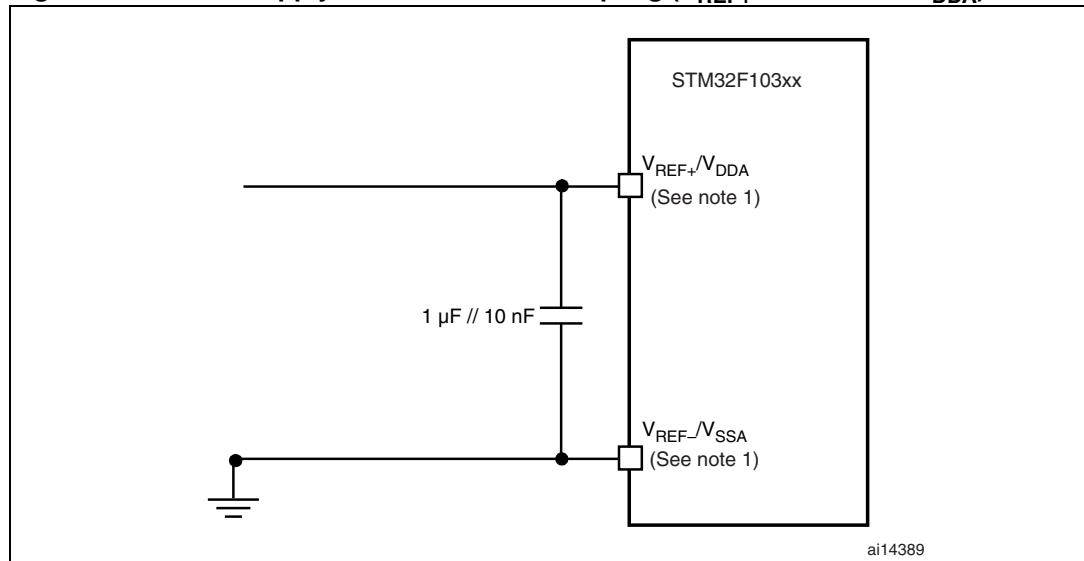
Power supply decoupling should be performed as shown in [Figure 31](#) or [Figure 32](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 31. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 32. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.18 Temperature sensor characteristics

Table 49. TS characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|------------|------|---------|---------|-----------------|
| $T_L^{(1)}$ | V_{SENSE} linearity with temperature | | | ± 1 | ± 2 | $^{\circ}C$ |
| $AV_{0_Slope}^{(1)}$ | Average slope | | 4.0 | 4.3 | 4.6 | mV/ $^{\circ}C$ |
| $V_{25}^{(1)}$ | Voltage at 25 $^{\circ}C$ | | 1.34 | 1.43 | 1.52 | V |
| $t_{START}^{(2)}$ | Startup time | | 4 | | 10 | μs |
| $T_{S_temp}^{(3)(2)}$ | ADC sampling time when reading the temperature | | | 2.2 | 17.1 | μs |

1. Guaranteed by characterization, not tested in production.
2. Data guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

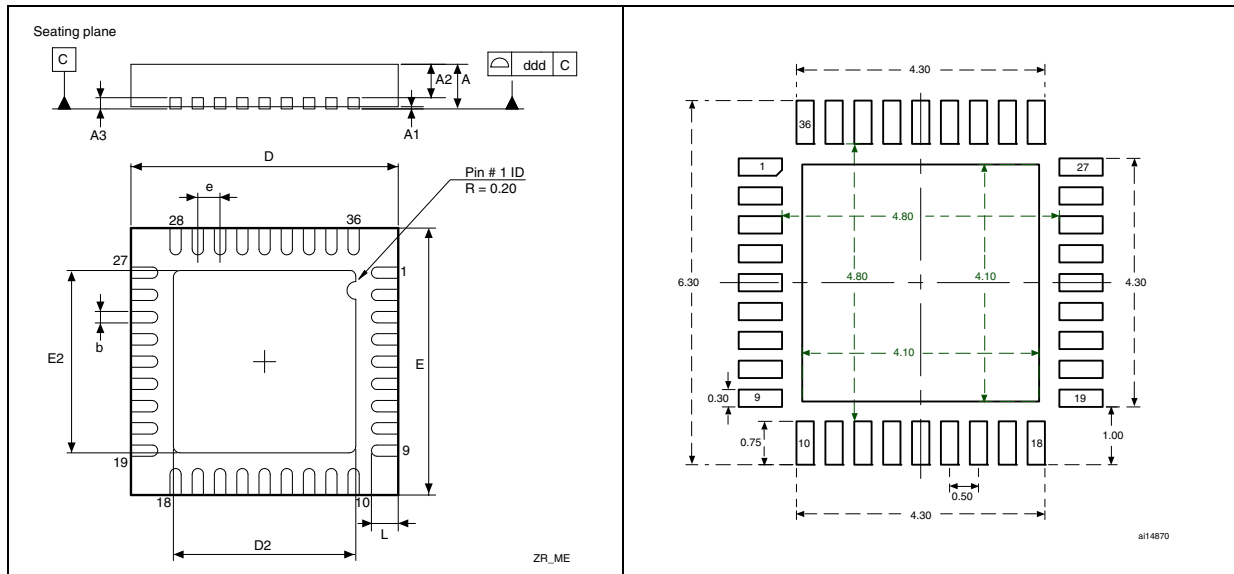
6.1 Package mechanical data

In order to meet environmental requirements, ST offers the STM32F103xx in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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Figure 33. VFQFPN36 6 x 6 mm, 0.5 mm pitch, Figure 34. Recommended footprint (dimensions in mm)⁽¹⁾⁽²⁾⁽³⁾



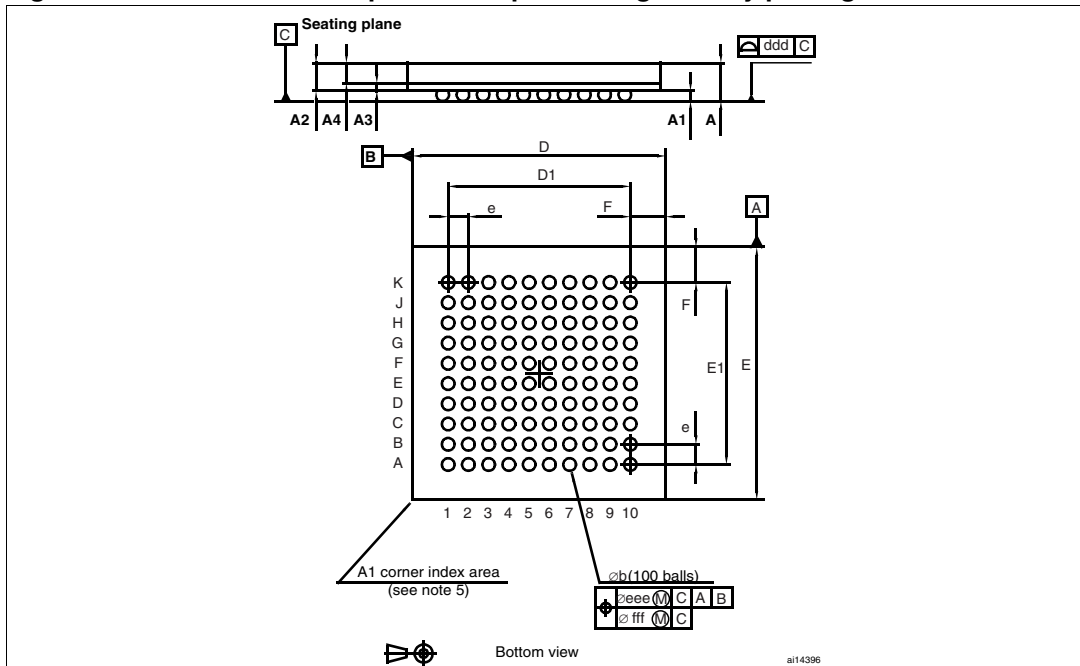
1. Drawing is not to scale.
2. The back-side pad is not internally connected to the V_{SS} or V_{DD} power pads.
3. There is an exposed die pad on the underside of the VFQFPN package. It should be soldered to the PCB. All leads should also be soldered to the PCB.

Table 50. VFQFPN36 6 x 6 mm, 0.5 mm pitch, package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.800 | 0.900 | 1.000 | 0.0315 | 0.0354 | 0.0394 |
| A1 | | 0.020 | 0.050 | | 0.0008 | 0.0020 |
| A2 | | 0.650 | 1.000 | | 0.0256 | 0.0394 |
| A3 | | 0.250 | | | 0.0098 | |
| b | 0.180 | 0.230 | 0.300 | 0.0071 | 0.0091 | 0.0118 |
| D | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| D2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| E | 5.875 | 6.000 | 6.125 | 0.2313 | 0.2362 | 0.2411 |
| E2 | 1.750 | 3.700 | 4.250 | 0.0689 | 0.1457 | 0.1673 |
| e | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| L | 0.350 | 0.550 | 0.750 | 0.0138 | 0.0217 | 0.0295 |
| ddd | | 0.080 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. LFBGA100 - low profile fine pitch ball grid array package outline



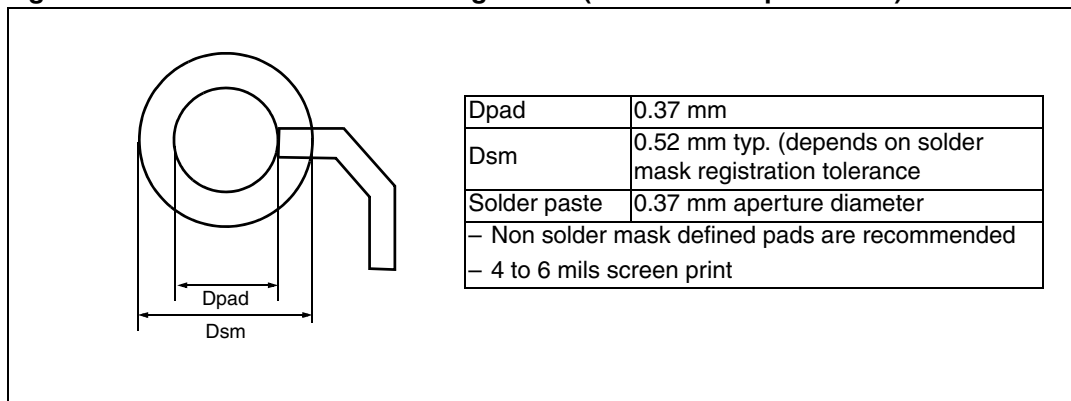
1. Drawing is not to scale.

Table 51. LFBGA100 - low profile fine pitch ball grid array package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|---------------------|-------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.700 | | | 0.0669 |
| A1 | 0.270 | | | 0.0106 | | |
| A2 | | 1.085 | | 0.0427 | | |
| A3 | | 0.30 | | 0.0118 | | |
| A4 | | | 0.80 | | | 0.0315 |
| b | 0.45 | 0.50 | 0.55 | 0.0177 | 0.0197 | 0.0217 |
| D | 9.85 | 10.00 | 10.15 | 0.3878 | 0.3937 | 0.3996 |
| D1 | | 7.20 | | 0.2835 | | |
| E | 9.85 | 10.00 | 10.15 | 0.3878 | 0.3937 | 0.3996 |
| E1 | | 7.20 | | 0.2835 | | |
| e | | 0.80 | | 0.0315 | | |
| F | | 1.40 | | 0.0551 | | |
| ddd | | | 0.12 | | | 0.0047 |
| eee | | | 0.15 | | | 0.0059 |
| fff | | | 0.08 | | | 0.0031 |
| N (number of balls) | 100 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

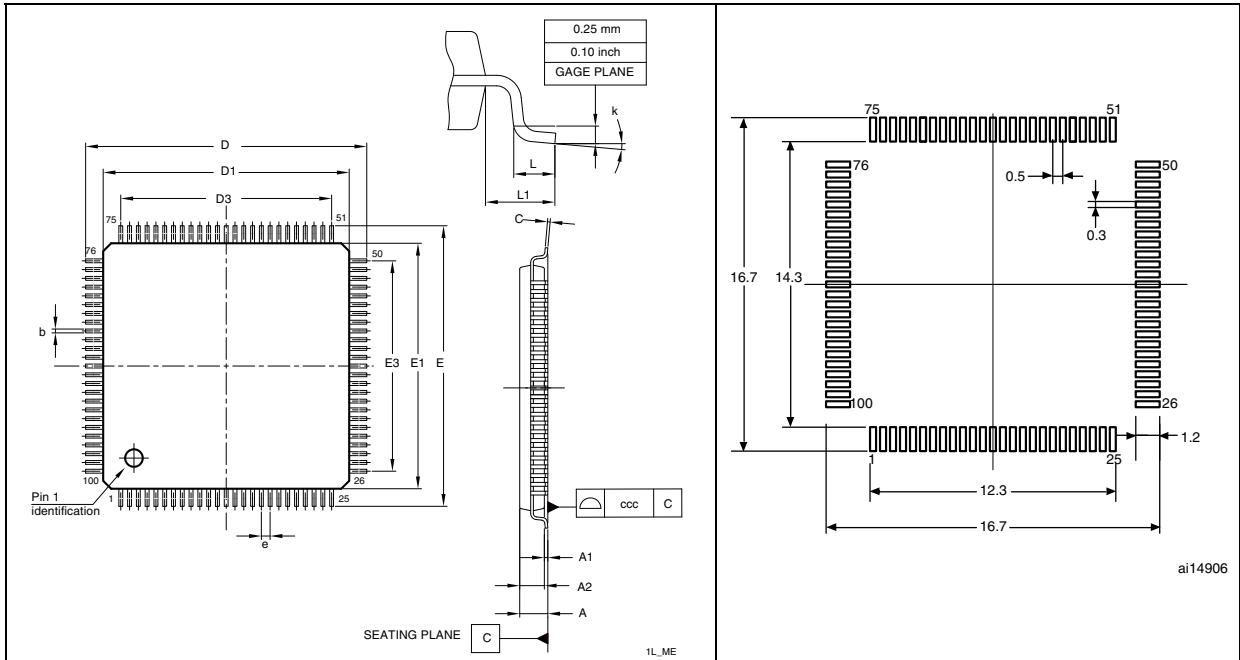
Figure 36. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



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Figure 37. LQFP100, 100-pin low-profile quad flat package outline⁽¹⁾

Figure 38. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 52. LQFP100, 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|------|------|-----------------------|--------|--------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.6 | | | 0.063 |
| A1 | | 0.05 | 0.15 | | 0.002 | 0.0059 |
| A2 | 1.4 | 1.35 | 1.45 | 0.0551 | 0.0531 | 0.0571 |
| b | 0.22 | 0.17 | 0.27 | 0.0087 | 0.0067 | 0.0106 |
| c | | 0.09 | 0.2 | | 0.0035 | 0.0079 |
| D | 16 | 15.8 | 16.2 | 0.6299 | 0.622 | 0.6378 |
| D1 | 14 | 13.8 | 14.2 | 0.5512 | 0.5433 | 0.5591 |
| D3 | 12 | | | 0.4724 | | |
| E | 16 | 15.8 | 16.2 | 0.6299 | 0.622 | 0.6378 |
| E1 | 14 | 13.8 | 14.2 | 0.5512 | 0.5433 | 0.5591 |
| E3 | 12 | | | 0.4724 | | |
| e | 0.5 | | | 0.0197 | | |
| L | 0.6 | 0.45 | 0.75 | 0.0236 | 0.0177 | 0.0295 |
| L1 | 1 | | | 0.0394 | | |
| k | 3.5° | 0.0° | 7.0° | 3.5° | 0.0° | 7.0° |
| ccc | | 0.08 | | | 0.0031 | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP64, 64-pin low-profile quad flat package outline⁽¹⁾

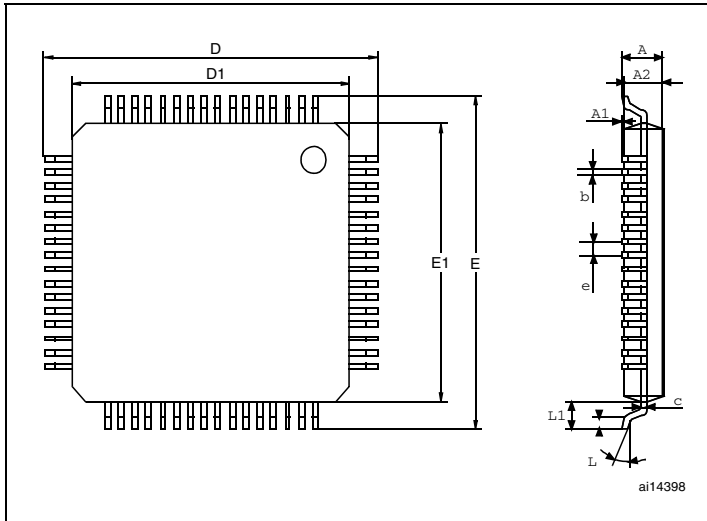
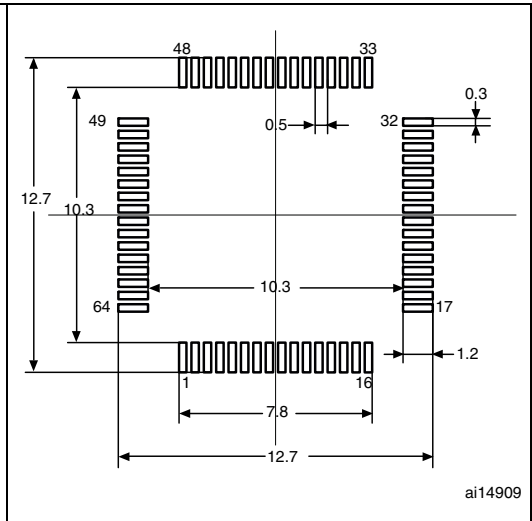


Figure 40. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 53. LQFP64, 64-pin low-profile quad flat package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|-------|------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.0630 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | | 12.00 | | | 0.4724 | |
| D1 | | 10.00 | | | 0.3937 | |
| E | | 12.00 | | | 0.4724 | |
| E1 | | 10.00 | | | 0.3937 | |
| e | | 0.50 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| N | Number of pins | | | | | |
| | 64 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 41. LQFP48, 48-pin low-profile quad flat package outline⁽¹⁾

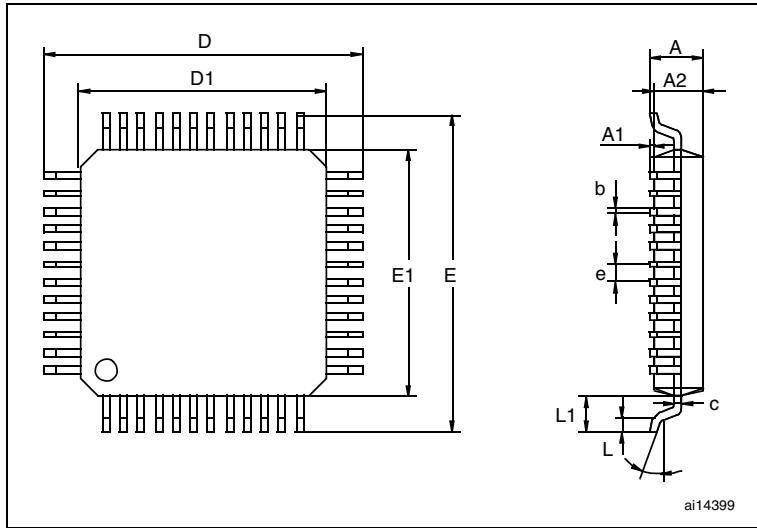
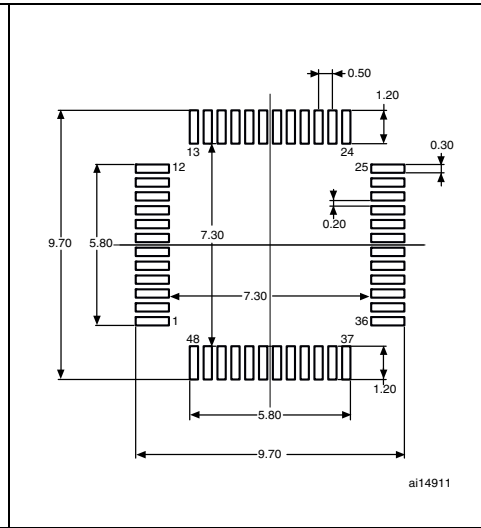


Figure 42. Recommended footprint⁽¹⁾⁽²⁾



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 54. LQFP48, 48-pin low-profile quad flat package mechanical data

| Dim. | mm | | | inches ⁽¹⁾ | | |
|------|----------------|------|------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.60 | | | 0.0630 |
| A1 | 0.05 | | 0.15 | 0.0020 | | 0.0059 |
| A2 | 1.35 | 1.40 | 1.45 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.17 | 0.22 | 0.27 | 0.0067 | 0.0087 | 0.0106 |
| C | 0.09 | | 0.20 | 0.0035 | | 0.0079 |
| D | | 9.00 | | | 0.3543 | |
| D1 | | 7.00 | | | 0.2756 | |
| E | | 9.00 | | | 0.3543 | |
| E1 | | 7.00 | | | 0.2756 | |
| e | | 0.50 | | | 0.0197 | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.45 | 0.60 | 0.75 | 0.0177 | 0.0236 | 0.0295 |
| L1 | | 1.00 | | | 0.0394 | |
| N | Number of pins | | | | | |
| | 48 | | | | | |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6.2 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 8: General operating conditions on page 32](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 55. Thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient LFBGA100 - 10 x 10 mm / 0.5 mm pitch | 41 | °C/W |
| | Thermal resistance junction-ambient LQFP100 - 14 x 14 mm / 0.5 mm pitch | 46 | |
| | Thermal Resistance Junction-Ambient LQFP64 - 10 x 10 mm / 0.5 mm pitch | 45 | |
| | Thermal resistance junction-ambient LQFP48 - 7 x 7 mm / 0.5 mm pitch | 55 | |
| | Thermal resistance junction-ambient VFQFPN 36 - 6 x 6 mm / 0.5 mm pitch | 18 | |

6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

6.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Table 56: Ordering information scheme](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Thus: $P_{Dmax} = 464\text{ mW}$

Using the values obtained in [Table 5](#), T_{Jmax} is calculated as follows.

For LQFP100, 46 °C/W

$$T_{Jmax} = 82\text{ °C} + (46\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.6\text{ °C} = 102.6\text{ °C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Table 56: Ordering information scheme](#)).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 115\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 55](#) T_{Jmax} is calculated as follows:

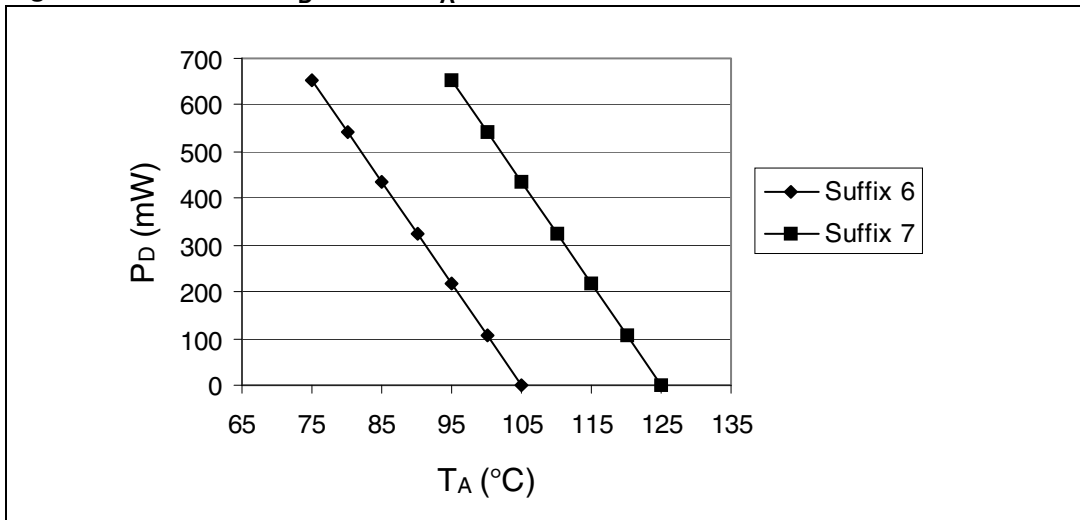
– For LQFP100, 46 °C/W

$$T_{Jmax} = 115\text{ °C} + (46\text{ °C/W} \times 134\text{ mW}) = 115\text{ °C} + 6.2\text{ °C} = 121.2\text{ °C}$$

This is within the range of the suffix 7 version parts ($-40 < T_J < 125\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Table 56: Ordering information scheme](#)).

Figure 43. LQFP100 P_D max vs. T_A



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7 Ordering information scheme

Table 56. Ordering information scheme

| | | | | | | | | |
|---|-------|---|-----|---|---|---|---|-----|
| Example: | STM32 | F | 103 | C | 6 | T | 7 | xxx |
| Device family STM32 = ARM-based 32-bit microcontroller | | | | | | | | |
| Product type F = general-purpose | | | | | | | | |
| Device subfamily 103 = performance line | | | | | | | | |
| Pin count T = 36 pins C = 48 pins R = 64 pins V = 100 pins | | | | | | | | |
| Flash memory size 6 = 32 Kbytes of Flash memory 8 = 64 Kbytes of Flash memory B = 128 Kbytes of Flash memory | | | | | | | | |
| Package H = BGA T = LQFP U = VFQFPN | | | | | | | | |
| Temperature range 6 = Industrial temperature range, -40 to 85 °C. 7 = Industrial temperature range, -40 to 105 °C. | | | | | | | | |
| Options xxx = programmed parts with 64 or 128 Kbytes of Flash memory Axx = programmable parts with 32 Kbytes of Flash memory TR = tape and reel | | | | | | | | |

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7.1 Future family enhancements

Further developments of the STM32F103xx performance line will see an expansion of the current options. Larger packages will soon be available with up to 512 KB Flash, 64 KB SRAM and with extended features such as flexible static memory controller (FSMC) support, SDIO, I²S, DAC and additional timers and USARTS.

8 Revision history

Table 57. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 01-jun-2007 | 1 | Initial release. |
| 20-Jul-2007 | 2 | <p>Flash memory size modified in Note 6, Note 4, Note 7, Note 8 and BGA100 pins added to Table 4: Pin definitions. Figure 3: STM32F103xx performance line BGA100 ballout added.</p> <p>T_{HSE} changed to T_{LSE} in Figure 19: Low-speed external clock source AC timing diagram. V_{BAT} ranged modified in Power supply schemes.</p> <p>$t_{SU(LSE)}$ changed to $t_{SU(HSE)}$ in Table 22: HSE 4-16 MHz oscillator characteristics. $I_{DD(HSI)}$ max value added to Table 24: HSI oscillator characteristics.</p> <p>Sample size modified and machine model removed in Electrostatic discharge (ESD).</p> <p>Number of parts modified and standard reference updated in Static latch-up. 25 °C and 85 °C conditions removed and class name modified in Table 33: Electrical sensitivities. R_{PU} and R_{PD} min and max values added to Table 34: I/O static characteristics. R_{PU} min and max values added to Table 37: NRST pin characteristics.</p> <p>Figure 24: I2C bus AC waveforms and measurement circuit and Figure 23: Recommended NRST pin protection corrected.</p> <p>Notes removed below Table 8, Table 37, Table 43.</p> <p>I_{DD} typical values changed in Table 11: Maximum current consumption in Run and Sleep modes, Table 38: TIMx characteristics modified.</p> <p>t_{STAB}, V_{REF} value, t_{lat} and f_{PIG} added to Table 45: ADC characteristics.</p> <p>In Table 29: Flash memory endurance and data retention, typical endurance and data retention for $T_A = 85$ °C added, data retention for $T_A = 25$ °C removed.</p> <p>V_{BG} changed to V_{REFINT} in Table 11: Embedded internal reference voltage. Document title changed. Controller area network (CAN) section modified.</p> <p>Figure 11: Power supply scheme modified.</p> <p>Features on page 1 list optimized. Small text changes.</p> |

Table 57. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|--|
| 18-Oct-2007 | 3 | <p>STM32F103CBT6, STM32F103T6 and STM32F103T8 root part numbers added (see Table 2: Device features and peripheral counts (STM32F103xx Medium-density performance line))</p> <p>VFQFPN36 package added (see Section 6: Package characteristics). All packages are ECOPACK® compliant. Package mechanical data inch values are calculated from mm and rounded to 4 decimal digits (see Section 6: Package characteristics).</p> <p>Table 4: Pin definitions updated and clarified.</p> <p>Table 26: Low-power mode wakeup timings updated.</p> <p>T_A min corrected in Table 11: Embedded internal reference voltage.</p> <p>Note 4 added below Table 22: HSE 4-16 MHz oscillator characteristics.</p> <p>$V_{ESD(CDM)}$ value added to Table 32: ESD absolute maximum ratings.</p> <p>Note 3 added and V_{OH} parameter description modified in Table 35: Output voltage characteristics.</p> <p>Note 1 modified under Table 36: I/O AC characteristics.</p> <p>Equation 1 and Table 46: RAIN max for fADC = 14 MHz added to Section 5.3.17: 12-bit ADC characteristics.</p> <p>V_{AIN}, t_S max, t_{CONV}, V_{REF+} min and t_{lat} max modified, notes modified and t_{latr} added in Table 45: ADC characteristics.</p> <p>Figure 29: ADC accuracy characteristics updated. Note 1 modified below Figure 30: Typical connection diagram using the ADC.</p> <p>Electrostatic discharge (ESD) on page 51 modified.</p> <p>Number of TIM4 channels modified in Figure 1: STM32F103xx performance line block diagram.</p> <p>Maximum current consumption Table 12, Table 13 and Table 14 updated. V_{YS} modified in Table 34: I/O static characteristics.</p> <p>Table 18: ADC accuracy updated. t_{VDD} modified in Table 9: Operating conditions at power-up / power-down. V_{FESD} value added in Table 30: EMS characteristics.</p> <p>Values corrected, note 2 modified and note 3 removed in Table 26: Low-power mode wakeup timings.</p> <p>Table 15: Typical and maximum current consumptions in Stop and Standby modes: Typical values added for $V_{DD}/V_{BAT} = 2.4$ V, Note 4 modified, Note 2 added.</p> <p>Table 18: Typical current consumption in Standby mode added. On-chip peripheral current consumption on page 42 added.</p> <p>ACC_{HSI} values updated in Table 24: HSI oscillator characteristics.</p> <p>V_{prog} added to Table 28: Flash memory characteristics.</p> <p>Upper option byte address modified in Figure 8: Memory map.</p> <p>Typical f_{LSI} value added in Table 25: LSI oscillator characteristics and internal RC value corrected from 32 to 40 kHz in entire document.</p> <p>T_{S_temp} added to Table 49: TS characteristics. N_{END} modified in Table 29: Flash memory endurance and data retention.</p> <p>$T_{S_vrefint}$ added to Table 11: Embedded internal reference voltage.</p> <p>Handling of unused pins specified in General input/output characteristics on page 52. All I/Os are CMOS and TTL compliant.</p> <p>Figure 31: Power supply and reference decoupling (VREF+ not connected to VDDA) modified.</p> <p>t_{JITTER} and f_{VCO} removed from Table 27: PLL characteristics.</p> <p>Appendix A: Important notes on page 81 added.</p> <p>Added Figure 13, Figure 14, Figure 15 and Figure 17.</p> |

Table 57. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 22 Nov-2007 | 4 | <p>Document status promoted from preliminary data to datasheet. The STM32F103xx is USB certified. Small text changes.</p> <p><i>Power supply schemes on page 11</i> modified. Number of communication peripherals corrected for STM32F103Tx and number of GPIOs corrected for LQFP package in <i>Table 2: Device features and peripheral counts (STM32F103xx Medium-density performance line)</i>.</p> <p>Main function and default alternate function modified for PC14 and PC15 in, <i>Note 5</i> added and Remap column added in <i>Table 4: Pin definitions</i>.</p> <p>$V_{DD}-V_{SS}$ ratings and <i>Note 1</i> modified in <i>Table 5: Voltage characteristics</i>, <i>Note 1</i> modified in <i>Table 6: Current characteristics</i>. <i>Note 1</i> and <i>Note 2</i> added in <i>Table 10: Embedded reset and power control block characteristics</i>.</p> <p>I_{DD} value at 72 MHz with peripherals enabled modified in <i>Table 13: Maximum current consumption in Run mode, code with data processing running from RAM</i>.</p> <p>I_{DD} value at 72 MHz with peripherals enabled modified in <i>Table 14: Maximum current consumption in Sleep mode, code running from Flash or RAM</i>.</p> <p>I_{DD_VBAT} typical value at 2.4 V modified and I_{DD_VBAT} maximum values added in <i>Table 15: Typical and maximum current consumptions in Stop and Standby modes</i>. Note added in <i>Table 16 on page 40</i> and <i>Table 17 on page 41</i>. ADC1 and ADC2 consumption and notes modified in <i>Table 19: Peripheral current consumption</i>.</p> <p>$t_{SU(HSE)}$ and $t_{SU(LSE)}$ conditions modified in <i>Table 22</i> and <i>Table 23</i>, respectively.</p> <p>Maximum values removed from <i>Table 26: Low-power mode wakeup timings</i>. t_{RET} conditions modified in <i>Table 29: Flash memory endurance and data retention</i>. <i>Figure 11: Power supply scheme</i> corrected.</p> <p><i>Figure 16: Current consumption in Stop mode with regulator in Low-power mode versus temperature at $V_{DD} = 3.3 V$ and $3.6 V$</i> added.</p> <p>Note removed below <i>Figure 25: SPI timing diagram - slave mode and $CPHA = 0$</i>. Note added below <i>Figure 26: SPI timing diagram - slave mode and $CPHA = 1(1)$</i>.</p> <p>Details on unused pins removed from <i>General input/output characteristics on page 52</i>.</p> <p><i>Table 41: SPI characteristics</i> updated. <i>Table 42: USB startup time</i> added. V_{AIN}, t_{lat} and t_{latr} modified, note added and I_{lkg} removed in <i>Table 45: ADC characteristics</i>. Test conditions modified and note added in <i>Table 48: ADC accuracy</i>. Note added below <i>Table 46</i> and <i>Table 49</i>.</p> <p>Inch values corrected in <i>Table 52: LQPF100, 100-pin low-profile quad flat package mechanical data</i>, <i>Table 53: LQFP64, 64-pin low-profile quad flat package mechanical data</i> and <i>Table 54: LQFP48, 48-pin low-profile quad flat package mechanical data</i>.</p> <p>Θ_{JA} value for VFQFPN36 package added in <i>Table 55: Thermal characteristics</i>.</p> <p>Order codes replaced by <i>Section 7: Ordering information scheme</i>.</p> <p>MCU 's operating conditions modified in <i>Typical current consumption on page 39</i>. Avg_Slope and V_{25} modified in <i>Table 49: TS characteristics</i>. <i>I2C interface characteristics on page 57</i> modified.</p> <p>Impedance size specified in <i>A.4: Voltage glitch on ADC input 0 on page 81</i>.</p> |

Table 57. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|--|
| 14-Mar-2008 | 5 | <p>Figure 2: Clock tree on page 17 added.</p> <p>Maximum T_J value given in Table 7: Thermal characteristics on page 32.</p> <p>CRC feature added (see CRC (cyclic redundancy check) calculation unit on page 9 and Figure 8: Memory map on page 27 for address).</p> <p>I_{DD} modified in Table 15: Typical and maximum current consumptions in Stop and Standby modes.</p> <p>ACC_{HSI} modified in Table 24: HSI oscillator characteristics on page 47, note 2 removed.</p> <p>P_D, T_A and T_J added, t_{prog} values modified and t_{prog} description clarified in Table 28: Flash memory characteristics on page 49.</p> <p>t_{RET} modified in Table 29: Flash memory endurance and data retention.</p> <p>$V_{NF(NRST)}$ unit corrected in Table 37: NRST pin characteristics on page 55.</p> <p>Table 41: SPI characteristics on page 59 modified.</p> <p>I_{VREF} added to Table 45: ADC characteristics on page 63.</p> <p>Table 47: ADC accuracy - limited test conditions added. Table 48: ADC accuracy modified.</p> <p>LQFP100 package specifications updated (see Section 6: Package characteristics on page 68).</p> <p>Recommended LQFP100, LQFP 64, LQFP48 and VFQFPN36 footprints added (see Figure 38, Figure 40, Figure 42 and Figure 34).</p> <p>Section 6.2: Thermal characteristics on page 75 modified, Section 6.2.1 and Section 6.2.2 added.</p> <p>Appendix A: Important notes on page 31 removed.</p> |
| 21-Mar-2008 | 6 | <p>Small text changes. Figure 8: Memory map clarified.</p> <p>In Table 29: Flash memory endurance and data retention:</p> <ul style="list-style-type: none"> – N_{END} tested over the whole temperature range – cycling conditions specified for t_{RET} – t_{RET} min modified at $T_A = 55\text{ °C}$ <p>V_{25}, Avg_Slope and T_L modified in Table 49: TS characteristics.</p> <p>CRC feature removed.</p> |
| 22-May-2008 | 7 | <p>CRC feature added back. Small text changes. Section 1: Introduction modified. Section 2.2: Full compatibility throughout the family added.</p> <p>I_{DD} at T_A max = 105 °C added to Table 15: Typical and maximum current consumptions in Stop and Standby modes on page 37.</p> <p>I_{DD_VBAT} removed from Table 18: Typical current consumption in Standby mode on page 42.</p> <p>Values added to Table 40: SCL frequency ($f_{PCLK1} = 36\text{ MHz}$, $V_{DD} = 3.3\text{ V}$) on page 58.</p> <p>Figure 25: SPI timing diagram - slave mode and $CPHA = 0$ on page 60 modified. Equation 1 corrected.</p> <p>t_{RET} at $T_A = 105\text{ °C}$ modified in Table 29: Flash memory endurance and data retention on page 49.</p> <p>V_{USB} added to Table 43: USB DC electrical characteristics on page 62.</p> <p>Figure 43: LQFP100 PD max vs. T_A on page 77 modified.</p> <p>Axx option added to Table 56: Ordering information scheme on page 78.</p> |

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