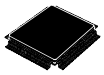
STM32F105xx
STM32F107xx

Connectivity line, ARM-based 32-bit MCU with 64/256 KB Flash, USB OTG, Ethernet, 10 timers, 2 CANs, 2 ADCs, 14 communication interfaces

Preliminary Data

Features

- Core: ARM 32-bit Cortex™-M3 CPU
  - 72 MHz maximum frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) performance at 0 wait state memory access
  - Single-cycle multiplication and hardware division
- Memories
  - 64 to 256 Kbytes of Flash memory
  - up to 64 Kbytes of SRAM
- Clock, reset and supply management
  - 2.0 to 3.6 V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 3-to-25 MHz crystal oscillator
  - Internal 8 MHz factory-trimmed RC
  - Internal 40 kHz RC with calibration
  - 32 kHz oscillator for RTC with calibration
- Low power
  - Sleep, Stop and Standby modes
  - V_{BAT} supply for RTC and backup registers
- 2 × 12-bit, 1 µs A/D converters (16 channels)
  - Conversion range: 0 to 3.6 V
  - Sample and hold capability
  - Temperature sensor
  - up to 2 MSps in interleaved mode
- 2 × 12-bit D/A converters
- DMA: 12-channel DMA controller
  - Supported peripherals: timers, ADCs, DAC, I^2Ss, SPIs, I^2Cs and USARTs
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M3 Embedded Trace Macrocell™
- Up to 80 fast I/O ports
  - 51/80 I/Os, all mappable on 16 external interrupt vectors and almost all 5 V-tolerant



LQFP64 10 × 10 mm,
LQFP100 14 × 14 mm,

LFBGA100 10 × 10 mm

- Up to 10 timers
  - Up to four 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
  - 1 × 16-bit motor control PWM timer with dead-time generation and emergency stop
  - 2 × watchdog timers (Independent and Window)
  - SysTick timer: a 24-bit downcounter
  - 2 × 16-bit basic timers to drive the DAC
- Up to 14 communication interfaces
  - Up to 2 × I^2C interfaces (SMBus/PMBus)
  - Up to 5 USARTs (ISO 7816 interface, LIN, IrDA capability, modem control)
  - Up to 3 SPIs (18 Mbit/s), 2 with a multiplexed I^2S interface that offers audio class accuracy via advanced PLL schemes
  - 2 × CAN interfaces (2.0B Active) with 512 bytes of dedicated SRAM
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY that supports HNP/SRP/ID with 1.25 Kbytes of dedicated SRAM
  - 10/100 Ethernet MAC with dedicated DMA and SRAM (4 Kbytes): IEEE1588 hardware support, MII/RMII available on all packages
- CRC calculation unit, 96-bit unique ID

Table 1. Device summary

Reference	Part number
STM32F105xx	STM32F105R8, STM32F105V8 STM32F105RB, STM32F105VB STM32F105RC, STM32F105VC
STM32F107xx	STM32F107RB, STM32F107VB STM32F107RC, STM32F107VC

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1 Introduction

This datasheet provides the description of the STM32F105xx and STM32F107xx connectivity line microcontrollers. For more details on the whole STMicroelectronics STM32F10xxx family, please refer to *Section 2.2: Full compatibility throughout the family*.

The STM32F105xx and STM32F107xx datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the STM32F10xxx Flash programming manual.
The reference and Flash programming manuals are both available from the STMicroelectronics website www.st.com.

For information on the Cortex™-M3 core please refer to the Cortex™-M3 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0337e/.

2 Description

The STM32F105xx and STM32F107xx connectivity line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 256 Kbytes and SRAM up to 64 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, four general-purpose 16-bit timers plus a PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs, two I2Ss, five USARTs, an USB OTG FS and two CANs. Ethernet is available on the STM32F107xx only.

The STM32F105xx and STM32F107xx connectivity line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F105xx and STM32F107xx connectivity line family offers devices in three different package types: from 64 pins to 100 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F105xx and STM32F107xx connectivity line microcontroller family suitable for a wide range of applications:

- Motor drive and application control
- Medical and handheld equipment
- Industrial applications: PLC, inverters, printers, and scanners
- Alarm systems, Video intercom, and HVAC
- Car audio, home audio equipment

Figure 1 shows the general block diagram of the device family.

2.1 Device overview

Table 2. STM32F105xx and STM32F107xx features and peripheral counts

Peripherals		STM32F105Rx			STM32F107Rx		STM32F105Vx			STM32F107Vx	
Flash memory in Kbytes		64	128	256	128	256	64	128	256	128	256
SRAM in Kbytes		20	32	64	48	64	20	32	64	48	64
Ethernet		No			Yes		No			Yes	
Timers	General-purpose	4									
	Advanced-control	1									
	Basic	2									
Communication interfaces	SPI(I^2S)(1)	3(2)									
	I^2C	2									
	USART	5									
	USB OTG FS	Yes									
	CAN	2									
GPIOs		51					80				
12-bit ADC Number of channels		2 16									
12-bit DAC Number of channels		2 2									
CPU frequency		72 MHz									
Operating voltage		2.0 to 3.6 V									
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C Junction temperature: –40 to + 125 °C									
Package		LQFP64					LQFP100, BGA100				

1. The SPI2 and SPI3 interfaces give the flexibility to work in either the SPI mode or the I^2S audio mode.

2.2 Full compatibility throughout the family

The STM32F105xx and STM32F107xx constitute the connectivity line family whose members are fully pin-to-pin, software and feature compatible.

The STM32F105xx and STM32F107xx are a drop-in replacement for the low-density (STM32F103x4/6), medium-density (STM32F103x8/B) and high-density (STM32F103xC/D/E) performance line devices, allowing the user to try different memory densities and peripherals providing a greater degree of freedom during the development cycle.

Table 3. STM32F105xx and STM32F107xx family versus STM32F103xx family

<table>
<tr><th>STM32 device</th><th colspan="2">Low-density STM32F103xx devices</th><th colspan="3">Medium-density STM32F103xx devices</th><th colspan="3">High-density STM32F103xx devices</th><th colspan="3">STM32F105xx</th><th colspan="2">STM32F107xx</th></tr>
<tr><td>Flash size (KB)</td><td>16</td><td>32</td><td>32</td><td>64</td><td>128</td><td>256</td><td>384</td><td>512</td><td>64</td><td>128</td><td>256</td><td>128</td><td>256</td></tr>
<tr><td>RAM size (KB)</td><td>6</td><td>10</td><td>10</td><td>20</td><td>20</td><td>48</td><td>64</td><td>64</td><td>20</td><td>32</td><td>64</td><td>48</td><td>64</td></tr>
<tr><td>144 pins</td><td colspan="5" rowspan="2"></td><td colspan="3" rowspan="3">5 × USARTs
4 × 16-bit timers,
2 × basic timers, 3 × SPIs,
2 × I²Ss, 2 × I2Cs, USB,
CAN, 2 × PWM timers
3 × ADCs, 1 × DAC,
1 × SDIO, FSMC (100- and 144-pin packages(1))</td><td colspan="3"></td><td colspan="2"></td></tr>
<tr><td>100 pins</td><td colspan="3" rowspan="3">3 × USARTs
3 × 16-bit timers
2 × SPIs,
2 × I²Cs, USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="3" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers, 3 × SPIs,
2 × I²Ss, 2 × I2Cs,
USB OTG FS,
2 × CANs, 1 × PWM timer,
2 × ADCs, 1 × DAC</td><td colspan="2" rowspan="2">5 × USARTs,
4 × 16-bit timers,
2 × basic timers,
3 × SPIs, 2 × I²Ss,
2 × I2Cs,
USB OTG FS,
2 × CANs,
1 × PWM timer,
2 × ADCs,
1 × DAC, Ethernet</td></tr>
<tr><td>64 pins</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI, 1 × I²C,
USB, CAN,
1 × PWM timer
2 × ADCs</td><td colspan="2" rowspan="3">2 × USARTs
2 × 16-bit timers
1 × SPI,
1 × I²C,
USB, CAN,
1 × PWM timer
2 × ADCs</td></tr>
<tr><td>48 pins</td><td colspan="3"></td></tr>
<tr><td>36 pins</td><td colspan="3"></td></tr>
</table>

1. Ports F and G are not available in devices delivered in 100-pin packages.

2.3 Overview

2.3.1 ARM® Cortex™-M3 core with embedded Flash and SRAM

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F105xx and STM32F107xx connectivity line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Embedded Flash memory

64 to 256 Kbytes of embedded Flash is available for storing programs and data.

2.3.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.4 Embedded SRAM

20 to 64 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.5 Nested vectored interrupt controller (NVIC)

The STM32F105xx and STM32F107xx connectivity line embeds a nested vectored interrupt controller able to handle up to 67 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 20 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 80 GPIOs can be connected to the 16 external interrupt lines.

2.3.7 Clocks and startup

System clock selection is performed on startup, however, the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 3-25 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full

interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

A single 25 MHz crystal can clock the entire system including the ethernet and USB OTG FS peripherals. Several prescalers and PLLs allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. Refer to *Figure 50: USB OTG FS + Ethernet solution on page 87*.

The advanced clock controller clocks the core and all peripherals using a single crystal or oscillator. In order to achieve audio class performance, an audio crystal can be used. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 96 kHz with less than 0.5% accuracy error. Refer to *Figure 51: USB OTG FS + I^2S (Audio) solution on page 87*.

To configure the PLLs, please refer to *Table 60 on page 88*, which provides PLL configurations according to the application type.

2.3.8 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1, USART2 (remapped), CAN2 (remapped), USB OTG FS in device mode (DFU: device firmware upgrade) and Ethernet.

2.3.9 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

2.3.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

2.3.11 Voltage regulator

The regulator has three operation modes: main (MR), low power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.12 Low-power modes

The STM32F105xx and STM32F107xx connectivity line supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB OTG FS wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.13 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.
Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced control timers TIMx, DAC, I^2S and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.4 Timers and watchdogs

The STM32F105xx and STM32F107xx devices include six general-purpose timers, two basic timers and two watchdog timers.

Table 4 compares the features of the general-purpose and basic timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIMx (TIM2, TIM3, TIM4, TIM5)	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

2.4.1 Advanced-control timer (TIM1)

The advanced control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard TIM timers which have the same architecture. The advanced control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

2.4.2 General-purpose timers (TIMx)

There are up to 4 synchronizable standard timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F105xx and STM32F107xx connectivity line devices. These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages. They can work together with the Advanced Control timer via the Timer Link feature for synchronization or event chaining.

The counter can be frozen in debug mode.

Any of the standard timers can be used to generate PWM outputs. Each of the timers has independent DMA request generations.

2.4.3 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

2.4.4 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

2.4.5 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.4.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.4.7 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.4.8 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F105xx and STM32F107xx connectivity line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

2.4.9 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.4.10 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 96 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency with less than 0.5% accuracy error owing to the advanced clock controller (see *Section 2.3.7: Clocks and startup*).

Please refer to the “Audio frequency precision” tables provided in the “Serial peripheral interface (SPI)” section of the STM32F10xxx reference manual.

2.4.11 Ethernet MAC interface with dedicated DMA and IEEE 1588 support

Peripheral not available on STM32F105xx devices.

The STM32F107xx devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The STM32F107xx requires an external physical interface device (PHY) to connect to the physical LAN bus

(twisted-pair, fiber, etc.). the PHY is connected to the STM32F107xx MII port using as many as 17 signals (MII) or 9 signals (RMII) and can be clocked using the 25 MHz (MII) or 50 MHz (RMII) output from the STM32F107xx.

The STM32F107xx includes the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA channel
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes (512 × 35 bits), that is 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 1.0 with the timestamp comparator connected to the TIM2 trigger input
- Triggers interrupt when system time becomes greater than target time

2.4.12 Controller area network (CAN)

The two CANs are compliant with the 2.0A and B (active) specifications with a bitrate up to 1 Mbit/s. They can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three transmit mailboxes, two receive FIFOS with 3 stages and 28 shared scalable filter banks (all of them can be used even if one CAN is used). The 256 bytes of SRAM which are allocated for each CAN (512 bytes in total) are not shared with any other peripheral.

2.4.13 Universal serial bus on-the-go full-speed (USB OTG FS)

The STM32F105xx and STM32F107xx connectivity line devices embed a USB OTG full-speed (12 Mb/s) device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- 1.25 KB of SRAM used exclusively by the endpoints (not shared with any other peripheral)
- 4 bidirectional endpoints
- HNP/SNP/IP inside (no need for any external resistor)
- for OTG/Host modes, a power switch is needed in case bus-powered devices are connected
- the SOF output can be used to synchronize the external audio DAC clock in isochronous mode
- in accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - in Host mode: full speed and low speed
  - in Device mode: full speed

2.4.14 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable except for analog inputs.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed

2.4.15 ADCs (analog-to-digital converters)

Two 12-bit analog-to-digital converters are embedded into STM32F105xx and STM32F107xx connectivity line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger, respectively, to allow the application to synchronize A/D conversion and timers.

2.4.16 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- external triggers for conversion
- input voltage reference V_{REF+}

Eight DAC trigger inputs are used in the STM32F105xx and STM32F107xx connectivity line family. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

2.4.17 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC1_IN16 input channel which is used to convert the sensor output voltage into a digital value.

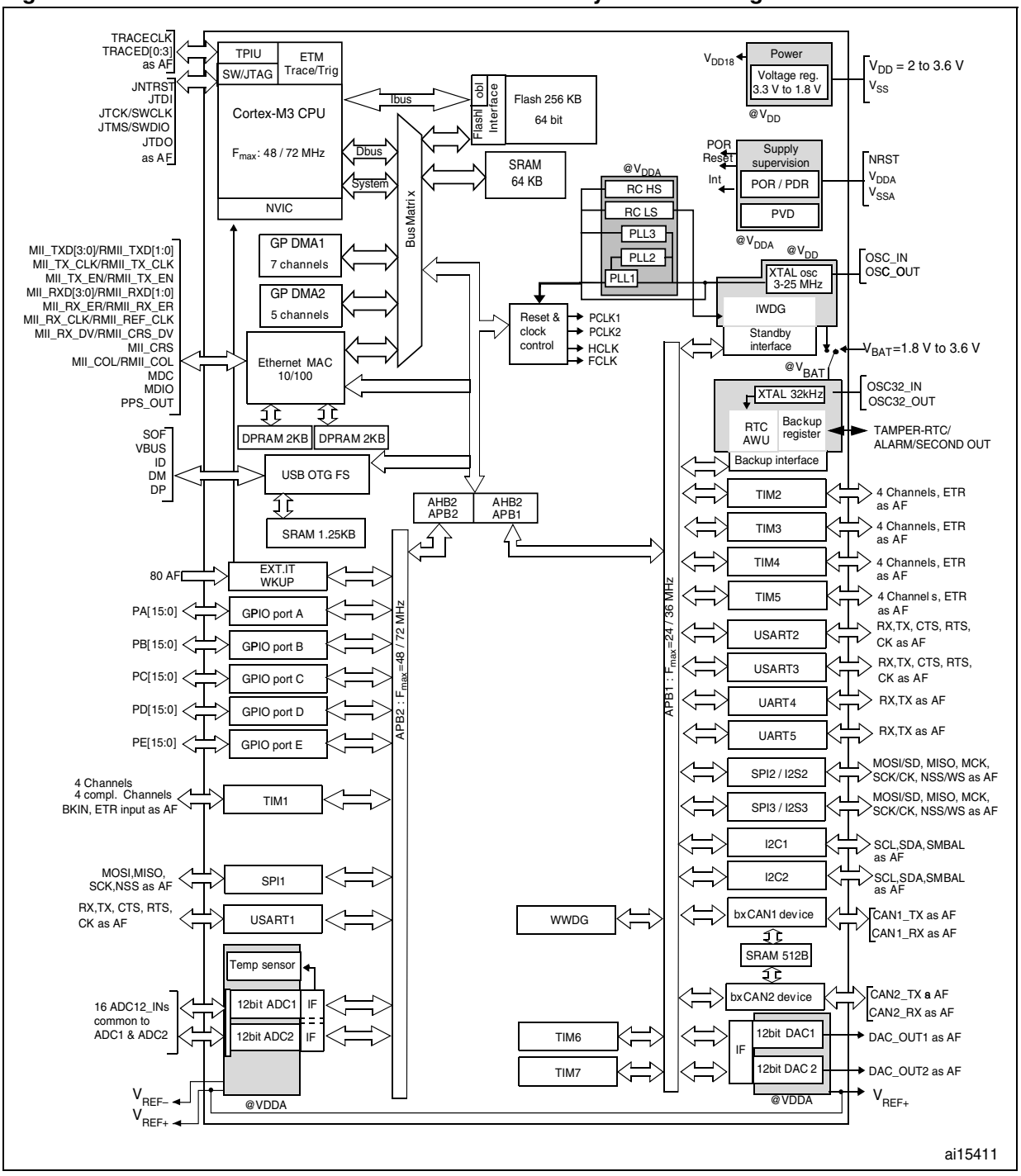
2.4.18 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared respectively with SWDIO and SWCLK and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

2.4.19 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F10xxx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB OTG FS, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 1. STM32F105xx and STM32F107xx connectivity line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 59*) or –40 °C to +105 °C (suffix 7, see *Table 59*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.

3 Pin descriptions

Figure 2. STM32F105xxx and STM32F107xxx connectivity line LQFP100 pinout

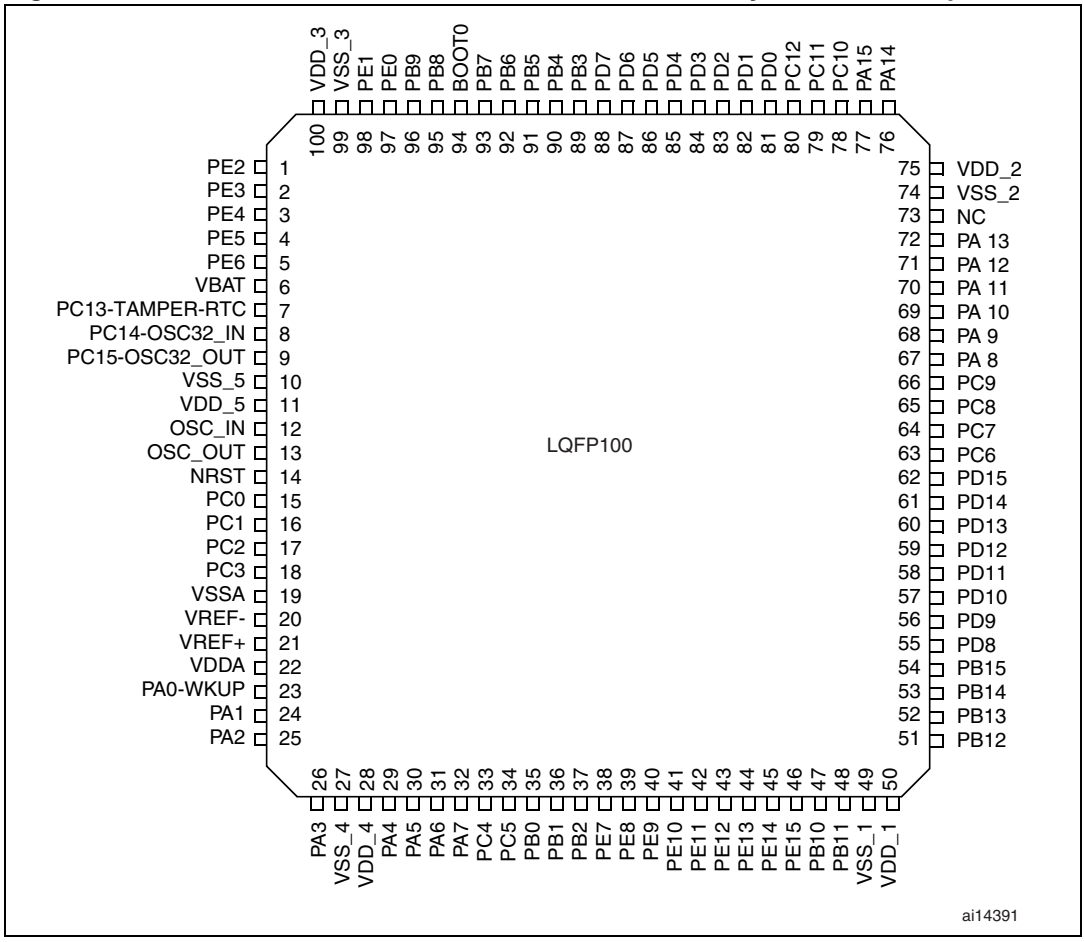


Figure 3. STM32F105xxx and STM32F107xxx connectivity line LQFP64 pinout

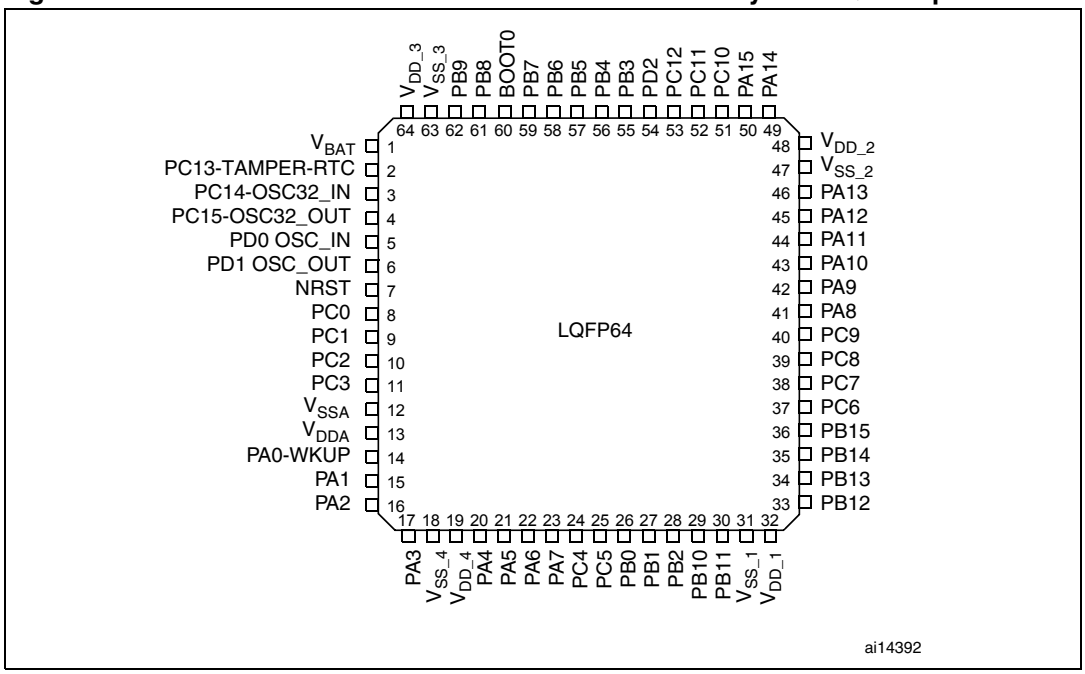


Figure 4. STM32F105xxx and STM32F107xxx connectivity line BGA100 ballout

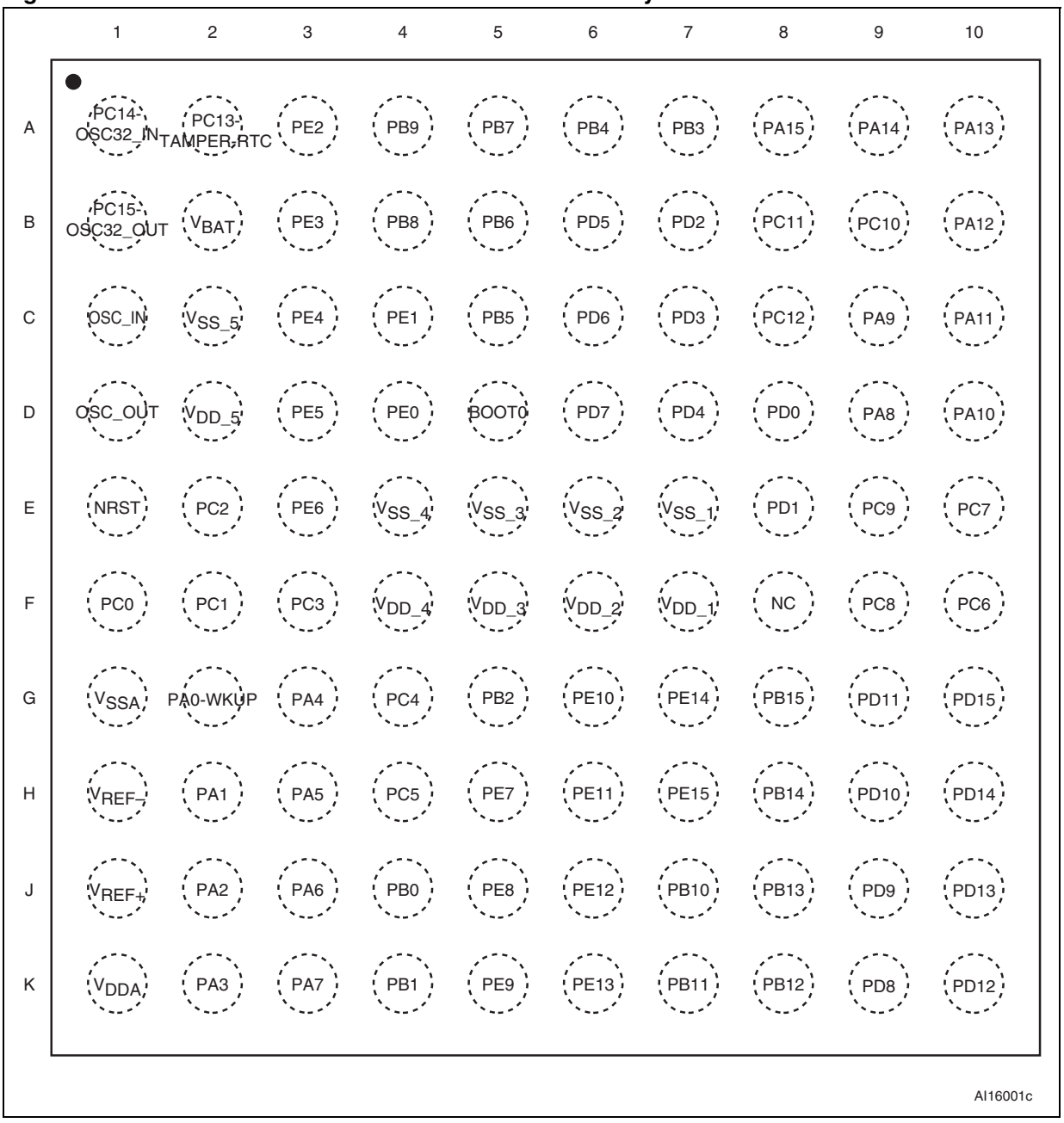


Table 5. Pin definitions

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
BGA100	LQFP64	LQFP100					Default	Remap
A3	-	1	PE2	I/O	FT	PE2	TRACECK	
B3	-	2	PE3	I/O	FT	PE3	TRACED0	
C3	-	3	PE4	I/O	FT	PE4	TRACED1	
D3	-	4	PE5	I/O	FT	PE5	TRACED2	
E3	-	5	PE6	I/O	FT	PE6	TRACED3	
B2	1	6	V_{BAT}	S		V_{BAT}		
A2	2	7	PC13-TAMPER-RTC(4)	I/O		PC13(5)	TAMPER-RTC	
A1	3	8	PC14-OSC32_IN(4)	I/O		PC14(5)	OSC32_IN	
B1	4	9	PC15-OSC32_OUT(4)	I/O		PC15(5)	OSC32_OUT	
C2	-	10	V_{SS_5}	S		V_{SS_5}		
D2	-	11	V_{DD_5}	S		V_{DD_5}		
C1	5	12	OSC_IN	I		OSC_IN		
D1	6	13	OSC_OUT	O		OSC_OUT		
E1	7	14	NRST	I/O		NRST		
F1	8	15	PC0	I/O		PC0	ADC12_IN10	
F2	9	16	PC1	I/O		PC1	ADC12_IN11/ ETH_MII_MDC/ ETH_RMII_MDC	
E2	10	17	PC2	I/O		PC2	ADC12_IN12/ ETH_MII_TXD2	
F3	11	18	PC3	I/O		PC3	ADC12_IN13/ ETH_MII_TX_CLK	
G1	12	19	V_{SSA}	S		V_{SSA}		
H1	-	20	V_{REF-}	S		V_{REF-}		
J1	-	21	V_{REF+}	S		V_{REF+}		
K1	13	22	V_{DDA}	S		V_{DDA}		
G2	14	23	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(6) ADC12_IN0/TIM2_CH1_ETR TIM5_CH1/ ETH_MII_CRS_WKUP	
H2	15	24	PA1	I/O		PA1	USART2_RTS(6)/ ADC12_IN1/ TIM5_CH2 /TIM2_CH2(6)/ ETH_MII_RX_CLK/ ETH_RMII_REF_CLK	

Table 5. Pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
BGA100	LQFP64	LQFP100					Default	Remap
J2	16	25	PA2	I/O		PA2	USART2_TX(6)/ TIM5_CH3/ADC12_IN2/ TIM2_CH3 (6)/ ETH_MII_MDIO/ ETH_RMII_MDIO	
K2	17	26	PA3	I/O		PA3	USART2_RX(6)/ TIM5_CH4/ADC12_IN3 TIM2_CH4(6)/ ETH_MII_COL	
E4	18	27	V_{SS_4}	S		V_{SS_4}		
F4	19	28	V_{DD_4}	S		V_{DD_4}		
G3	20	29	PA4	I/O		PA4	SPI1_NSS(6)/DAC_OUT1 USART2_CK(6) ADC12_IN4	
H3	21	30	PA5	I/O		PA5	SPI1_SCK(6) DAC_OUT2 ADC12_IN5	
J3	22	31	PA6	I/O		PA6	SPI1_MISO(6)/ADC12_IN6 TIM3_CH1(6)	TIM1_BKIN
K3	23	32	PA7	I/O		PA7	SPI1_MOSI(6)/ADC12_IN7 TIM3_CH2(6)/ ETH_MII_RX_DV/ ETH_RMII_CRS_DV	TIM1_CH1N
G4	24	33	PC4	I/O		PC4	ADC12_IN14/ ETH_MII_RXD0/ ETH_RMII_RXD0	
H4	25	34	PC5	I/O		PC5	ADC12_IN15/ ETH_MII_RXD1/ ETH_RMII_RXD1	
J4	26	35	PB0	I/O		PB0	ADC12_IN8/TIM3_CH3/ ETH_MII_RXD2	TIM1_CH2N
K4	27	36	PB1	I/O		PB1	ADC12_IN9/TIM3_CH4(6)/ ETH_MII_RXD3	TIM1_CH3N
G5	28	37	PB2	I/O	FT	PB2/BOOT1		
H5	-	38	PE7	I/O	FT	PE7		TIM1_ETR
J5	-	39	PE8	I/O	FT	PE8		TIM1_CH1N
K5	-	40	PE9	I/O	FT	PE9		TIM1_CH1
-	-	-	V_{SS_7}	S				
-	-	-	V_{DD_7}	S				
G6	-	41	PE10	I/O	FT	PE10		TIM1_CH2N
H6	-	42	PE11	I/O	FT	PE11		TIM1_CH2
J6	-	43	PE12	I/O	FT	PE12		TIM1_CH3N

Table 5. Pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
BGA100	LQFP64	LQFP100					Default	Remap
K6	-	44	PE13	I/O	FT	PE13		TIM1_CH3
G7	-	45	PE14	I/O	FT	PE14		TIM1_CH4
H7	-	46	PE15	I/O	FT	PE15		TIM1_BKIN
J7	29	47	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX(6)/ ETH_MII_RX_ER	TIM2_CH3
K7	30	48	PB11	I/O	FT	PB11	I2C2_SDA/USART3_RX(6)/ ETH_MII_TX_EN/ ETH_RMII_TX_EN	TIM2_CH4
E7	31	49	V_{SS_1}	S		V_{SS_1}		
F7	32	50	V_{DD_1}	S		V_{DD_1}		
K8	33	51	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBAL// USART3_CK(6)/ TIM1_BKIN(6)/CAN2_RX/ ETH_MII_TXD0/ ETH_RMII_TXD0	
J8	34	52	PB13	I/O	FT	PB13	SPI2_SCK/I2S2_CK USART3_CTS(6)/ TIM1_CH1N/CAN2_TX/ ETH_MII_TXD1/ ETH_RMII_TXD1	
H8	35	53	PB14	I/O	FT	PB14	SPI2_MISO/TIM1_CH2N USART3_RTS(6)	
G8	36	54	PB15	I/O	FT	PB15	SPI2_MOSI/I2S2_SD TIM1_CH3N(6)	
K9	-	55	PD8	I/O	FT	PD8		USART3_TX/ ETH_MII_RX_DV
J9	-	56	PD9	I/O	FT	PD9		USART3_RX/ ETH_MII_RX_D0
H9	-	57	PD10	I/O	FT	PD10		USART3_CK/ ETH_MII_RX_D1
G9	-	58	PD11	I/O	FT	PD11		USART3_CTS/ ETH_MII_RX_D2
K10	-	59	PD12	I/O	FT	PD12		TIM4_CH1 / USART3_RTS/ ETH_MII_RX_D3
J10	-	60	PD13	I/O	FT	PD13		TIM4_CH2
H10	-	61	PD14	I/O	FT	PD14		TIM4_CH3
G10	-	62	PD15	I/O	FT	PD15		TIM4_CH4
F10	37	63	PC6	I/O	FT	PC6	I2S2_MCK/	TIM3_CH1

Table 5. Pin definitions (continued)

Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
BGA100	LQFP64	LQFP100					Default	Remap
E10	38	64	PC7	I/O	FT	PC7	I2S3_MCK/	TIM3_CH2
F9	39	65	PC8	I/O	FT	PC8		TIM3_CH3
E9	40	66	PC9	I/O	FT	PC9		TIM3_CH4
D9	41	67	PA8	I/O	FT	PA8	USART1_CK/OTG_FS_SOF TIM1_CH1(6)/MCO	
C9	42	68	PA9	I/O	FT	PA9	USART1_TX(6)/ TIM1_CH2(6)/ OTG_FS_VBUS	
D10	43	69	PA10	I/O	FT	PA10	USART1_RX(6)/ TIM1_CH3(6)/OTG_FS_ID	
C10	44	70	PA11	I/O	FT	PA11	USART1_CTS/CAN1_RX TIM1_CH4(6)/OTG_FS_DM	
B10	45	71	PA12	I/O	FT	PA12	USART1_RTS/OTG_FS_DP CAN1_TX(6)/TIM1_ETR(6)	
A10	46	72	PA13	I/O	FT	JTMS-SWDIO		PA13
F8	-	73	Not connected					
E6	47	74	V_{SS_2}	S		V_{SS_2}		
F6	48	75	V_{DD_2}	S		V_{DD_2}		
A9	49	76	PA14	I/O	FT	JTCK-SWCLK		PA14
A8	50	77	PA15	I/O	FT	JTDI	SPI3_NSS/	TIM2_CH1_ETR / PA15 SPI1_NSS
B9	51	78	PC10	I/O	FT	PC10	UART4_TX	USART3_TX/ SPI3_SCK
B8	52	79	PC11	I/O	FT	PC11	UART4_RX	USART3_RX/ SPI3_MISO
C8	53	80	PC12	I/O	FT	PC12	UART5_TX	USART3_CK/ SPI3_MOSI
D8	5	81	PD0	I/O	FT	OSC_IN(7)		CAN1_RX
E8	6	82	PD1	I/O	FT	OSC_OUT(7)		CAN1_TX
B7	54	83	PD2	I/O	FT	PD2	TIM3_ETR/UART5_RX	
C7	-	84	PD3	I/O	FT	PD3		USART2_CTS
D7	-	85	PD4	I/O	FT	PD4		USART2_RTS
B6	-	86	PD5	I/O	FT	PD5		USART2_TX
C6	-	87	PD6	I/O	FT	PD6		USART2_RX
D6	-	88	PD7	I/O	FT	PD7		USART2_CK
A7	55	89	PB3	I/O	FT	JTDO	SPI3_SCK	PB3 / TRACESWO/ TIM2_CH2 / SPI1_SCK

Table 5. Pin definitions (continued)

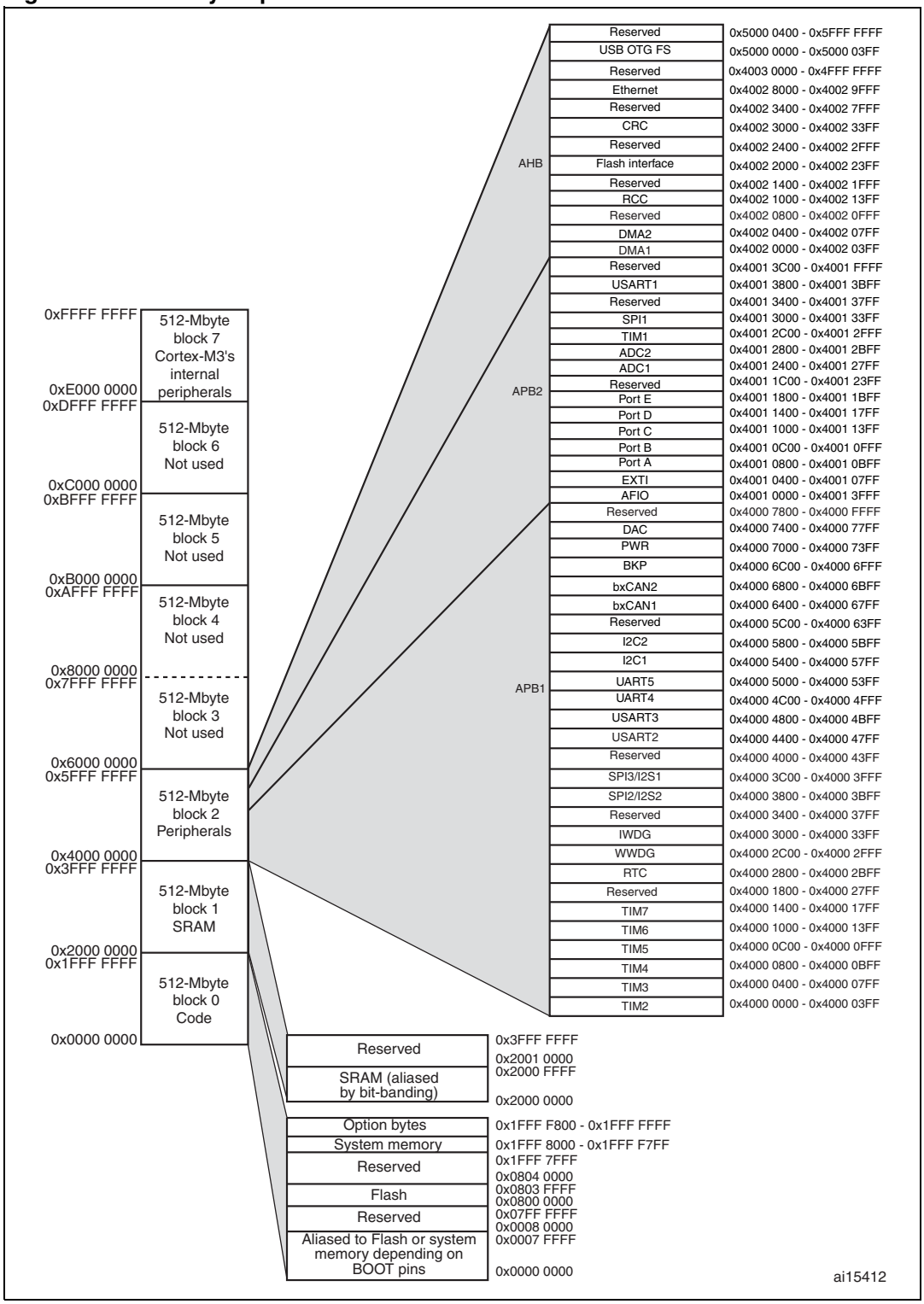
Pins			Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions	
BGA100	LQFP64	LQFP100					Default	Remap
A6	56	90	PB4	I/O	FT	JNTRST	SPI3_MISO	PB4 / TIM3_CH1/ SPI1_MISO
C5	57	91	PB5	I/O		PB5	I2C1_SMBAI/ SPI3_MOSI/ ETH_MII_PPS_OUT/ ETH_RMII_PPS_OUT	TIM3_CH2/SPI1_MOSI/ CAN2_RX
B5	58	92	PB6	I/O	FT	PB6	I2C1_SCL(6)/TIM4_CH1(6)	USART1_TX/CAN2_TX
A5	59	93	PB7	I/O	FT	PB7	I2C1_SDA(6)/TIM4_CH2(6)	USART1_RX
D5	60	94	BOOT0	I		BOOT0		
B4	61	95	PB8	I/O	FT	PB8	TIM4_CH3(6)/ ETH_MII_TXD3	I2C1_SCL/CAN1_RX
A4	62	96	PB9	I/O	FT	PB9	TIM4_CH4(6)	I2C1_SDA / CAN1_TX
D4	-	97	PE0	I/O	FT	PE0	TIM4_ETR	
C4	-	98	PE1	I/O	FT	PE1		
E5	63	99	V_{SS_3}	S		V_{SS_3}		
F5	64	100	V_{DD_3}	S		V_{DD_3}		

1. I = input, O = output, S = supply, HiZ = high impedance.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.
4. PC13, PC14 and PC15 are supplied through the power switch, and so their use in output mode is limited: they can be used only in output 2 MHz mode with a maximum load of 30 pF and only one pin can be put in output mode at a time.
5. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
6. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and BGA100 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.

4 Memory mapping

The memory map is shown in *Figure 5*.

Figure 5. Memory map



5 Electrical characteristics

5.1 Test conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 6. Pin loading conditions

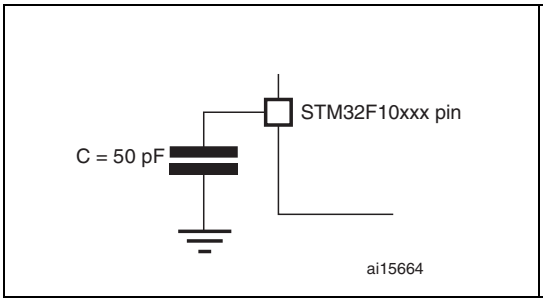
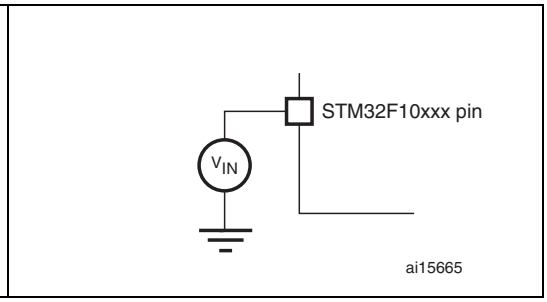
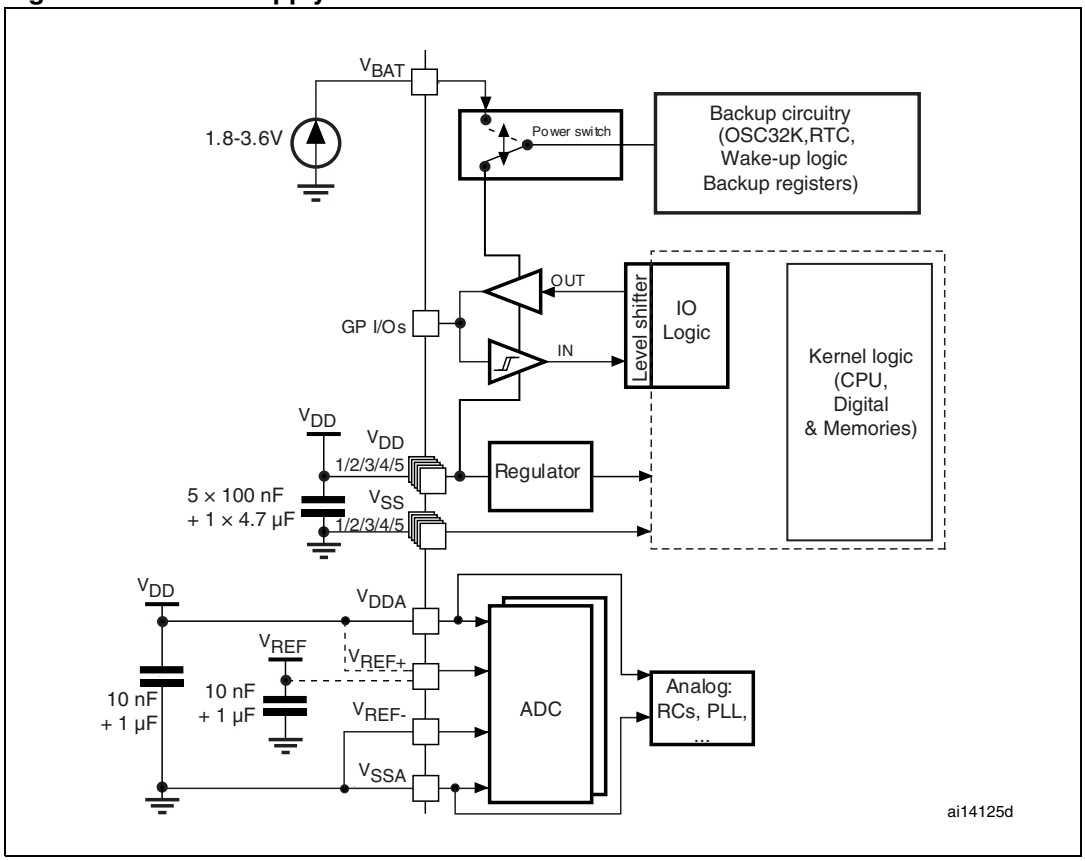


Figure 7. Pin input voltage



5.1.6 Power supply scheme

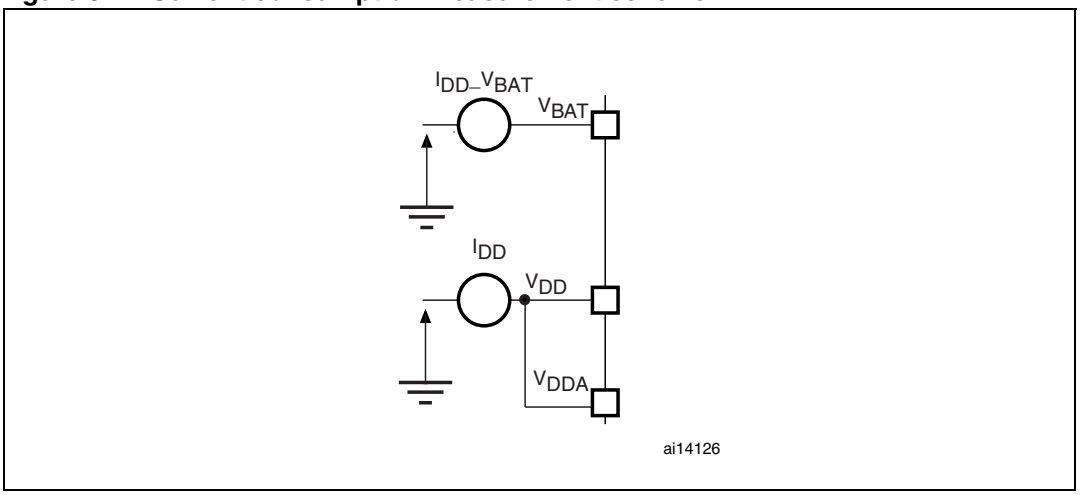
Figure 8. Power supply scheme



Caution: In *Figure 8*, the 4.7 µF capacitor must be connected to V_{DD3}.

5.1.7 Current consumption measurement

Figure 9. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 6: Voltage characteristics*, *Table 7: Current characteristics*, and *Table 8: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}	Input voltage on five volt tolerant pin(2)	V_{SS} –0.3	+5.5	
	Input voltage on any other pin(2)	V_{SS} –0.3	V_{DD}+0.3	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 5.3.11: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded (see *Table 7: Current characteristics*). This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{IN}$max while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 7. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD}/V_{DDA} power lines (source)(1)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)	150	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	–25	
$I_{INJ(PIN)}$ (2)(3)	Injected current on NRST pin	± 5	
	Injected current on HSE OSC_IN and LSE OSC_IN pins	± 5	
	Injected current on any other pin(4)	± 5	
$\Sigma I_{INJ(PIN)}$(2)	Total injected current (sum of all I/O and control pins)(4)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See note in *Section 5.3.16: 12-bit ADC characteristics*.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 8. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 9. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency		0	36	
f_{PCLK2}	Internal APB2 clock frequency		0	72	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LFBGA100		487	mW
		LQFP100		434	
		LQFP64		444	
		LQFP48		363	
		VFQFPN36		1110	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 50: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 8: Thermal characteristics on page 34*).
4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 8: Thermal characteristics on page 34*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	µs/V
	V_{DD} fall time rate		20	∞	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis			40		mV
$T_{RSTTEMPO}$(2)	Reset temporization		1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 12. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.20	1.26	V
		–40 °C < T_A < +85 °C	1.16	1.20	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage			5.1	17.1(2)	µs

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 9: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 13*, *Table 14* and *Table 15* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 13. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	69	70	mA
			48 MHz	50	50.5	
			36 MHz	39	39.5	
			24 MHz	27	28	
			16 MHz	20	20.5	
			8 MHz	11	11.5	
		External clock(2), all peripherals disabled	72 MHz	37	37.5	
			48 MHz	28	28.5	
			36 MHz	22	22.5	
			24 MHz	16.5	17	
			16 MHz	12.5	13	
			8 MHz	8	8	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 14. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	66	67	mA
			48 MHz	43.5	45.5	
			36 MHz	33	35	
			24 MHz	23	24.5	
			16 MHz	16	18	
			8 MHz	9	10.5	
		External clock(2), all peripherals disabled	72 MHz	33	33.5	
			48 MHz	23	23.5	
			36 MHz	18	18.5	
			24 MHz	13	13.5	
			16 MHz	10	10.5	
			8 MHz	6	6.5	

1. Based on characterization, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 10. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

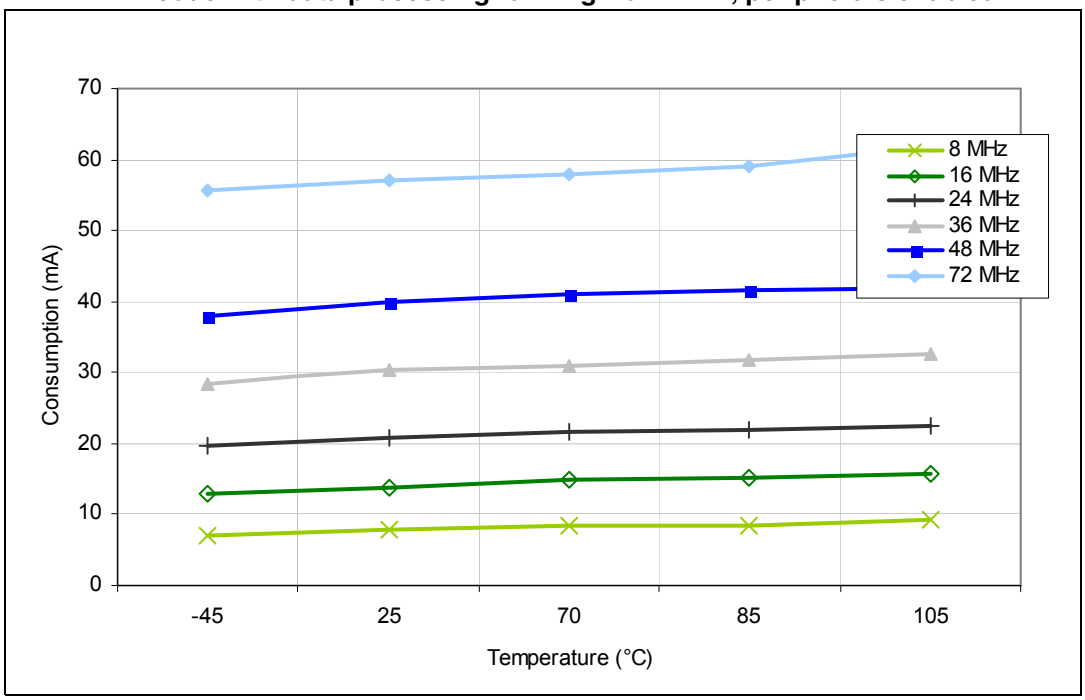


Figure 11. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

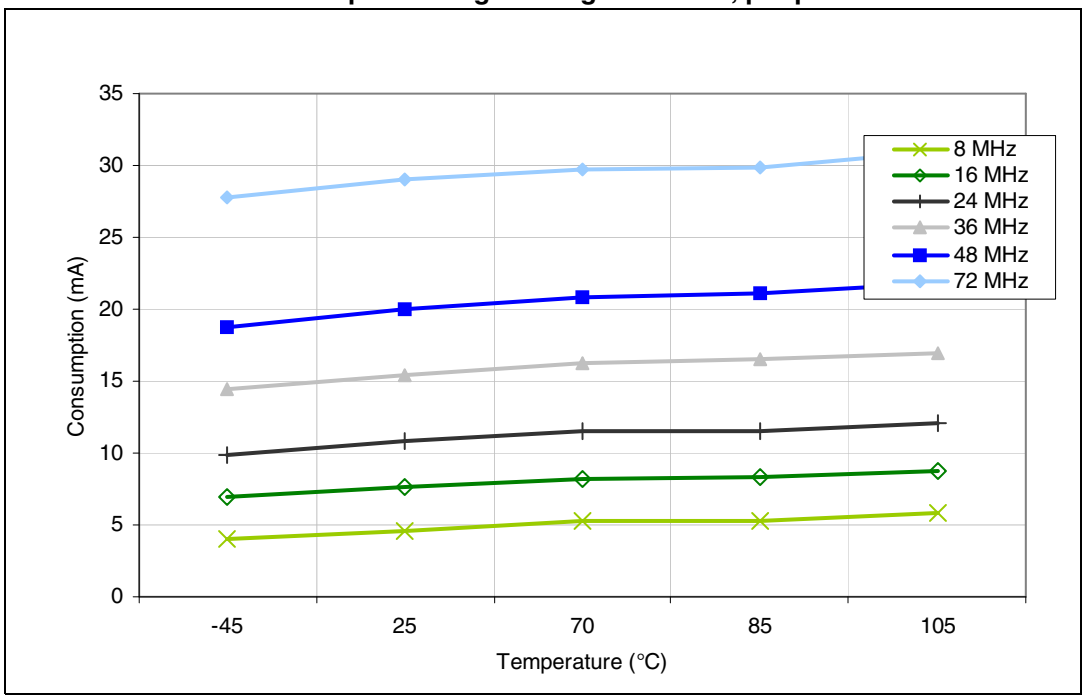


Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	66	67	mA
			48 MHz	43.5	45.5	
			36 MHz	33	35	
			24 MHz	23	24.5	
			16 MHz	16	18	
			8 MHz	9	10.5	
		External clock(2), all peripherals disabled	72 MHz	33	33.5	
			48 MHz	23	23.5	
			36 MHz	18	18.5	
			24 MHz	13	13.5	
			16 MHz	10	10.5	
			8 MHz	6	6.5	

1. Based on characterization, tested in production at V_{DD} max and f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)		Max		Unit
			V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	34.5	35	379	1130	µA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	24.5	25	365	1110	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	3	3.8	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	2.8	3.6	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.9	2.1	5(2)	6.5(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.1	1.4	2(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Figure 12. Typical current consumption in Stop mode with regulator in Run mode versus temperature at different V_{DD} values

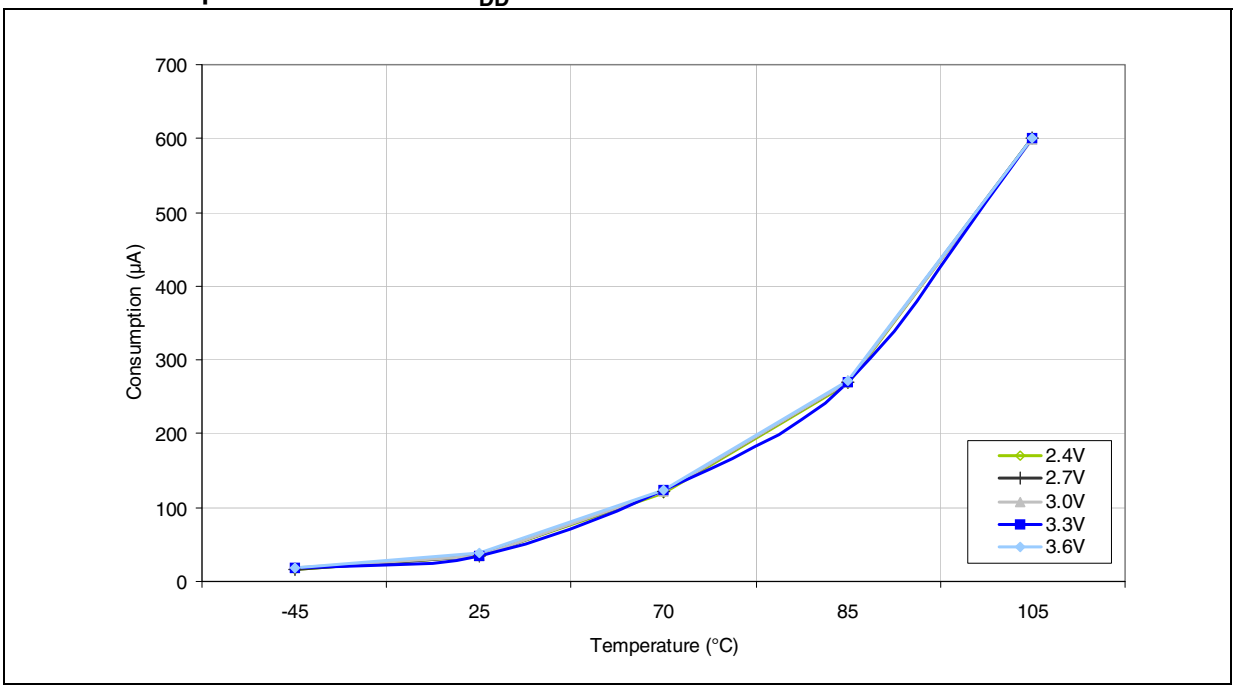


Figure 13. Current consumption in Stop mode with regulator in Low-power mode versus temperature at different V_{DD} values

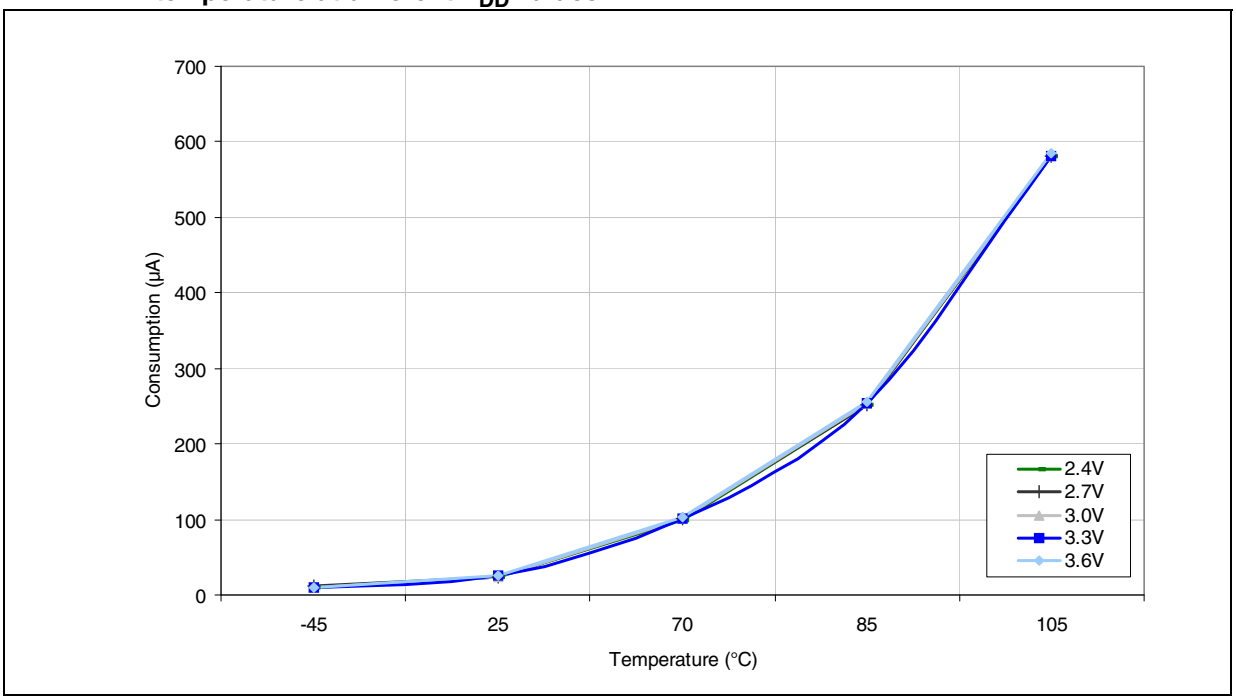
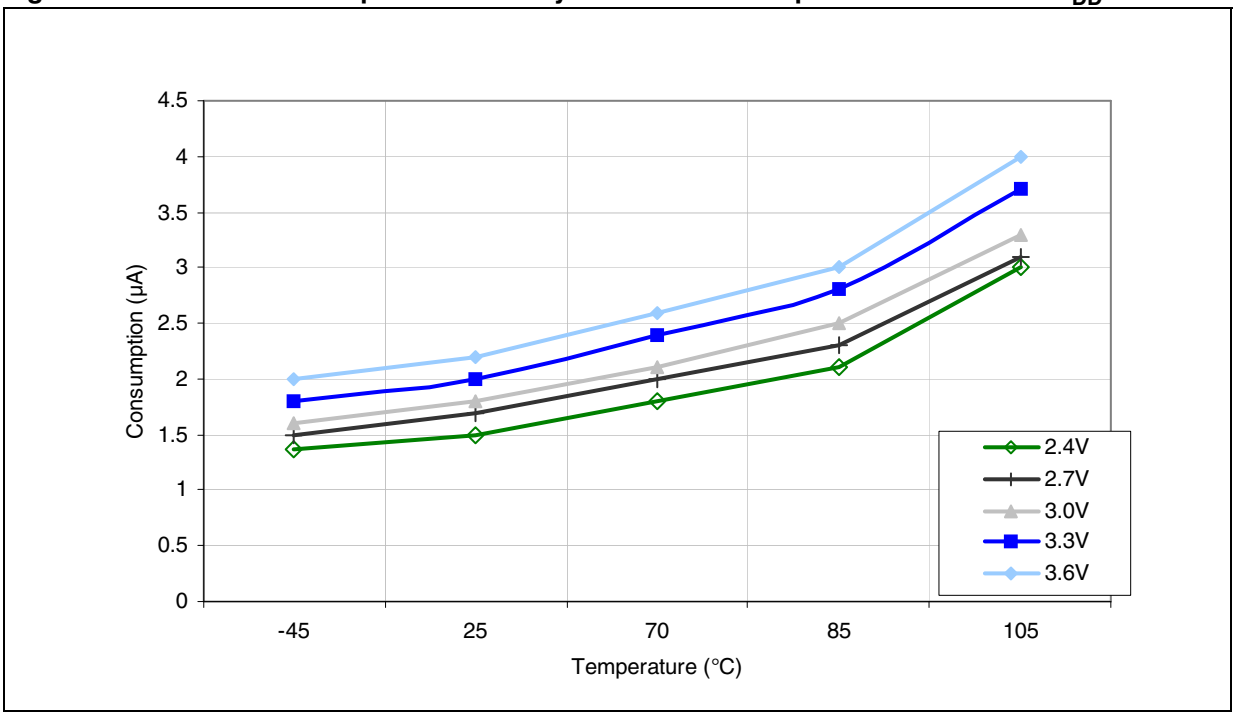


Figure 14. Current consumption in Standby mode versus temperature at different V_{DD} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	51	30.5	mA
			48 MHz	34.6	20.7	
			36 MHz	26.6	16.2	
			24 MHz	18.5	11.4	
			16 MHz	12.8	8.2	
			8 MHz	7.2	5	
			4 MHz	4.2	3.1	
			2 MHz	2.7	2.1	
			1 MHz	2	1.7	
			500 kHz	1.6	1.4	
			125 kHz	1.3	1.2	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45	27	mA
			48 MHz	34	20.1	
			36 MHz	26	15.6	
			24 MHz	17.9	10.8	
			16 MHz	12.2	7.6	
			8 MHz	6.6	4.4	
			4 MHz	3.6	2.5	
			2 MHz	2.1	1.5	
			1 MHz	1.4	1.1	
			500 kHz	1	0.8	
			125 kHz	0.7	0.6	

1. Typical values are measures at $T_A = 25$ °C, $V_{DD} = 3.3$ V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 18. Typical current consumption in Sleep mode, code with data processing code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	29.5	6.4	mA
			48 MHz	20	4.6	
			36 MHz	15.1	3.6	
			24 MHz	10.4	2.6	
			16 MHz	7.2	2	
			8 MHz	3.9	1.3	
			4 MHz	2.6	1.2	
			2 MHz	1.85	1.15	
			1 MHz	1.5	1.1	
			500 kHz	1.3	1.05	
			125 kHz	1.2	1.05	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	25.6	5.1	
			48 MHz	19.4	4	
			36 MHz	14.5	3	
			24 MHz	9.8	2	
			16 MHz	6.6	1.4	
			8 MHz	3.3	0.7	
			4 MHz	2	0.6	
			2 MHz	1.25	0.55	
			1 MHz	0.9	0.5	
			500 kHz	0.7	0.45	
			125 kHz	0.6	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*

Table 19. Peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit
APB1	TIM2	1.2	mA
	TIM3	1.2	
	TIM4	0.9	
	SPI2	0.2	
	USART2	0.35	
	USART3	0.35	
	I2C1	0.39	
	I2C2	0.39	
	USB OTG FS	0.65	
	CAN	0.72	
APB2	GPIO A	0.47	mA
	GPIO B	0.47	
	GPIO C	0.47	
	GPIO D	0.47	
	GPIO E	0.47	
	ADC1(2)	1.81	
	ADC2	1.78	
	TIM1	1.6	
	SPI1	0.43	
	USART1	0.85	

1. f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. Specific conditions for ADC: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2/4}$, ADON bit in the ADC_CR2 register is set to 1.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		0	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		16			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
$DuCy_{(HSE)}$	Duty cycle		45		55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)			5		pF
$DuCy_{(LSE)}$	Duty cycle		30		70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram

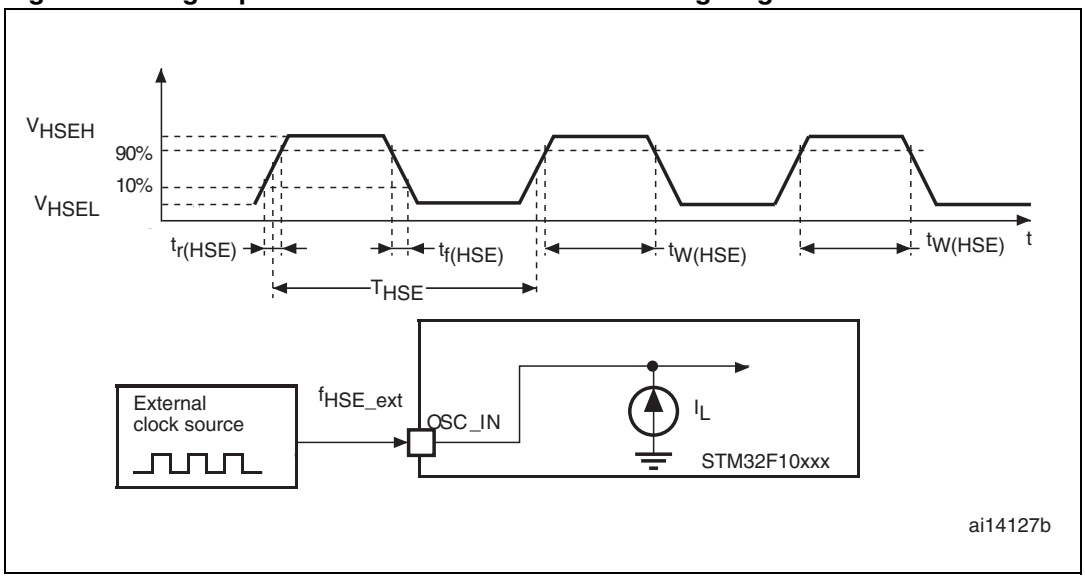
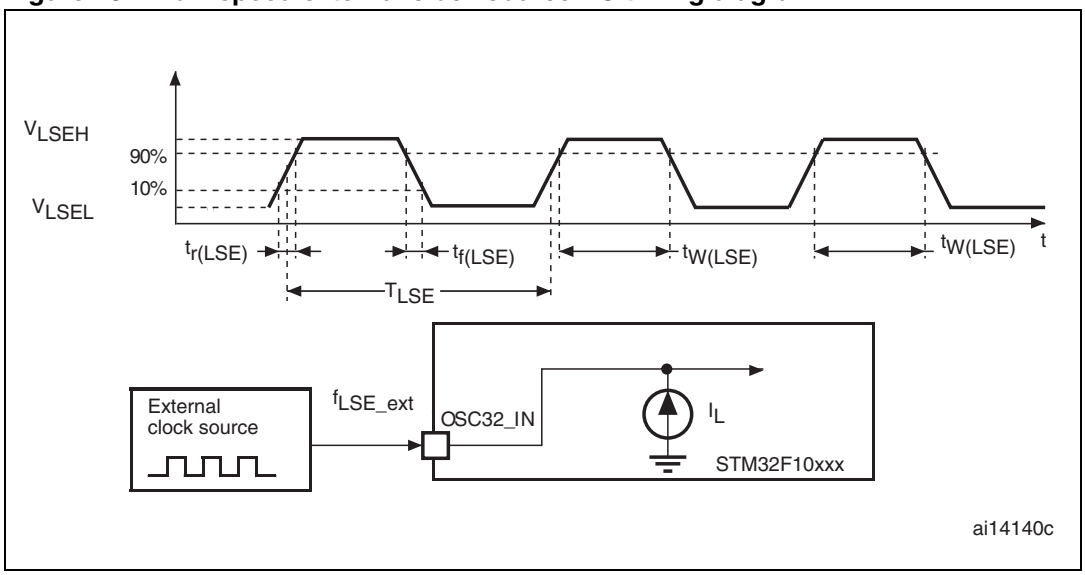


Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

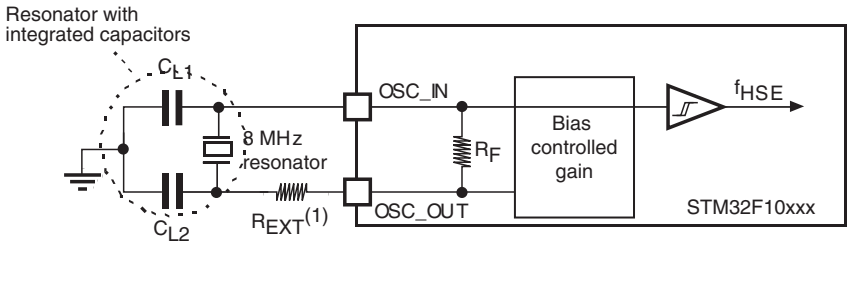
The high-speed external (HSE) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 22*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HSE 3-25 MHz oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		3		25	MHz
R_F	Feedback resistor			200		kΩ
C_{L1} C_{L2}(3)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(4)	R_S = 30 Ω		30		pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load			1	mA
g_m	Oscillator transconductance	Startup	25			mA/V
$t_{SU(HSE}$(5)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.
4. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics. Typical value is in the range of 5 to 6R_S.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

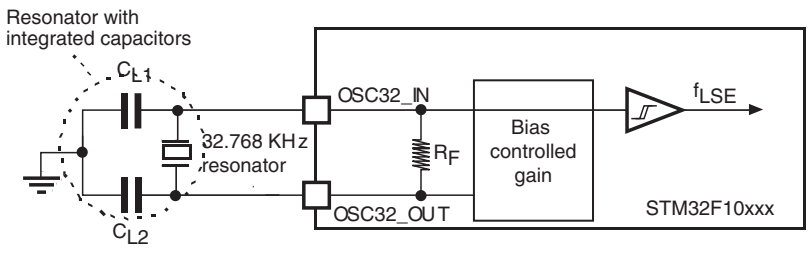
Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Table 23. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			5		MΩ
C_{L1} C_{L2}(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ			15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}			1.4	µA
g_m	Oscillator Transconductance		5			µA/V
$t_{SU(LSE)}$(4)	startup time	V_{DD} is stabilized		3		s

1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs above the table.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

Figure 18. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 24* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

High-speed internal (HSI) RC oscillator

Table 24. HSI oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
ACC_{HSI}	Accuracy of HSI oscillator	T_A = –40 to 105 °C		±1	±3	%
		T_A = –10 to 85 °C		±1	±2.5	%
		T_A = 0 to 70 °C		±1	±2.2	%
		T_A = 25 °C		±1	±2	%
$t_{su(HSI)}$	HSI oscillator start up time		1		2	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100	µA

1. Guaranteed by design, not tested in production.
2. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption		0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 26. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	Wakeup on HSI RC clock	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	HSI RC wakeup time = 2 µs	3.6	µs
	Wakeup from Stop mode (regulator in low power mode)	HSI RC wakeup time = 2 µs, Regulator wakeup from LP mode time = 5 µs	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	HSI RC wakeup time = 2 µs, Regulator wakeup from power down time = 38 µs	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

5.3.8 PLL characteristics

The parameters given in *Table 27* and *Table 28* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 27. PLL1 characteristics

Symbol	Parameter	Value		Unit
		Min(1)	Max(1)	
f_{PLL_IN}	PLL input clock(2)	8	12	MHz
	Pulse width at high level	30		ns
f_{PLL_OUT}	PLL multiplier output clock	48	72	MHz
f_{VCO_OUT}	PLL VCO output	96	144	MHz
t_{LOCK}	PLL lock time		350	µs

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

Table 28. PLL2 and PLL3 characteristics

Symbol	Parameter	Value		Unit
		Min(1)	Max(1)	
f_{PLL_IN}	PLL input clock(2)	3	5	MHz
	Pulse width at high level	30		ns
f_{PLL_OUT}	PLL multiplier output clock	40	74	MHz
f_{VCO_OUT}	PLL VCO output	80	148	MHz
t_{LOCK}	PLL lock time		350	µs

1. Based on characterization, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V			20	mA
		Write / Erase modes f_{HCLK} = 72 MHz, V_{DD} = 3.3 V			5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value			Unit
			Min(1)	Typ	Max	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10			kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30			Years
		1 kcycle(2) at T_A = 105 °C	10			
		10 kcycles(2) at T_A = 55 °C	20			

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 1000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 31*. They are based on the EMS levels and classes defined in application note AN1709.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 1000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 1000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with SAE J 1752/3 standard which specifies the test board and the pin loading.

Table 32. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with SAE J 1752/3	0.1 to 30 MHz	12	12	dBµV
			30 to 130 MHz	22	19	
			130 MHz to 1GHz	23	29	
			SAE EMI Level	4	4	-

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 33. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 34. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.12 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	TTL ports	–0.5		0.8	V
V_{IH}	Standard IO input high level voltage		2		V_{DD}+0.5	
	IO FT(1) input high level voltage		2		5.5V	
V_{IL}	Input low level voltage	CMOS ports	–0.5		0.35 V_{DD}	V
V_{IH}	Input high level voltage		0.65 V_{DD}		V_{DD}+0.5	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)		200			mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			mV
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os			±1	µA
		V_{IN}= 5 V I/O FT			3	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required), their characteristics consider the most strict CMOS-technology or TTL parameters:

- For V_{IH}:
  - if V_{DD} is in the [2.00 V - 3.08 V] range: CMOS characteristics but TTL included
  - if V_{DD} is in the [3.08 V - 3.60 V] range: TTL characteristics but CMOS included
- For V_{IL}:
  - if V_{DD} is in the [2.00 V - 2.28 V] range: TTL characteristics but CMOS included
  - if V_{DD} is in the [2.28 V - 3.60 V] range: CMOS characteristics but TTL included

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink +20 mA (with a relaxed V_{OL}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 36* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 36. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH}(2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V		0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4		
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		1.3	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3		
V_{OL}(1)(3)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V		0.4	V
V_{OH}(2)(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4		

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 7* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. Based on characterization data, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 19* and *Table 37*, respectively.

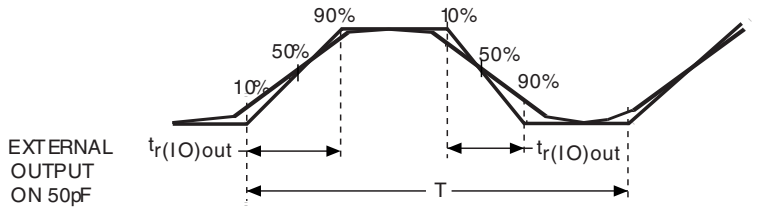
Unless otherwise specified, the parameters given in *Table 37* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 37. I/O AC characteristics(1)

MODEx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			25(3)	
11	$F_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 19*.
3. Guaranteed by design, not tested in production.

Figure 19. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%) when loaded by 50pF

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5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 35*).

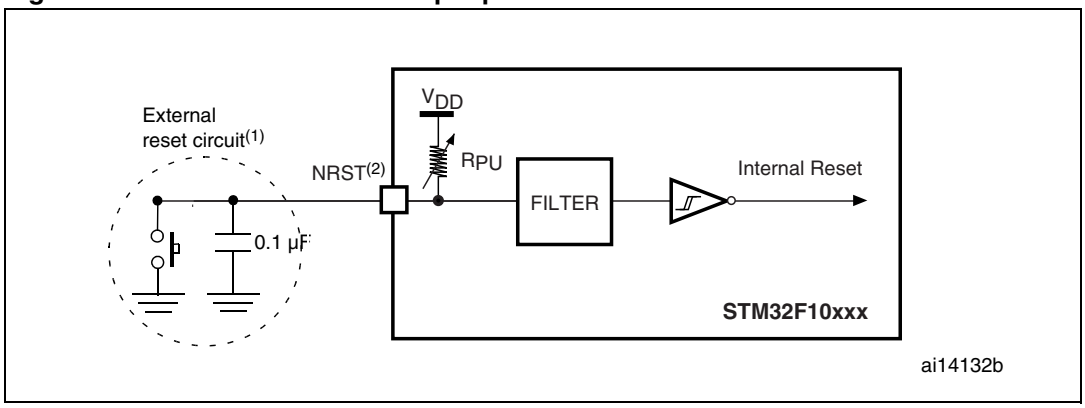
Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 38. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 20. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 38*. Otherwise the reset will not be taken into account by the device.

5.3.14 TIM timer characteristics

The parameters given in *Table 39* are guaranteed by design.

Refer to *Section 5.3.12: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 39. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution			16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz		59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

5.3.15 Communications interfaces

I²C interface characteristics

Unless otherwise specified, the parameters given in *Table 40* are derived from tests performed under the ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

The STM32F105xx and STM32F107xx I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

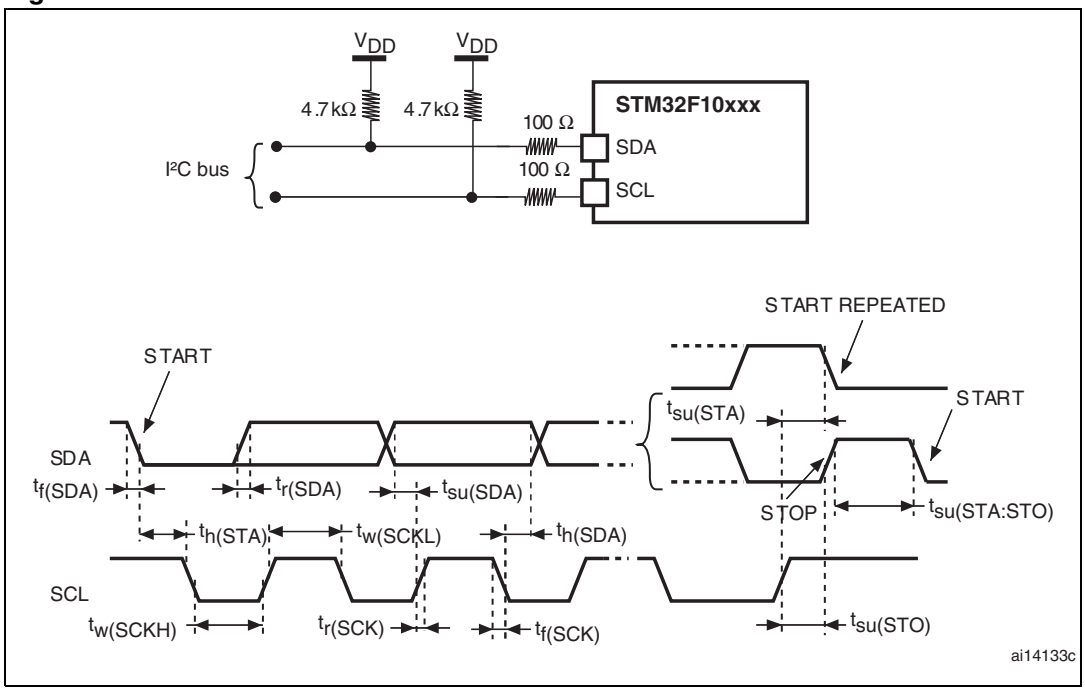
The I²C characteristics are described in *Table 40*. Refer also to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 40. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 4 MHz to achieve the maximum fast mode I²C frequency.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Figure 21. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 41. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I^2S - SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 42* for SPI or in *Table 43* for I^2S are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 42. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	18	MHz
		Slave mode	0	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
$t_{su(NSS)}$(2)	NSS setup time	Slave mode	4 t_{PCLK}		
$t_{h(NSS)}$(2)	NSS hold time	Slave mode	73		
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (2)	Data input setup time Master mode	SPI1	1		
		SPI2	5		
$t_{su(SI)}$(2)	Data input setup time Slave mode		1		
$t_{h(MI)}$ (2)	Data input hold time Master mode	SPI1	1		
		SPI2	5		
$t_{h(SI)}$(2)	Data input hold time Slave mode		3		
$t_{a(SO)}$(2)(3)	Data output access time	Slave mode, f_{PCLK} = 36 MHz, presc = 4	0	55	
		Slave mode, f_{PCLK} = 24 MHz	0	4 t_{PCLK}	
$t_{dis(SO)}$(2)(4)	Data output disable time	Slave mode	10		
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)		25	
$t_{v(MO)}$(2)(1)	Data output valid time	Master mode (after enable edge)		3	
$t_{h(SO)}$(2)	Data output hold time	Slave mode (after enable edge)	25		
$t_{h(MO)}$(2)		Master mode (after enable edge)	4		

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 22. SPI timing diagram - slave mode and CPHA = 0

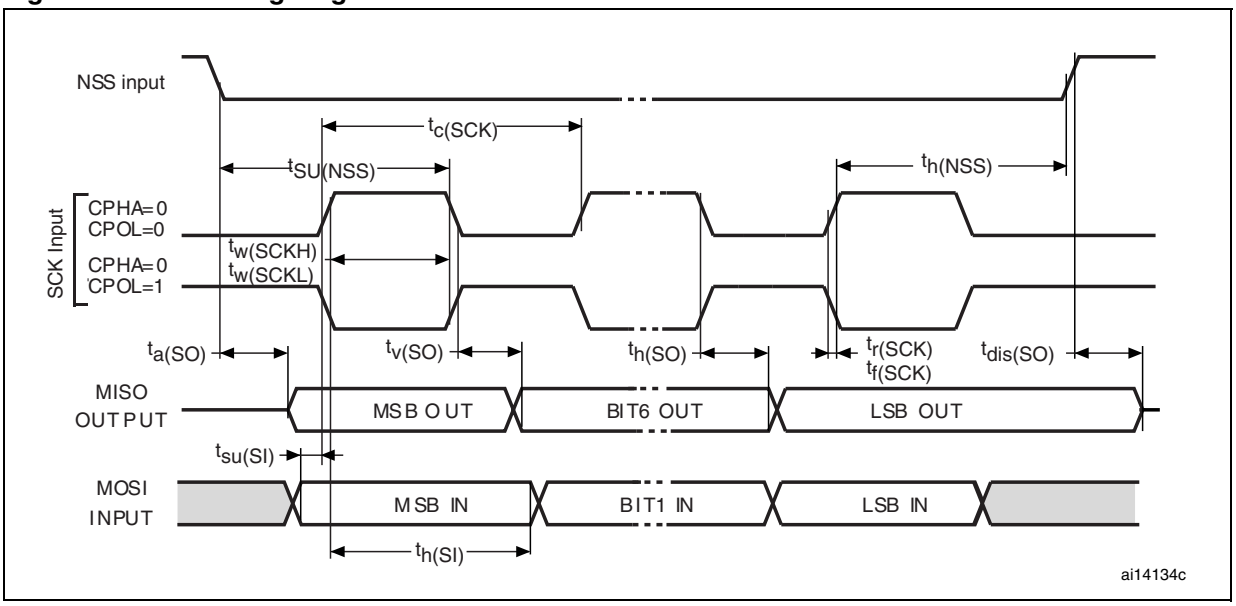
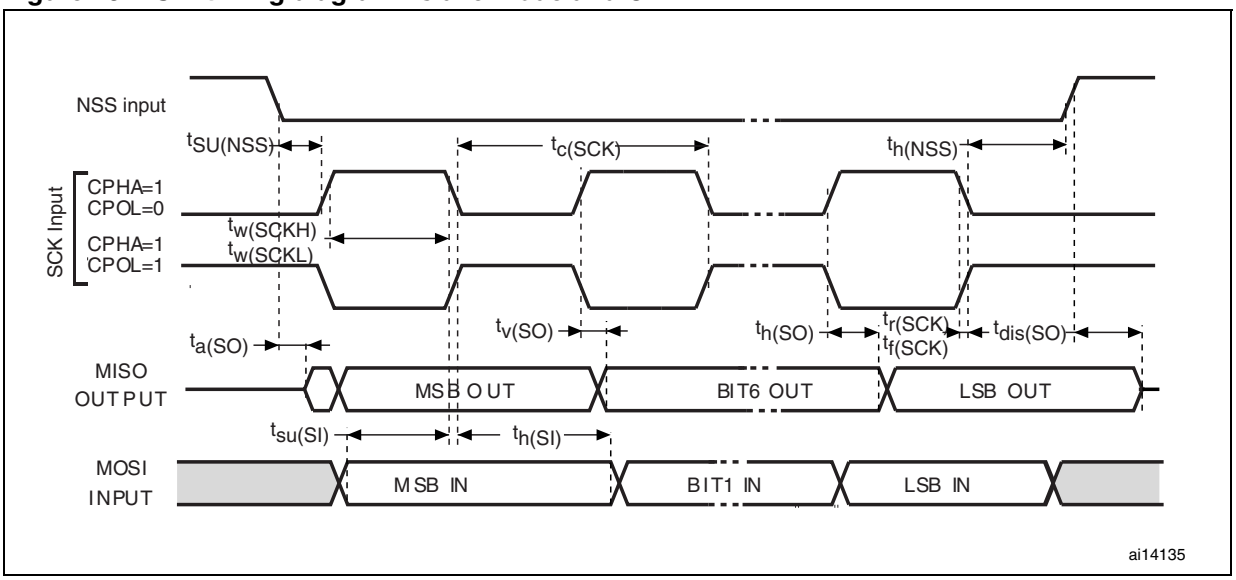
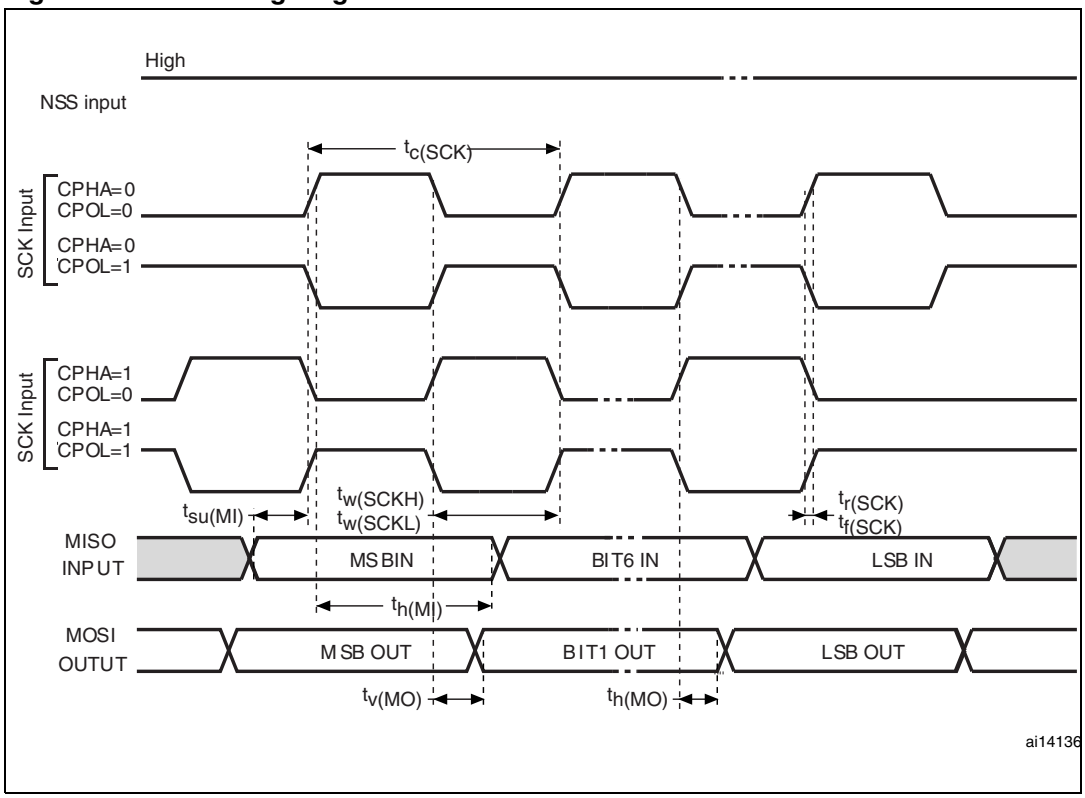


Figure 23. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 24. SPI timing diagram - master mode(1)



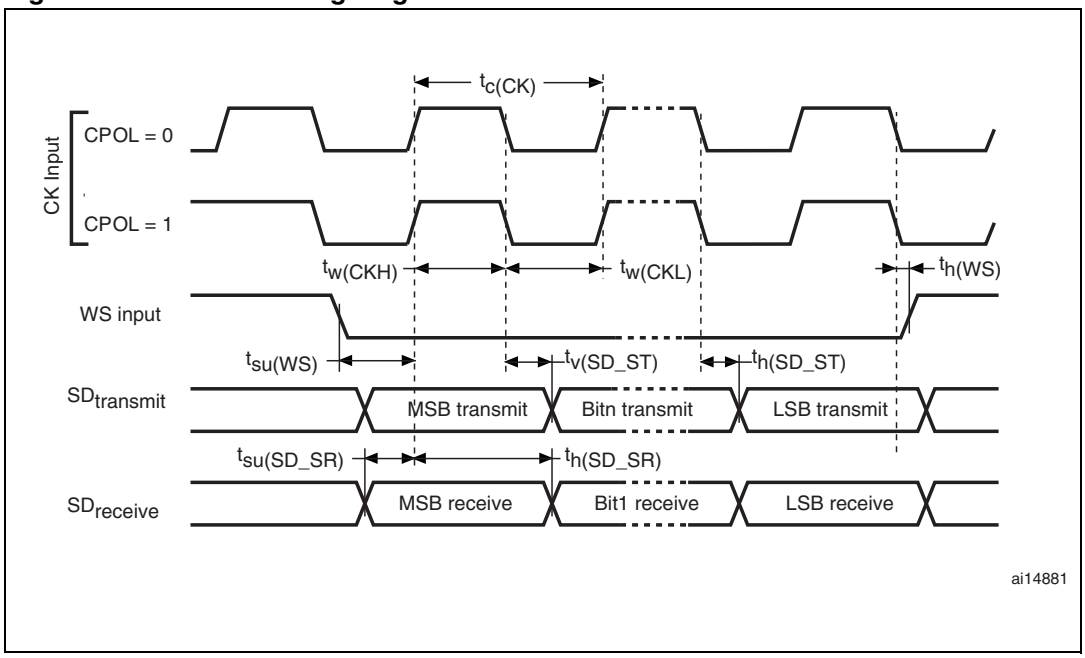
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 43. I^2S characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master	TBD	TBD	MHz
		Slave	0	TBD	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF		TBD	ns
$t_{v(WS)}$ (2)	WS valid time	Master	TBD		
$t_{h(WS)}$ (2)	WS hold time	Master	TBD		
$t_{su(WS)}$ (2)	WS setup time	Slave	TBD		
$t_{h(WS)}$ (2)	WS hold time	Slave	TBD		
$t_{w(CKH)}$ (2) $t_{w(CKL)}$ (2)	CK high and low time	Master f_{PCLK}= TBD, presc = TBD	TBD		
$t_{su(SD\_MR)}$ (2) $t_{su(SD\_SR)}$ (2)	Data input setup time	Master receiver Slave receiver	TBD TBD		
$t_{h(SD\_MR)}$ (2)(3) $t_{h(SD\_SR)}$ (2)(3)	Data input hold time	Master receiver Slave receiver	TBD TBD		
$t_{h(SD\_MR)}$ (2) $t_{h(SD\_SR)}$ (2)	Data input hold time	Master f_{PCLK} = TBD Slave f_{PCLK} = TBD	TBD TBD		
$t_{v(SD\_ST)}$ (2)(3)	Data output valid time	Slave transmitter (after enable edge)		TBD	
		f_{PCLK} = TBD		TBD	
$t_{h(SD\_ST)}$ (2)	Data output hold time	Slave transmitter (after enable edge)	TBD		
$t_{v(SD\_MT)}$ (2)(3)	Data output valid time	Master transmitter (after enable edge)		TBD	
		f_{PCLK} = TBD	TBD	TBD	
$t_{h(SD\_MT)}$ (2)	Data output hold time	Master transmitter (after enable edge)	TBD		

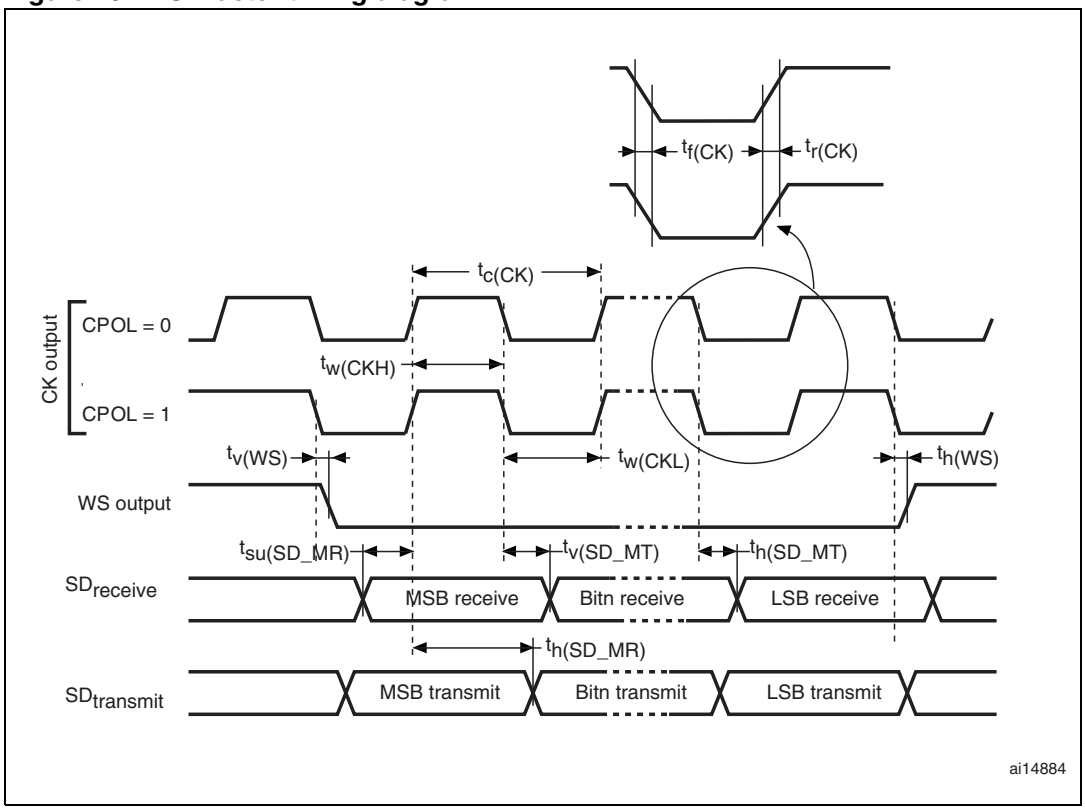
1. TBD = to be determined.
2. Based on design simulation and/or characterization results, not tested in production.
3. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Figure 25. I²S slave timing diagram(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Figure 26. I²S master timing diagram(1)



1. Based on characterization, not tested in production.

USB OTG FS characteristics

The USB OTG interface is USB-IF certified (Full-Speed).

Table 44. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Table 45. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage(2)		3.0(3)	3.6	V
	V_{DI}(4)	Differential input sensitivity	I(USBDP, USBDM)	0.2		V
	V_{CM}(4)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
	V_{SE}(4)	Single ended receiver threshold		1.3	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(5)		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(5)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The STM32F105xx and STM32F107xx USB OTG FS functionality is ensured down to 2.7 V but not the full USB OTG FS electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
4. Guaranteed by design, not tested in production.
5. R_L is the load connected on the USB OTG FS drivers

Figure 27. USB OTG FS timings: definition of data signal rise and fall time

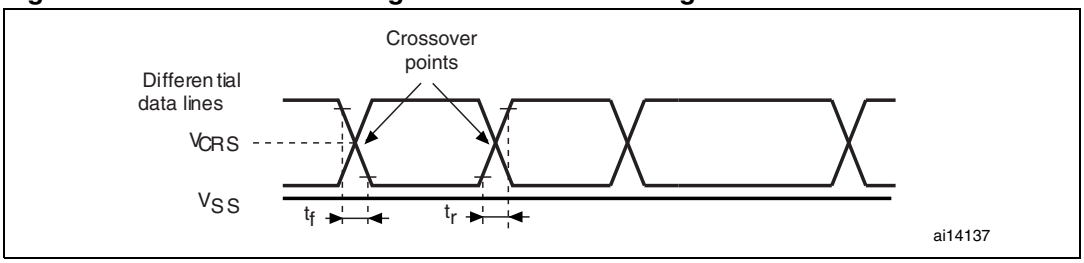


Table 46. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design, not tested in production.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

Ethernet dynamic characteristics

Table 47 gives the list of Ethernet MAC signals for the SMI (station management interface) and *Figure 28* shows the corresponding timing diagram.

Figure 28. Ethernet SMI timing diagram

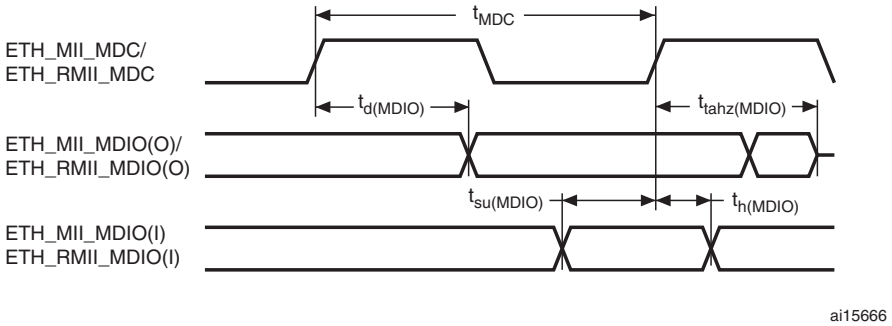


Table 47. Dynamics characteristics: Ethernet MAC signals for SMI(1)

Symbol	Rating	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time	TBD	TBD	TBD	ns
$t_{d(MDIO)}$	MDIO write data valid time	TBD	TBD	TBD	ns
$t_{tahz(MDIO)}$	MDC clock rise time to high impedance (turn around)	TBD	TBD	TBD	ns
$t_{su(MDIO)}$	Read data setup time	TBD	TBD	TBD	ns
$t_{h(MDIO)}$	Read data hold time	TBD	TBD	TBD	ns

1. TBD stands for to be determined.

Table 48 gives the list of Ethernet MAC signals for the RMII and *Figure 29* shows the corresponding timing diagram.

Figure 29. Ethernet RMII timing diagram

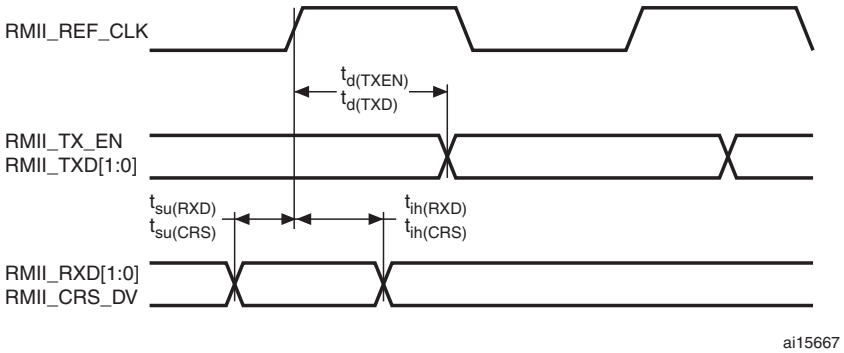


Table 48. Dynamics characteristics: Ethernet MAC signals for RMII(1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	TBD	TBD	TBD	ns
$t_{ih(RXD)}$	Receive data hold time	TBD	TBD	TBD	ns
$t_{su(CRS)}$	Carrier sense set-up time	TBD	TBD	TBD	ns
$t_{ih(CRS)}$	Carrier sense hold time	TBD	TBD	TBD	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	TBD	TBD	TBD	ns
$t_{d(TXD)}$	Transmit data valid delay time	TBD	TBD	TBD	ns

1. TBD stands for to be determined.

Table 49 gives the list of Ethernet MAC signals for MII and *Figure 29* shows the corresponding timing diagram.

Figure 30. Ethernet MII timing diagram

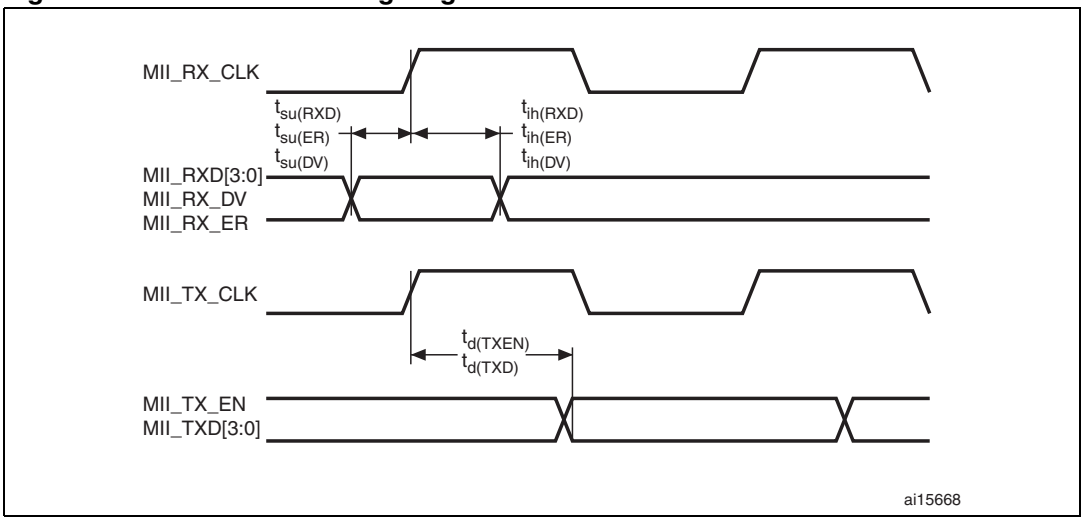


Table 49. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Rating	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	TBD	TBD	TBD	ns
$t_{ih(RXD)}$	Receive data hold time	TBD	TBD	TBD	ns
$t_{su(DV)}$	Data valid setup time	TBD	TBD	TBD	ns
$t_{ih(DV)}$	Data valid hold time	TBD	TBD	TBD	ns
$t_{su(ER)}$	Error setup time	TBD	TBD	TBD	ns
$t_{ih(ER)}$	Error hold time	TBD	TBD	TBD	ns
$t_{d(TXEN)}$	Transmit enable valid delay time	TBD	TBD	TBD	ns
$t_{d(TXD)}$	Transmit data valid delay time	TBD	TBD	TBD	ns

1. TBD stands for to be determined.

CAN (controller area network) interface

Refer to *Section 5.3.12: I/O port characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 9*.

Note: It is recommended to perform a calibration after each power-up.

Table 50. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply		2.4		3.6	V
V_{REF+}	Positive reference voltage		2.4		V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin			160(1)	220(1)	µA
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(2)	Sampling rate		0.05		1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)		V_{REF+}	V
R_{AIN}(2)	External input impedance		See *Equation 1* and *Table 51*			kΩ
R_{ADC}(2)	Sampling switch resistance				1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor				12	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz			0.214	µs
					3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 50*.

Equation 1: R_{AIN} max formula:

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 51. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	1.2
7.5	0.54	10
13.5	0.96	19
28.5	2.04	41
41.5	2.96	60
55.5	3.96	80
71.5	5.11	104
239.5	17.1	350

1. Based on characterization, not tested in production.

Table 52. ADC accuracy - limited test conditions(1) (2)

Symbol	Parameter	Test conditions	Typ	Max(3)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V, T_A = 25 °C, Measurements made after ADC calibration	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
3. Based on characterization, not tested in production.

Table 53. ADC accuracy(1) (2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.12* does not affect the ADC accuracy.
4. Based on characterization, not tested in production.

Figure 31. ADC accuracy characteristics

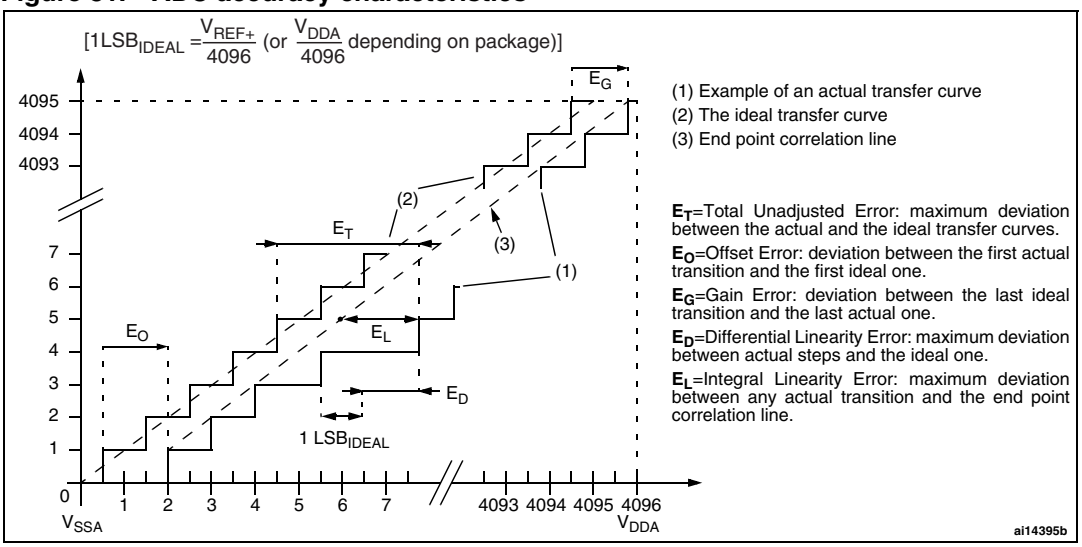
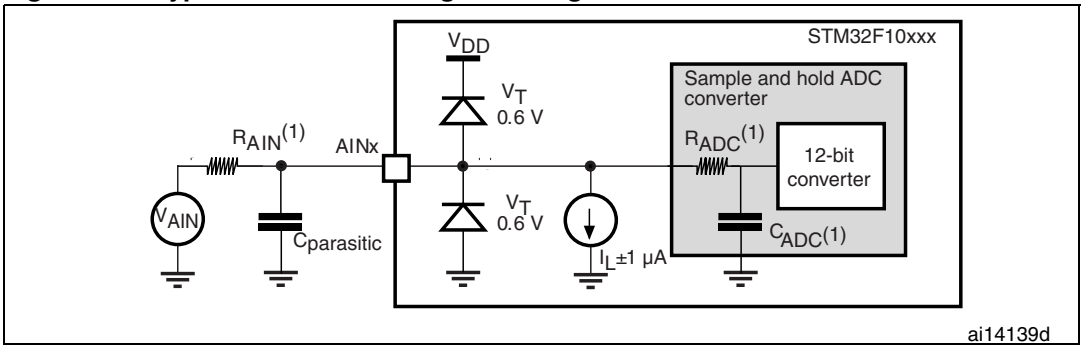


Figure 32. Typical connection diagram using the ADC

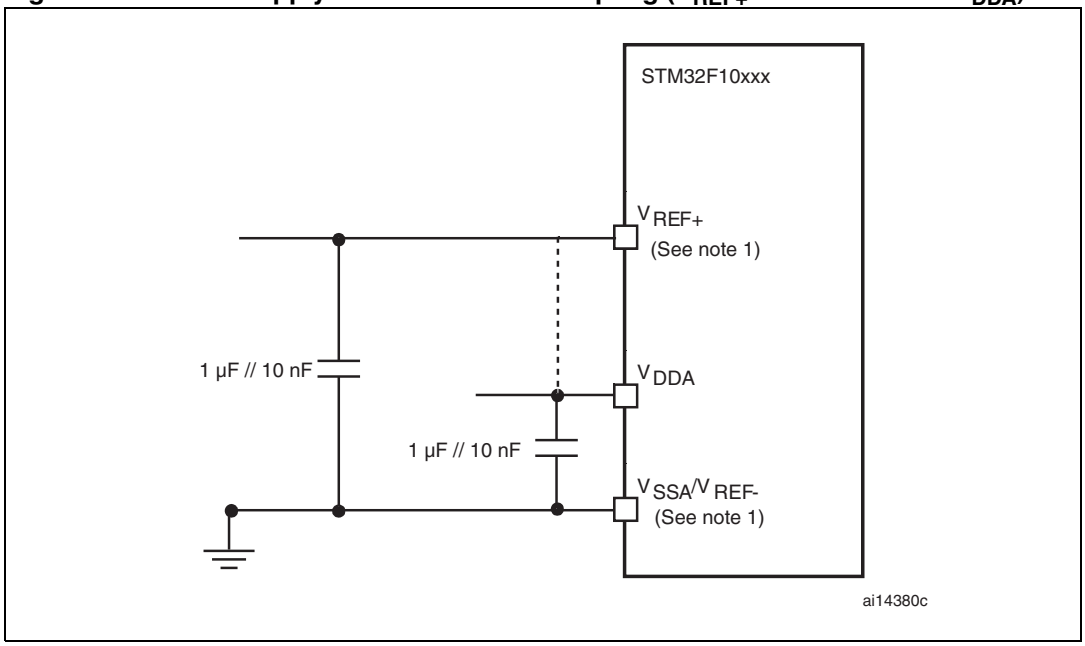


1. Refer to *Table 50* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

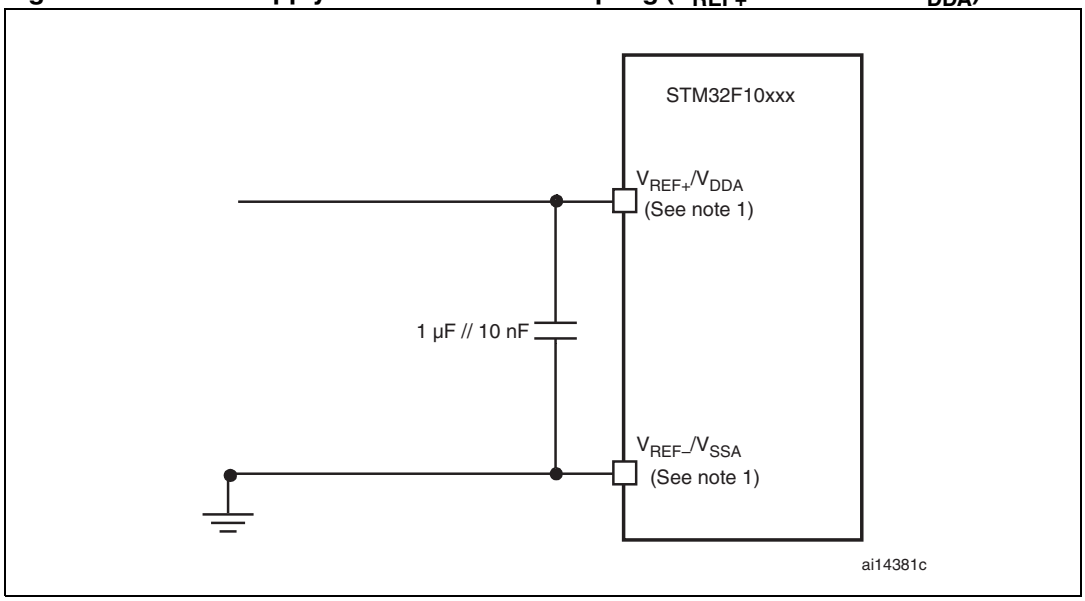
Power supply decoupling should be performed as shown in *Figure 33* or *Figure 34*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 33. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 34. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

5.3.17 DAC electrical specifications

Table 54. DAC characteristics

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
V_{DD33A}	Analog supply voltage	2.4		3.6	V	
V_{DD18D}	Digital supply voltage	1.6	1.8	2	V	
V_{REF+}	Reference supply voltage	2.4		3.6	V	V_{REF+} must always be below V_{DD33A}
V_{SSA}	Ground	0		0	V	
R_L	Resistive load with buffer ON	5			kΩ	Minimum resistive load between DAC_OUT and V_{SSA}
C_L	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin.
DAC_OUT min	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC it corresponds to 12-bit input code (0E0)h to (F1C)h @ V_{REF+} = 3.6 V and (155)h and (EAB)h @ V_{REF+} = 2.4 V
DAC_OUT max	Higher DAC_OUT voltage with buffer ON			V_{REF+}– 0.2 V	V	
I_{DD}	DAC DC current consumption in quiescent mode (Standby mode) (in V_{DD18D}+V_{DD33A}+ V_{REF+})		425	600	µA	With no load, middle code (800)H on the inputs
			500	700	µA	With no load, worst code (F1C)H @ V_{REF+} = 3.6 V in terms of DC consumption on the inputs
I_{DDQ}	DAC DC current consumption in Power Down mode (in V_{DD18D}+V_{DD33A}+V_{REF+})		5	350	nA	With no load.
	DAC DC current consumption in Power Down mode (in V_{DD33A}+V_{REF+})		5	200		
DNL	Differential non linearity (Difference between two consecutive code-1LSB)		±0.5		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
INL	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)		±1		LSB	Given for the DAC in 10-bit configuration (B1=B0=0 always)
Offset	Offset error (difference between measured value at Code (800)H and the ideal value = V_{REF+}/2		±10		mV	Given for the DAC in 10-bit configuration (B1=B0=0 always)
			±3		LSB	Given for the DAC in 10-bit @ V_{REF+} = 3.6 V
Gain error	Gain error		±0.5		%	Given for the DAC in 10-bit configuration (B1=B0=0 always)
Amplifier gain	Gain of the amplifier in open loop	80	85		dB	with a 5 kΩ load (worst case)

Table 54. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max(1)	Unit	Comments
$t_{SETTLING}$	Settling time (full scale: for an 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB		3	4	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
t_{WAKEUP}	Wakeup time from off state (PDV18 from 1 to 0)		6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+	Power supply rejection ratio (to V_{DD33A}) (static DC measurement		–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by characterization, not tested in production.

5.3.18 Temperature sensor characteristics

Table 55. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4		10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature			17.1	µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

6 Package characteristics

6.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 35. LFBGA100 - low profile fine pitch ball grid array package outline

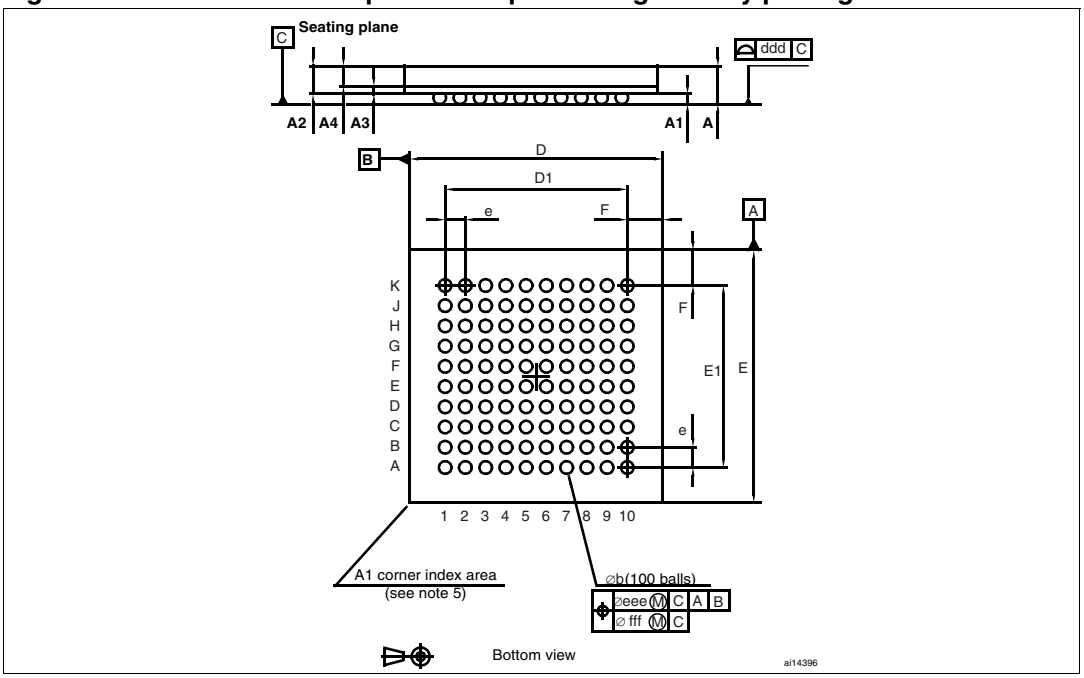
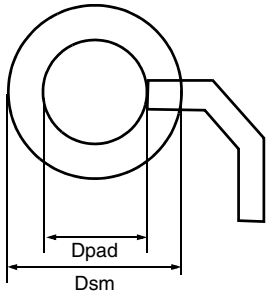


Table 56. LFBGA100 - low profile fine pitch ball grid array package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.700			0.0026
A1	0.270			0.0004		
A2		1.085			0.0017	
A3		0.30			0.0005	
A4			0.80			0.0012
b	0.45	0.50	0.55	0.0007	0.0008	0.0009
D	9.85	10.00	10.15	0.0153	0.0155	0.0157
D1		7.20			0.0111	
E	9.85	10.00	10.15	0.0153	0.0155	0.0157
E1		7.20			0.0111	
e		0.80			0.0012	
F		1.40			0.0022	
ddd		0.12			0.0002	
eee		0.15			0.0002	
fff		0.08			0.0001	
N (number of balls)	100					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. Recommended PCB design rules (0.80/0.75 mm pitch BGA)



Dpad	0.37 mm
Dsm	0.52 mm typ. (depends on solder mask registration tolerance
Solder paste	0.37 mm aperture diameter
– Non solder mask defined pads are recommended – 4 to 6 mils screen print	

Figure 37. LQFP100, 100-pin low-profile quad flat package outline(1)

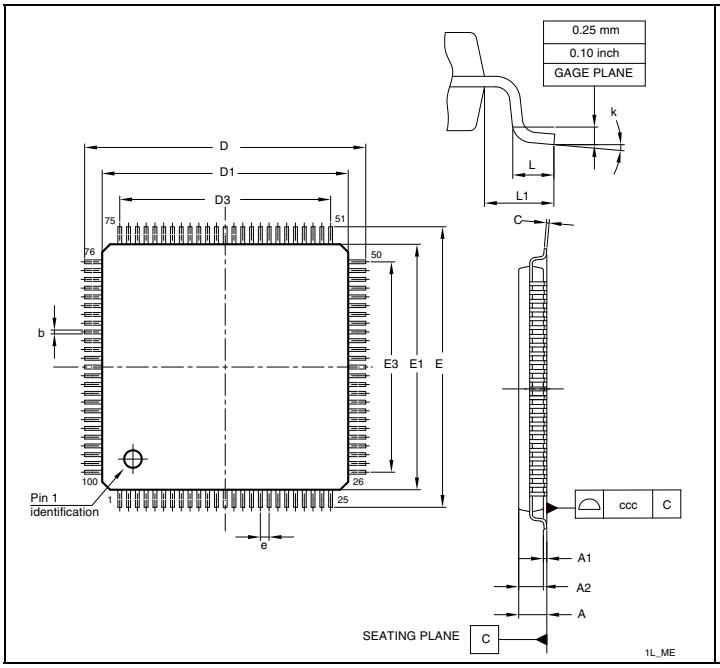
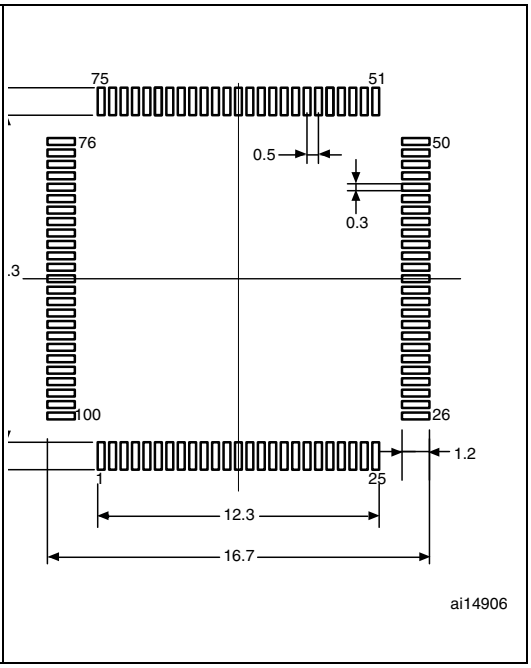


Figure 38. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 57. LQPF100 – 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.60			0.063
A1		0.05	0.15		0.002	0.0059
A2	1.40	1.35	1.45	0.0551	0.0531	0.0571
b	0.22	0.17	0.27	0.0087	0.0067	0.0106
c		0.09	0.20		0.0035	0.0079
D	16.00	15.80	16.20	0.6299	0.622	0.6378
D1	14.00	13.80	14.20	0.5512	0.5433	0.5591
D3	12.00			0.4724		
E	16.00	15.80	16.20	0.6299	0.622	0.6378
E1	14.00	13.80	14.20	0.5512	0.5433	0.5591
E3	12.00			0.4724		
e	0.50			0.0197		
L	0.60	0.45	0.75	0.0236	0.0177	0.0295
L1	1.00			0.0394		
k	3.5°	0°	7°	3.5°	0°	7°
ccc	0.08			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 39. LQFP64 – 64 pin low-profile quad flat package outline(1)

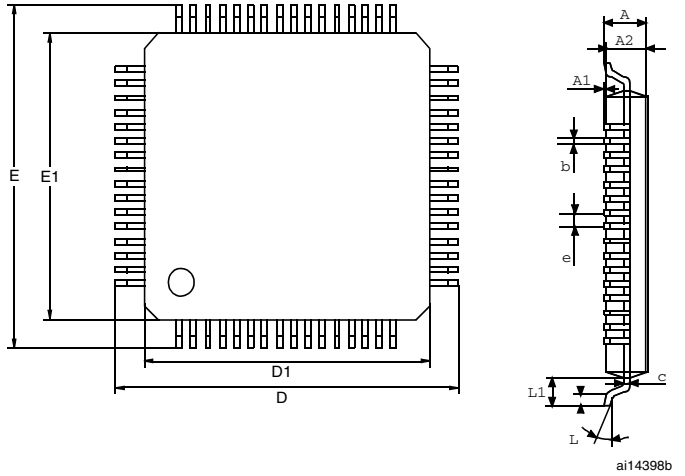
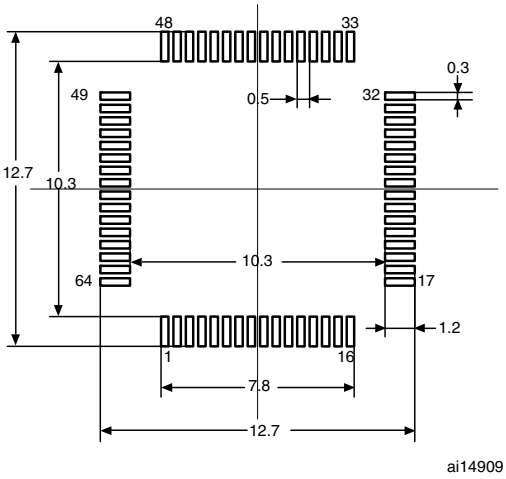


Figure 40. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 58. LQFP64 – 64 pin low-profile quad flat package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7 Part numbering

Table 59. Ordering information scheme

Example: STM32 F 105 R C T 6 xxx

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

105 = connectivity, USB OTG FS

107= connectivity, USB OTG FS & Ethernet

Pin count

R = 64 pins

V = 100 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

H = BGA

T = LQFP

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Options

xxx = programmed parts

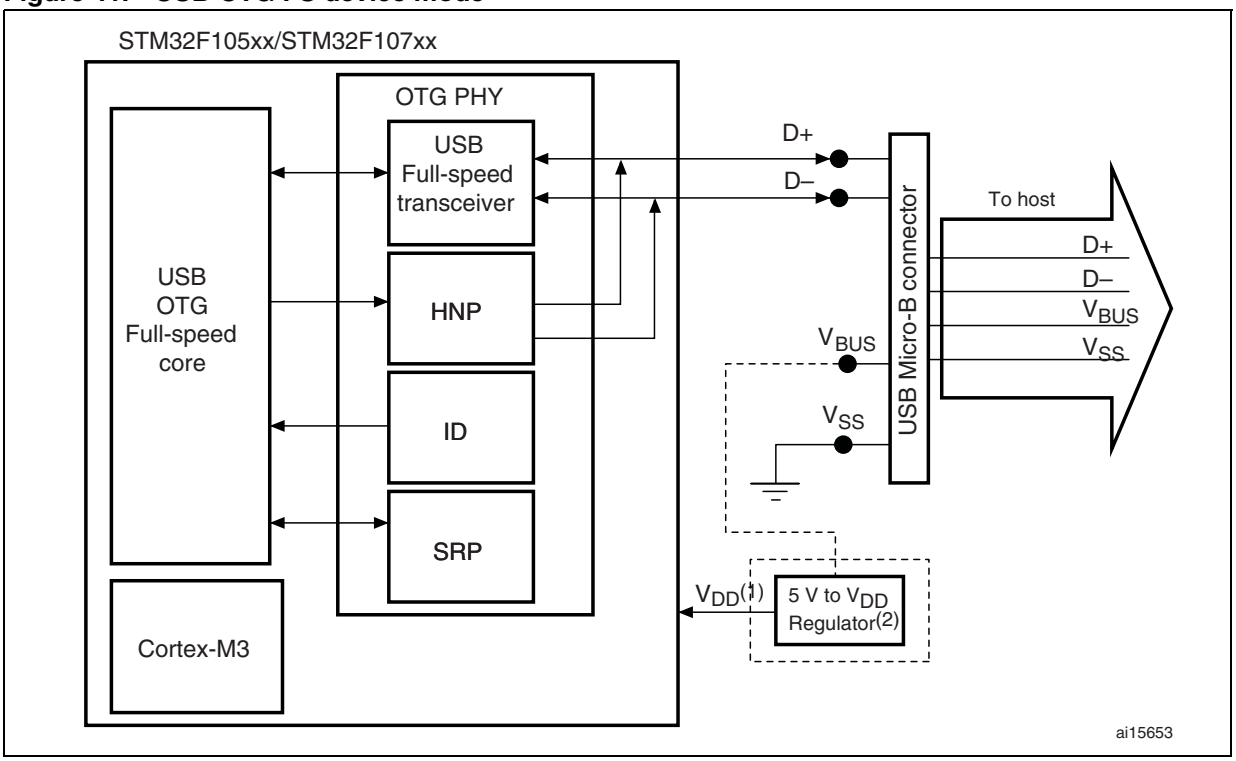
TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Applicative block diagrams

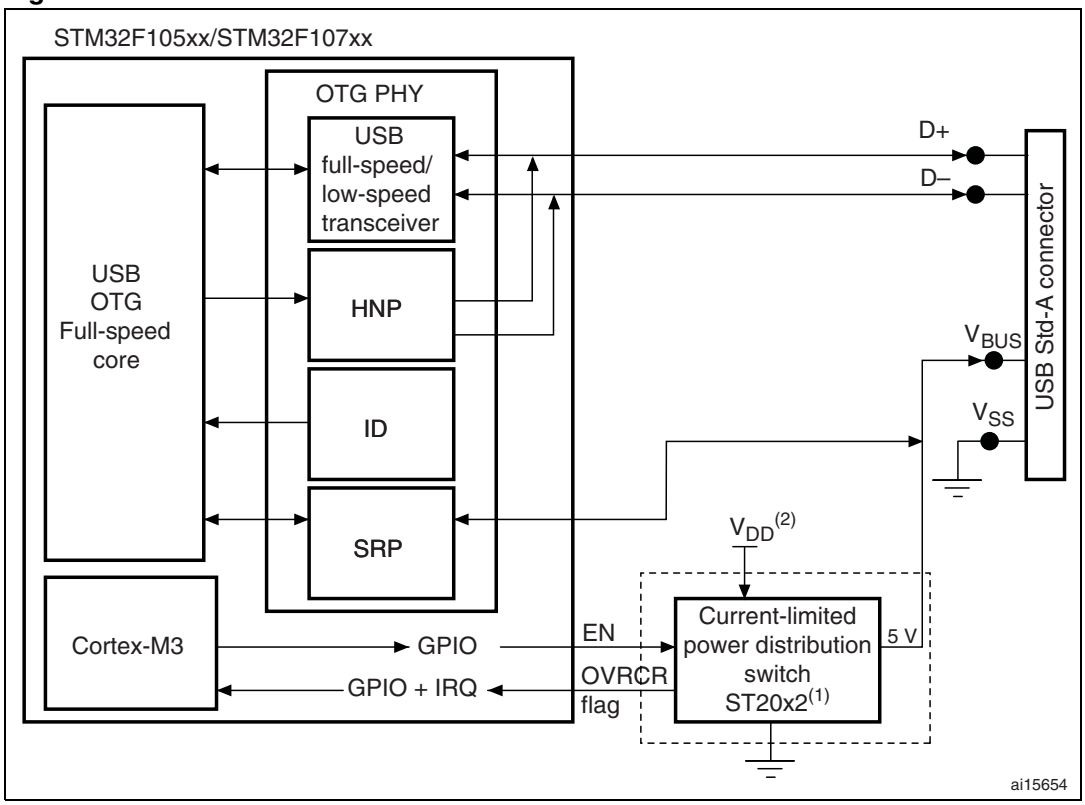
A.1 USB OTG FS interface solutions

Figure 41. USB OTG FS device mode



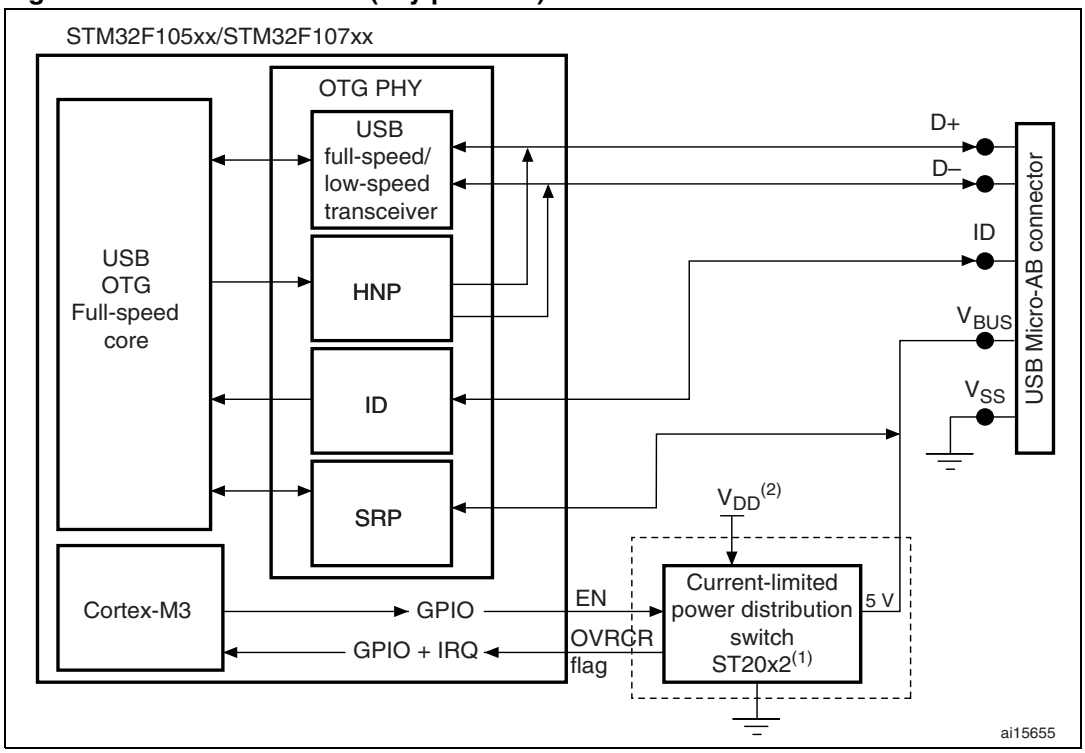
1. V_{DD} ranges between 2 V and 3.6 V.
2. Use a regulator if you want to build a bus-powered device.

Figure 42. Host connection



1. ST20x2 needed only if the application has to support bus-powered devices.
2. V_{DD} ranges between 2 V and 3.6 V.

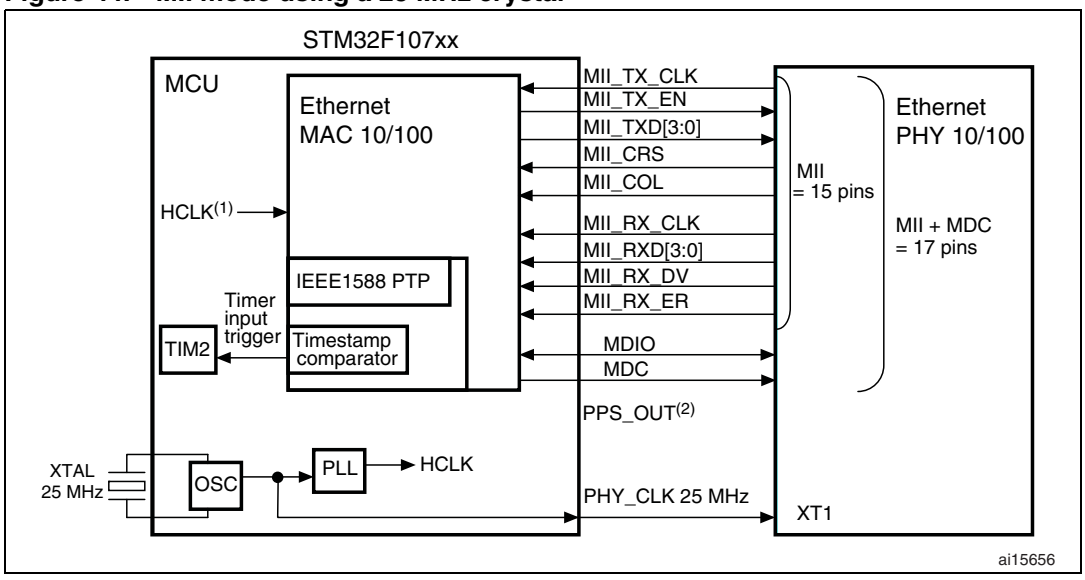
Figure 43. OTG connection (any protocol)



1. ST20x2 needed only if the application has to support bus-powered devices.
2. V_{DD} ranges between 2 V and 3.6 V.

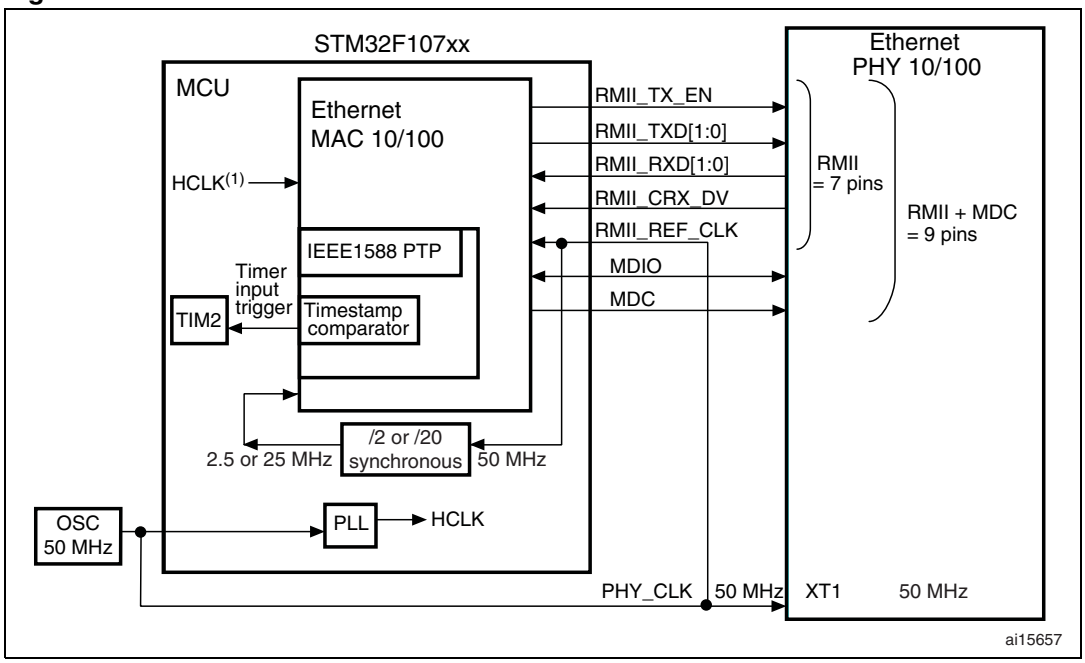
A.2 Ethernet interface solutions

Figure 44. MII mode using a 25 MHz crystal



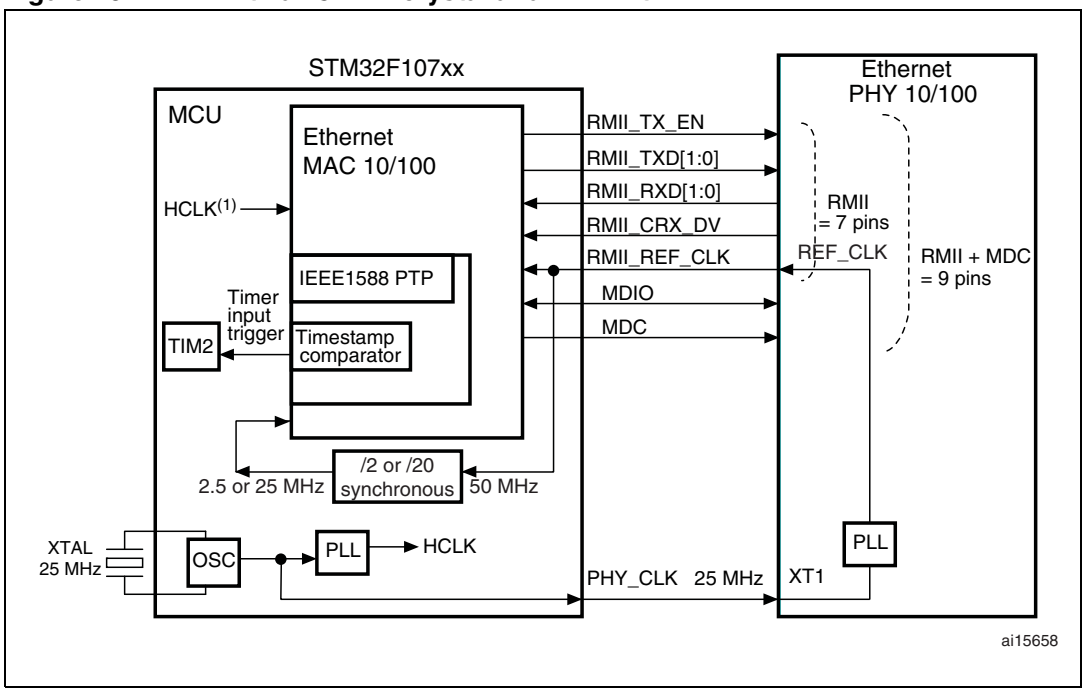
1. HCLK must be greater than 25 MHz.
2. Pulse per second when using IEEE1588 PTP, optional signal.

Figure 45. RMII with a 50 MHz oscillator



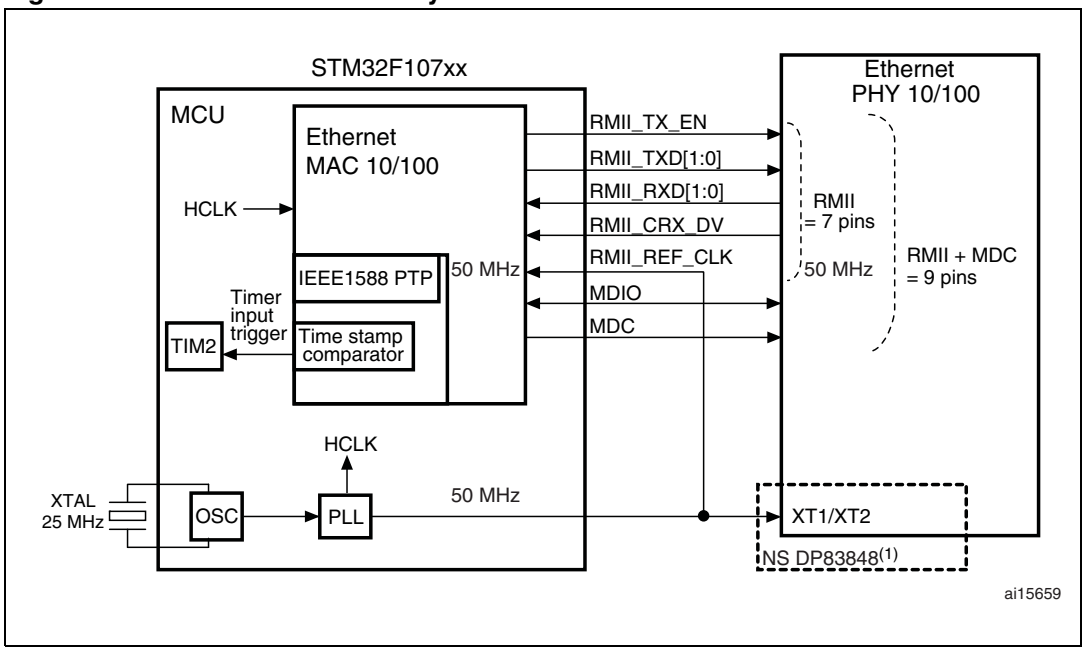
1. HCLK must be greater than 25 MHz.

Figure 46. RMII with a 25 MHz crystal and PHY with PLL



1. HCLK must be greater than 25 MHz.

Figure 47. RMII with a 25 MHz crystal



1. The NS DP83848 is recommended as the input jitter requirement of this PHY. It is compliant with the output jitter specification of the MCU.

A.3 Complete audio player solutions

Two solutions are offered, illustrated in *Figure 48* and *Figure 49*.

Figure 48 shows storage media to audio DAC/amplifier streaming using a software Codec. This solution implements an audio crystal to provide audio class I^2S accuracy on the master clock (0.5% error maximum, see the Serial peripheral interface section in the reference manual for details).

Figure 48. Complete audio player solution 1

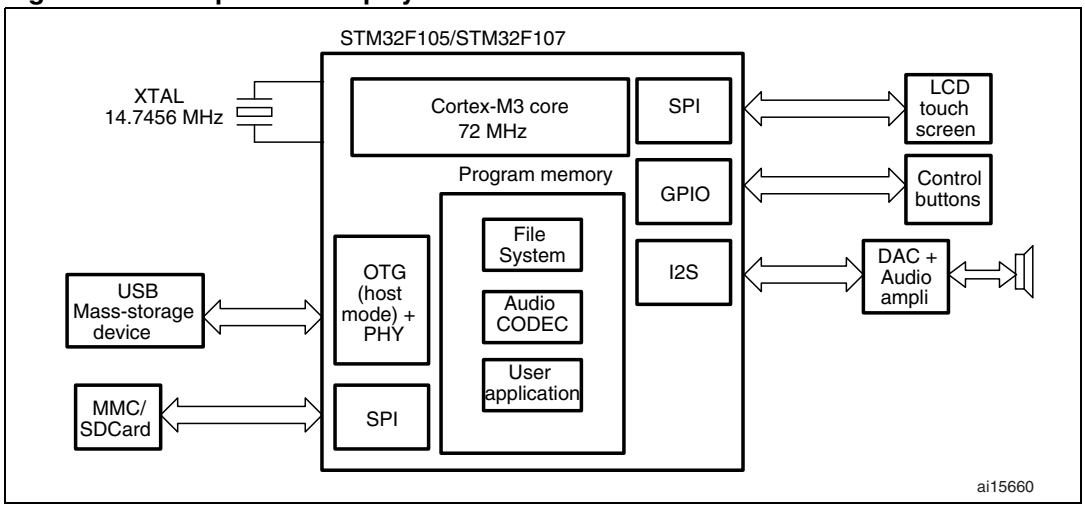
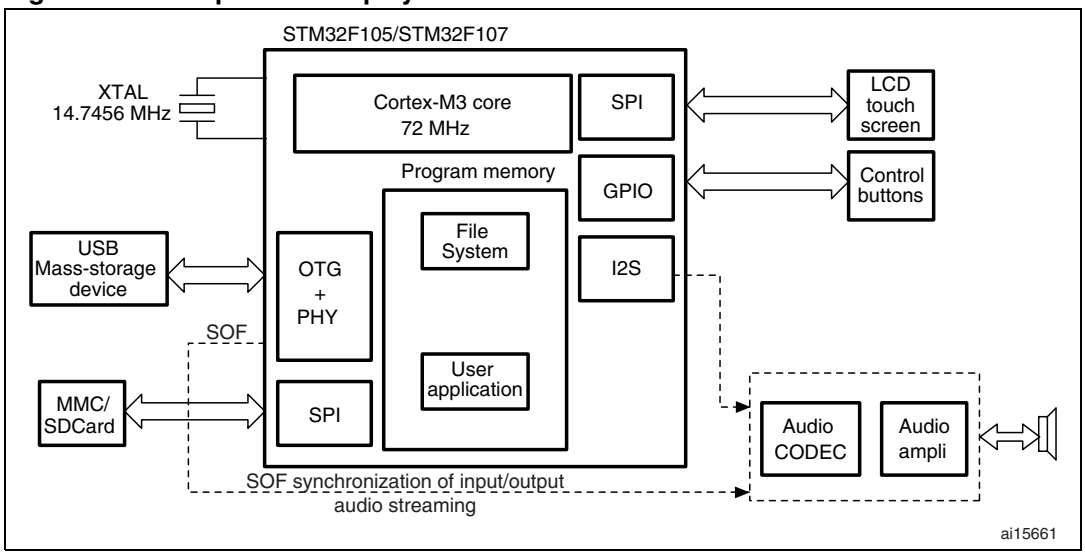


Figure 49 shows storage media to audio Codec/amplifier streaming with SOF synchronization of input/output audio streaming using a hardware Codec.

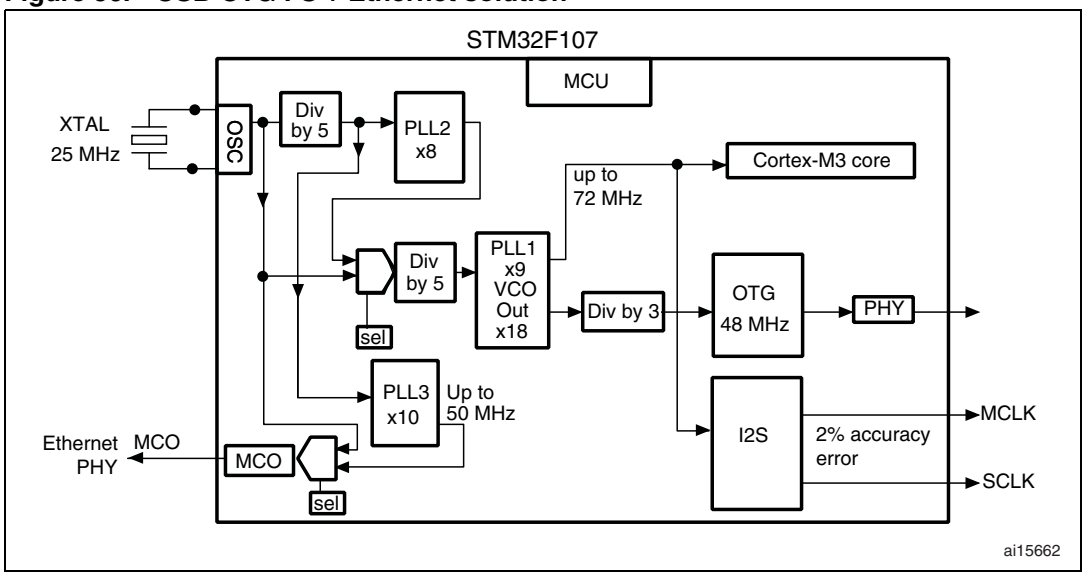
Figure 49. Complete audio player solution 2



A.4 USB OTG FS interface + Ethernet/I²S interface solutions

With the clock tree implemented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the Ethernet (MII/RMII) interfaces. *Figure 50* illustrate the solution.

Figure 50. USB OTG FS + Ethernet solution



With the clock tree implemented on the STM32F107xx, only one crystal is required to work with both the USB (host/device/OTG) and the I²S (Audio) interfaces. *Figure 51* illustrate the solution.

Figure 51. USB OTG FS + I²S (Audio) solution

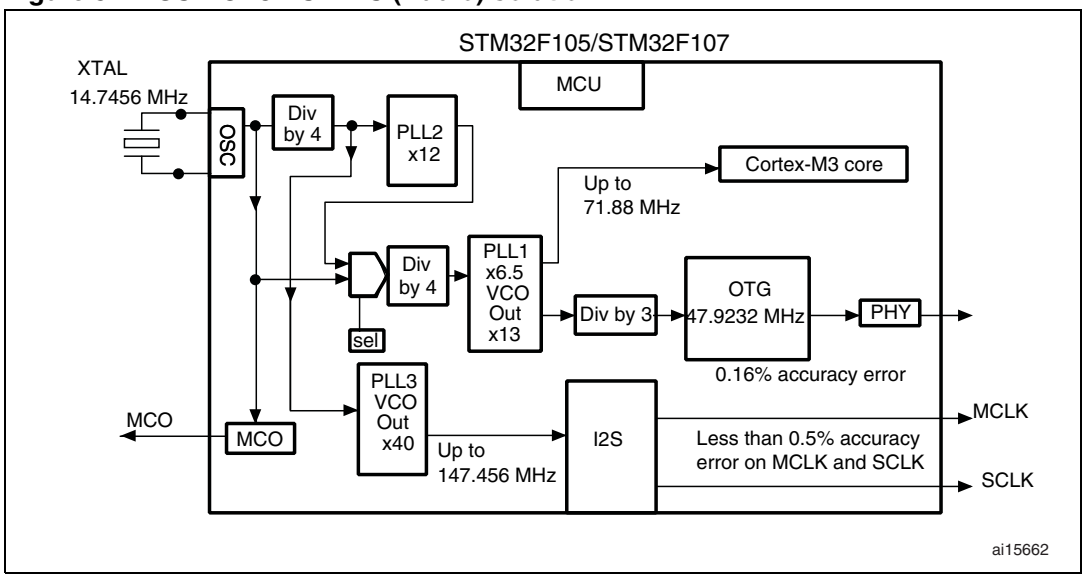


Table 60. PLL configurations

Application	Crystal value in MHz (XT1)	PREDIV2	PLL2MUL	PLL1SRC	PREDIV1	PLL1MUL	USB prescaler (PLL2 VCO output)	PLL3MUL	I2Sn clock input	MCO (main clock output)
Ethernet only	25	/5	PLL2ON x8	PLL2	/5	PLL1ON x9	NA	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG	25	/5	PLL2ON x8	PLL2	/5	PLL1ON x9	/3	PLL3ON x10	NA	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + basic audio	25	/5	PLL2ON x8	PLL2	/5	PLL1ON x9	/3	PLL3ON x10	PLL1	XT1 (MII) PLL3 (RMII)
Ethernet + OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLL1ON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA ETH PHY must use its own crystal
OTG only	8	NA	PLL2OFF	XT1	/1	PLL1ON x9	/3	PLL3OFF	NA	NA
OTG + basic audio	8	NA	PLL2OFF	XT1	/1	PLL1ON x9	/3	PLL3OFF	PLL1	NA
OTG + Audio class I^2S(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLL1ON x6.5	/3	PLL3ON x20	PLL3 VCO Out	NA
Audio class I^2S only(1)	14.7456	/4	PLL2ON x12	PLL2	/4	PLL1ON x6.5	NA	PLL3ON x20	PLL3 VCO out	NA

1. SYSCLK is set to be at 72 MHz except in this case where SYSCLK is at 71.88 MHz.

Revision history

Table 61. Document revision history

Date	Revision	Changes
18-Dec-2008	1	Initial release.
20-Feb-2009	2	I/O information clarified *on page 1*. *Figure 4: STM32F105xxx and STM32F107xxx connectivity line BGA100 ballout* corrected. *Section 2.3.8: Boot modes* updated. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column, plus small additional changes in *Table 5: Pin definitions*. Consumption values modified in *Section 5.3.5: Supply current characteristics*. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. *Table 27: PLL1 characteristics* modified and *Table 28: PLL2 and PLL3 characteristics* added.

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