STM8AF61xx
STM8AH61xx

Automotive 8-bit MCU, with up to 32 Kbytes Flash, EEPROM, 10-bit ADC, timers, LIN, SPI, I^2C, 3 V to 5.5 V

Features

Core

- Max f_{CPU}: 16 MHz
- Advanced STM8A core with Harvard architecture and 3-stage pipeline
- Average 1.6 cycles/instruction resulting in 10 MIPS at 16 MHz f_{CPU} for industry standard benchmark

Memories

- Program memory: 16 to 32 Kbytes Flash; data retention 20 years at 55 °C after 1 kcycle
- Data memory: 0.5 to 1 Kbyte true data EEPROM; endurance 300 kcycles
- RAM: 1 to 2 Kbytes

Clock management

- Low power crystal resonator oscillator with external clock input
- Internal, user-trimmable 16 MHz RC and low power 128 kHz RC oscillators
- Clock security system with clock monitor

Reset and supply management

- Multiple low power modes (wait, slow, auto wake-up, halt) with user definable clock gating
- Low consumption power-on and power-down reset

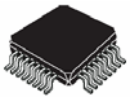
Interrupt management

- Nested interrupt controller with 32 interrupt vectors
- Up to 35 external interrupts on 5 vectors

Timers

- Up to 2 auto-reload 16-bit PWM timers with up to 3 CAPCOM channels each (IC, OC or PWM)
- Multipurpose timer: 16-bit, 4 CAPCOM channels, 3 complementary outputs, dead-time insertion and flexible synchronization
- 8-bit AR system timer with 8-bit prescaler
- Auto wake-up timer
- 2 watchdog timers: Window and standard


LQFP48 7x7


LQFP32 7x7

Communication interfaces

- LINUART LIN 2.1 compliant, master/slave modes with automatic resynchronization
- SPI interface up to 8 Mbit/s or (f_{CPU}/2)
- I^2C interface up to 400 Kbit/s

Analog to digital converter (ADC)

- 10-bit, 3 LSB ADC with up to 10 multiplexed channels with individual data buffer
- Analog watchdog, scan and continuous sampling mode

I/Os

- Up to 38 user pins including 10 high sink I/Os
- Highly robust I/O design, immune against current injection

Table 1. Device summary[1]

Part numbers: STM8AF61xx/STM8AH61xx
STM8AF6168, STM8AF6148, STM8AF6166, STM8AF6146, STM8AH6168, STM8AH6148, STM8AH6166, STM8AH6146

1. This datasheet applies to product versions with and without data EEPROM. The order code identifier is 'F' or 'H' respectively.

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1 Introduction

This datasheet refers to the STM8AF61xx and STM8AH61xx products with 16 to 32 Kbytes of program memory. The STM8AF61xx and STM8AH61xx are hereafter referred to as the STM8AF/H61xx. ‘F’ refers to product versions with data EEPROM and ‘H’ refers to product versions without EEPROM. The identifiers ‘F’ and ‘H’ do not both appear in an order code.

The datasheet contains the description of family features, pinout, electrical characteristics, mechanical data and ordering information.

- For complete information on the STM8A microcontroller memory, registers and peripherals, please refer to STM8A microcontroller family reference manual (RM0009).
- For information on programming, erasing and protection of the internal Flash memory please refer to the STM8 Flash programming manual (PM0047).
- For information on the debug and SWIM (single wire interface module) refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).
- For information on the STM8 core, please refer to the STM8 CPU programming manual (PM0044).

2 Description

The STM8A automotive 8-bit microcontrollers offer from 16 to 32 Kbytes of program memory and integrated true data EEPROM.

All devices of the STM8A product line provide the following benefits:

- Reduced system cost
  - Integrated true data EEPROM for up to 300 k write/erase cycles
  - High system integration level with internal clock oscillators, watchdog and brown-out reset
- Performance and robustness
  - Average performance 10 MIPS at 16 MHz CPU clock frequency
  - Robust I/O, independent watchdogs with separate clock source
  - Clock security system
- Short development cycles
  - Applications scalability across a common family product architecture with compatible pinout, memory map and and modular peripherals.
  - Full documentation and a wide choice of development tools
- Product longevity
  - Advanced core and peripherals made in a state-of-the art technology
  - Native automotive product family operating both at 3.3 V and 5 V supply

All STM8A and ST7 microcontrollers are supported by the same tools including STVD/STVP development environment, the STice emulator and a low-cost, third party in-circuit debugging tool (for more details, see *Section 14: STM8 development tools on page 87*).

3 Product line-up

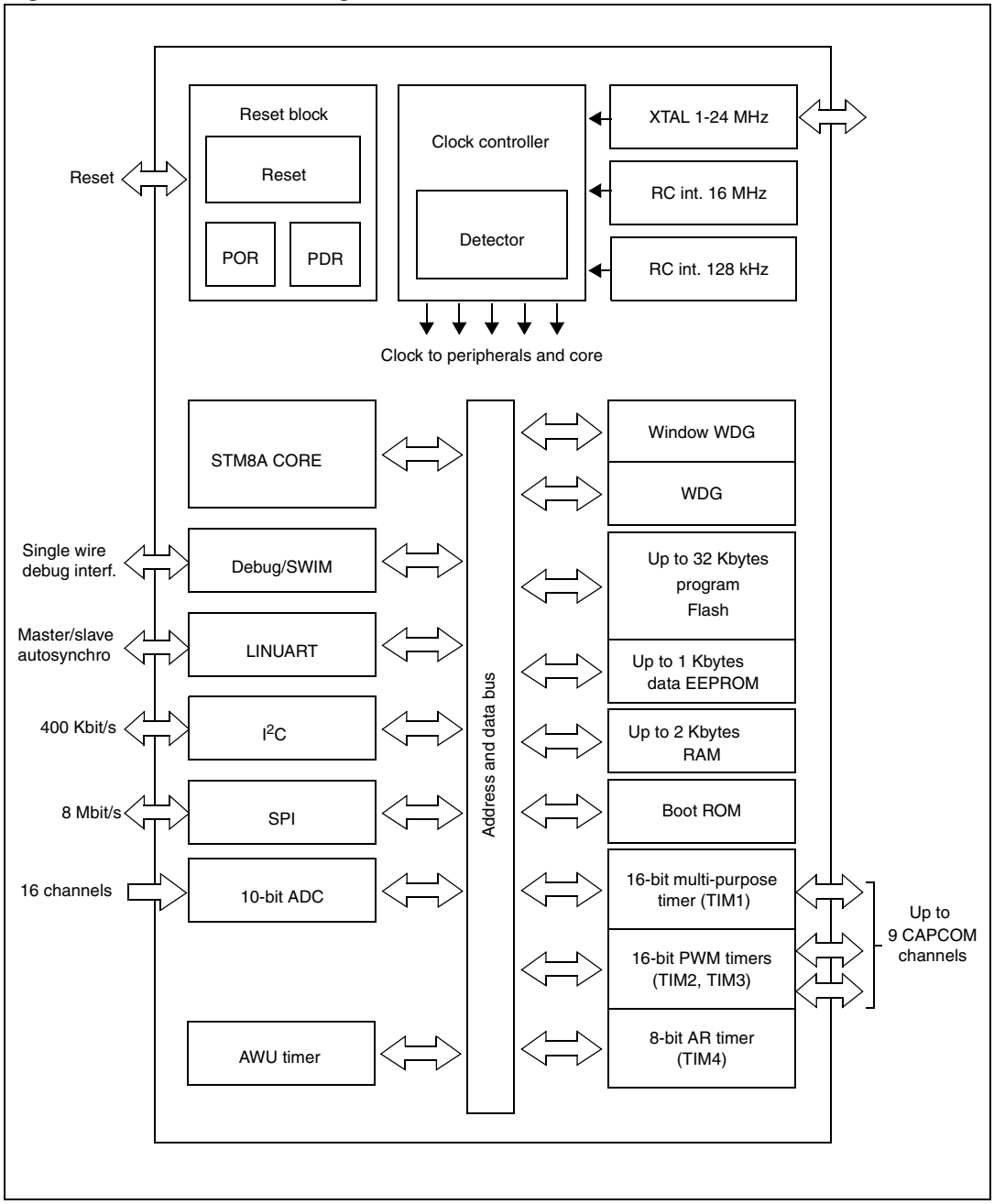
Table 2. STM8AF/H61xx product line-up

Order code	Package	Prog. (bytes)	RAM (bytes)	Data EE (bytes)	10-bit A/D ch.	Timers (IC/OC/PWM)	Serial interfaces	I/0 wakeup pins
STM8AF/H6168T	LQFP48 (7x7)(1)	32 K	2 K	1 K	10	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (9/9/9)	LIN(UART), SPI, I²C	38/35
STM8AF/H6148T		16 K	1 K	0.5 K				
STM8AF/H6166T	LQFP32 (7x7)(1)	32 K	2 K	1 K	7	1x8-bit: TIM4 3x16-bit: TIM1, TIM2, TIM3 (8/8/8)	LIN(UART), SPI, I²C	25/23
STM8AF/H6146T		16 K	1 K	0.5 K				

1. Also QFN package available

4 Block diagram

Figure 1. STM8A block diagram



5 Product overview

The following section intends to give an overview of the basic features of the STM8A functional modules and peripherals.

For more detailed information please refer to the STM8A microcontroller family reference manual (RM0009).

5.1 Central processing unit STM8A

The 8-bit STM8A core is designed for code efficiency and performance.

It contains 21 internal registers (six directly addressable in each execution context), 20 addressing modes including indexed indirect and relative addressing and 80 instructions.

5.1.1 Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus with single cycle fetching for most instructions
- X and Y 16-bit index registers, enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter with 16-Mbyte linear memory space
- 16-bit stack pointer with access to a 64 Kbyte stack
- 8-bit condition code register with seven condition flags for the result of the last instruction

5.1.2 Addressing

- 20 addressing modes
- Indexed indirect addressing mode for look-up tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

5.1.3 Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

5.2 Single wire interface module (SWIM) and debug module

The single wire interface module, SWIM, together with an integrated debug module, permits non-intrusive, real-time in-circuit debugging and fast memory programming.

5.2.1 SWIM

Single wire interface for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes and supports hot-plugging. The maximum data transmission speed is 145 bytes/ms.

5.2.2 Debug module

The non-intrusive debugging module features a performance close to a full-featured emulator. Besides memory and peripheral operation, CPU operation can also be monitored in real-time by means of shadow registers.

- R/W of RAM and peripheral registers in real-time
- R/W for all resources when the application is stopped
- Breakpoints on all program-memory instructions (software breakpoints) except the vector table
- Two advanced breakpoints and 23 predefined configurations

5.3 Interrupt controller

- Nested interrupts with three software priority levels
- 32 interrupt vectors with hardware priority
- Up to 37 external interrupts on five vectors
- Trap and reset interrupts

5.4 Non-volatile memory

- Up to 32 Kbytes of program single voltage Flash memory
- Up to 1 Kbyte true (not emulated) data EEPROM
- Read while write: Writing in the data memory is possible while executing code in the program memory
- 128 user option bytes permit permanent device set up

5.4.1 Architecture

- Array: Up to 32 Kbytes of Flash program memory organized in blocks of 128 bytes each
- Read granularity: 1 word = 4 bytes
- Write/erase granularity: 1 word (4 bytes) or 1 block (128 bytes) in parallel

Writing, erasing, word and block register management is handled automatically by the memory interface.

5.4.2 Write protection (WP)

Write protection in application mode is intended to avoid unintentional overwriting of the memory in case of user software malfunction. Code update in user mode is still possible after execution of a specific MASS key sequence.

The program memory is divided into two areas:

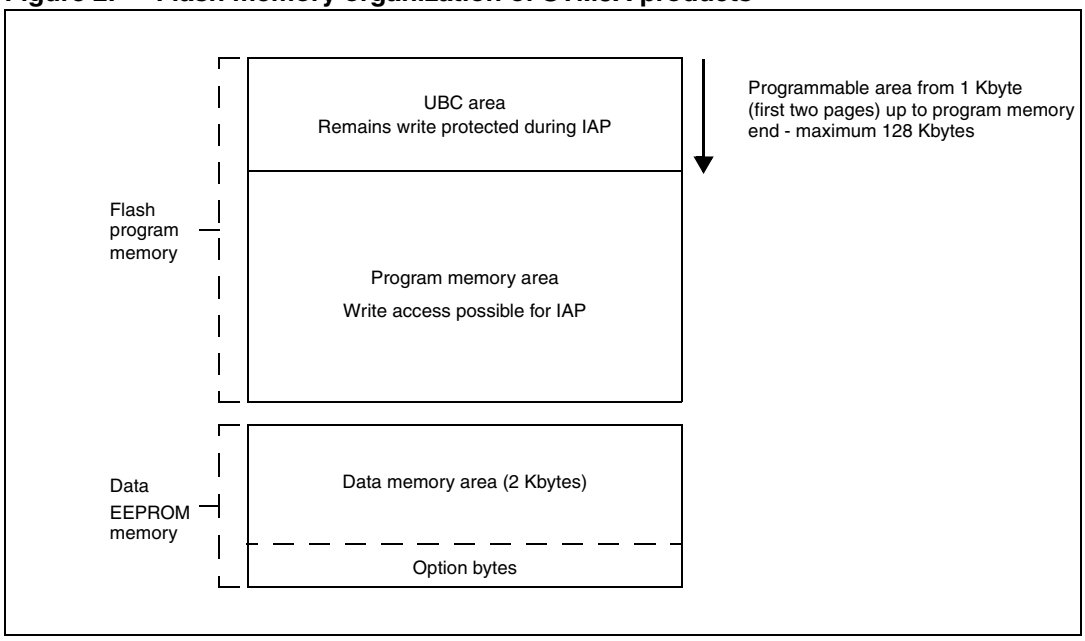
- Main program memory: Up to 32 Kbytes minus user-specific boot code (UBC)
- UBC: Configurable up to 32 Kbytes

The UBC area also remains write-protected during in-application programming. It permits storage of the boot program or specific code libraries.

The boot area is a part of the program memory that contains the reset and interrupt vectors, the reset routine and usually the IAP and communication routines. The UBC area has a second level of protection to prevent unintentional erasing or modification during IAP programming. This means that the MASS keys do not unlock the UBC area.

The size of the UBC is programmable through the UBC option byte, in increments of 512 bytes, by programming the UBC option byte in ICP mode.

Figure 2. Flash memory organization of STM8A products



5.4.3 Read-out protection (ROP)

STM8A devices provide a read-out protection of the code and data memory by programming the lock byte at address 4800h with the value AAh.

Read-out protection prevents reading and writing the program and data memory via the debug module and SWIM interface. This protection is active in all device operation modes. Any attempt to remove the protection by overwriting the lock byte triggers a global erase of the program and data memory.

The ROP circuit may provide a temporary access for debugging or failure analysis. This is a specific product option and must be specified while ordering STM8A products.

Temporary read access is protected by a user defined, 8-byte keyword that is different from 00h or FFh. The keys are stored in the option byte area.

Temporary read-out can be permanently disabled by means of the option byte TMU_DIS.

For enabling temporary read access the eight access keys have to be written in the TMU registers. A wrong code does not change the protection status. More than eight unsuccessful access trials trigger an erase of the program and data memory.

Entering the right key sequence enables a temporary read access to the code and data memory after a delay of several milliseconds.

The procedure for temporary read access is as follows:

- Activate SWIM mode under device reset - the CPU is stalled, code and data memory are not visible by the debug module.
- Enable the internal 128 KHz LSI oscillator
- Write the 8eight key bytes into the TMU registers
- Set the bit(0) of the TMU status register to 1. A dedicated state machine on an isolated bus, compares the TMU register content with the key stored in the TMU option bytes. During this periode read and write operations have no effect. A reset re-activates the initial protection status. The comparison can be monitored by means of the TU_CTL_ST register.
- In case of a successful key comparison, the SWIM interface enables read access to the code and data memory and program execution. A comparison error does not change the protection status but increments the counter MAXATT. If the counter content exceedes eight unsuccessful trials, a global erase of the data and code memory is triggered.

The read access is temporary. A device reset restores the initial protection.

5.4.4 Speed

- Operation at up to 16 MHz CPU clock frequency without wait states.
- Programming time modes (same for word or block)
  - Fast programming: Without erase
  - Standard programming: Erase and program

5.5 Low-power operating modes

The product features various low-power modes:

- Slow mode: Prescaled CPU clock, selected peripherals at full clock speed
- Active halt mode: CPU and peripheral clocks are stopped
- Halt mode: CPU and peripheral clocks are stopped, the device remains powered on. Wake-up is triggered by an external interrupt.

In all modes the CPU and peripherals remain permanently powered on, the system clock is applied only to selected modules.

The RAM content is preserved and the brown-out reset circuit remains activated.

5.6 Clock and clock controller

The clock controller distributes the system clock coming from different oscillators to the core and the peripherals. It also manages clock gating for low power modes and ensures clock robustness.

5.6.1 Features

- **Clock sources:**
  - Internal 16 MHz and 128 kHz RC oscillators
  - Crystal oscillator
  - External clock input
- **Reset:** After reset the microcontroller restarts by default with an internal 2-MHz clock (16 MHz/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register. The clock signal is not switched until the new clock source is ready. The design guarantees glitch-free switching.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **Wake-up:** Recovery from halt and AWU (auto wake-up) low power modes uses the internal RC oscillator (16 MHz/8) for quick start-up and then switches to the last selected clock source before halt mode is entered.
- **Clock security system (CSS):** The CSS permits monitoring of external clock sources and automatic switching to the internal RC (16 MHz/8) in case of a clock failure.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

5.6.2 Internal 16 MHz RC oscillator

- Default clock after reset 2 MHz (16 MHz/8)
- Wake-up time: < 2 µs

User trimming

The register CLK_HSITRIMR with three trimming bits plus one additional bit for the sign permits frequency tuning to a precision of 1% by the application program. The trimming step granularity is 0.7%. A position of the optionbyte 3 (16MHZTIMO) allows to select between the two or three bit trimming mode.

The adjustment range covers all possible frequency variations versus supply voltage and temperature. This trimming does not change the initial production setting.

5.6.3 Internal 128 kHz RC oscillator

The frequency of this clock is 128 kHz and it is independent from the main clock. It drives the watchdog or the AWU wake-up timer.

In systems which do not need independent clock sources for the watchdog counters, the 128 kHz signal can be used as the system clock. This configuration has to be enabled by setting an option byte (OPT3, LSI_EN).

5.6.4 Internal high-speed crystal oscillator

The internal high-speed crystal oscillator delivers the main clock in normal run mode. It operates with quartz crystals and ceramic resonators.

- Frequency range: 1 to 16 MHz
- Crystal oscillation mode: Preferred fundamental
- I/Os: Standard I/O pins multiplexed with OSCIN, OSCOUT

Optionally, an external clock signal can be injected into the OSCIN input pin.

5.6.5 External clock input

The external clock signal is applied to the OSCIN input pin of the crystal oscillator. The frequency range is 0 to 16 MHz.

5.6.6 Clock security system (CSS)

The clock security system protects against a system stall in case of an external crystal clock failure.

In case of a clock failure an interrupt is generated and the high speed internal clock (HSI) is automatically selected with a frequency of 2 MHz (16 MHz/8). This function can be enabled using the CSS register (CLK_CSSR).

The CSS operates by detecting when the external clock signal (crystal or external clock) falls below 500 kHz. With active CSS this is the minimum operating frequency.

5.7 Timers

5.7.1 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

The WDG timer activity is controlled by the application program or option bytes. Once the watchdog is activated, it cannot be disabled by the user program without a reset.

Window watchdog timer

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

The window function can be used to trim the watchdog behavior to match the application perfectly.

The application software must refresh the counter before time-out and during a limited time window.

A reset is generated in two situations:

1. Timeout
2. Refresh out of window: The downcounter is refreshed before its value is lower then the one stored in the window register.

Independent watchdog timer

The independent watchdog peripheral can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the 128 kHz LSI internal RC clock source, and thus stays active even in case of a CPU clock failure. If the hardware watchdog feature is enabled through the device option bits, the watchdog is automatically enabled at power-on, and generates a reset unless the key register is written by software before the counter reaches the end of count.

The IWDG time base spans from 60 µs to 1 s. It can be adjusted by setting the registers of the 7-bit prescaler and 8-bit down-counter.

5.7.2 Auto wake-up counter

- Used for auto wake-up from active halt mode.
- Clock source: Internal 128 kHz internal low frequency RC oscillator or external clock.

5.7.3 Multipurpose and PWM timers

STM8A devices described in this datasheet, contain up to three 16-bit multipurpose and PWM timers providing nine CAPCOM channels in total.

Table 3. STM8A timer configuration

Timer	Counter	Prescaler	Type	CAPCOM	Complementary outputs	Synchronization module
Timer1	16	16	Up/down	4	3	Yes
Timer2		15-bit fixed power of 2 ratios	Up	3	0	No
Timer3				2		
Timer4	8	7-bit fixed power of 2 ratios		0		

Timer 1: Multipurpose PWM timer

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down AR (auto-reload) counter with 16-bit prescaler
- Four independent CAPCOM channels configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- Trigger module which allows the interaction of timer 1 with other timers or the ADC to be controlled
- Break input to force the timer outputs into a defined state
- Three complementary outputs with adjustable dead time
- Interrupt sources: 4 x input capture/output compare, 1 x overflow/update, 1 x break

Timer 2 and 3: 16-bit PWM timers

- 16-bit auto-reload up-counter
- 15-bit prescaler adjustable to fixed power of two ratios 1…32768
- Timers with three or two individually configurable CAPCOM channels
- Interrupt sources: 2 or 3 x input capture/output compare, 1 x overflow/update

5.7.4 Timer 4: System timer

- 8-bit auto-reload, adjustable prescaler ratio to any power of two from 1 to 128
- Clock source: master clock
- Interrupt source: 1 x overflow/update

5.8 ADC

The STM8A products described in this datasheet, contain a 10-bit successive approximation ADC with 10 multiplexed input channels.

General features:

- 10-bit ADC with up to 10 channels
- Input voltage range: 0 to V_{DDA}
- Acqusition modes
  - Single conversion
  - Continous acquisition - up to 100 ksamples/s effective sampling rate
  - Analog watchdog with two adjustable threshold levels
  - Individual conversion result buffer for each channel
  - Scan mode for single and continuous conversion
  - Trigger register and external trigger input
- Interrupts
  - End of conversion (EOC) - can be masked
  - Analog watchdog event interrupt

5.9 Communication interfaces

The following communication interfaces are implemented on STM8A products:

- LINUART: LIN2.1 master/slave capability, full feature UART
- SPI - full and half-duplex, 8 Mbit/s
- I²C - up to 400 Kbit/s
- SWIM for debugging and device programming

5.9.1 LINUART

Main features

- LIN master/slave rev. 2.1 compliant
- Auto-synchronization in LIN slave mode
- 16-bit baud rate prescaler
- 1 Mbit full duplex SCI

LIN master

- Autonomous header handling
- 13-bit LIN synch break generation

LIN slave

- Autonomous header handling - one single interrupt per valid message header
- Automatic baud rate synchronization - maximum tolerated initial clock deviation ±15 %
- Synch delimiter checking
- 11-bit LIN synch break detection - break detection always active
- Parity check on the LIN identifier field
- LIN error management
- Hot plugging support

Asynchronous communication (UART)

- Full duplex, asynchronous communications - NRZ standard format (mark/space)
- Independently programmable transmit and receive baud rates up to 500 Kbit/s
- Programmable data word length (8 or 9 bits)
- Low-power standby mode - two receiver wake-up modes:
  - Address bit (MSB)
  - Idle line
- Muting function for multiprocessor configurations
- Overrun, noise and frame error detection
- Six interrupt sources
- Tx, Rx parity control

5.9.2 SPI

- Maximum speed: 8 Mbit/s or $f_{CPU}/2$ both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on two lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- CRC calculation
- 1 byte Tx and Rx buffer
- Slave/master selection input pin

5.9.3 I²C

- I²C master features:
  - Clock generation
  - Start and stop generation
- I²C slave features:
  - Programmable I²C address detection
  - Stop bit detection
- Generation and detection of 7-bit/10-bit addressing and general call
- Supports different communication speeds:
  - Standard speed (up to 100 kHz),
  - Fast speed (up to 400 kHz)
- Interrupt:
  - Successful address/data communication
  - Error condition
  - Wake-up from halt
- Wake-up from halt on address detection in slave mode

5.10 Input/output specifications

The product features four different I/O types:

- Standard I/O 2 MHz
- Fast I/O 10 MHz
- High sink 8 mA, 2 MHz
- True open drain (I²C interface)

To decrease EMI (electromagnetic interference), high sink I/Os have a limited maximum slew rate. The rise and fall times are similar to those of standard I/Os. Selected I/Os include a low leakage analog switch.

STM8A I/Os are designed to withstand current injection. For a negative injection current of 4 mA, the resulting leakage current in the adjacent input does not exceed 1 µA. External protection diodes are no longer required.

6 Pinouts and pin description

6.1 Package pinouts

Figure 3. LQFP 48-pin pinout

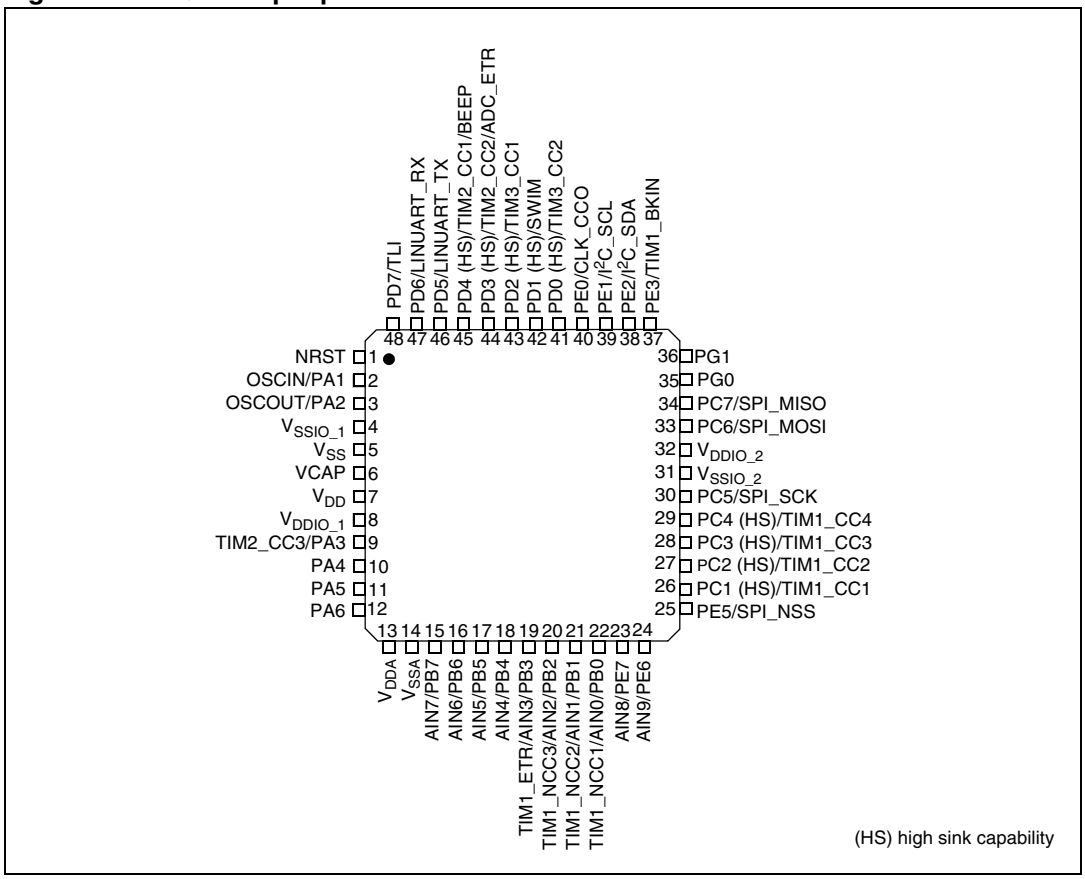
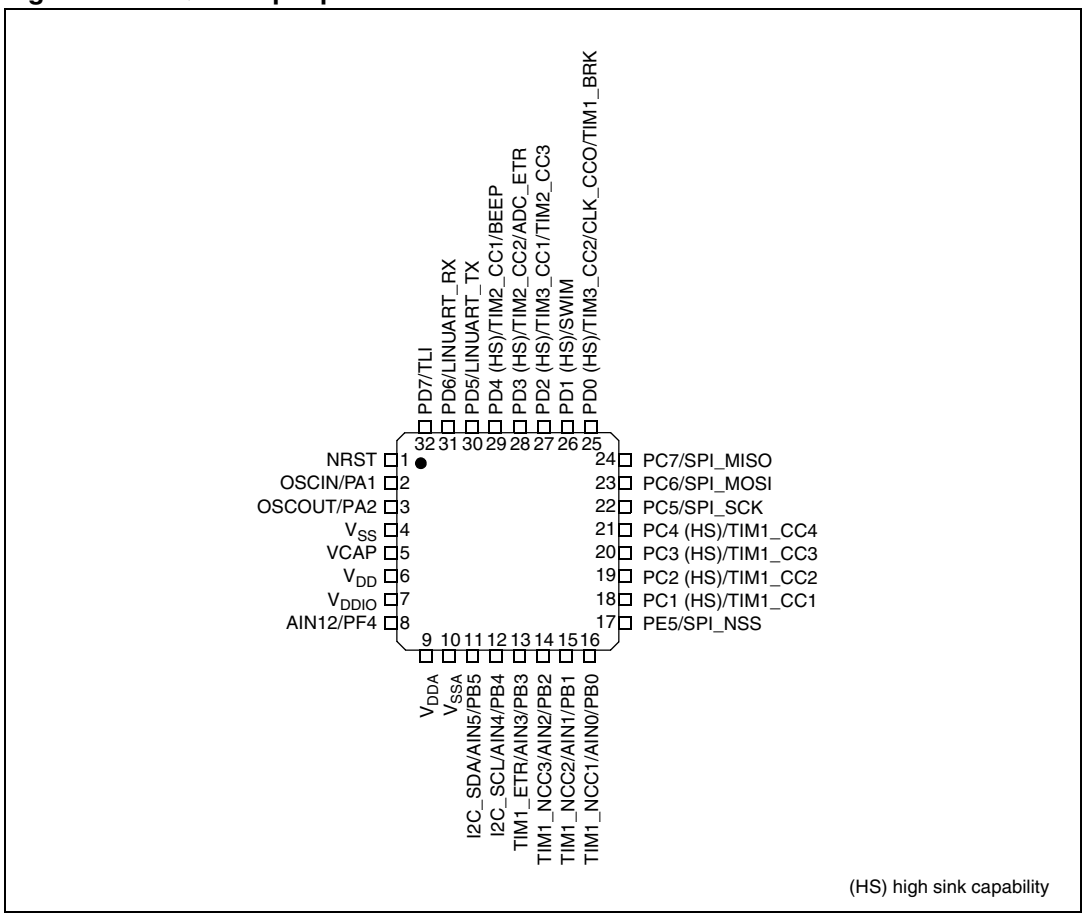


Figure 4. LQFP 32-pin pinout



6.2 Pin description

Table 4. Legend/abbreviation for *Table 5*

Type	I= input, O = output, S = power supply	
Level	Input	CM = CMOS (standard for all I/Os)
	Output	HS = High sink (8 mA)
Output speed	O1 = Standard (up to 2 MHz) O2 = Fast (up to 10 MHz) O3 = Fast/slow programmability with slow as default state after reset O4 = Fast/slow programmability with fast as default state after reset	
Port and control configuration	Input	float = floating, wpu = weak pull-up
	Output	T = true open drain, OD = open drain, PP = push pull

Reset state is shown in **bold**.

Table 5. STM8A 32 Kbyte microcontroller pin description

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
1	1	NRST	I/O		**X**						Reset		
2	2	PA1/OSCIN	I/O	**X**	X			O1	X	X	**Port A1**	Resonator/crystal in	
3	3	PA2/OSCOUT	I/O	**X**	X	X		O1	X	X	**Port A2**	Resonator/crystal out	
4	-	V_{SSIO_1}	S								I/O ground		
5	4	V_{SS}	S								Digital ground		
6	5	VCAP	S								1.8 V regulator capacitor		
7	6	V_{DD}	S								Digital power supply		
8	7	V_{DDIO_1}	S								I/O power supply		
-	8	PF4/AIN12	I/O	**X**	X			O1	X	X	**Port F4**	Analog input 12	
9	-	PA3/TIM2_CC3	I/O	**X**	X	X		O1	X	X	**Port A3**	Timer 2 - channel3	TIM3_CC1 [AFR1]
10	-	PA4	I/O	**X**	X	X		O3	X	X	**Port A4**		
11	-	PA5	I/O	**X**	X	X		O3	X	X	**Port A5**		
12	-	PA6	I/O	**X**	X	X		O3	X	X	**Port A6**		
13	9	V_{DDA}	S								Analog power supply		
14	10	V_{SSA}	S								Analog ground		
15	-	PB7/AIN7	I/O	**X**	X	X		O1	X	X	**Port B7**	Analog input 7	
16	-	PB6/AIN6	I/O	**X**	X	X		O1	X	X	**Port B6**	Analog input 6	
17	11	PB5/AIN5	I/O	**X**	X	X		O1	X	X	**Port B5**	Analog input 5	I^2C_SDA [AFR6]
18	12	PB4/AIN4	I/O	**X**	X	X		O1	X	X	**Port B4**	Analog input 4	I^2C_SCL [AFR6]
19	13	PB3/AIN3	I/O	**X**	X	X		O1	X	X	**Port B3**	Analog input 3	TIM1_ETR [AFR5]
20	14	PB2/AIN2	I/O	**X**	X	X		O1	X	X	**Port B2**	Analog input	TIM1_ NCC3 [AFR5]
21	15	PB1/AIN1	I/O	**X**	X	X		O1	X	X	**Port B1**	Analog input 1	TIM1_ NCC2 [AFR5]
22	16	PB0/AIN0	I/O	**X**	X	X		O1	X	X	**Port B0**	Analog input 0	TIM1_ NCC1 [AFR5]
23	-	PE7/AIN8	I/O	**X**	X			O1	X	X	**Port E7**	Analog input 8	

Table 5. STM8A 32 Kbyte microcontroller pin description (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
24		PE6/AIN9	I/O	**X**	X	X		O1	X	X	**Port E7**	Analog input 9	
25	17	PE5/SPI_NSS	I/O	**X**	X	X		O1	X	X	**Port E5**	SPI master/slave select	
26	18	PC1/TIM1_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port C1**	Timer 1 - channel 1	
27	19	PC2/TIM1_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port C2**	Timer 1- channel 2	
28	20	PC3/TIM1_CC3	I/O	**X**	X	X	HS	O3	X	X	**Port C3**	Timer 1 - channel 3	
29	21	PC4/TIM1_CC4	I/O	**X**	X	X	HS	O3	X	X	**Port C4**	Timer 1 - channel 4	
30	22	PC5/SPI_SCK	I/O	**X**	X	X		O3	X	X	**Port C5**	SPI clock	
31	-	V_{SSIO_2}	S								I/O ground		
32	-	V_{DDIO_2}	S								I/O power supply		
33	23	PC6/SPI_MOSI	I/O	**X**	X	X		O3	X	X	**Port C6**	SPI master out/ slave in	
34	24	PC7/SPI_MISO	I/O	**X**	X	X		O3	X	X	**Port C7**	SPI master in/ slave out	
35	-	PG0	I/O	**X**	X			O1	X	X	**Port G0**		
36	-	PG1	I/O	**X**	X			O1	X	X	**Port G1**		
37	-	PE3/TIM1_BKIN	I/O	**X**	X	X		O1	X	X	**Port E3**	Timer 1 - break input	
38	-	PE2/I^2C_SDA	I/O	**X**	X	X		O1	T(1)	X	**Port E2**	I^2C data	
39	-	PE1/I^2C_SCL	I/O	**X**	X	X		O1	T(1)	X	**Port E1**	I^2C clock	
40	-	PE0/CLK_CCO	I/O	**X**	X	X		O3	X	X	**Port E0**	Configurable clock output	
41	25	PD0/TIM3_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D0**	Timer 3 - channel 2	TIM1_BKIN [AFR3]/ CLK_CCO [AFR2]
42	26	PD1/SWIM	I/O	X	**X**	X	HS	O4	X	X	**Port D1**	SWIM data interface	
43	27	PD2/TIM3_CC1	I/O	**X**	X	X	HS	O3	X	X	**Port D2**	Timer 3 - channel 1	TIM2_CC3 [AFR1]
44	28	PD3/TIM2_CC2	I/O	**X**	X	X	HS	O3	X	X	**Port D3**	Timer 2 - channel 2	ADC_ETR [AFR0]
45	29	PD4/TIM2_CC1/BEEP	I/O	**X**	X	X	HS	O3	X	X	**Port D4**	Timer 2 - channel 1	BEEP output [AFR7]
46	30	PD5/ LINUART_TX	I/O	**X**	X	X		O1	X	X	**Port D5**	LINUART data transmit	

Table 5. STM8A 32 Kbyte microcontroller pin description (continued)

Pin number		Pin name	Type	Input			Output				Main function (after reset)	Default alternate function	Alternate function after remap [option bit]
LQFP48	LQFP32			floating	wpu	Ext. interrupt	High sink	Speed	OD	PP			
47	31	PD6/ LINUART_RX	I/O	**X**	X	X		O1	X	X	**Port D6**	LINUART data receive	
											Caution: This pin must be held low during power on		
48	32	PD7/TLI	I/O	**X**	X	X		O1	X	X	**Port D7**	Top level interrupt	TIM1_CC4 [AFR4]

1. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer and protection diode to V_{DD} are not implemented)

6.2.1 Alternate function remapping

As shown in the rightmost column of *Table 5*, some alternate functions can be remapped at different I/O ports by programming one of eight AFR (alternate function remap) option bits. Refer to *Section 10: Option bytes on page 43*. When the remapping option is active, the default alternate function is no longer available.

To use an alternate function, the corresponding peripheral must be enabled in the peripheral registers.

Alternate function remapping does not effect GPIO capabilities of the I/O ports (see the GPIO section of the STM8A microcontroller family reference manual, RM0009).

7 Memory map

Figure 5. Register and memory map of STM8A products

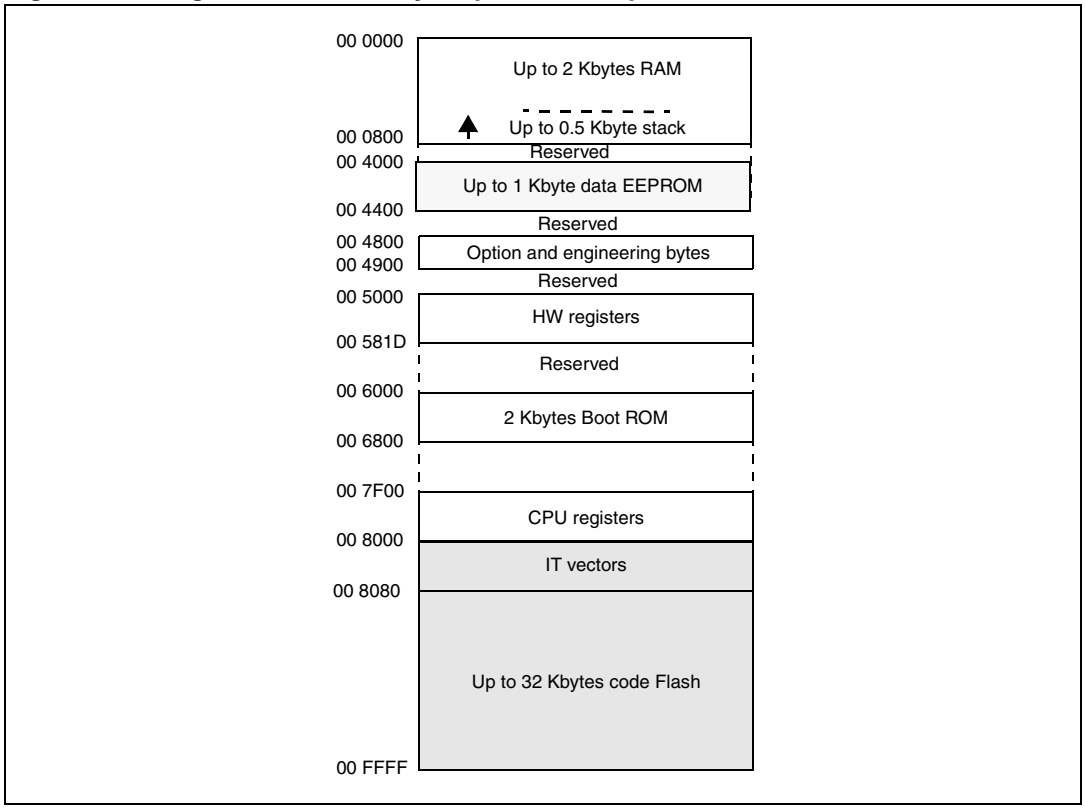


Table 6. Stack and RAM partitioning

Product Kbytes	RAM size Kbytes	RAM end	Stack size		Stack start
			Dec	Hex	
32	2	07FF	512	0200	0600

8 Interrupt table

Table 7. STM8A interrupt table

Priority	Source block	Description	Interrupt vector address	Wake-up from halt	Comments
-	Reset	Reset	6000h	Yes	Reset vector in ROM
-	TRAP	SW interrupt	8004h		
0	TLI	External top level interrupt	8008h		
1	AWU	Auto wake up from halt	800Ch	Yes	
2	Clock controller	Main clock controller	8010h		
3	MISC	Ext interrupt E0	8014h	Yes	Port A interrupts
4	MISC	Ext interrupt E1	8018h	Yes	Port B interrupts
5	MISC	Ext interrupt E2	801Ch	Yes	Port C interrupts
6	MISC	Ext interrupt E3	8020h	Yes	Port D interrupts
7	MISC	Ext interrupt E4	8024h	Yes	Port E interrupts
8	CAN	CAN interrupt Rx	8028h	Yes	
9	CAN	CAN interrupt TX/ER/SC	802Ch		
10	SPI	End of transfer	8030h	Yes	
11	Timer 1	Update/overflow/ trigger/break	8034h		
12	Timer 1	Capture/compare	8038h		
13	Timer 2	Update/overflow/ break	803Ch		Trigger not available on medium end timer
14	Timer 2	Capture/compare	8040h		
15	Timer 3	Update/overflow/ break	8044h		Trigger not available on medium end timer
16	Timer 3	Capture/compare	8048h		
17	USART (SCI1)	Tx complete/ ER/SPI EOT/SPI error	804Ch		
18	USART (SCI1)	Receive data full reg.	8050h		
19	I^2C	I^2C interrupts	8054h	Yes	
20	LINUART (SCI2)	Tx complete/error/ SPI EOT/SPI error	8058h		
21	LINUART (SCI2)	Receive data full reg.	805Ch		

Table 7. STM8A interrupt table (continued)

Priority	Source block	Description	Interrupt vector address	Wake-up from halt	Comments
22	ADC	End of conversion	8060h		
23	Timer 4	Update/overflow	8064h		
24	Reserved(1)	Reserved	8068h		

1. Also unused interrupts should be initialized with “IRET” for robust programming.

9 Register mapping

Table 8. STM8A I/O port hardware register map

Address	Block	Register label	Register name	Reset status
00 5000h	Port A	PA_ODR	Port A data output latch register	00h
00 5001h		PA_IDR	Port A input pin value register	00h
00 5002h		PA_DDR	Port A data direction register	00h
00 5003h		PA_CR1	Port A control register 1	00h
00 5004h		PA_CR2	Port A control register 2	00h
00 5005h	Port B	PB_ODR	Port B data output latch register	00h
00 5006h		PB_IDR	Port B input pin value register	00h
00 5007h		PB_DDR	Port B data direction register	00h
00 5008h		PB_CR1	Port B control register 1	00h
00 5009h		PB_CR2	Port B control register 2	00h
00 500Ah	Port C	PC_ODR	Port C data output latch register	00h
00 500Bh		PC_IDR	Port C input pin value register	00h
00 500Ch		PC_DDR	Port C data direction register	00h
00 500Dh		PC_CR1	Port C control register 1	00h
00 500Eh		PC_CR2	Port C control register 2	00h
00 500Fh	Port D	PD_ODR	Port D data output latch register	00h
00 5010h		PD_IDR	Port D input pin value register	00h
00 5011h		PD_DDR	Port D data direction register	00h
00 5012h		PD_CR1	Port D control register 1	00h
00 5013h		PD_CR2	Port D control register 2	00h
00 5014h	Port E	PE_ODR	Port E data output latch register	00h
00 5015h		PE_IDR	Port E input pin value register	00h
00 5016h		PE_DDR	Port E data direction register	00h
00 5017h		PE_CR1	Port E control register 1	00h
00 5018h		PE_CR2	Port E control register 2	00h
00 5019h	Port F	PF_ODR	Port F data output latch register	00h
00 501Ah		PF_IDR	Port F input pin value register	00h
00 501Bh		PF_DDR	Port F data direction register	00h
00 501Ch		PF_CR1	Port F control register 1	00h
00 501Dh		PF_CR2	Port F control register 2	00h

Table 8. STM8A I/O port hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 501Eh	Port G	PG_ODR	Port G data output latch register	00h
00 501Fh		PG_IDR	Port G input pin value register	00h
00 5020h		PG_DDR	Port G data direction register	00h
00 5021h		PG_CR1	Port G control register 1	00h
00 5022h		PG_CR2	Port G control register 2	00h
00 5023h	Port H	PH_ODR	Port H data output latch register	00h
00 5024h		PH_IDR	Port H input pin value register	00h
00 5025h		PH_DDR	Port H data direction register	00h
00 5026h		PH_CR1	Port H control register 1	00h
00 5027h		PH_CR2	Port H control register 2	00h
00 5028h	Port I	PI_ODR	Port I data output latch register	00h
00 5029h		PI_IDR	Port I input pin value register	00h
00 502Ah		PI_DDR	Port I data direction register	00h
00 502Bh		PI_CR1	Port I control register 1	00h
00 502Ch		PI_CR2	Port I control register 2	00h

Table 9. STM8A general hardware register map

Address	Block	Register label	Register name	Reset status
00 5050h to 00 5059h	Reserved area (10 bytes)			
00 505Ah	Flash	FLASH_CR1	Flash control register 1	00h
00 505Bh		FLASH_CR2	Flash control register 2	00h
00 505Ch		FLASH_NCR2	Flash complementary control register 2	FFh
00 505Dh		FLASH _FPR	Flash protection register	00h
00 505Eh		FLASH _NFPR	Flash complementary protection register	FFh
00 505Fh		FLASH _IAPSR	Flash in-application programming status register	00h
00 5060h to 00 5061h	Reserved area (2 bytes)			
00 5062h	Flash	FLASH _PUKR	Flash program memory unprotection register	00h
00 5063h	Reserved area (1 byte)			
00 5064h	Flash	FLASH _DUKR	Data EEPROM unprotection register	00h
00 5065h to 00 509Fh	Reserved area (59 bytes)			
00 50A0h	ITC	EXTI_CR1	External interrupt control register 1	00h
00 50A1h		EXTI_CR2	External interrupt control register 2	00h
00 50A2h to 00 50B2h	Reserved area (17 bytes)			
00 50B3h	RST	RST_SR	Reset status register	xxh
00 50B4h to 00 50BFh	Reserved area (12 bytes)			
00 50C0h	CLK	CLK_ICKR	Internal clock control register	01h
00 50C1h		CLK_ECKR	External clock control register	00h
00 50C2h	Reserved area (1 byte)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 50C3h	CLK	CLK_CMSR	Clock master status register	E1h
00 50C4h		CLK_SWR	Clock master switch register	E1h
00 50C5h		CLK_SWCR	Clock switch control register	xxxx 0000b
00 50C6h		CLK_CKDIVR	Clock divider register	18h
00 50C7h		CLK_PCKENR1	Peripheral clock gating register 1	FFh
00 50C8h		CLK_CSSR	Clock security system register	00h
00 50C9h		CLK_CCOR	Configurable clock control register	00h
00 50CAh		CLK_PCKENR2	Peripheral clock gating register 2	FFh
00 50CBh		CLK_CANCCR	CAN clock control register	00h
00 50CCh		CLK_HSITRIMR	HSI clock calibration trimming register	xxh
00 50CDh		CLK_SWIMCCR	SWIM clock control register	x0h
00 50CEh to 00 50D0h	Reserved area (3 bytes)			
00 50D1h	WWDG	WWDG_CR	WWDG control register	7Fh
00 50D2h		WWDG_WR	WWDR window register	7Fh
00 50D3h to 00 50DFh	Reserved area (13 bytes)			
00 50E0h	IWDG	IWDG_KR	IWDG key register	-
00 50E1h		IWDG_PR	IWDG prescaler register	00h
00 50E2h		IWDG_RLR	IWDG reload register	FFh
00 50E3h to 00 50EFh	Reserved area (13 bytes)			
00 50F0h	AWU	AWU_CSR1	AWU control/status register 1	00h
00 50F1h		AWU_APR	AWU asynchronous prescaler buffer register	3Fh
00 50F2h		AWU_TBR	AWU timebase selection register	00h
00 50F3h	BEEP	BEEP_CSR	BEEP control/status register	1Fh
00 50F4h to 00 50FFh	Reserved area (12 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5200h	SPI	SPI_CR1	SPI control register 1	00h
00 5201h		SPI_CR2	SPI control register 2	00h
00 5202h		SPI_ICR	SPI interrupt control register	00h
00 5203h		SPI_SR	SPI status register	02h
00 5204h		SPI_DR	SPI data register	00h
00 5205h		SPI_CRCPR	SPI CRC polynomial register	07h
00 5206h		SPI_RXCRCR	SPI Rx CRC register	FFh
00 5207h		SPI_TXCRCR	SPI Tx CRC register	FFh
00 5208h to 00 520Fh	Reserved area (8 bytes)			
00 5210h	I^2C	I2C_CR1	I^2C control register 1	00h
00 5211h		I2C_CR2	I^2C control register 2	00h
00 5212h		I2C_FREQR	I^2C frequency register	00h
00 5213h		I2C_OARL	I^2C own address register low	00h
00 5214h		I2C_OARH	I^2C own address register high	00h
00 5215h		Reserved		
00 5216h		I2C_DR	I^2C data register	00h
00 5217h		I2C_SR1	I^2C status register 1	00h
00 5218h		I2C_SR2	I^2C status register 2	00h
00 5219h		I2C_SR3	I^2C status register 3	00h
00 521Ah		I2C_ITR	I^2C interrupt control register	00h
00 521Bh		I2C_CCRL	I^2C clock control register low	00h
00 521Ch		I2C_CCRH	I^2C clock control register high	00h
00 521Dh		I2C_TRISER	I^2C TRISE register	02h
00 521Eh		I2C_PECR	I^2C packet error checking register	00h
00 521Fh to 00 523Fh	Reserved area (33 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5240h	LINUART	LINUART_SR	LINUART status register	C0h
00 5241h		LINUART_DR	LINUART data register	xxh
00 5242h		LINUART_BRR1	LINUART baud rate register 1	00h
00 5243h		LINUART_BRR2	LINUART baud rate register 2	00h
00 5244h		LINUART_CR1	LINUART control register 1	00h
00 5245h		LINUART_CR2	LINUART control register 2	00h
00 5246h		LINUART_CR3	LINUART control register 3	00h
005247h		LINUART_CR4	LINUART control register 4	00h
00 5248h		Reserved		
00 5249h		LINUART_CR6	LINUART control register 6	00h
00 524Ah		LINUART_GT	LINUART guard time register	00h
00 524Bh		LINUART_PSCR	LINUART prescaler register	00h
00 524Ch to 00 524Fh	Reserved area (4 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5250h	TIM1	TIM1_CR1	TIM1 control register 1	00h
00 5251h		TIM1_CR2	TIM1 control register 2	00h
00 5252h		TIM1_SMCR	TIM1 slave mode control register	00h
00 5253h		TIM1_ETR	TIM1 external trigger register	00h
00 5254h		TIM1_IER	TIM1 interrupt enable register	00h
00 5255h		TIM1_SR1	TIM1 status register 1	00h
00 5256h		TIM1_SR2	TIM1 status register 2	00h
00 5257h		TIM1_EGR	TIM1 event generation register	00h
00 5258h		TIM1_CCMR1	TIM1 capture/compare mode register 1	00h
00 5259h		TIM1_CCMR2	TIM1 capture/compare mode register 2	00h
00 525Ah		TIM1_CCMR3	TIM1 capture/compare mode register 3	00h
00 525Bh		TIM1_CCMR4	TIM1 capture/compare mode register 4	00h
00 525Ch		TIM1_CCER1	TIM1 capture/compare enable register 1	00h
00 525Dh		TIM1_CCER2	TIM1 capture/compare enable register 2	00h
00 525Eh		TIM1_CNTRH	TIM1 counter high	00h
00 525Fh		TIM1_CNTRL	TIM1 counter low	00h
00 5260h		TIM1_PSCRH	TIM1 prescaler register high	00h
00 5261h		TIM1_PSCRL	TIM1 prescaler register low	00h
00 5262h		TIM1_ARRH	TIM1 auto-reload register high	FFh
00 5263h		TIM1_ARRL	TIM1 auto-reload register low	FFh
00 5264h		TIM1_RCR	TIM1 repetition counter register	00h
00 5265h		TIM1_CCR1H	TIM1 capture/compare register 1 high	00h
00 5266h		TIM1_CCR1L	TIM1 capture/compare register 1 low	00h
00 5267h		TIM1_CCR2H	TIM1 capture/compare register 2 high	00h
00 5268h		TIM1_CCR2L	TIM1 capture/compare register 2 low	00h
00 5269h		TIM1_CCR3H	TIM1 capture/compare register 3 high	00h
00 526Ah		TIM1_CCR3L	TIM1 capture/compare register 3 low	00h
00 526Bh		TIM1_CCR4H	TIM1 capture/compare register 4 high	00h
00 526Ch		TIM1_CCR4L	TIM1 capture/compare register 4 low	00h
00 526Dh		TIM1_BKR	TIM1 break register	00h
00 526Eh		TIM1_DTR	TIM1 dead-time register	00h
00 526Fh		TIM1_OISR	TIM1 output idle state register	00h
00 5270h to 00 52FFh	Reserved area (147 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5300h	TIM2	TIM2_CR1	TIM2 control register 1	00h
00 5301h		TIM2_IER	TIM2 interrupt enable register	00h
00 5302h		TIM2_SR1	TIM2 status register 1	00h
00 5303h		TIM2_SR2	TIM2 status register 2	00h
00 5304h		TIM2_EGR	TIM2 event generation register	00h
00 5305h		TIM2_CCMR1	TIM2 capture/compare mode register 1	00h
00 5306h		TIM2_CCMR2	TIM2 capture/compare mode register 2	00h
00 5307h		TIM2_CCMR3	TIM2 capture/compare mode register 3	00h
00 5308h		TIM2_CCER1	TIM2 capture/compare enable register 1	00h
00 5309h		TIM2_CCER2	TIM2 capture/compare enable register 2	00h
00 530Ah		TIM2_CNTRH	TIM2 counter high	00h
00 530Bh		TIM2_CNTRL	TIM2 counter low	00h
00 530Ch		TIM2_PSCR	TIM2 prescaler register	00h
00 530Dh		TIM2_ARRH	TIM2 auto-reload register high	FFh
00 530Eh		TIM2_ARRL	TIM2 auto-reload register low	FFh
00 530Fh		TIM2_CCR1H	TIM2 capture/compare register 1 high	00h
00 5310h		TIM2_CCR1L	TIM2 capture/compare register 1 low	00h
00 5311h		TIM2_CCR2H	TIM2 capture/compare register 2 high	00h
00 5312h		TIM2_CCR2L	TIM2 capture/compare register 2 low	00h
00 5313h		TIM2_CCR3H	TIM2 capture/compare register 3 high	00h
00 5314h		TIM2_CCR3L	TIM2 capture/compare register 3 low	00h
00 5315h to 00 531Fh	Reserved area (11 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5320h	TIM3	TIM3_CR1	TIM3 control register 1	00h
00 5321h		TIM3_IER	TIM3 interrupt enable register	00h
00 5322h		TIM3_SR1	TIM3 status register 1	00h
00 5323h		TIM3_SR2	TIM3 status register 2	00h
00 5324h		TIM3_EGR	TIM3 event generation register	00h
00 5325h		TIM3_CCMR1	TIM3 capture/compare mode register 1	00h
00 5326h		TIM3_CCMR2	TIM3 capture/compare mode register 2	00h
00 5327h		TIM3_CCER1	TIM3 capture/compare enable register 1	00h
00 5328h		TIM3_CNTRH	TIM3 counter high	00h
00 5329h		TIM3_CNTRL	TIM3 counter low	00h
00 532Ah		TIM3_PSCR	TIM3 prescaler register	00h
00 532Bh		TIM3_ARRH	TIM3 auto-reload register high	FFh
00 532Ch		TIM3_ARRL	TIM3 auto-reload register low	FFh
00 532Dh		TIM3_CCR1H	TIM3 capture/compare register 1 high	00h
00 532Eh		TIM3_CCR1L	TIM3 capture/compare register 1 low	00h
00 532Fh		TIM3_CCR2H	TIM3 capture/compare register 2 high	00h
00 5330h		TIM3_CCR2L	TIM3 capture/compare register 2 low	00h
00 5331h to 00 533Fh	Reserved area (15 bytes)			
00 5340h	TIM4	TIM4_CR1	TIM4 control register 1	00h
00 5341h		TIM4_IER	TIM4 interrupt enable register	00h
00 5342h		TIM4_SR	TIM4 status register	00h
00 5343h		TIM4_EGR	TIM4 event generation register	00h
00 5344h		TIM4_CNTR	TIM4 counter	00h
00 5345h		TIM4_PSCR	TIM4 prescaler register	00h
00 5346h		TIM4_ARR	TIM4 auto-reload register	FFh
00 5347h to 00 53DFh	Reserved area (152 bytes)			

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
53E0h	ADC	ADC_DBH_0	ADC data buffer high register 0	00h
53E1h		ADC_DBL_0	ADC data buffer low register 0	00h
53E2h		ADC_DBH_1	ADC data buffer high register 1	00h
53E3h		ADC_DBL_1	ADC data buffer low register 1	00h
53E4h		ADC_DBH_2	ADC data buffer high register 2	00h
53E5h		ADC_DBL_2	ADC data buffer low register 2	00h
53E6h		ADC_DBH_3	ADC data buffer high register 3	00h
53E7h		ADC_DBL_3	ADC data buffer low register 3	00h
53E8h		ADC_DBH_4	ADC data buffer high register 4	00h
53E9h		ADC_DBL_4	ADC data buffer low register 4	00h
53EAh		ADC_DBH_5	ADC data buffer high register 5	00h
53EBh		ADC_DBL_5	ADC data buffer low register 5	00h
53ECh		ADC_DBH_6	ADC data buffer high register 6	00h
53EDh		ADC_DBL_6	ADC data buffer low register 6	00h
53EEh		ADC_DBH_7	ADC data buffer high register 7	00h
53EFh		ADC_DBL_7	ADC data buffer low register 7	00h
53F0h		ADC_DBH_8	ADC data buffer high register 8	00h
53F1h		ADC_DBL_8	ADC data buffer low register 8	00h
53F2h		ADC_DBH_9	ADC data buffer high register 9	00h
53F3h		ADC_DBL_9	ADC data buffer low register 9	00h
53F4h to 5F3FFh	Reserved area (12 bytes)			
00 5400h	ADC	ADC _CSR	ADC control/status register	00h
00 5401h		ADC_CR1	ADC configuration register 1	00h
00 5402h		ADC_CR2	ADC configuration register 2	00h
00 5403h		ADC_CR3	ADC configuration register 3	00h
00 5404h		ADC_DRH	ADC data register high	00h
00 5405h		ADC_DRL	ADC data register low	00h
00 5406h		ADC_TDRH	ADC Schmitt trigger disable register high	00h
00 5407h		ADC_TDRL	ADC Schmitt trigger disable register low	00h

Table 9. STM8A general hardware register map (continued)

Address	Block	Register label	Register name	Reset status
00 5408h	ADC	ADC_VRHM	Analog WDG threshold high - MSB	00h
00 5409h		ADC_VRHL	Analog WDG threshold high - LSB	00h
00 540Ah		ADC_VRLM	Analog WDG threshold low - MSB	00h
00 540Bh		ADC_VRLL	Analog WDG threshold low - LSB	00h
00 540Ch		ADC_AWH	Analog WDG status register - high	00h
00 540Dh		ADC_AWL	Analog WDG status register - low	00h
00 540Eh		ADC_AWENH	Analog WDG enable register - high	00h
00 540Fh		ADC_AWENL	Analog WDG enable register - low	00h
00 5410h to 00 57FFh	Reserved area (1008 bytes)			
5800h	TMU	TU_KEYS_REG0	TMU key register 0 [7:0]	00h
5801h		TU_KEYS_REG1	TMU key register 1 [7:0]	00h
5802h		TU_KEYS_REG2	TMU key register 2 [7:0]	00h
5803h		TU_KEYS_REG3	TMU key register 3 [7:0]	00h
5804h		TU_KEYS_REG4	TMU key register 4 [7:0]	00h
5805h		TU_KEYS_REG5	TMU key register 5 [7:0]]	00h
5806h		TU_KEYS_REG6	TMU key register 6 [7:0]	00h
5807h		TU_KEYS_REG7	TMU key register 7 [7:0]	00h
5808h		TU_CTL_ST	TMU control and status register	00h

Table 10. CPU/SWIM/debug module/interrupt controller registers

Address	Block	Register label	Register name	Reset status
00 7F00h	CPU	A	Accumulator	00h
00 7F01h		PCE	Program counter extended	00h
00 7F02h		PCH	Program counter high	60h
00 7F03h		PCL	Program counter low	00h
00 7F04h		XH	X index register high	00h
00 7F05h		XL	X index register low	00h
00 7F06h		YH	Y index register high	00h
00 7F07h		YL	Y index register low	00h
00 7F08h		SPH	Stack pointer high	07h
00 7F09h		SPL	Stack pointer low	FFh
00 7F0Ah		CCR	Condition code register	28h
00 7F0Bh to 00 7F5Fh	Reserved area (85 bytes)			
00 7F60h	CFG	CFG_GCR	Global configuration register	00h
00 7F70h	ITC	ITC_SPR1	Interrupt software priority register 1	FFh
00 7F71h		ITC_SPR2	Interrupt software priority register 2	FFh
00 7F72h		ITC_SPR3	Interrupt software priority register 3	FFh
00 7F73h		ITC_SPR4	Interrupt software priority register 4	FFh
00 7F74h		ITC_SPR5	Interrupt software priority register 5	FFh
00 7F75h		ITC_SPR6	Interrupt software priority register 6	FFh
00 7F76h		ITC_SPR7	Interrupt software priority register 7	FFh
00 7F77h to 00 7F79h	Reserved area (3 bytes)			
00 7F80h	SWIM	SWIM_CSR	SWIM control status register	00h
00 7F81h to 00 7F8Fh	Reserved area (15 bytes)			

Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)

Address	Block	Register label	Register name	Reset status
00 7F90h	DM	DM_BK1RE	DM breakpoint 1 register extended byte	FFh
00 7F91h		DM_BK1RH	DM breakpoint 1 register high byte	FFh
00 7F92h		DM_BK1RL	DM breakpoint 1 register low byte	FFh
00 7F93h		DM_BK2RE	DM breakpoint 2 register extended byte	FFh
00 7F94h		DM_BK2RH	DM breakpoint 2 register high byte	FFh
00 7F95h		DM_BK2RL	DM breakpoint 2 register low byte	FFh
00 7F96h		DM_CR1	Debug module control register 1	00h
00 7F97h		DM_CR2	Debug module control register 2	00h
00 7F98h		DM_CSR1	Debug module control/status register 1	10h
00 7F99h		DM_CSR2	Debug module control/status register 2	00h
00 7F9Ah		DM_ENFCTR	DM enable function register	FFh
00 7F9Bh to 00 7F9Fh	Reserved area (5 bytes)			

10 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated block of the memory. Except for the ROP (read-out protection) byte, each option byte has to be stored twice, in a regular form (OPTx) and a complemented one (NOPTx) for redundancy.

Option bytes can be modified in ICP mode (via SWIM) by accessing the EEPROM address shown in *Table 11: Option bytes* below.

Option bytes can also be modified 'on the fly' by the application in IAP mode, except the ROP and UBC options that can only be toggled in ICP mode (via SWIM).

Refer to the STM8 Flash programming manual (PM0047) and STM8 SWIM communication protocol and debug modulel user manual (UM0470) for information on SWIM programming procedures.

Table 11. Option bytes

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4800h	Read-out protection (ROP)	OPT0	ROP[7:0]								00h
4801h	User boot code (UBC)	OPT1	UBC[7:0]								00h
4802h		NOPT1	NUBC[7:0]								FFh
4803h	Alternate function remapping (AFR)	OPT2	AFR7	AFR6	AFR5	AFR4	AFR3	AFR2	AFR1	AFR0	00h
4804h		NOPT2	NAFR7	NAFR6	NAFR5	NAFR4	NAFR3	NAFR2	NAFR1	NAFR0	FFh
4805h	Watchdog option	OPT3	Reserved			16MHZ TIM0	LSI_EN	IWDG_HW	WWDG_HW	WWDG_HALT	00h
4806h		NOPT3	Reserved			N16MHZ TIM0	NLSI_EN	NIWDG_HW	NWWDG_HW	NWWG_HALT	FFh
4807h	Clock option	OPT4	Reserved				EXTCLK	CKAWUSEL	PRSC1	PRSC0	00h
4808h		NOPT4	Reserved				NEXTCLK	NCKAWUSEL	NPRSC1	NPRSC0	FFh
4809h	HSE clock startup	OPT5	HSECNT[7:0]								00h
480Ah		NOPT5	NHSECNT[7:0]								FFh
480Bh	TMU	OPT6	TMU[0:3]								00h
480Ch		NOPT6	NTMU[0:3]								FFh
480Dh	Flash wait states	OPT7	Reserved							WAITSTATE	00h
480Eh		NOPT7	Reserved							NWAITSTATE	FFh
480Fh	Reserved										

Table 11. Option bytes (continued)

Addr.	Option name	Option byte no.	Option bits								Factory default setting
			7	6	5	4	3	2	1	0	
4810h	TMU	OPT8	TMU_KEY 0 [7:0]								00h
4811h		OPT9	TMU_KEY 1 [7:0]								00h
4812h		OPT10	TMU_KEY 2 [7:0]								00h
4813h		OPT11	TMU_KEY 3 [7:0]								00h
4814h		OPT12	TMU_KEY 4 [7:0]								00h
4815h		OPT13	TMU_KEY 5 [7:0]								00h
4816h		OPT14	TMU_KEY 6 [7:0]								00h
4817h		OPT15	TMU_KEY 7 [7:0]								00h
4818h		OPT16	TMU MAX_ATT [7:0]								00h
4819h to 487D	Reserved										
487E	Boot-loader	OPT17	BL_EN [7:0]								00h
487F		NOPT17	NBL_EN [7:0]								00h

Table 12. Option byte description

Option byte no.	Description
OPT0	**ROP[7:0]: Memory readout protection (ROP)** AAh: Enable readout protection (write access via SWIM protocol) *Note: Refer to the STM8A microcontroller family reference manual (RM0009) section on Flash/EEPROM memory readout protection for details.*
OPT1	**UBC[7:0]: User boot code area** 00h: No UBC, no write-protection 01h: Page 0 to 1 defined as UBC, memory write-protected 02h: Page 0 to 3 defined as UBC, memory write-protected 03h to FFh: Pages 4 to 255 defined as UBC, memory write-protected *Note: Refer to the STM8A microcontroller family reference manual (RM0009) section on Flash/EEPROM write protection for more details.*
OPT2	**AFR7: Alternate function remapping option 7** 0: Port D4 alternate function = TIM2_CC1 1: Port D4 alternate function = BEEP **AFR6: Alternate function remapping option 6** 0: Port B5 alternate function = AIN5, port B4 alternate function = AIN4 1: Port B5 alternate function = I^2C_SDA, port B4 alternate function = I^2C_SCL. **AFR5: Alternate function remapping option 5** 0: Port B3 alternate function = AIN3, port B2 alternate function = AIN2, port B1 alternate function = AIN1, port B0 alternate function = AIN0. 1: Port B3 alternate function = TIM1_ETR, port B2 alternate function = TIM1_NCC3, port B1 alternate function = TIM1_NCC2, port B0 alternate function = TIM1_NCC1. **AFR4: Alternate function remapping option 4** 0: Port D7 alternate function = TLI 1: Port D7 alternate function = TIM1_CC4 **AFR3: Alternate function remapping option 3** 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = TIM1_BKIN **AFR2: Alternate function remapping option 2** 0: Port D0 alternate function = TIM3_CC2 1: Port D0 alternate function = CLK_CCO *Note: AFR2 option has priority over AFR3 if both are activated* **AFR1: Alternate function remapping option 1** 0: Port A3 alternate function = TIM2_CC3, port D2 alternate function TIM3_CC1. 1: Port A3 alternate function = TIM3_CC1, port D2 alternate function TIM2_CC3. **AFR0: Alternate function remapping option 0** 0: Port D3 alternate function = TIM2_CC2 1: Port D3 alternate function = ADC_ETR

Table 12. Option byte description (continued)

Option byte no.	Description
OPT3	**16MHZTRIM0: Trimming option for 16 MHz internal RC oscillator** 0: 3-bit on-the-fly trimming (compatible with 128 Kbyte device) 1: 4-bit on-the-fly trimming
	LSI_EN: Low speed internal clock enable 0: LSI clock is not available as CPU clock source 1: LSI clock is available as CPU clock source
	IWDG_HW: Independent watchdog 0: IWDG Independent watchdog activated by software 1: IWDG Independent watchdog activated by hardware
	WWDG_HW: Window watchdog activation 0: WWDG window watchdog activated by software 1: WWDG window watchdog activated by hardware
	WWDG_HALT: Window watchdog reset on halt 0: No reset generated on halt if WWDG active 1: Reset generated on halt if WWDG active
OPT4	**EXTCLK: External clock selection** 0: External crystal connected to OSCIN/OSCOUT 1: External clock signal on OSCIN
	CKAWUSEL: Auto wake-up unit/clock 0: LSI clock source selected for AWU 1: HSE clock with prescaler selected as clock source for for AWU
	PRSC[1:0]: AWU clock prescaler 00: 24 MHz to 128 kHz prescaler 01: 16 MHz to 128 kHz prescaler 10: 8 MHz to 128 kHz prescaler 11: 4 MHz to 128 kHz prescaler
OPT5	**HSECNT[7:0]: HSE crystal oscillator stabilization time** This configures the stabilisation time to 0, 16, 256, 4096 HSE cycles.
OPT6	**TMU[3:0]: Enable temporary memory unprotection** 0101: Read-out protection can be temporary disabled using a key sequence. Any other value: Permanent ROP
OPT7	**WAIT STATE: Wait state configuration** This option configures the number of wait states inserted when reading from the Flash/data EEPROM memory. 0: No wait state 1: One wait state
OPT8	**TMU_KEY 0 [7:0]: Temporary unprotection key 0** Temporary unprotection key: Must be different from 00h or FFh
OPT9	**TMU_KEY 1 [7:0]: Temporary unprotection key 1** Temporary unprotection key: Must be different from 00h or FFh
OPT10	**TMU_KEY 2 [7:0]: Temporary unprotection key 2** Temporary unprotection key: Must be different from 00h or FFh

Table 12. Option byte description (continued)

Option byte no.	Description
OPT11	**TMU_KEY 3 [7:0]: Temporary unprotection key 3** Temporary unprotection key: Must be different from 00h or FFh
OPT12	**TMU_KEY 4 [7:0]: Temporary unprotection key 4** Temporary unprotection key: Must be different from 00h or FFh
OPT13	**TMU_KEY 5 [7:0]: Temporary unprotection key 5** Temporary unprotection key: Must be different from 00h or FFh
OPT14	**TMU_KEY 6 [7:0]: Temporary unprotection key 6** Temporary unprotection key: Must be different from 00h or FFh
OPT15	**TMU_KEY 7 [7:0]: Temporary unprotection key 7** Temporary unprotection key: Must be different from 00h or FFh
OPT16	**TMU_MAXATT [7:0]: TMU access failure counter** Every unsuccessful trial to enter the temporary unprotection procedure increments the counter. More than eight unsuccessful trials trigger the global erase of the code and data memory.
OPT17	**BL_EN [7:0]: Bootloader enable** If this optionbyte is set to 55h (complementary value AAh) the bootloader program is activated also in case of a programmed code memory (for more details, see the bootloader user manual, UM0500).

11 Electrical characteristics

11.1 Parameter conditions

Unless otherwise specified, all voltages are referred to V_{SS}.

11.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production.

11.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 5.0 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

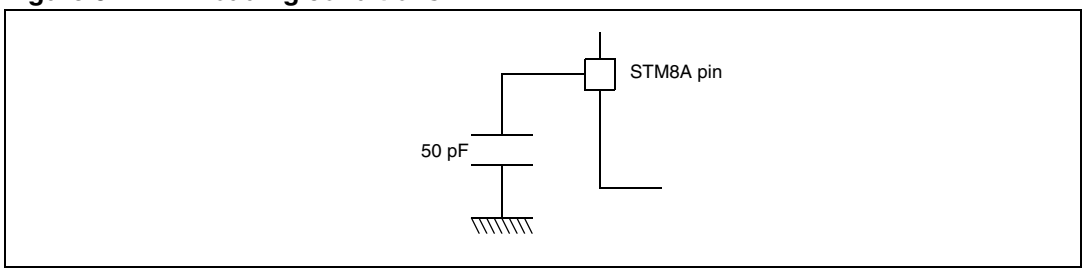
11.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

11.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 6*.

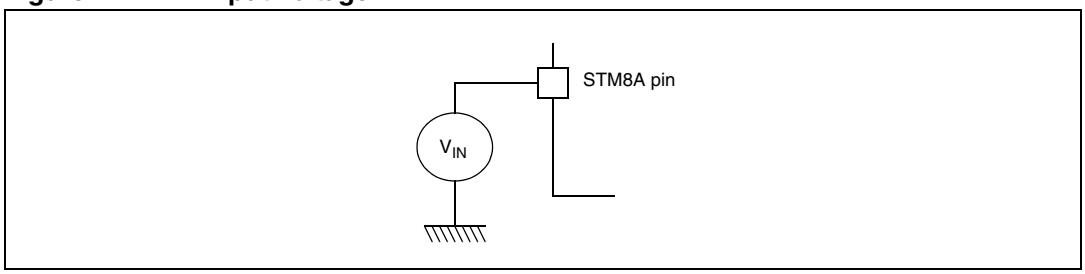
Figure 6. Pin loading conditions



11.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 7*.

Figure 7. Pin input voltage



11.2 Absolute maximum ratings

Stresses above those listed as 'absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 13. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	Supply voltage (including V_{DDA} and V_{DDIO})(1)	-0.3	6.5	V
V_{IN}	Input voltage on true open drain pins (PE1, PE2)(2)	V_{SS} - 0.3	6.5	
	Input voltage on any other pin(2)	V_{SS} - 0.3	V_{DD} + 0.3	
$\lvert V_{DDx} - V_{SS} \rvert$	Variations between different power pins		50	mV
$\lvert V_{SSx} - V_{SS} \rvert$	Variations between all the different ground pins		50	
V_{ESD}	Electrostatic discharge voltage	see *Absolute maximum ratings (electrical sensitivity) on page 79*		

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external power supply
2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current, and the corresponding V_{IN} maximum must always be respected

Table 14. Current characteristics

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(1)(2)	60	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(1)(2)	60	
I_{IO}	Output current sunk by any I/O and control pin	20	
	Output current source by any I/Os and control pin	- 20	
$I_{INJ(PIN)}$(3)	Injected current on NRST pin	± 10	
	Injected current on OSCIN pin	± 10	
	Injected current on any other pin	± 10	
$\Sigma I_{INJ(PIN)}$(4)	Total injected current (sum of all I/O and control pins)	± 20	

1. All power (V_{DD}, V_{DDIO}, V_{DDA}) and ground (V_{SS}, V_{SSIO}, V_{SSA}) pins must always be connected to the external supply.
2. The total limit applies to the sum of operation and injected currents.
3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. For true open-drain pads, there is no positive injection current allowed and the corresponding V_{IN} maximum must always be respected.
4. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the sum of the absolute positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 15. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	

11.3 Operating conditions

Table 16. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CPU}	Internal CPU clock frequency	Full range	0	16	MHz
V_{DD}/V_{DD_IO}	Standard operating voltage		3.0	5.5	V
T_A	Ambient temperature	Suffix A	-40	85	°C
		Suffix B	-40	105	°C
		Suffix C	-40	125	°C
		Suffix D	-40	145	°C
T_J	Junction temperature range	A suffix version	-40	90	°C
		B suffix version	-40	110	°C
		C suffix version	-40	130	°C
		D suffix version	-40	150	°C

Figure 8. f_{CPUmax} versus V_{DD}

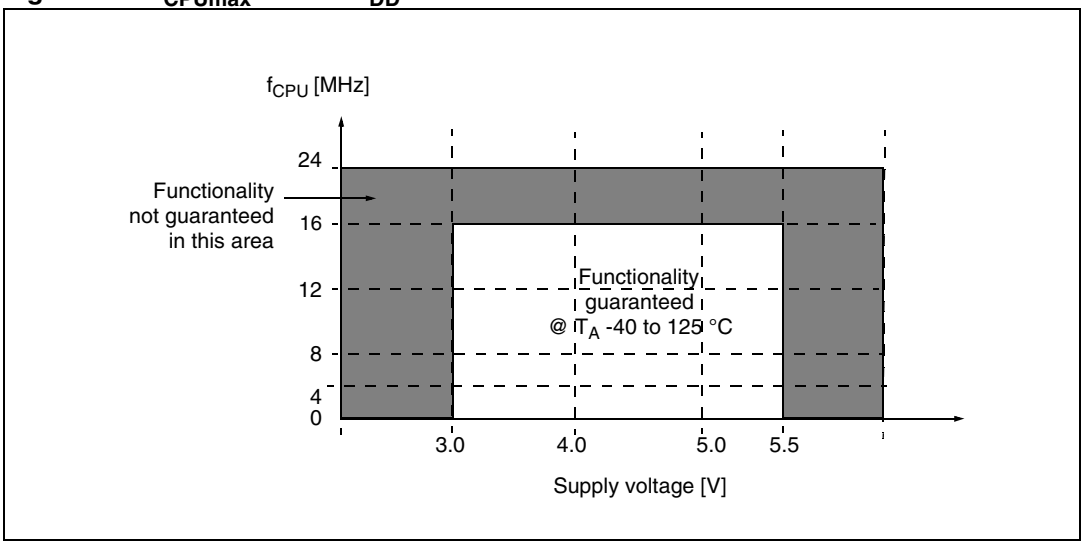


Table 17. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VDD}	V_{DD} rise time rate		20(1)		∞	µs/V
	V_{DD} fall time rate(3)		20(2)		∞	
t_{TEMP}	Reset release delay	V_{DD} rising	TBD(2)	3		ms
	Reset generation delay(3)	V_{DD} falling	TBD(2)	3		µs
V_{IT+}	Power-on reset threshold		2.65	2.8	2.95	V
V_{IT-}	Brown-out reset threshold		2.58	2.73	2.88	V
$V_{HYS(BOR)}$	Brown-out reset hysteresis			70(1)		mV

1. Guaranteed by design, not tested in production
2. TBD = To be determined
3. Reset is always generated after a t_{TEMP} delay. The application must ensure that V_{DD} is still above the minimum operating voltage (V_{DD} min) when the t_{TEMP} delay has elapsed.

11.3.1 Supply current characteristics

The current consumption is measured as described in *Figure 6 on page 48* and *Figure 7 on page 49*.

Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except if explicitly mentioned.

Subject to general operating conditions for V_{DD} and T_A.

Note on the run-current typical and worst-case values

- Typical device currents values are representative of an application set-up without any I/O activity at 25 °C. The worst case values correspond to the actual test-limits and include both internal and external device I/O current.
- During the execution of an actual application program, the number of read access cycles to the code memory depends on its structure. A code doing arithmetical calculations reads the memory less frequently than programs with jump, loop or data manipulation instructions. The fast-reading access in a Flash memory needs much more power compared to a RAM. Consequently, the run-current for EEPROM execution depends strongly on the actual application code structure. The measurements in the tables below were made using a short, representative code with move, jump and arithmetic operations. The worst case, an infinite loop of ‘while’ instructions takes approximately 25 % more power. For RAM execution, such power to program structure relations has not been observed.

Table 18. Total current consumption in run, wait and slow mode at V_{DD} = 5.0 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from RAM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	3.3		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	2.7	6.0(1)	
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	2.55		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.2		
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from EEPROM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	9.0		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	8.35	15.0(1)	
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	8.2		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.9		
$I_{DD(RUN)}$	Supply current in run mode	All digital peripherals on, code executed from RAM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	4.3		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	3.7	8.0(1)	
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	3.5		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.2		
$I_{DD(RUN)}$	Supply current in run mode	All digital peripherals on, code executed from EEPROM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	10.0		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	9.35		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	9.2		
			HSI internal RC 16 MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	2.1		
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals off	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	2.0		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	1.38	4.0(1)	
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	1.21		
			HSI internal RC 16 MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.05		

Table 18. Total current consumption in run, wait and slow mode at V_{DD} = 5.0 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(SLOW)}$	Supply current in slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	HSE external clock 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.15	4.0(1)	mA
			HSI internal RC 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.04		
			LSI internal RC 128 kHz $f_{CPU} = f_{MASTER} = 0.128$ MHz	0.5		
		f_{CPU} scaled down, all peripherals off, code executed from EEPROM	HSE external clock 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.21		
			HSI internal RC 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.09		
			LSI internal RC 128 kHz $f_{CPU} = f_{MASTER} = 0.128$ MHz	0.56		

1. Prodution test limits

Table 19. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 5.0 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash powered down	6.5	10(1)	µA
		Flash in stand-by mode	64		
$I_{DD(FAH)}$	Supply current in fast active halt mode	Crystal osc 16 MHz/128	1050		
		HSE osc 16 MHz/128	490		
		LSI RC 128 kHz	150	200(1)	
$I_{DD(SAH)}$	Supply current in slow active halt mode	LSI RC 128 kHz	11	30(1)	
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode			2(2)	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode			100(2)	

1. Maximum values at 55 °C, tested in production according to the actual product temperature ranges.
2. Data based on characterization results, not tested in production.

Table 20. Total current consumption in run, wait and slow mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from RAM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	2.9		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	2.7		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	2.55		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.2		
$I_{DD(RUN)}$	Supply current in run mode	All peripherals off, code executed from EEPROM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	8.6		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	8.35		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	8.2		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.6		
$I_{DD(RUN)}$	Supply current in run mode	All peripherals on, code executed from RAM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	3.9		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	3.7		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	3.55		
			HSI internal RC 16MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.4		
$I_{DD(RUN)}$	Supply current in run mode	All peripherals on, code executed from EEPROM	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	9.6		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	9.35		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	9.2		
			HSI internal RC 16 MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.8		
$I_{DD(WFI)}$	Supply current in wait mode	CPU not clocked, all peripherals off	HSE Crystal oscillator $f_{CPU} = f_{MASTER}$ = 16 MHz	1.6		mA
			HSE external clock $f_{CPU} = f_{MASTER}$ = 16 MHz	1.38		
			HSI internal RC $f_{CPU} = f_{MASTER}$ = 16 MHz	1.21		
			HSI internal RC 16 MHz/8 $f_{CPU} = f_{MASTER}$ = 2 MHz	1.05		

Table 20. Total current consumption in run, wait and slow mode at V_{DD} = 3.3 V

Symbol	Parameter	Conditions		Typ	Max	Unit
$I_{DD(SLOW)}$	Supply current in slow mode	f_{CPU} scaled down, all peripherals off, code executed from RAM	HSE external clock 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.15		mA
			HSI internal RC 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.04		
			LSI internal RC 128 kHz $f_{CPU} = f_{MASTER} = 0.128$MHz	0.5		
		f_{CPU} scaled down, all peripherals off, code executed from EEPROM	HSE external clock 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.21		
			HSI internal RC 16 MHz/128 $f_{CPU} = f_{MASTER} = 0.125$ MHz	1.09		
			LSI internal RC 128 kHz $f_{CPU} = f_{MASTER} = 0.128$ MHz	0.56		

Table 21. Total current consumption and timing in halt, fast active halt and slow active halt modes at V_{DD} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$I_{DD(H)}$	Supply current in halt mode	Flash powered down	4.7		µA
		Flash in stand-by mode	62		
$I_{DD(FAH)}$	Supply current in fast active halt mode	Crystal osc 16 MHz/128	600		
		HSE osc 16 MHz/128	490		
		LSI RC 128 kHz	140		
$I_{DD(SAH)}$	Supply current in slow active halt mode	LSI RC 128 kHz	9		
$t_{WU(FAH)}$	Wake-up time from fast active halt mode to run mode			2(1)	µs
$t_{WU(SAH)}$	Wake-up time from slow active halt mode to run mode			100(1)	

1. Data based on characterization results, not tested in production

On-chip peripherals

Table 22. Typical peripheral current consumption V_{DD} = 5.0 V(1)

Symbol	Parameter	Typ. f_{master} = 2 MHz	Typ. f_{master} = 16 MHz	Typ. f_{master} = 24 MHz	Unit
$I_{DD(TIM1)}$	TIM1 supply current(2)	0.03	0.23	0.34	mA
$I_{DD(TIM2)}$	TIM2 supply current (2)	0.02	0.12	0.19	
$I_{DD(TIM3)}$	TIM3 supply current(2)	0.01	0.1	0.16	
$I_{DD(TIM4)}$	TIM4 supply current(2)	0.004	0.03	0.05	
$I_{DD(USART)}$	USART supply current(2)	0.03	0.09	0.15	
$I_{DD(LINUART)}$	LINUART supply current(2)	0.03	0.11	0.18	
$I_{DD(SPI)}$	SPI supply current(2)	0.01	0.04	0.07	
$I_{DD(I^2C)}$	I^2C supply current(2)	0.02	0.06	0.91	
$I_{DD(CAN)}$	CAN supply current(3)	0.06	0.22	0.34	
$I_{DD(AWU)}$	AWU supply current(2)	0.003	0.02	0.05	
$I_{DD(TOT\_DIG)}$	All digital peripherals on	0.22	1	2.4	
$I_{DD(ADC)}$	ADC supply current when converting(4)	0.93	0.95	0.96	
$I_{DD(EE\_PROG)}$	Data EEPROM programming current	2.5	2.9	3.1	

1. Typical values - not tested in production. Since the peripherals are powered by an internally regulated, constant digital supply voltage, the values are similar in the full supply voltage range.
2. Data based on a differential I_{DD} measurement between no peripheral clocked and a single active peripheral. This measurement does not include the pad toggling consumption.
3. Data based on a differential IDD measurement between reset configuration (CAN disabled) and a permanent CAN data transmit sequence in loopback mode at 1 MHz. This measurement does not include the pad toggling consumption.
4. Data based on a differential I_{DD} measurement between reset configuration and continuous A/D conversions.

Current consumption curves

Figure 9 to *Figure 14* show typical current consumption measured with code executing in RAM.

Figure 9. Typ. $I_{DD(RUN)HSE}$ vs. V_{DD} @f_{CPU} = 16 MHz, periph = on

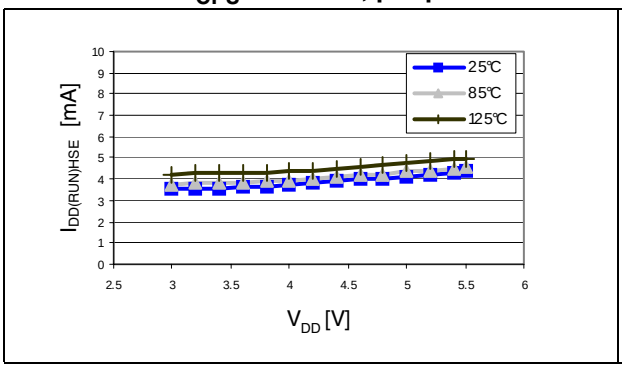


Figure 10. Typ. $I_{DD(RUN)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, periph = on

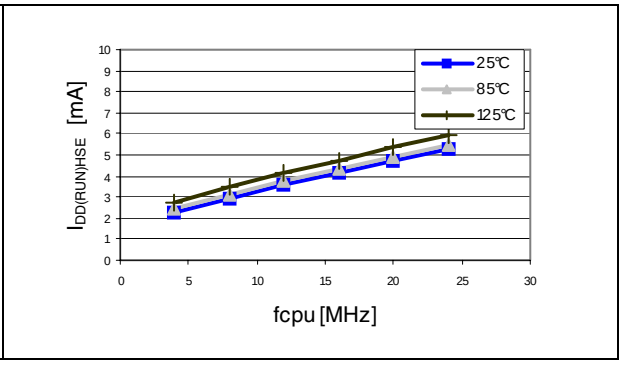


Figure 11. Typ. $I_{DD(RUN)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, periph = off

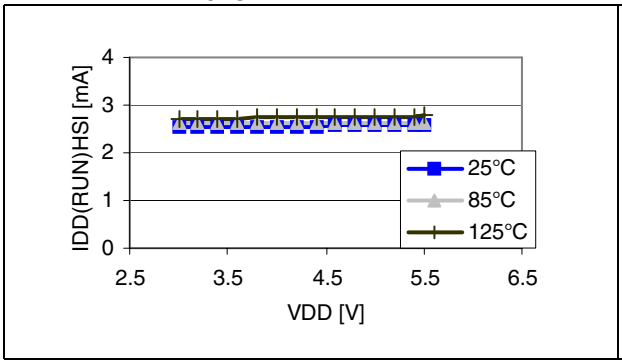


Figure 12. Typ. $I_{DD(WFI)HSE}$ vs. V_{DD} @ f_{CPU} = 16 MHz, periph = on

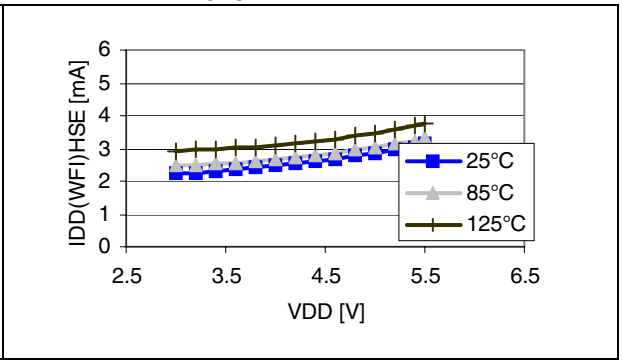


Figure 13. Typ. $I_{DD(WFI)HSE}$ vs. f_{CPU} @ V_{DD} = 5.0 V, periph = on

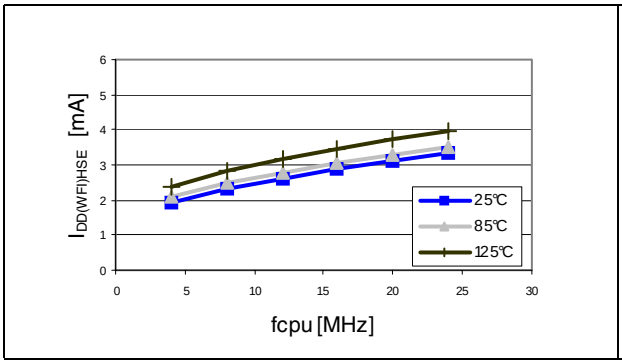
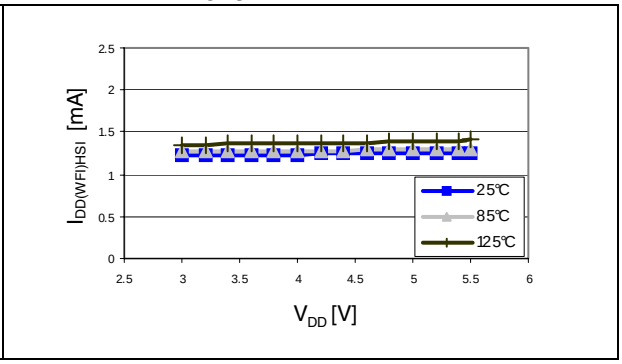


Figure 14. Typ. $I_{DD(WFI)HSI}$ vs. V_{DD} @ f_{CPU} = 16 MHz, periph = off



11.3.2 External clock sources and timing characteristics

HSE user external clock

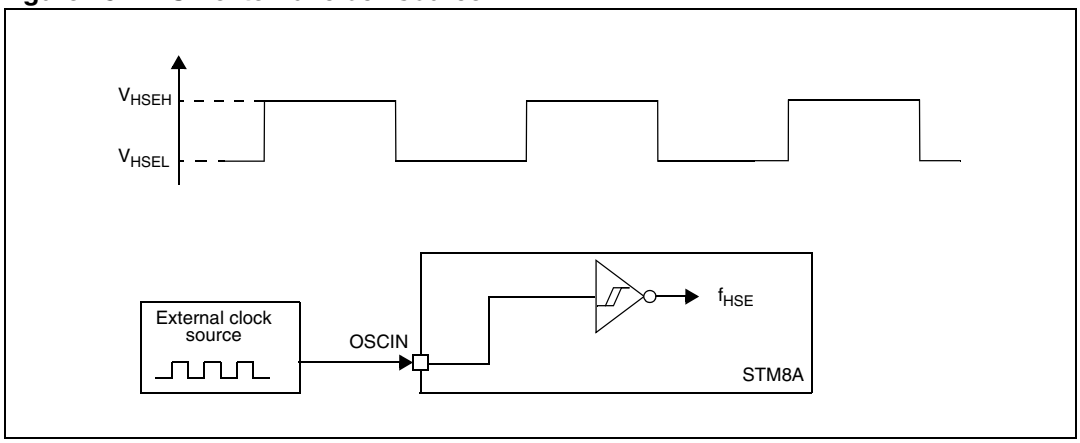
Subject to general operating conditions for V_{DD} and T_A.

Table 23. HSE user external clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency		0(1)		16	MHz
V_{HSEdHL}	Comparator hysteresis		0.1 x V_{DD}			V
V_{HSEH}	OSCIN input pin high level voltage		0.7 x V_{DD}		V_{DD}	V
V_{HSEL}	OSCIN input pin low level voltage		V_{SS}		0.3 x V_{DD}	
I_{LEAK_HSE}	OSCIN input leakage current	$V_{SS} < V_{IN} < V_{DD}$	-1		+1	µA

1. In case of CSS, the external clock must have a frequency above 500 kHz.

Figure 15. HSE external clock source



HSE crystal/ceramic resonator oscillator

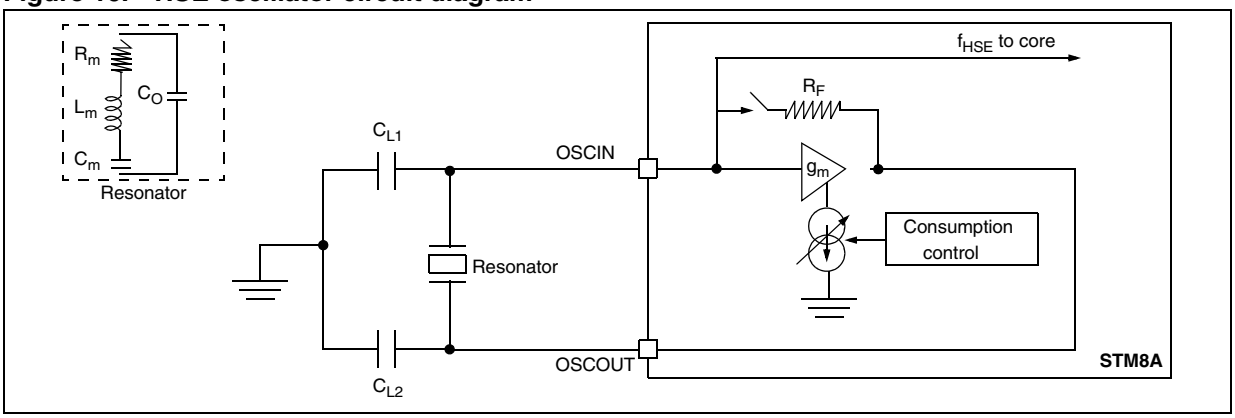
The HSE clock can be supplied using a crystal/ceramic resonator oscillator of up to 16 MHz. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

Table 24. HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor			220		kΩ
$C^{(1)}$	Recommended load capacitance$^{(2)}$				20	pF
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF			6 (startup) 2 (stabilized)	mA
		C = 10 pF			6 (startup) 1.5 (stabilized)	
g_m	Oscillator transconductance		5			mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized		1		ms

1. C is approximately equivalent to 2 x crystal Cload.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small R_m value. Refer to crystal manufacturer for more details
3. $t_{SU(HSE)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Figure 16. HSE oscillator circuit diagram



HSE oscillator critical g_m formula

$$g_{mcrit} = (2 \times \Pi \times {}^{f}HSE)^2 \times R_m(2Co + C)^2$$

R_m: Notional resistance (see crystal specification)
L_m: Notional inductance (see crystal specification)
C_m: Notional capacitance (see crystal specification)
Co: Shunt capacitance (see crystal specification)
$C_{L1} = C_{L2} = C$: Grounded external capacitance
$g_m >> g_{mcrit}$

11.3.3 Internal clock sources and timing characteristics

Subject to general operating conditions for V_{DD} and T_A.

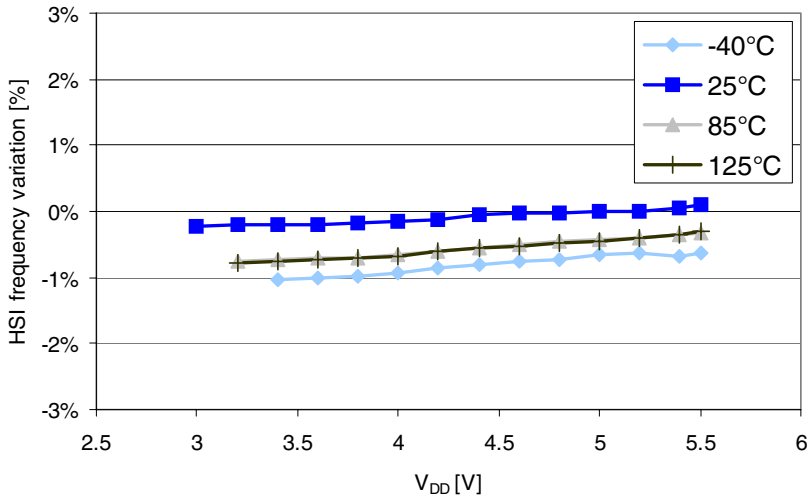
High speed internal RC oscillator (HSI)

Table 25. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			16		MHz
ACC_{HS}	HSI oscillator user trimming accuracy	Trimmed by the application for any V_{DD} and T_A conditions	-1(1)		1(1)	%
	HSI oscillator accuracy (factory calibrated)	V_{DD} = 5.0 V, T_A = 25°C	-1(1)		1(1)	
		V_{DD} = 5.0 V, 25 °C ≤T_A ≤85 °C		±2		
		V_{DD} = 5.0 V, 25 °C ≤T_A ≤125 °C	-3(1)		3(1)	
		V_{DD} = 3.0 V ≤V_{DD} ≤ 5.5 V, -40 °C ≤T_A ≤ 125 °C	-5(1)		5(1)	
$t_{su(HSI)}$	HSI oscillator wake-up time including calibration				2(2)	µs

1. Tested in production
2. Guaranteed by design, not tested in production

Figure 17. Typical HSI frequency vs V_{DD} @ four temperatures



Low speed internal RC oscillator (LSI)

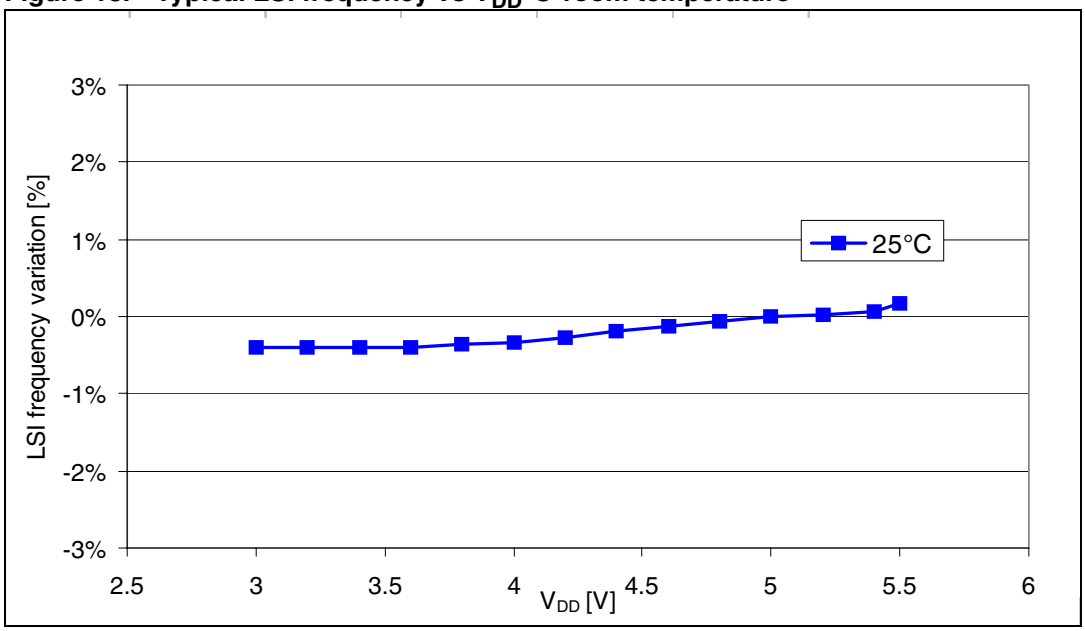
Subject to general operating conditions for V_{DD} and T_A.

Table 26. LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency		112	128	144	kHz
$t_{su(LSI)}$	LSI oscillator wake-up time				7(1)	µs

1. Data based on characterization results, not tested in production.

Figure 18. Typical LSI frequency vs V_{DD} @ room temperature



11.3.4 Memory characteristics

RAM and hardware registers

Table 27. RAM and hardware registers

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RM}	Data retention mode(1)	Halt mode (or reset)	1.8			V

1. Minimum supply voltage without losing data stored in RAM (in halt mode or under reset) or in hardware registers (only in halt mode). Guaranteed by design, not tested in production. refer to *Table 17 on page 52* for the value of V_{IT-max}

Flash program memory/data EEPROM memory

General conditions: T_A = -40 to 125 °C.

Table 28. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
V_{DD}	Operating voltage (all modes, execution/write/erase)	f_{CPU} ≤16 MHz	3.0		5.5	V
t_{prog}	Standard programming time (including erase) for byte/word/block (1 byte/4 bytes/128 bytes)			6	6.6	ms
	Fast programming time for 1 block (128 bytes)			3	3.3	ms
t_{erase}	Erase time for 1 block (128 bytes)			3	3.3	ms
N_{RW}	Program memory endurance erase/write cycles(2)	T_A = 25 °C	1 k			cycles
		T_A = 125 °C	100			
	Data memory endurance erase/write cycles(2)	T_A = 25 °C	300 k			
		T_A = 125 °C	100 k			
		T_A = 145 °C	80 k			
t_{RET}	Program memory after cycling	T_A = 25 °C	40			years
		T_A = 55 °C	20			
		T_A = 85 °C	10			
	Data memory retention after cycling at the endurance limits (T, n)	Full temperature range	1000			hours
t_{RETI}	Intrinsic data retention	T_A = 25 °C	40			years
		T_A = 55 °C	20			
		T_A = 85 °C	10			

1. Guaranteed by characterization, not tested in production.
2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

11.3.5 I/O port pin characteristics

General characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified. All unused pins must be kept at a fixed voltage, using the output mode of the I/O for example or an external pull-up or pull-down resistor.

Table 29. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	V_{DD} = 5.0 V	-0.3 V		0.3 x V_{DD}	V
V_{IH}	Input high level voltage		0.7 x V_{DD}		V_{DD} + 0.3 V	V
V_{hys}	Hysteresis(1)			0.1 x V_{DD}		mV
V_{OH}	I = 3 mA	Standard I/0, V_{DD} = 5 V	V_{DD} - 0.5 V			V
	I = 1.5 mA	Standard I/0, V_{DD} = 3 V	V_{DD} - 0.4 V			
V_{OL}	I = 8mA	High sink and true open drain I/0, V_{DD} = 5 V			0.5	
	I = 3 mA	Standard I/0, V_{DD} = 5 V			0.6	
	I = 1.5 mA	Standard I/0, V_{DD} = 3 V			0.4	
R_{pu}	Pull-up resistor	V_{DD} = 5 V, V_{IN} = V_{SS}	35	50	65	kΩ
t_R, t_F	Rise and fall time (10% - 90%)	Fast I/Os Load = 50 pF			20(2)	ns
		Standard and high sink I/Os Load = 50 pF			125(2)	ns
I_{lkg}	Input leakage current, analog and digital	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1(2)	µA
$I_{lkg\ ana}$	Analog input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$ -40 °C < T_A < 125 °C			±250(2)	nA
$I_{lkg(inj)}$	Leakage current in adjacent I/O(2)	Injection current ±4 mA			±1(2)	µA

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested in production.
2. Data based on characterization results, not tested in production.

Figure 19. Typical V_{IL} and V_{IH} vs V_{DD} @ four temperatures

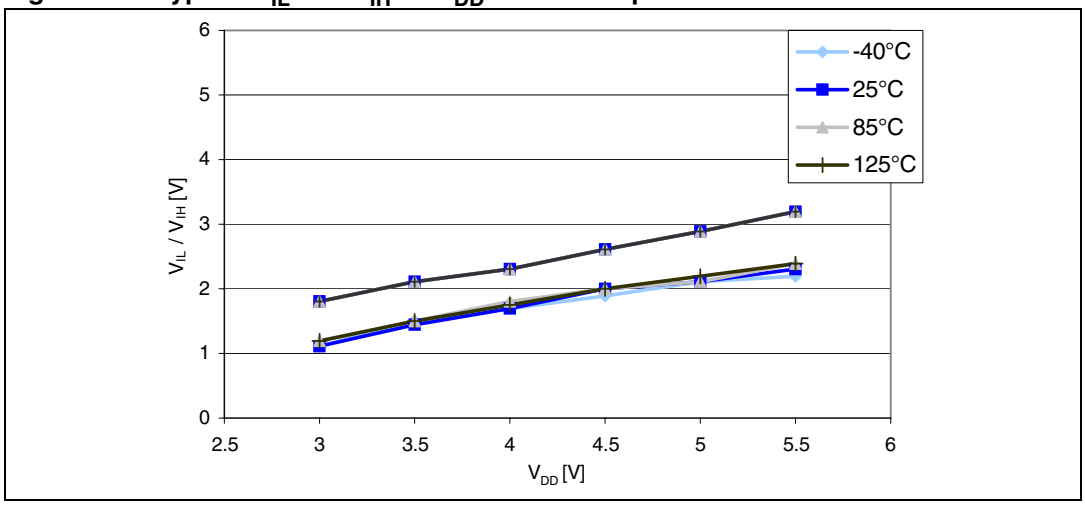


Figure 20. Typical pull-up resistance R_{PU} vs V_{DD} @ four temperatures

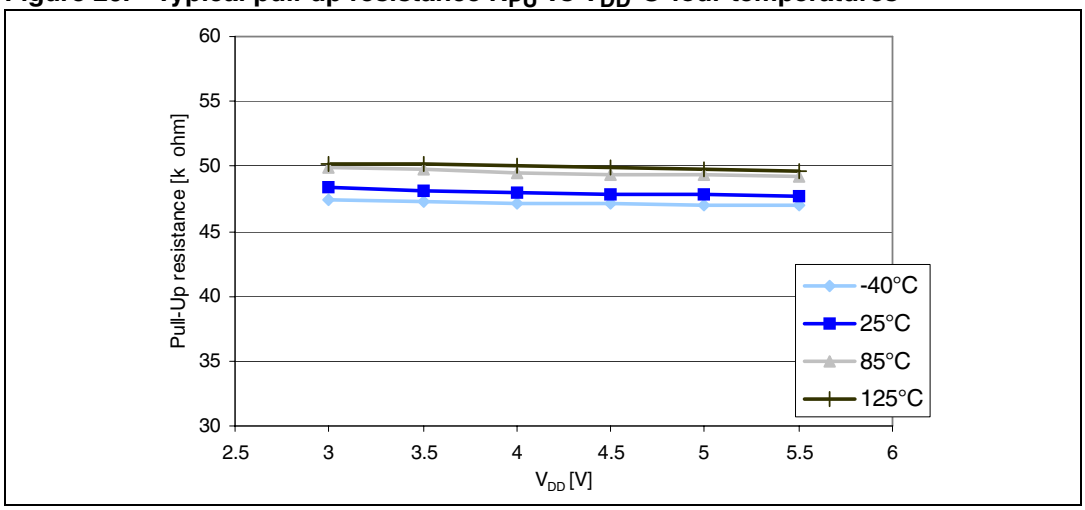
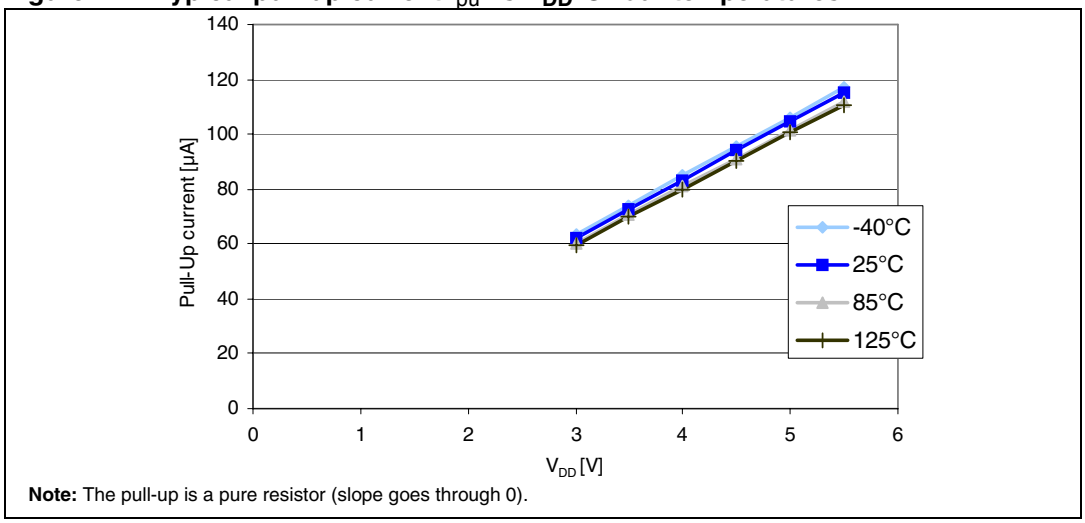


Figure 21. Typical pull-up current I_{pu} vs V_{DD} @ four temperatures



Note: The pull-up is a pure resistor (slope goes through 0).

Typical output level curves

Figure 22 to *Figure 31* show typical output level curves measured with output on a single pin.

Figure 22. Typ. V_{OL} @ V_{DD} = 3.3 V (standard ports)

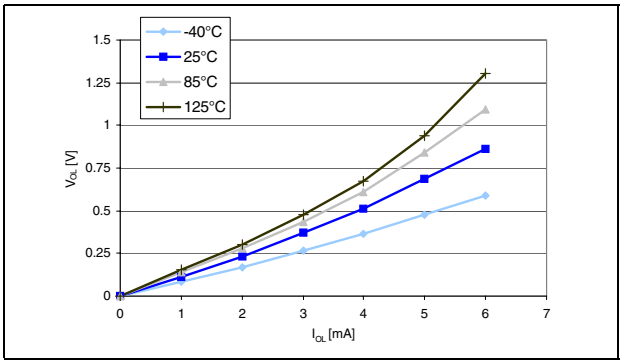


Figure 23. Typ. V_{OL} @ V_{DD} = 5.0 V (standard ports)

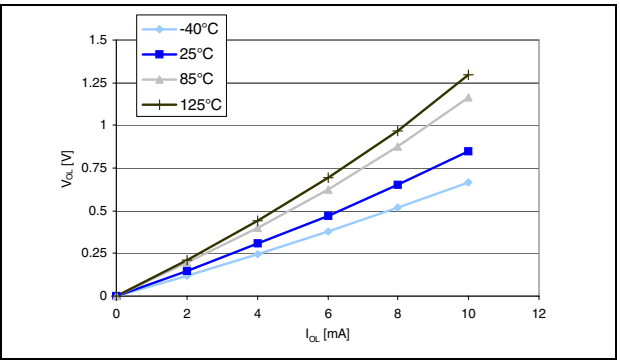


Figure 24. Typ. V_{OL} @ V_{DD} = 3.3 V (true open drain ports)

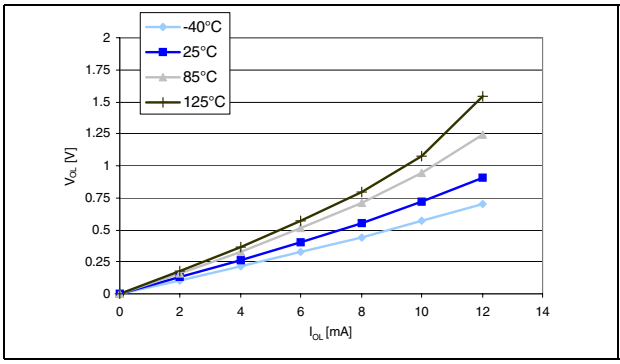


Figure 25. Typ. V_{OL} @ V_{DD} = 5.0 V (true open drain ports)

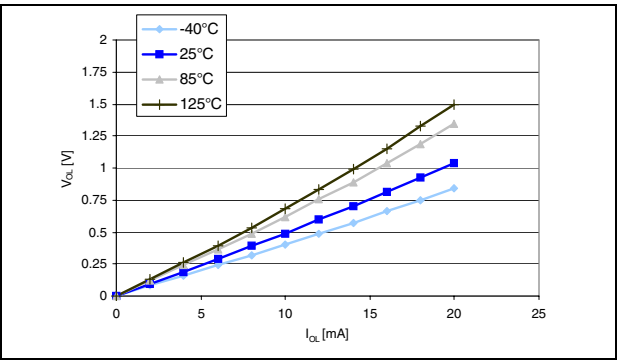


Figure 26. Typ. V_{OL} @ V_{DD} = 3.3 V (high sink ports)

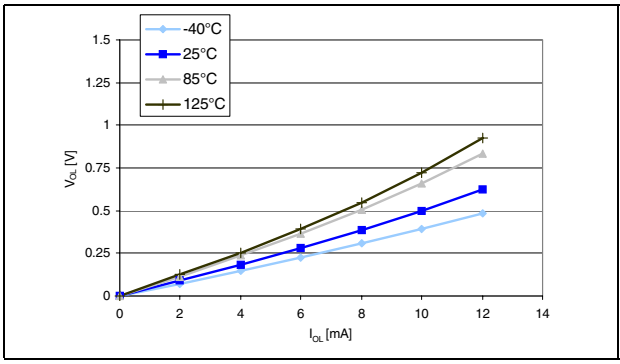


Figure 27. Typ. V_{OL} @ V_{DD} = 5.0 V (high sink ports)

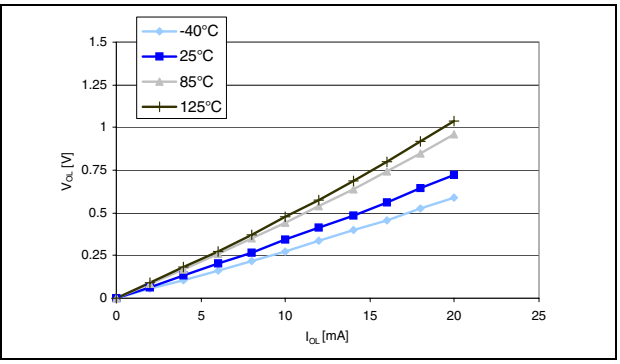


Figure 28. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (standard ports)

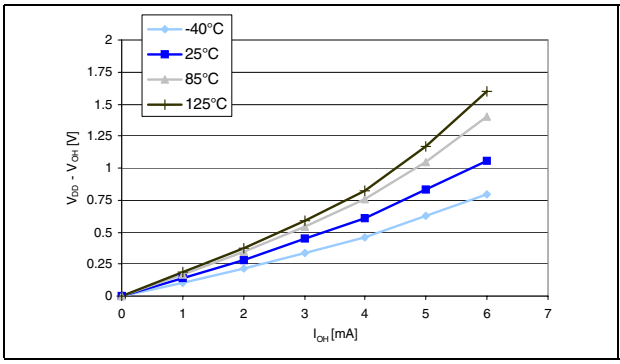


Figure 29. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (standard ports)

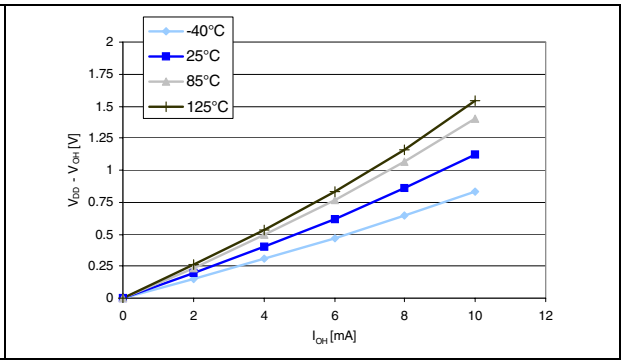


Figure 30. Typ. V_{DD} - V_{OH} @ V_{DD} = 3.3 V (high sink ports)

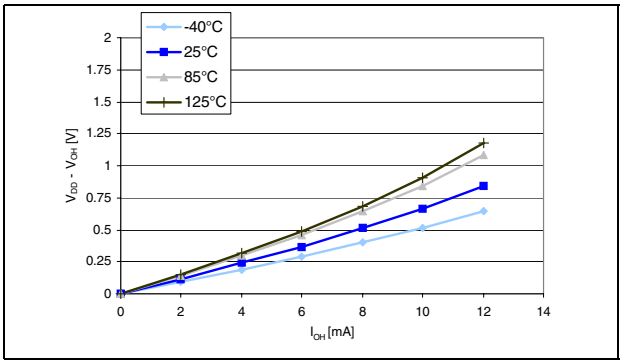
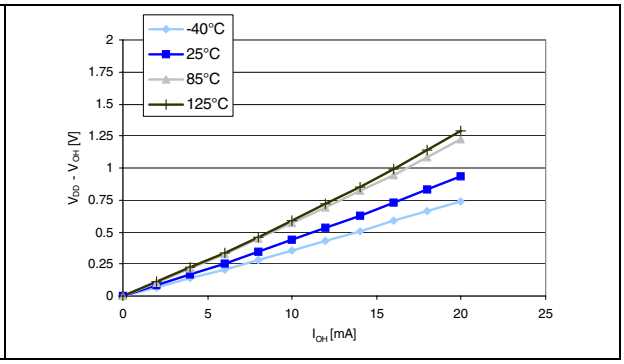


Figure 31. Typ. V_{DD} - V_{OH} @ V_{DD} = 5.0 V (high sink ports)



11.3.6 Reset pin characteristics

Subject to general operating conditions for V_{DD} and T_A unless otherwise specified.

Table 30. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage(1)		V_{SS}		TBD(2)	V
$V_{IH(NRST)}$	NRST input high level voltage(1)		TBD(2)		V_{DD}	
$V_{OL(NRST)}$	NRST output low level voltage(1)	I_{OL}=TBD(2) mA			TBD(2)	
$R_{PU(NRST)}$	NRST pull-up resistor(3)		30	40	60	kΩ
$V_{F(NRST)}$	NRST input filtered pulse(4)			TBD(2)		ns
$V_{NF(NRST)}$	NRST input not filtered pulse(4)			TBD(2)		µs

1. Data based on characterization results, not tested in production.
2. TBD = To be determined.
3. The R_{PU} pull-up equivalent resistor is based on a resistive transistor
4. Data guaranteed by design, not tested in production.

Figure 32. Typical NRST V_{IL} and V_{IH} vs V_{DD} @ four temperatures

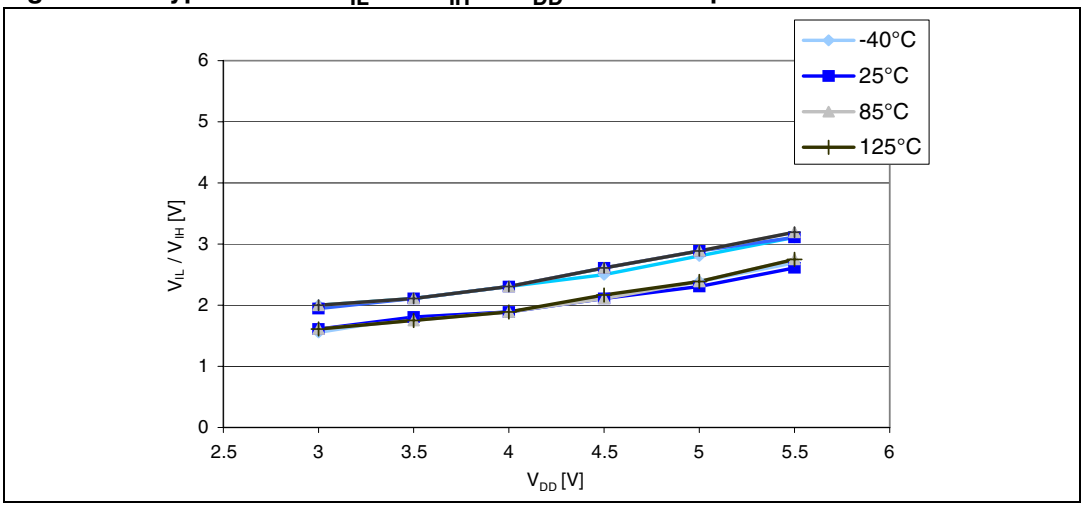


Figure 33. Typical NRST pull-up resistance R_{PU} vs V_{DD} @ four temperatures

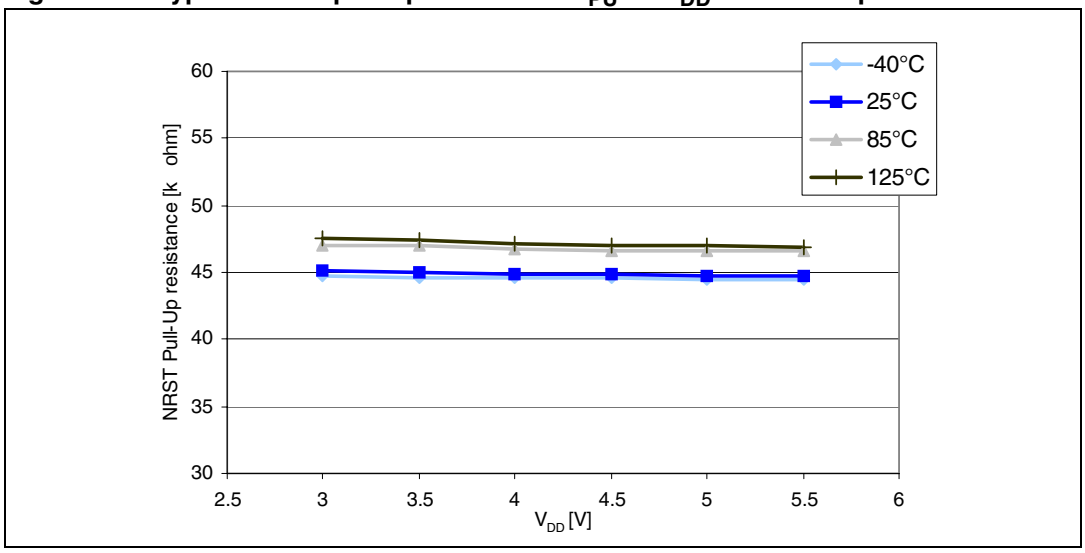
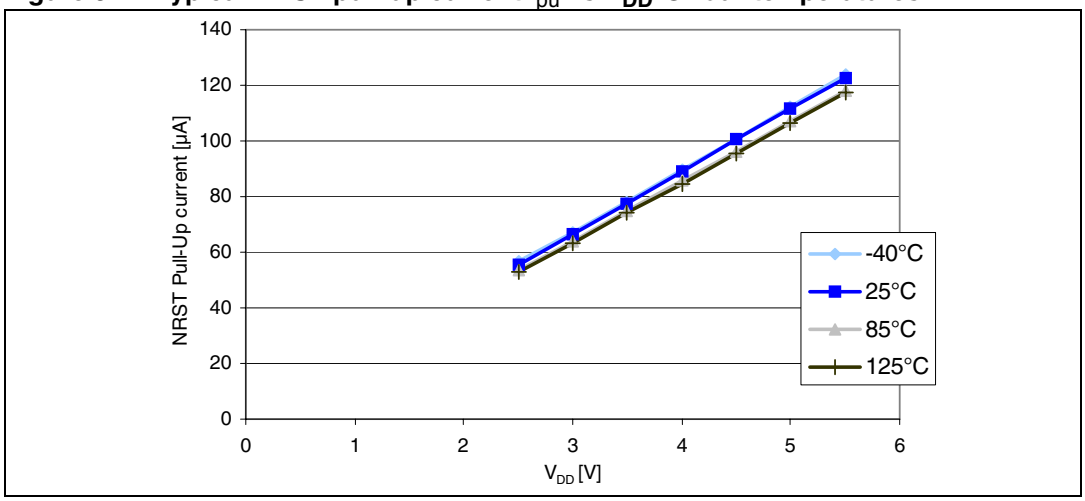
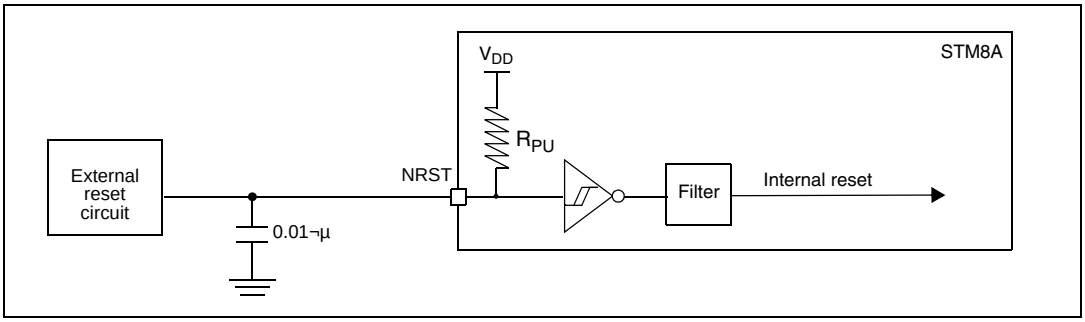


Figure 34. Typical NRST pull-up current I_{pu} vs V_{DD} @ four temperatures



The reset network shown in *Figure 35* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the V_{IL} max. level specified in *Table 29*. Otherwise the reset is not taken into account internally.

Figure 35. Recommended reset pin protection



11.3.7 TIM 1, 2, 3, and 4 timer characteristics

Subject to general operating conditions for V_{DD}, f_{MASTER}, and T_A unless otherwise specified.

Table 31. TIM 1, 2, 3 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(ICAP)in}$	Input capture pulse time(1)		2			T_{MASTER}
$t_{res(TIM)}$	Timer resolution time(1)		1			T_{MASTER}
f_{EXT}	Timer external clock frequency(1)				24	MHz
Res_{TIM}	Timer resolution(1)			16		bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected(1)			1		T_{MASTER}
t_{MAX_COUNT}	Maximum possible count(1)				65 536	T_{MASTER}

1. Not tested in production

11.3.8 SPI serial peripheral interface

Unless otherwise specified, the parameters given in *Table 32* are derived from tests performed under ambient temperature, f_{MASTER} frequency and V_{DD} supply voltage conditions. $t_{MASTER} = 1/f_{MASTER}$.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 32. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	0	8	MHz
		Slave mode	0	8	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		25	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4*T_{MASTER}$		
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	70		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{MASTER} = 16 MHz, f_{SCK}= 8 MHz	110	140	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5		
		Slave mode	2		
$t_{h(MI)}$ (1) $t_{h(SI)}$ (1)	Data input hold time	Master mode, f_{MASTER} = 16 MHz, f_{SCK} = 8 MHz	7		
		Slave mode, f_{MASTER} = 16 MHz, f_{SCK} = 8 MHz	3		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{MASTER} = 16 MHz, f_{SCK} = 8 MHz		400	
		Slave mode		$4*t_{MASTER}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	25		
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge), f_{MASTER} = 16 MHz, f_{SCK} = 8 MHz		100	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge), f_{MASTER} = 16 MHz, f_{SCK} = 8 MHz		3	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	100		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	6		

1. Values based on design simulation and/or characterization results, and not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 36. SPI timing diagram where slave mode and CPHA = 0

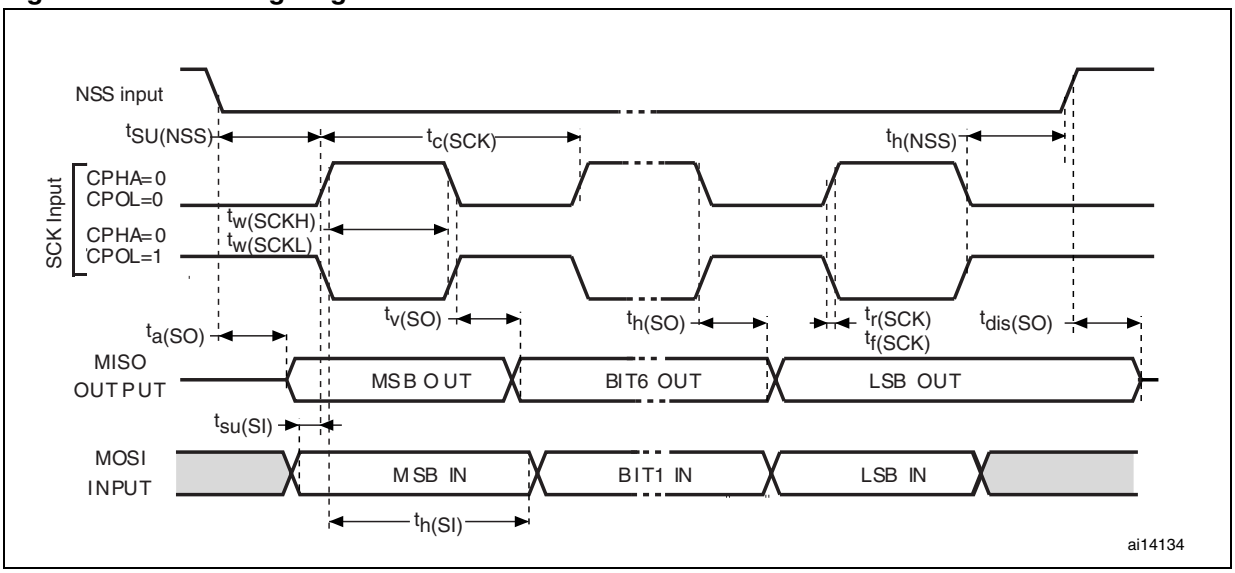
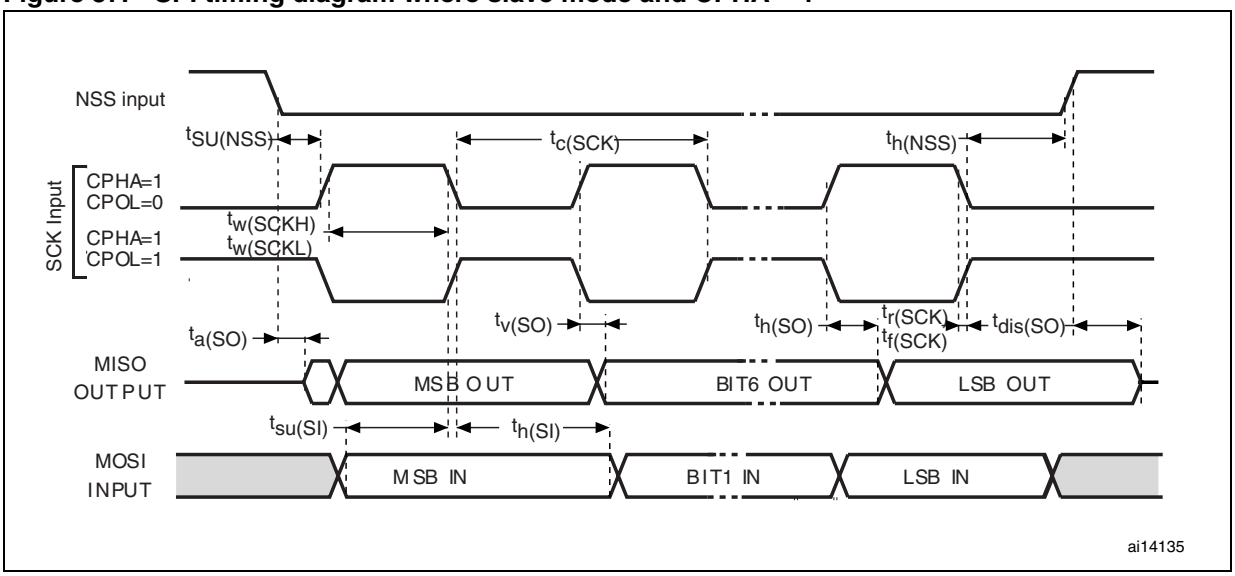
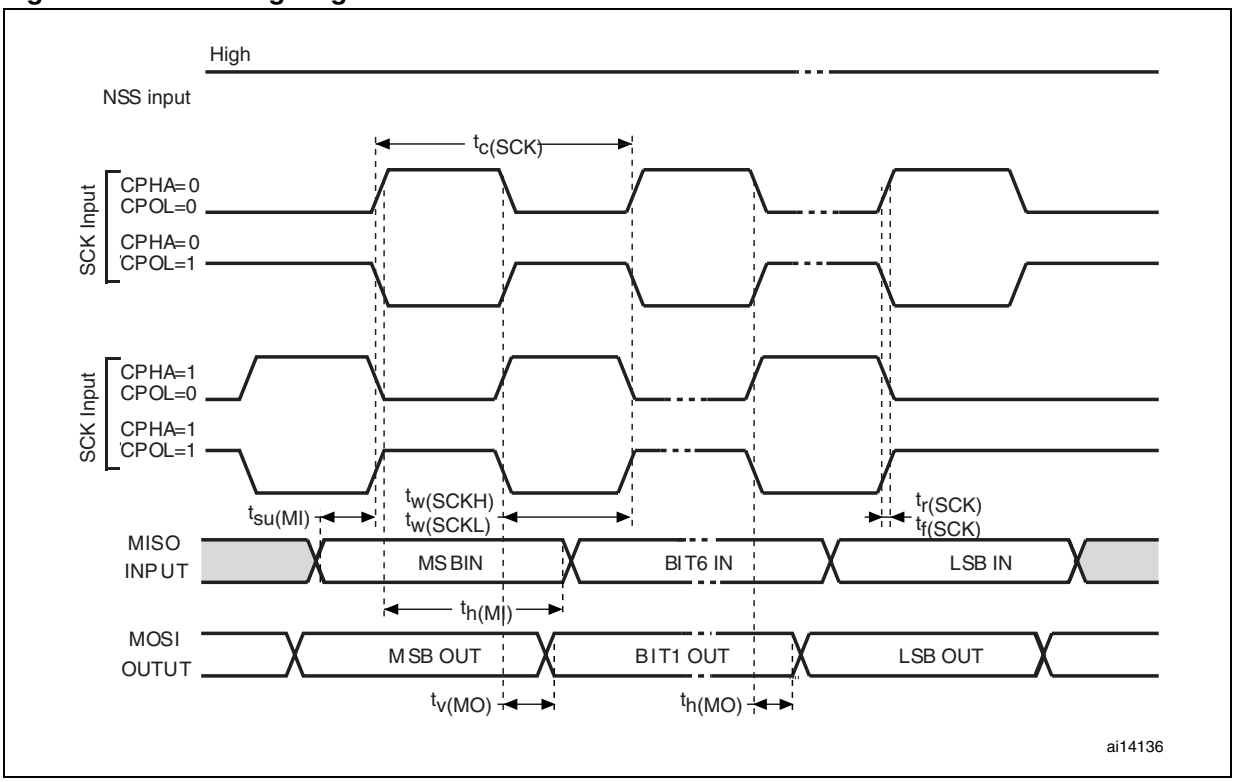


Figure 37. SPI timing diagram where slave mode and CPHA = 1(1)



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 38. SPI timing diagram - master mode(1)



1. Measurement points are at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

11.3.9 I²C interface characteristics

Table 33. I²C characteristics

Symbol	Parameter	Standard mode I²C		Fast mode I²C(1)		Unit
		Min(2)	Max(2)	Min(2)	Max(2)	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0(3)		0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time (V_{DD} 3 ... 5.5 V)		1000		300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time (V_{DD} 3 ... 5.5 V)		300		300	
$t_{h(STA)}$	START condition hold time	4.0		0.6		µs
$t_{su(STA)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(STO)}$	STOP condition setup time	4.0		0.6		µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7		1.3		µs
C_b	Capacitive load for each bus line		400		400	pF

1. f_{MASTER}, must be at least 8 MHz to achieve max fast I²C speed (400 kHz)
2. Data based on standard I²C protocol requirement, not tested in production
3. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL

11.3.10 10-bit ADC characteristics

Subject to general operating conditions for V_{DDA}, f_{MASTER}, and T_A unless otherwise specified.

Table 34. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC clock frequency			2		MHz
V_{DDA}	Analog supply		3		5.5	V
V_{REF+}	Positive reference voltage		2.75		V_{DDA}	V
V_{REF-}	Negative reference voltage		V_{SSA}		0.5	V
V_{AIN}	Conversion voltage range(1)		V_{SSA}		V_{DDA}	V
		Devices with external V_{REF+}/ V_{REF-} pins	V_{REF-}		V_{REF+}	V
C_{ADC}	Internal sample and hold capacitor			3		pF
t_S(1)	Sampling time (3 x 1/f_{ADC})	f_{ADC} = 2 MHz		1.5		µs
t_{STAB}	Wake-up time from standby			7		µs
t_{CONV}	Total conversion time including sampling time (14 x 1/f_{ADC})	f_{ADC} = 2 MHz		7		µs

1. During the sample time the input capacitance C_{AIN} (3 pF max) can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

Table 35. ADC accuracy with R_{AIN} < 10 kΩ R_{AIN}, V_{DDA} = 3.3 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\lvert E_T \rvert$	Total unadjusted error(1)	f_{ADC} = 2 MHz	1.5	TBD(1)	LSB
$\lvert E_O \rvert$	Offset error(1)		1.1	TBD(1)	
$\lvert E_G \rvert$	Gain error(1)		-0.2/0.6	TBD(1)	
$\lvert E_D \rvert$	Differential linearity error(1)		0.9	TBD(1)	
$\lvert E_L \rvert$	Integral linearity error(1)		1	TBD(1)	

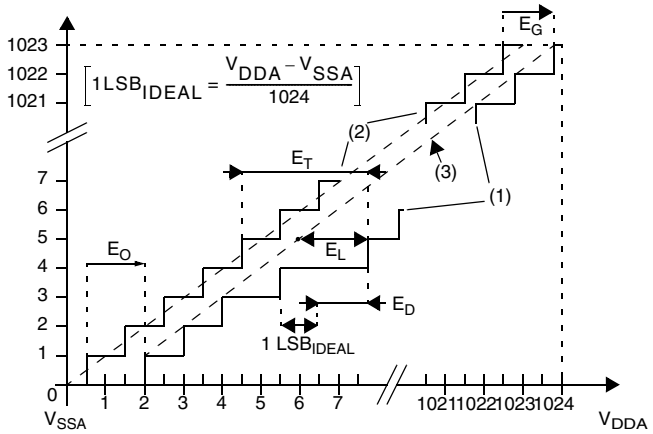
1. TBD = To be determined

Table 36. ADC accuracy with R_{AIN} < 10 kΩ , V_{DDA} = 5 V

Symbol	Parameter	Conditions	Typ	Max	Unit
$\lvert E_T \rvert$	Total unadjusted error(1)	f_{ADC} = 2 MHz	1.4	3	LSB
$\lvert E_O \rvert$	Offset error(1)		0.8	2	
$\lvert E_G \rvert$	Gain error(1)		0.1	1	
$\lvert E_D \rvert$	Differential linearity error(1)		0.9	2	
$\lvert E_L \rvert$	Integral linearity error(1)		0.7	2	

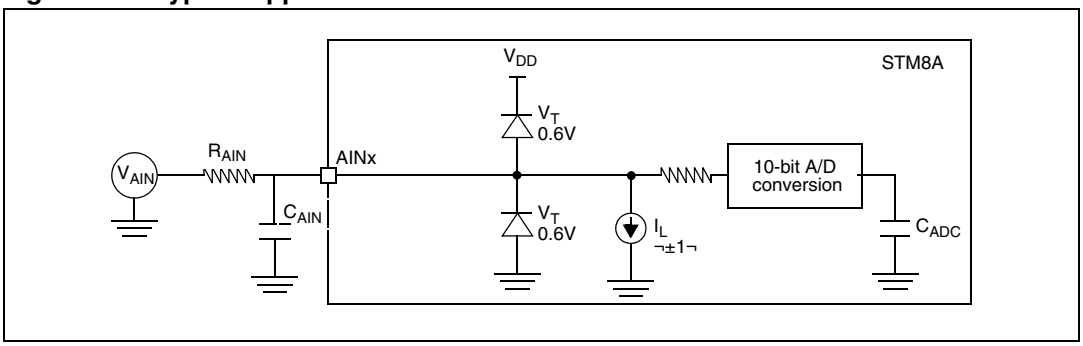
1. ADC accuracy vs. injection current: Any positive or negative injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 11.3.5* does not affect the ADC accuracy.

Figure 39. ADC accuracy characteristics



1. Example of an actual transfer curve
2. The ideal transfer curve
3. End point correlation line
   E_T = Total unadjusted error: Maximum deviation between the actual and the ideal transfer curves.
   E_O = Offset error: Deviation between the first actual transition and the first ideal one.
   E_G = Gain error: Deviation between the last ideal transition and the last actual one.
   E_D = Differential linearity error: Maximum deviation between actual steps and the ideal one.
   E_L = Integral linearity error: Maximum deviation between any actual transition and the end point correlation line.

Figure 40. Typical application with ADC



11.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

Functional EMS (electromagnetic susceptibility)

While executing a simple application (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 1000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 1000-4-4 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be recovered by applying a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Table 37. EMS data

Symbol	Parameter	Conditions	Level/class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD}= 3.3 V, T_A= 25 °C, f_{MASTER} = 16 MHz (HSI clock), Conforms to IEC 1000-4-4	4A

Electromagnetic interference (EMI)

Emission tests conform to the SAE J 1752/3 standard for test software, board layout and pin loading.

Table 38. EMI data

Symbol	Parameter	Conditions					Unit
		General conditions	Monitored frequency band	Max f_{CPU}(1)			
				8 MHz	16 MHz	24 MHz	
S_{EMI}	Peak level	V_{DD} = 5 V, T_A = 25 °C, LQFP80 package conforming to SAE J 1752/3	0.1 MHz to 30 MHz	15	17	22	dBµV
			30 MHz to 130 MHz	18	22	16	
			130 MHz to 1 GHz	-1	3	5	
	SAE EMI level			2	2.5	2.5	-

1. Data based on characterization results, not tested in production.

Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

Electrostatic discharge (ESD)

Electrostatic discharges (3 positive then 3 negative pulses separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). This test conforms to the JESD22-A114A/A115A standard. For more details, refer to the application note AN1181.

Table 39. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model)	T_A = 25°C, conforming to JESD22-A114	3A	4000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge device model)	T_A= 25°C, conforming to JESD22-C101	3	500	
$V_{ESD(MM)}$	Electrostatic discharge voltage (Machine model)	T_A= 25°C, conforming to JESD22-A115	B	200	

1. Data based on characterization results, not tested in production

Static latch-up

Two complementary static tests are required on 10 parts to assess the latch-up performance.

- A supply overvoltage (applied to each power supply pin) and
- A current injection (applied to each input, output and configurable I/O pin) are performed on each sample.

This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

Table 40. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A = 25 °C	A
		T_A = 85 °C	A
		T_A = 125 °C	A
		T_A = 145 °C	A

1. Class description: A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications, that means when a device belongs to class A it exceeds the JEDEC standard. B class strictly covers all the JEDEC criteria (international standard).

11.4 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in *Table 16: General operating conditions on page 51*.

The maximum chip-junction temperature, T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- T_{Amax} is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance in ° C/W
- P_{Dmax} is the sum of P_{INTmax} and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- P_{INTmax} is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 41. Thermal characteristics(1)

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm	57	°C/W
Θ_{JA}	Thermal resistance junction-ambient LQFP 32 - 7 x 7 mm	59	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

11.4.1 Reference document

JESD51-2 integrated circuits thermal test method environment conditions - natural convection (still air). Available from www.jedec.org.

11.4.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the order code (see *Figure 43: STM8A order codes on page 86*).

The following example shows how to calculate the temperature range needed for a given application.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax}= 82 °C (measured according to JESD51-2), I_{DDmax} = 8 mA, V_{DD} = 5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

$$P_{INTmax} = 8 \text{ mA} \times 5 \text{ V} = 400 \text{ mW}$$

$$P_{IOmax} = 20 \times 8 \text{ mA} \times 0.4 \text{ V} = 64 \text{ mW}$$

This gives: P_{INTmax} = 400 mW and P_{IOmax} 64 mW:

$$P_{Dmax} = 400 \text{ mW} + 64 \text{ mW}$$

Thus: P_{Dmax} = 464 mW

Using the values obtained in *Table 41: Thermal characteristics on page 81* T_{Jmax} is calculated as follows:

– For LQFP64 46°C/W

$$T_{Jmax} = 82° \text{ C} + (46° \text{ C/W} \times 464 \text{ mW}) = 82°\text{C} + 21°\text{C} = 103° \text{ C}$$

This is within the range of the suffix B version parts ($-40 < T_J < 105°$ C).

Parts must be ordered at least with the temperature range suffix B.

12 Package characteristics

To meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at *www.st.com*.

12.1 Package mechanical data

Figure 41. 48-pin low profile quad flat package (7 x 7)

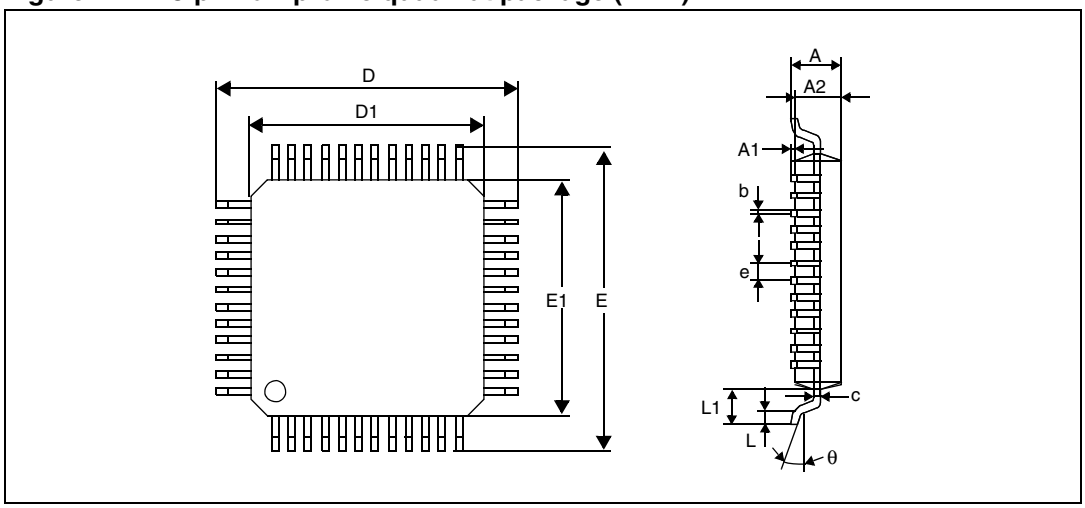


Table 42. 48-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

Figure 42. 32-pin low profile quad flat package (7 x 7)

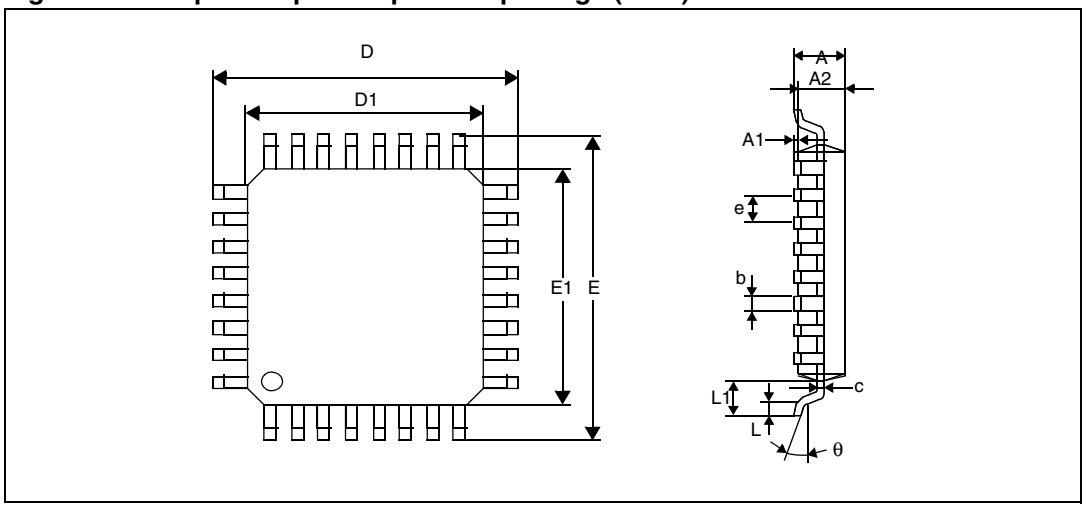


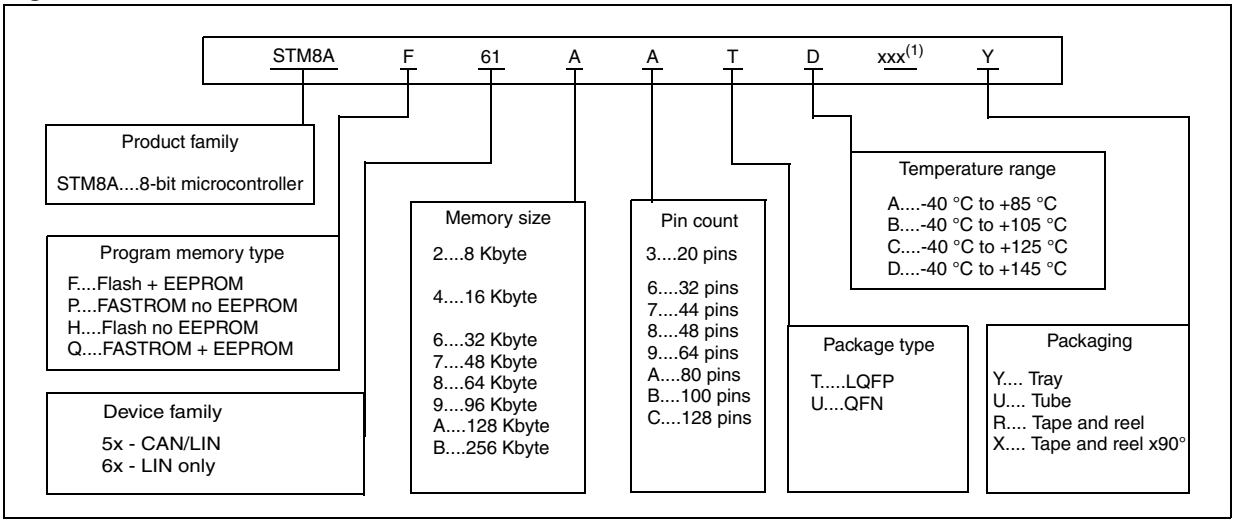
Table 43. 32-pin low profile quad flat package mechanical data

Dim.	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.30	0.37	0.45	0.0118	0.0146	0.0177
c	0.09		0.20	0.0035		0.0079
D		9.00			0.3543	
D1		7.00			0.2756	
E		9.00			0.3543	
E1		7.00			0.2756	
e		0.80			0.0315	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	

1. Values in inches are converted from mm and rounded to 4 decimal digits

13 Ordering information

Figure 43. STM8A order codes



1. Customer specific FASTROM code

14 STM8 development tools

Development tools for the STM8A microcontrollers include the

- STice emulation system offering tracing and code profiling
- STVD high-level language debugger including assembler and visual development environment - seamless integration of third party C compilers
- STVP Flash programming software

In addition, the STM8A comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

14.1 Emulation and in-circuit debugging tools

The STM8 tool line includes the STice emulation system offering a complete range of emulation and in-circuit debugging features on a platform that is designed for versatility and cost-effectiveness. In addition, STM8A application development is supported by a low-cost in-circuit debugger/programmer.

The STice is the fourth generation of full-featured emulators from STMicroelectronics. It offers new advanced debugging capabilities including tracing, profiling and code coverage analysis to help detect execution bottlenecks and dead code.

In addition, STice offers in-circuit debugging and programming of STM8A microcontrollers via the STM8 single wire interface module (SWIM), which allows non-intrusive debugging of an application while it runs on the target microcontroller.

For improved cost effectiveness, STice is based on a modular design that allows you to order exactly what you need to meet your development requirements and to adapt your emulation system to support existing and future ST microcontrollers.

STice key features

- Program and data trace recording up to 128 K records
- Advanced breakpoints with up to 4 levels of conditions
- Data breakpoints
- Real-time read/write of all device ressources during emulation
- Occurrence and time profiling and code coverage analysis (new features)
- In-circuit debugging/programming via SWIM protocol
- 8-bit probe analyzer
- 1 input and 2 output triggers
- USB 2.0 high speed interface to host PC
- Power supply follower managing application voltages between 1.62 to 5.5 V
- Modularity that allows you to specify the components you need to meet your development requirements and adapt to future requirements
- Supported by free software tools that include integrated development environment (IDE), programming software interface and assembler for STM8

14.2 Software tools

STM8 development tools are supported by a complete, free software package from STMicroelectronics that includes ST visual develop (STVD) IDE and the ST visual programmer (STVP) software interface. STVD provides seamless integration of the Cosmic C compiler for STM8, which is available in a free version that outputs up to 16 Kbytes of code.

14.2.1 STM8 toolset

STM8 toolset with STVD integrated development environment and STVP programming software is available for free download at www.st.com/mcu. This package includes:

ST visual develop – Full-featured integrated development environment from STMicroelectronics, featuring

- Seamless integration of C and ASM toolsets
- Full-featured debugger
- Project management
- Syntax highlighting editor
- Integrated programming interface
- Support of advanced emulation features for STice such as code profiling and coverage

ST visual programmer (STVP) – Easy-to-use, unlimited graphical interface allowing read, write and verify of your STM8A microcontroller's Flash memory. STVP also offers project mode for saving programming configurations and automating programming sequences.

14.2.2 C and assembly toolchains

Control of C and assembly toolchains is seamlessly integrated into the STVD integrated development environment, making it possible to configure and control the building of your application directly from an easy-to-use graphical interface.

Available toolchains include:

- **C compiler for STM8** – Available in a free version that outputs up to 16 Kbytes of code. For more information, see www.cosmic-software.com, www.raisonance.com
- **STM8 assembler linker** – Free assembly toolchain included in the STM8 toolset, which allows you to assemble and link your application source code.

14.3 Programming tools

During the development cycle, STice provides in-circuit programming of the STM8A Flash microcontroller on your application board via the SWIM protocol. Additional tools are to include a low-cost in-circuit programmer as well as ST socket boards, which provide dedicated programming platforms with sockets for programming your STM8A.

For production environments, programmers will include a complete range of gang and automated programming solutions from third-party tool developers already supplying programmers for the STM8 family.

15 Revision history

Table 44. Document revision history

Date	Revision	Changes
22-Aug-2008	Rev 1	Initial release

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