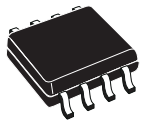
STS7PF30L

P-CHANNEL 30V - 0.16Ω - 7A - SO-8
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS7PF30L	30V	<0.021Ω	7A

- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

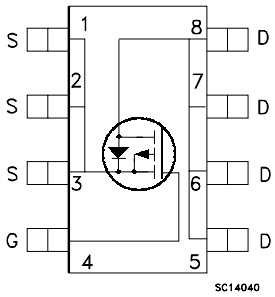


SO-8

Description

This Power MOSFET is the latest development of STMicroelectronics' unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing densisty for low on-resistance, rugged avalanche characteristics and less critical alignment steps, therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT.
- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT

Order Codes

Sales Type	Marking	Package	Packaging
STS7PF30L	S7PF30L	SO-8	TAPE & REEL

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20kΩ)	30	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	7	A
I_D	Drain Current (continuous) at T_C = 100°C	4.4	A
I_{DM} *Note* 1	Drain Current (pulsed)	28	A
P_{TOT}	Total Dissipation at T_C = 25°C	2.5	W

Table 2. Thermal data

Rthj-amb *Note* 2	Thermal Resistance Junction-ambient	50	°C/W
T_j T_{stg}	Operating Junction Temperature Storage Temperature Range	150 -55 to 150	°C °C

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS}= 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0) V_{DS} = Max Rating, V_{DS} = Max Rating, T_c=125°C				1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{DS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250µA	1	1.6	2.5	V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10 V, I_D= 3.5A V_{GS}= 4.5 V, I_D = 3.5A	0.011 0.016	0.016 0.022	0.021 0.028	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} *Note* 3	Forward Transconductance	V_{DS} = 20V, I_D= 3.5A		16		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} =0		2600 523 174		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 15V, I_D= 7A, V_{GS}= 4.5V		28 8.75 12.35	7	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 15V, I_D = 3.5A R_G= 4.7Ω, V_{GS}= 4.5V, (see Figure 13)		68 54		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 15V, I_D = 3.5A R_G= 4.7Ω, V_{GS}= 4.5V, (see Figure 13)		65 23		ns ns

Table 6. Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} *Note* 1	Source-Drain Current Source-Drain Current (pulsed)				7 28	A A
V_{SD}	Forward On Voltage	I_{SD} = 7A, V_{GS} = 0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 7A, di/dt = 100A/µs V_{DD} = 15V, T_j = 150°C (see Figure 15)		40 46 2.3		ns nC A

(1) Pulse with limited by safe operating area

(2) When mounted on 1inch² FR-4 board (t ≤ 10µs)

(3) Pulsed: pulse duration = 300µs, duty cycle 1.5%

Note: For the P-CHANNEL MOSFET the polarity of voltages and current have to be reversed

2.1 Electrical characteristics (curves)

Figure 1. Safe Operating Area

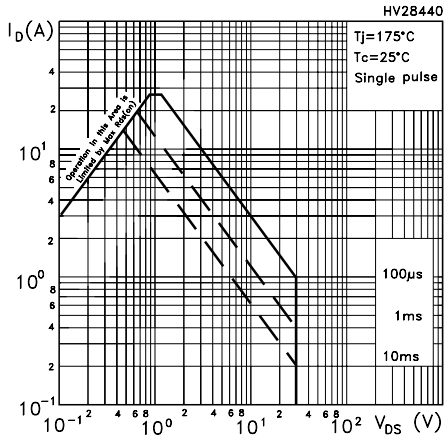


Figure 2. Thermal Impedance

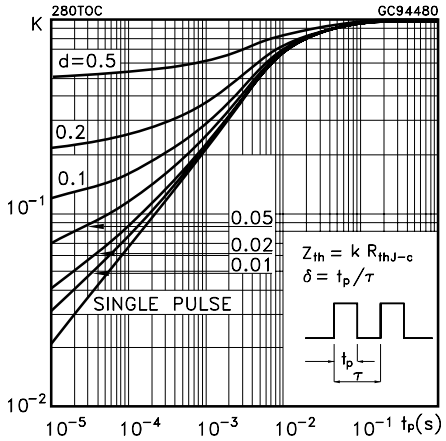


Figure 3. Output Characteristics

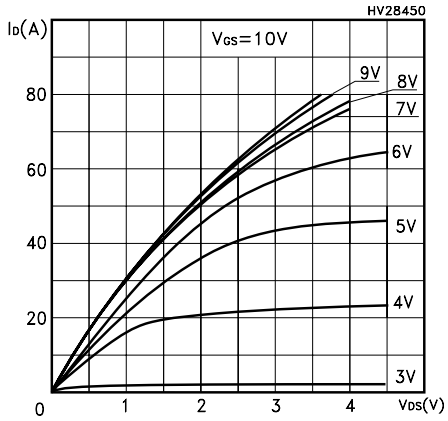


Figure 4. Transfer Characteristics

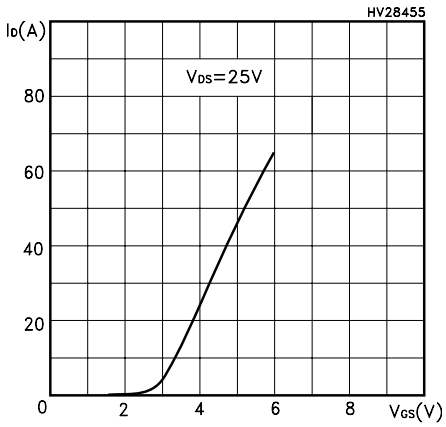


Figure 5. Transconductance

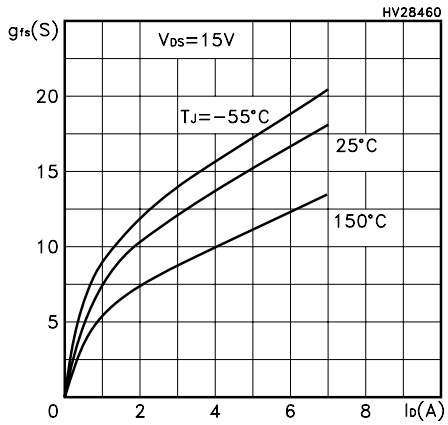


Figure 6. Static Drain-Source on Resistance

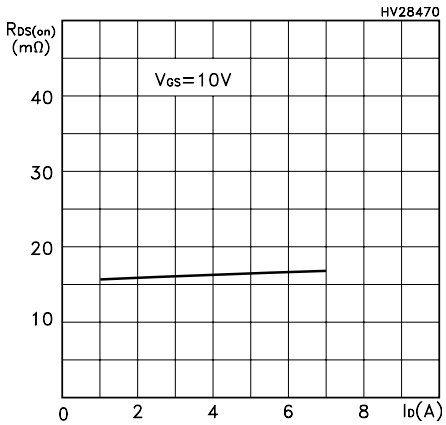


Figure 7. Gate Charge vs Gate-Source Voltage

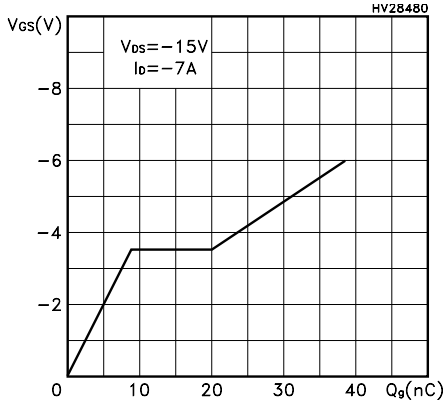


Figure 8. Capacitance Variations

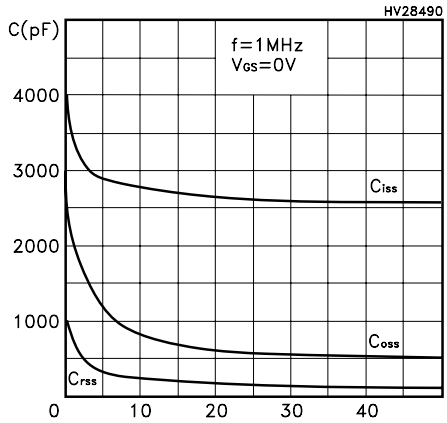


Figure 9. Normalized Gate Threshold Voltage vs Temperature

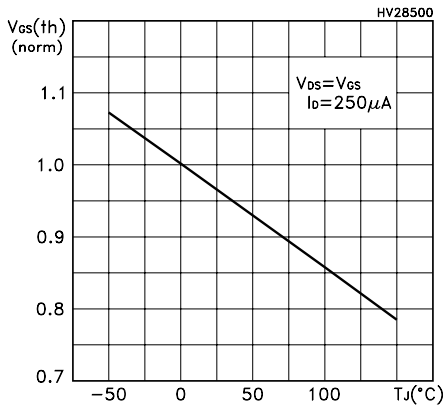


Figure 10. Normalized on Resistance vs Temperature

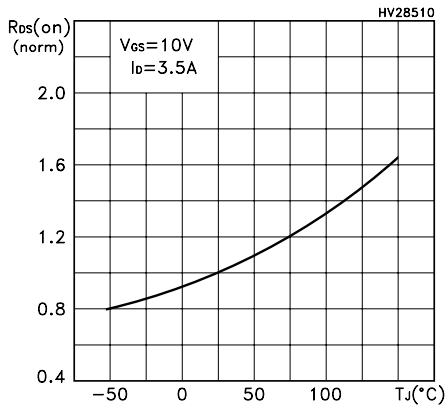


Figure 11. Source-Drain Diode Forward Characteristics

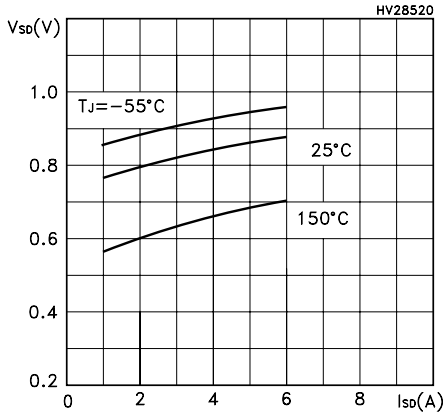
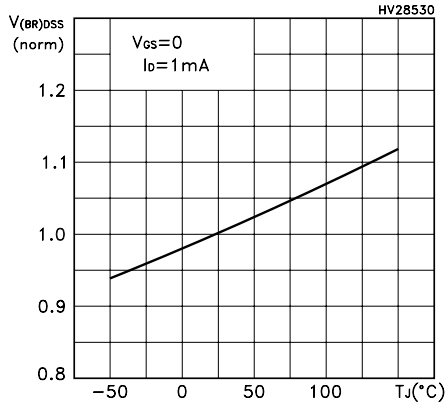


Figure 12. Normalized Breakdown Voltage vs Temperature



3 Test Circuits

Figure 13. Switching Times Test Circuit For Resistive Load

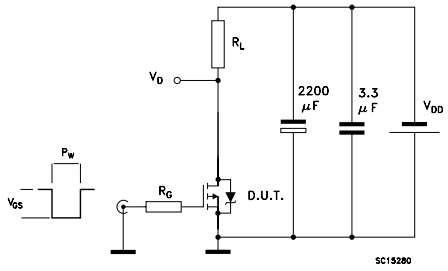


Figure 14. Gate Charge Test Circuit

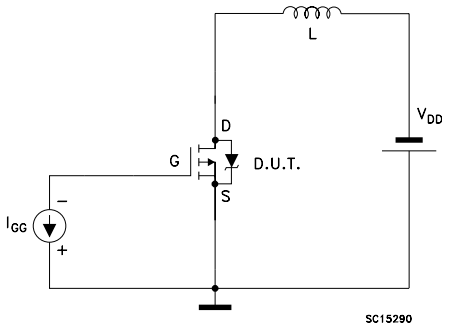
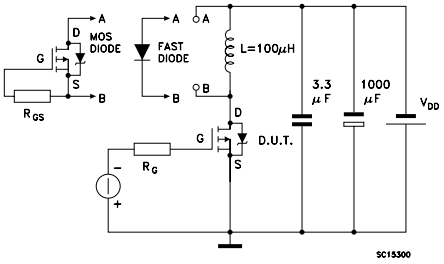


Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times

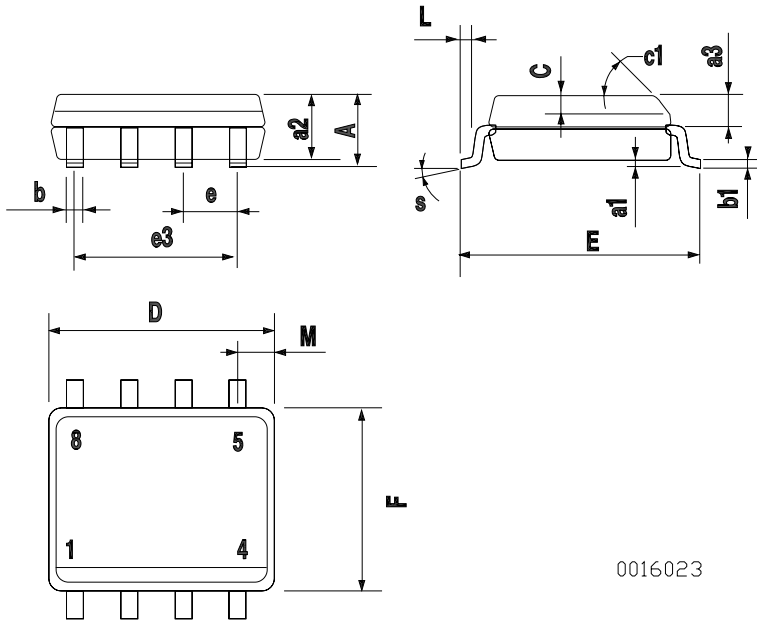


4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision History

Date	Revision	Changes
13-Dec-2003	1	First Issue
25-Jun-2004	2	Preliminary Data
18-Jan-2005	3	Modified value on table 5
29-Sep-2005	4	Complete version
09-Nov-2005	5	New template