



# STD10NM60ND, STF10NM60ND STP10NM60ND

N-channel 600 V, 0.57  $\Omega$ , 8 A, DPAK, TO-220FP, TO-220  
FDmesh™ II Power MOSFET (with fast diode)

## Features

Order codes	V <sub>DSS</sub> @T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD10NM60ND	650 V	< 0.6 $\Omega$	8 A	70 W
STF10NM60ND				25 W
STP10NM60ND				70 W

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt avalanche capabilities

## Applications

- Switching applications

## Description

This FDmesh™ II Power MOSFET with intrinsic fast-recovery body diode is produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, this revolutionary device features extremely low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

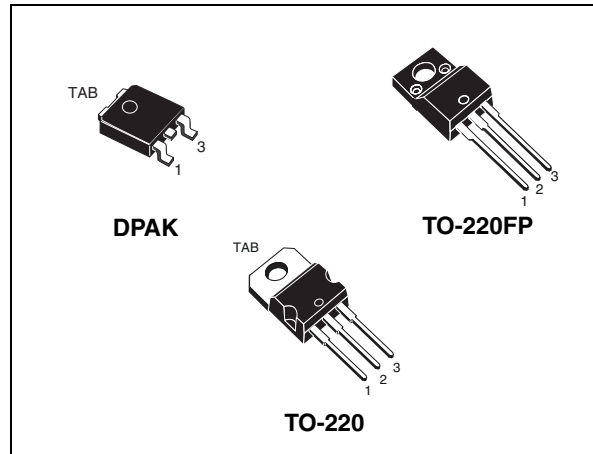


Figure 1. Internal schematic diagram

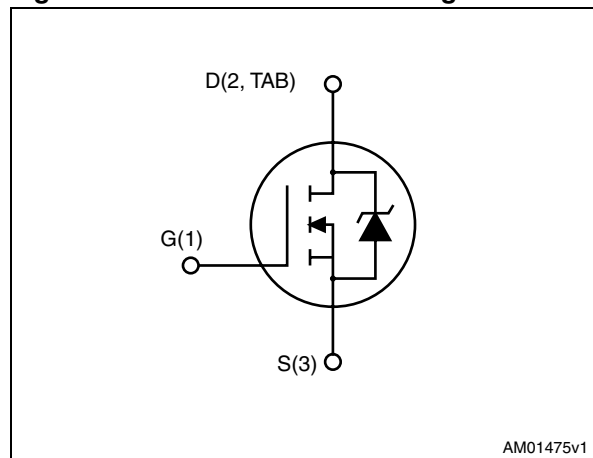


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD10NM60ND	10NM60ND	DPAK	Tape and reel
STF10NM60ND		TO-220FP	Tube
STP10NM60ND		TO-220	

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
$V_{DS}$	Drain-source voltage	600			V
$V_{GS}$	Gate- source voltage	± 25			V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	8	8 <sup>(1)</sup>	8	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	5	5 <sup>(1)</sup>	5	A
$I_{DM}^{(2)}$	Drain current (pulsed)	32	32 <sup>(1)</sup>	32	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	70	25	70	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	40			V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25\text{ °C}$ )		2500		V
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150			°C

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	TO-220	
$R_{thj-case}$	Thermal resistance junction-case max	1.79	5	1.79	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.50	62.50		°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50			°C/W
$T_J$	Maximum lead temperature for soldering purpose		300		°C/W

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J\text{ Max}$ )	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25\text{ °C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	130	mJ

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage (V <sub>GS</sub> = 0)	I <sub>D</sub> = 1 mA	600			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 600 V V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C			1 100	μA μA
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 25 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4 A		0.57	0.6	Ω

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0	-	577	-	pF
C <sub>oss</sub>	Output capacitance			32.4		pF
C <sub>rss</sub>	Reverse transfer capacitance			1.76		pF
C <sub>oss eq</sub> <sup>(1)</sup>	Equivalent capacitance time related	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0	-	138	-	pF
R <sub>g</sub>	Gate input resistance	f = 1 MHz open drain	-	6	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 8 A,	-	20	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10 V		4.3		nC
Q <sub>gd</sub>	Gate-drain charge	(see Figure 19)		11.6		nC

1. C<sub>oss eq</sub> time related is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 4 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see Figure 18)	-	9.2	-	ns
t <sub>r</sub>	Rise time			10		ns
t <sub>d(off)</sub>	Turn-off-delay time			32		ns
t <sub>f</sub>	Fall time			9.8		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	118		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	680		nC
$I_{RRM}$	Reverse recovery current	(see Figure 20)	-	11		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	150		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$	-	918		nC
$I_{RRM}$	Reverse recovery current	(see Figure 20)	-	12		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for DPAK

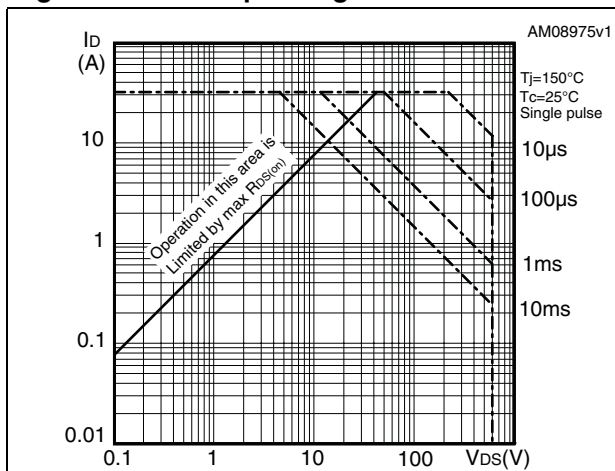


Figure 3. Thermal impedance for DPAK

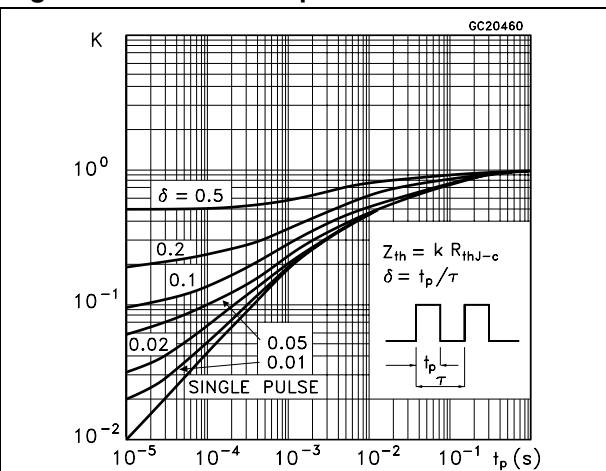


Figure 4. Safe operating area for TO-220FP

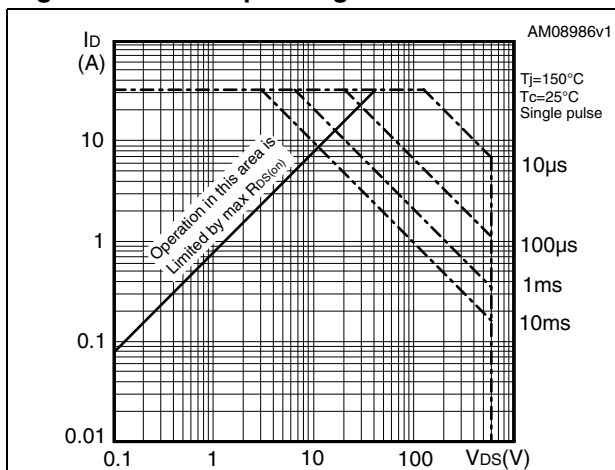


Figure 5. Thermal impedance for TO-220FP

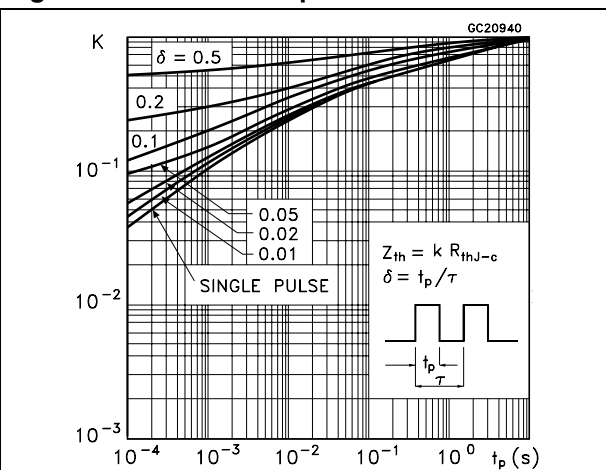


Figure 6. Safe operating area for TO-220

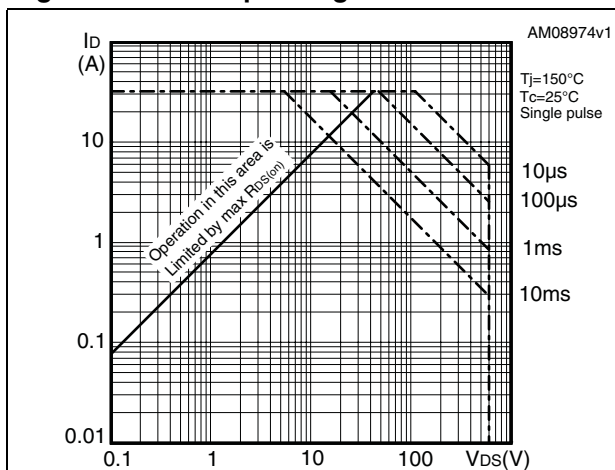


Figure 7. Thermal impedance for TO-220

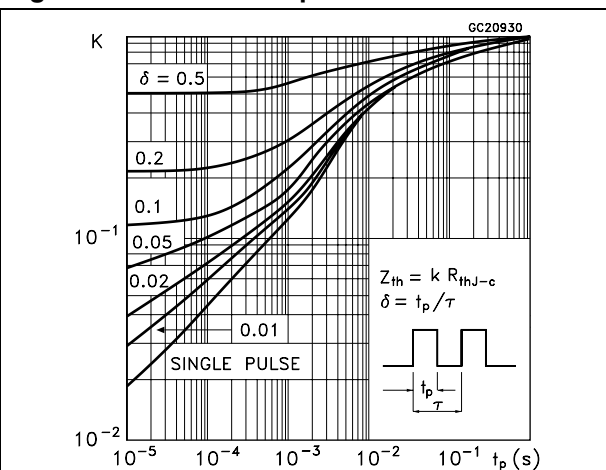


Figure 8. Output characteristics

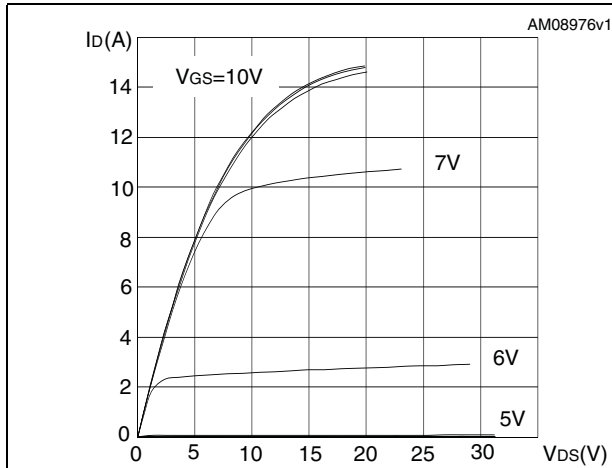


Figure 9. Transfer characteristics

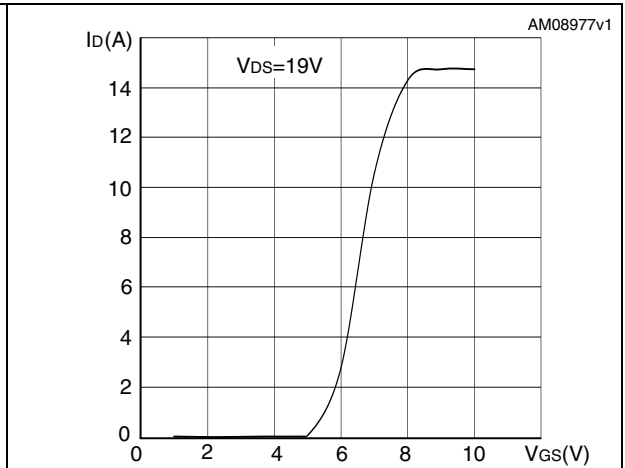


Figure 10. Gate charge vs gate-source voltage Figure 11. Static drain-source on resistance

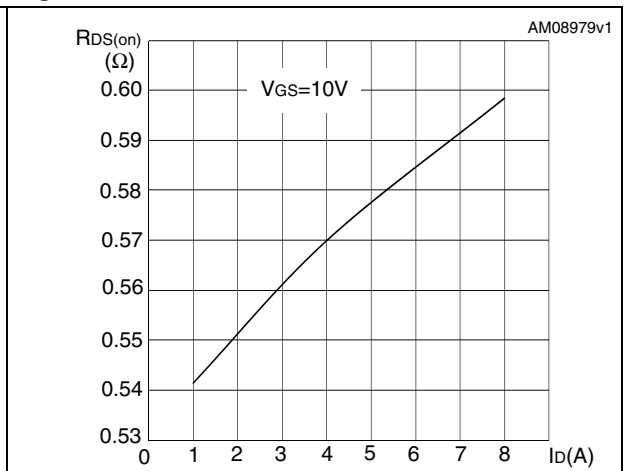
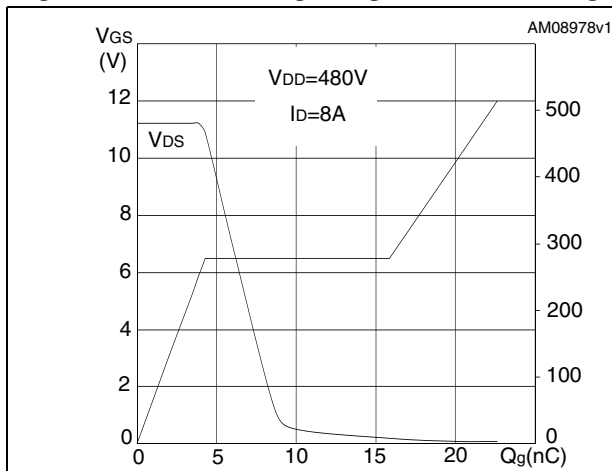


Figure 12. Capacitance variations

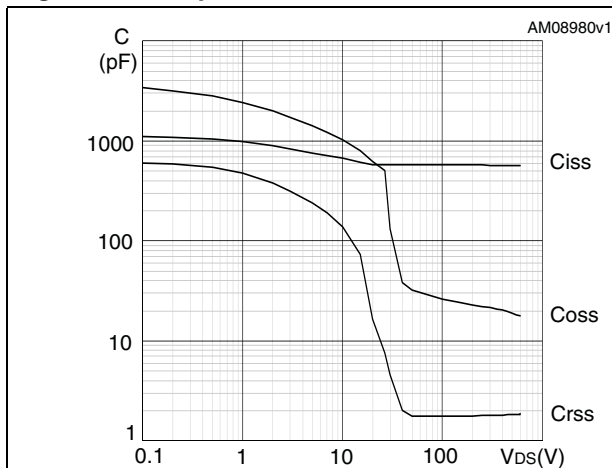


Figure 13. Output capacitance stored energy

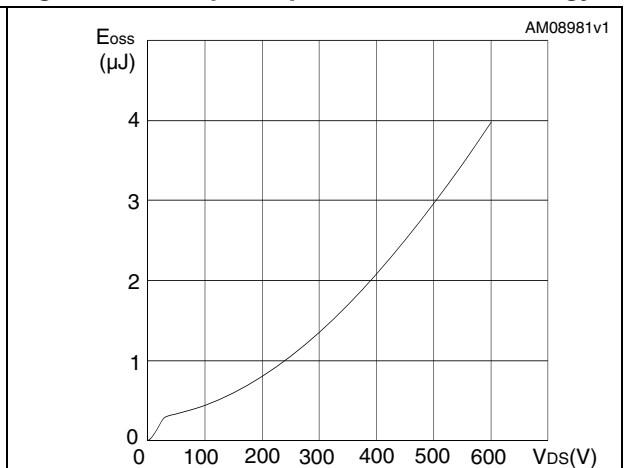


Figure 14. Normalized gate threshold voltage vs temperature

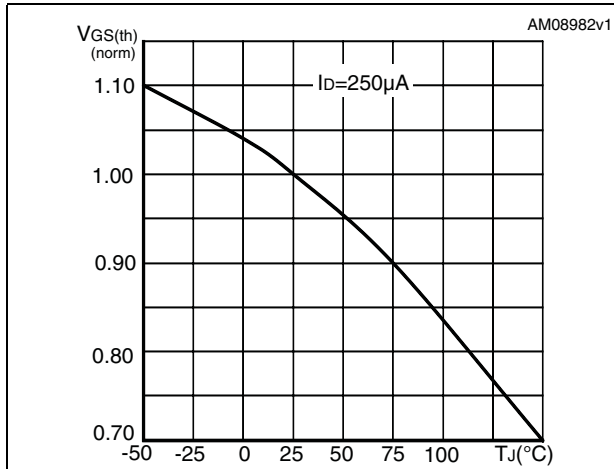


Figure 15. Normalized on resistance vs temperature

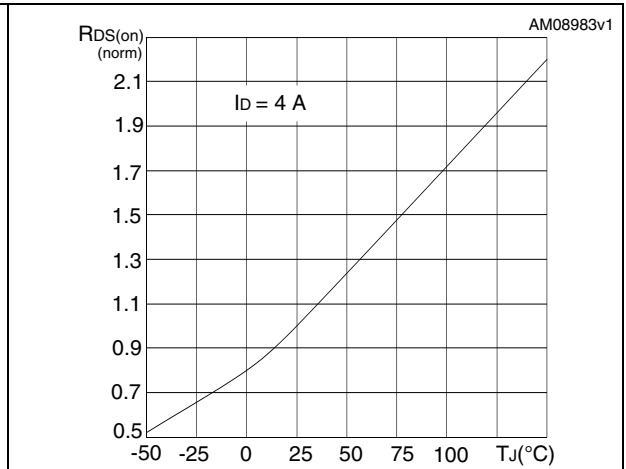


Figure 16. Source-drain diode forward characteristics

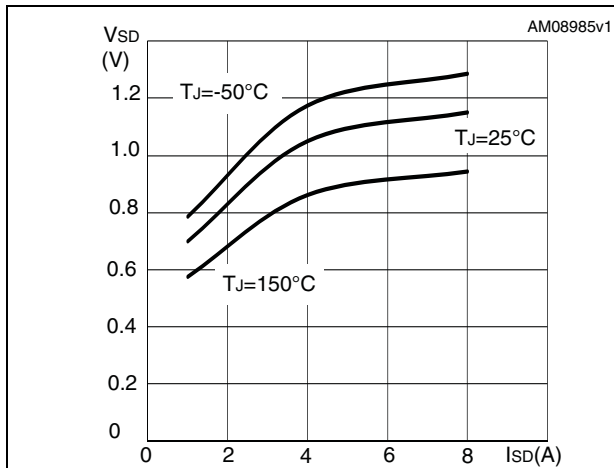
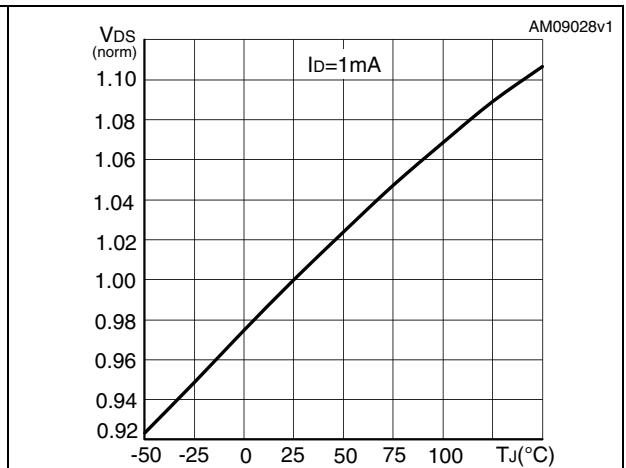


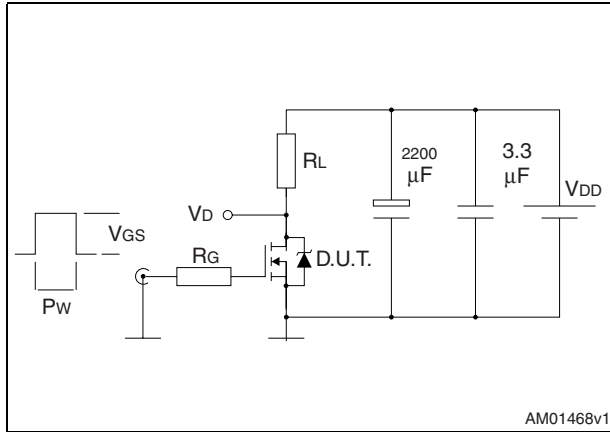
Figure 17. Normalized  $V_{DS}$  vs temperature



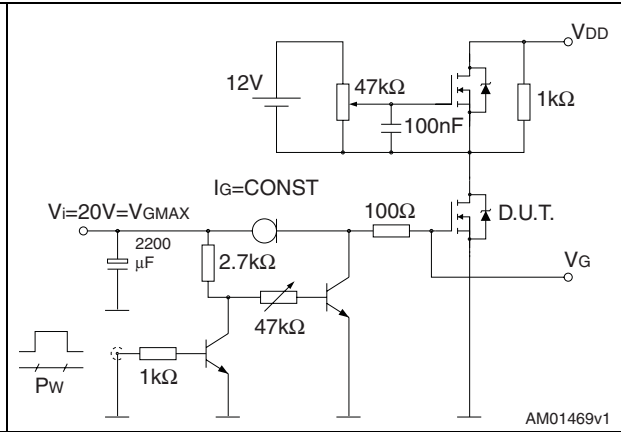


### 3 Test circuits

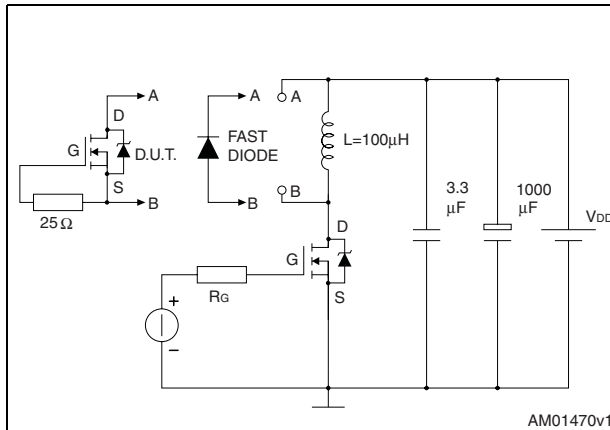
**Figure 18. Switching times test circuit for resistive load**



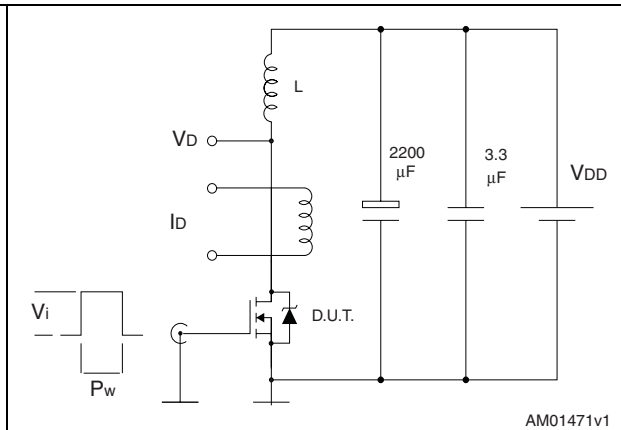
**Figure 19. Gate charge test circuit**



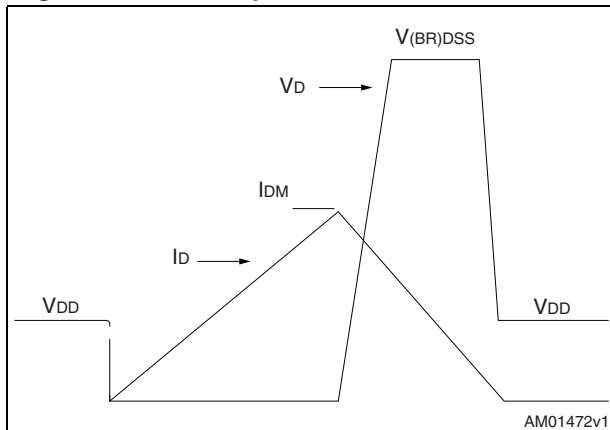
**Figure 20. Test circuit for inductive load switching and diode recovery times**



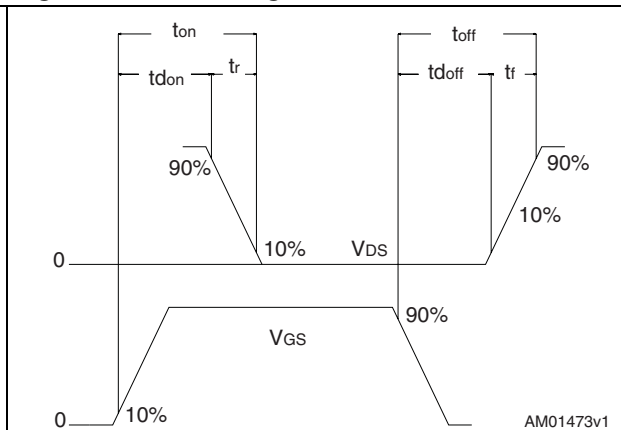
**Figure 21. Unclamped inductive load test circuit**



**Figure 22. Unclamped inductive waveform**



**Figure 23. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 24. DPAK (TO-252) drawing

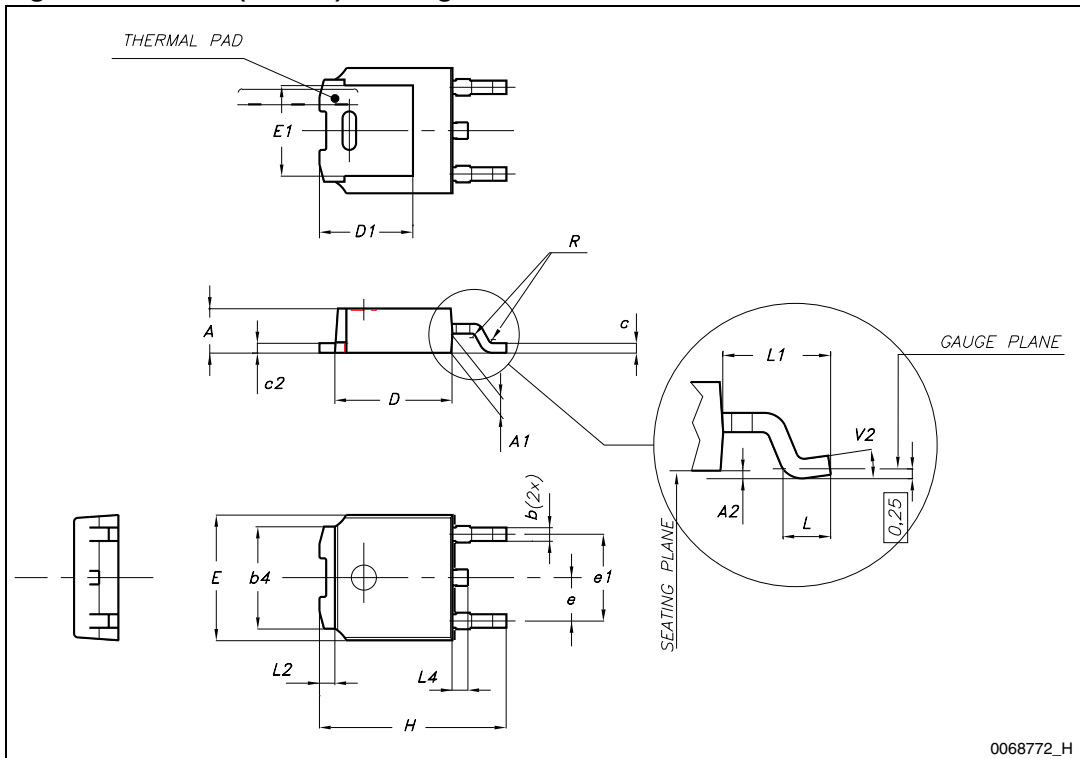
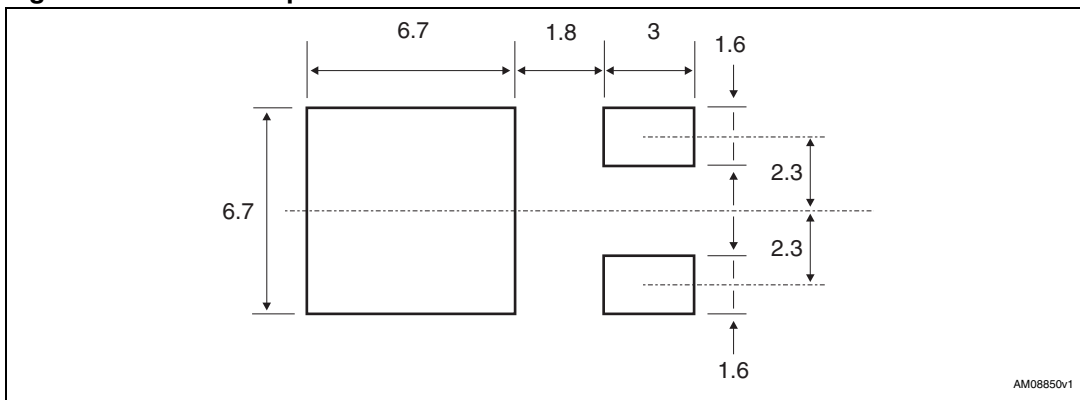


Figure 25. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 26. TO-220FP drawing

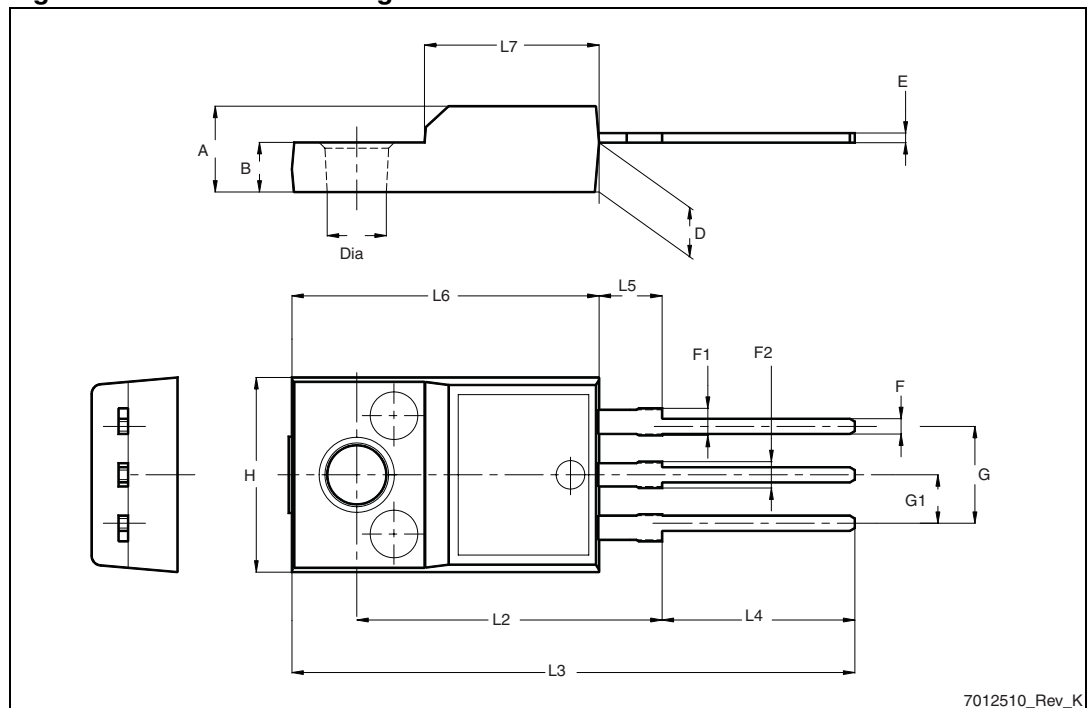
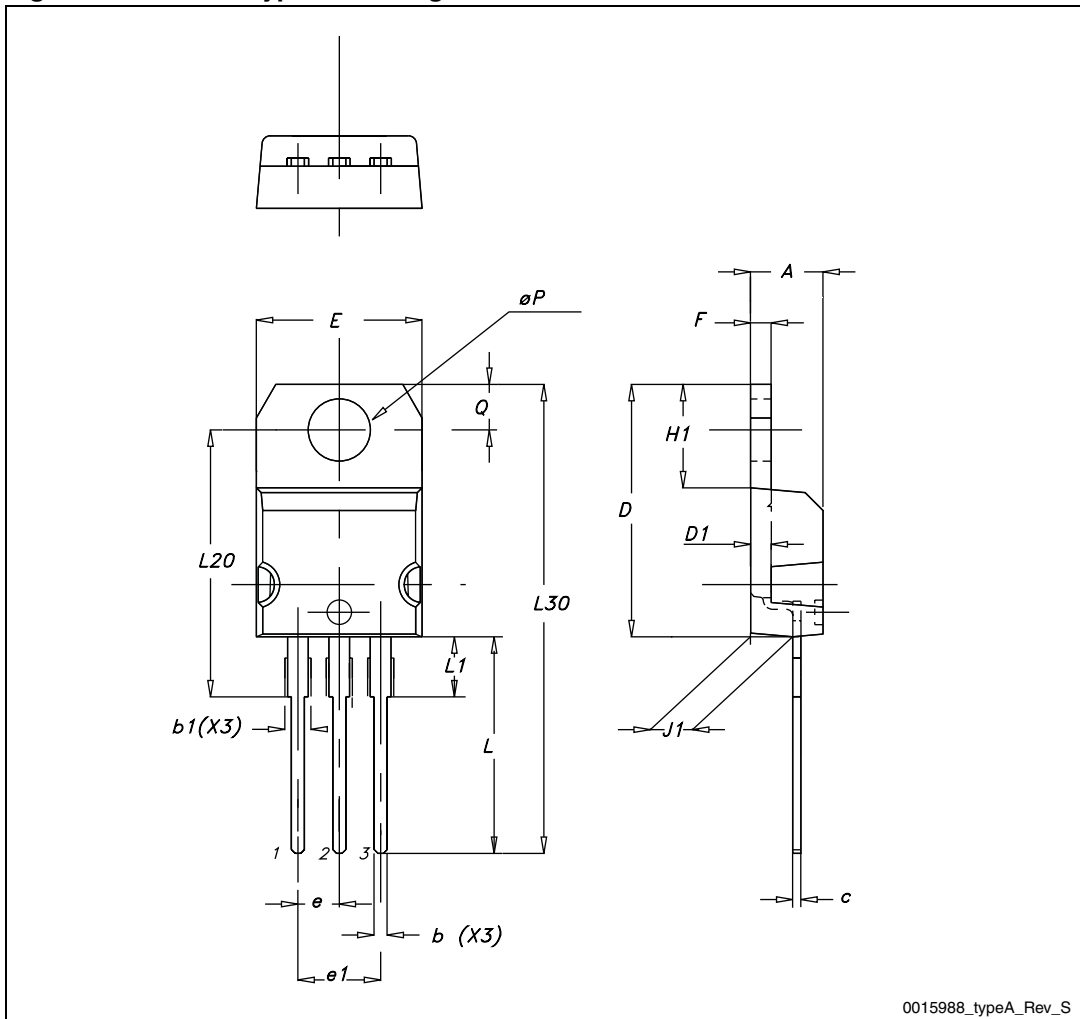


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 27. TO-220 type A drawing



## 5 Packaging mechanical data

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			



Figure 28. Tape for DPAK (TO-252)

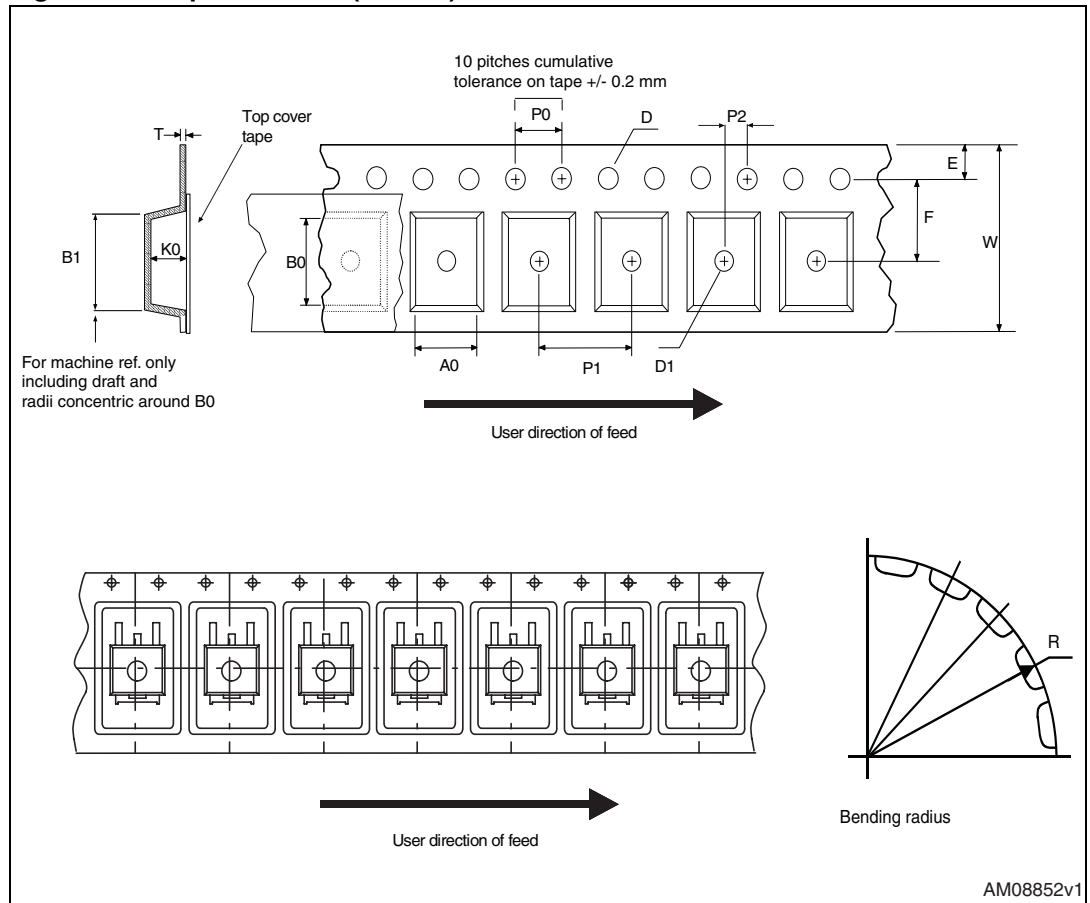
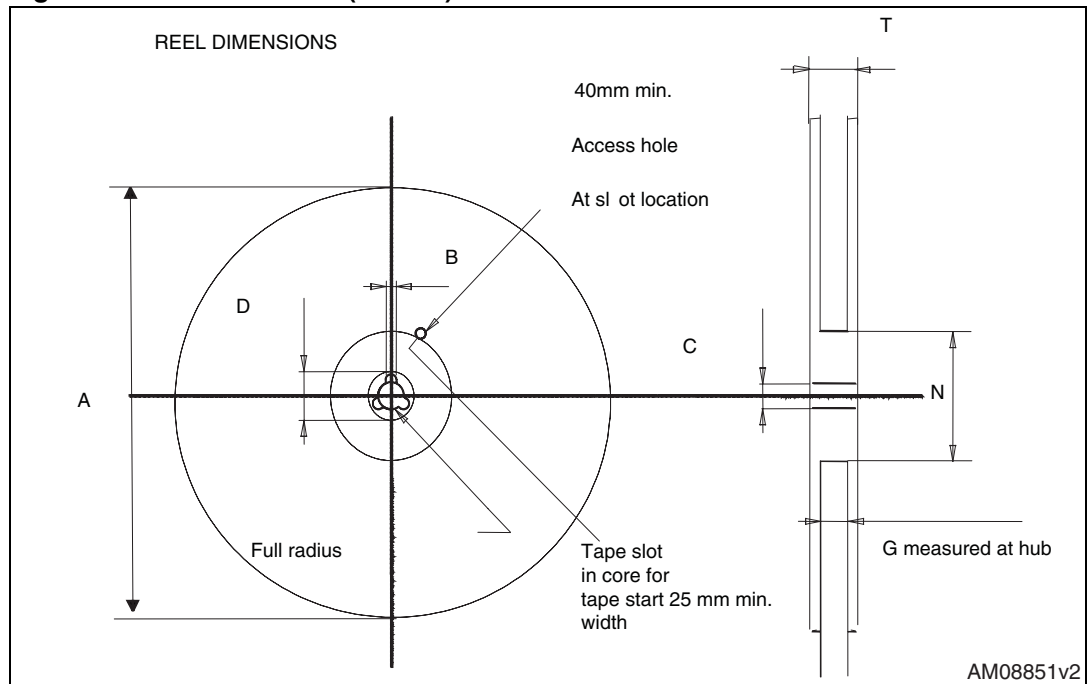


Figure 29. Reel for DPAK (TO-252)



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
10-Feb-2011	1	First release.
17-Nov-2011	2	Updated features in table and description in cover page. Updated <a href="#">Table 2: Absolute maximum ratings</a> , <a href="#">Table 5: On /off states</a> , <a href="#">Table 15: Normalized on resistance vs temperature</a> , <a href="#">Figure 17: Normalized <math>V_{DS}</math> vs temperature</a> and <a href="#">Section 4: Package mechanical data</a> .

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