



# STB12N120K5, STFW12N120K5 STP12N120K5, STW12N120K5

N-channel 1200 V, 0.58  $\Omega$ , 12 A D<sup>2</sup>PAK, TO-3PF, TO-220, TO-247  
Zener-protected SuperMESH™ 5 Power MOSFET

Preliminary data

## Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>W</sub>
STB12N120K5	1200 V	< 0.69 $\Omega$	12 A	250 W
STFW12N120K5				63 W
STP12N120K5				250 W
STW12N120K5				

- Worldwide best R<sub>DS(on)</sub> in TO-220
- Worldwide best FOM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

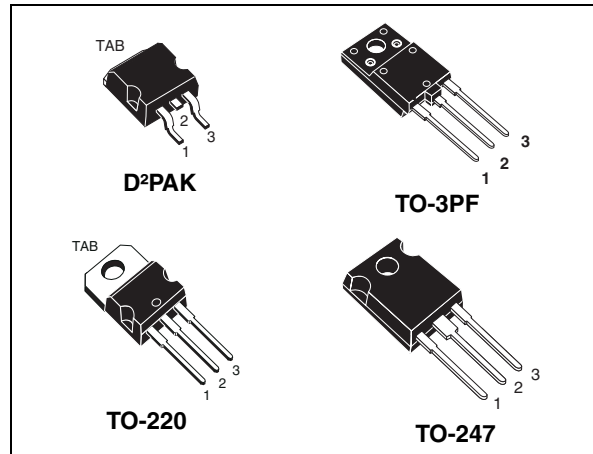


Figure 1. Internal schematic diagram

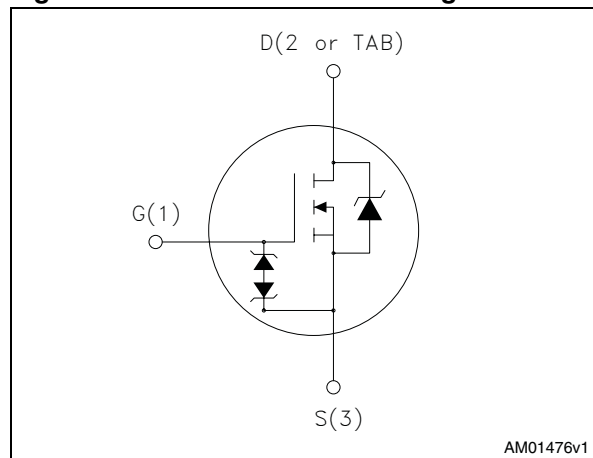


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB12N120K5	12N120K5	D <sup>2</sup> PAK	Tape and reel
STFW12N120K5		TO-3PF	Tube
STP12N120K5		TO-220	
STW12N120K5		TO-247	

# Contents

1	Electrical ratings .....	3
2	Electrical characteristics .....	4
3	Test circuits .....	6
4	Package mechanical data .....	7
5	Packaging mechanical data .....	16
6	Revision history .....	18

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-3PF	TO-220	TO-247	
V <sub>GS</sub>	Gate-source voltage	30				V
I <sub>D</sub>	Drain current (single pulse 10 ms width), T <sub>C</sub> = 25 °C	12				A
I <sub>D</sub>	Drain current (single pulse 10 ms width), T <sub>C</sub> = 100 °C	7.6				A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	48				A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	250	63	250		W
I <sub>AR</sub> <sup>(2)</sup>	Max current during repetitive or single pulse avalanche	TBD				A
E <sub>AS</sub> <sup>(3)</sup>	Single pulse avalanche energy	TBD				mJ
dv/dt <sup>(4)</sup>	Peak diode recovery voltage slope	TBD				V/ns
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	- 55 to 150				°C

1. Pulse width limited by safe operating area.
2. Pulse width limited by T<sub>Jmax</sub>.
3. Starting T<sub>J</sub> = 25 °C, I<sub>D</sub>=I<sub>AS</sub>, V<sub>DD</sub>= 50 V
4. I<sub>SD</sub> ≤ 12 A, di/dt ≤ 100 A/μs, V<sub>Peak</sub> ≤ V<sub>(BR)DSS</sub>

**Table 3. Thermal data**

Symbol	Parameter	Value				Unit
		D <sup>2</sup> PAK	TO-3PF	TO-220	TO-247	
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.5	1.98	0.5		°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb max		50	62.5	50	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	30				°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purposes		300			°C

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	1200			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 1200\text{ V}$ , $V_{DS} = 1200\text{ V}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6\text{ A}$		0.58	0.69	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			1700		pF
$C_{oss}$	Output capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	110	-	pF
$C_{rss}$	Reverse transfer capacitance			2		
$C_{o(tr)}^{(1)}$	Equivalent capacitance, time-related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }960\text{ V}$	-	TBD	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance, energy-related			TBD		
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	TBD	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 960\text{ V}$ , $I_D = 6\text{ A}$		49		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$	-	TBD	-	nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 3</a> )		TBD		nC

1. Time-related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy-related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 600\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 5</a> )	-	TBD	-	ns
$t_r$	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
$t_f$	Fall time			TBD		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		12	A
$I_{SDM}$	Source-drain current (pulsed)				48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 4</a> )	-	TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			TBD		A

1. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

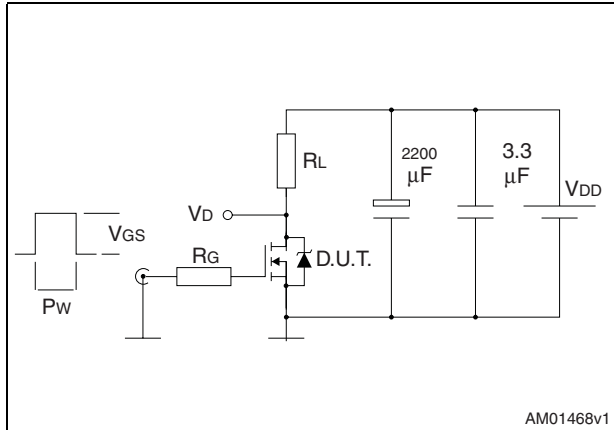
**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$ , (open drain)	30	-		V

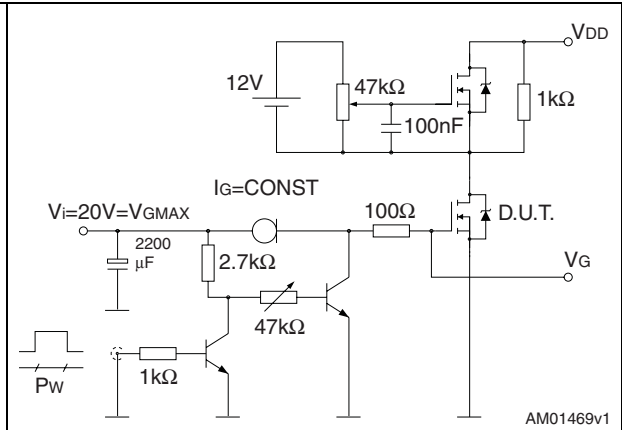
The built-in-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing possible voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage helps to achieve efficient and cost-effective protection of device integrity. These integrated Zener diodes thus reduce the necessity for external components.

### 3 Test circuits

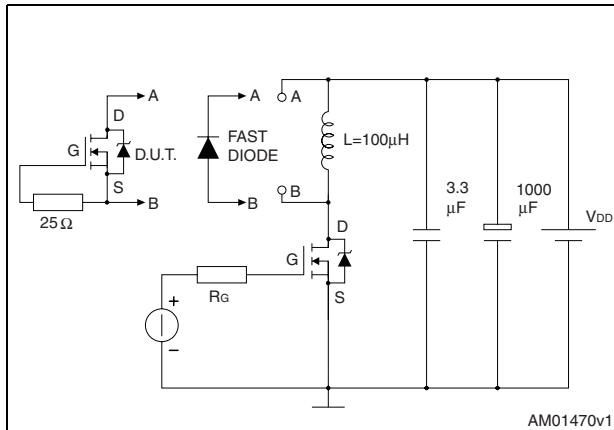
**Figure 2. Switching time test circuit for resistive load**



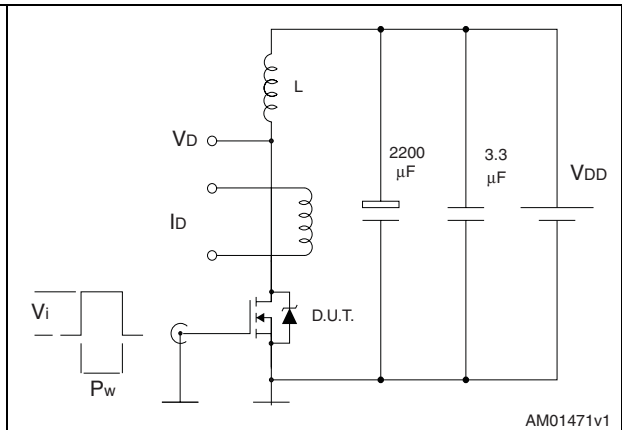
**Figure 3. Gate charge test circuit**



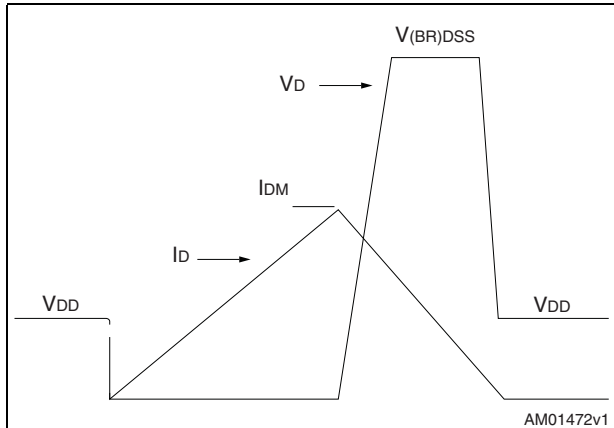
**Figure 4. Test circuit for inductive load switching and diode recovery times**



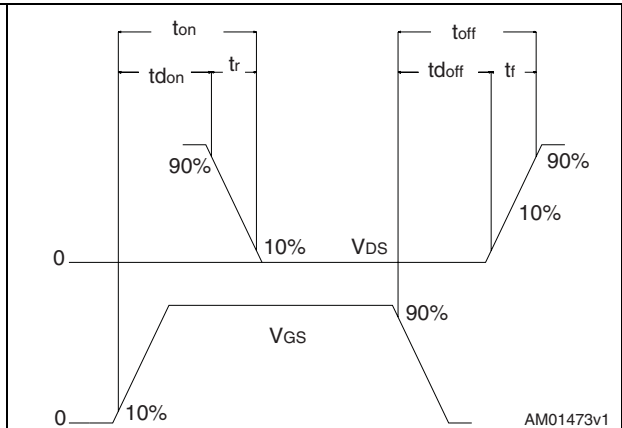
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°



Figure 8. D<sup>2</sup>PAK (TO-263) drawing

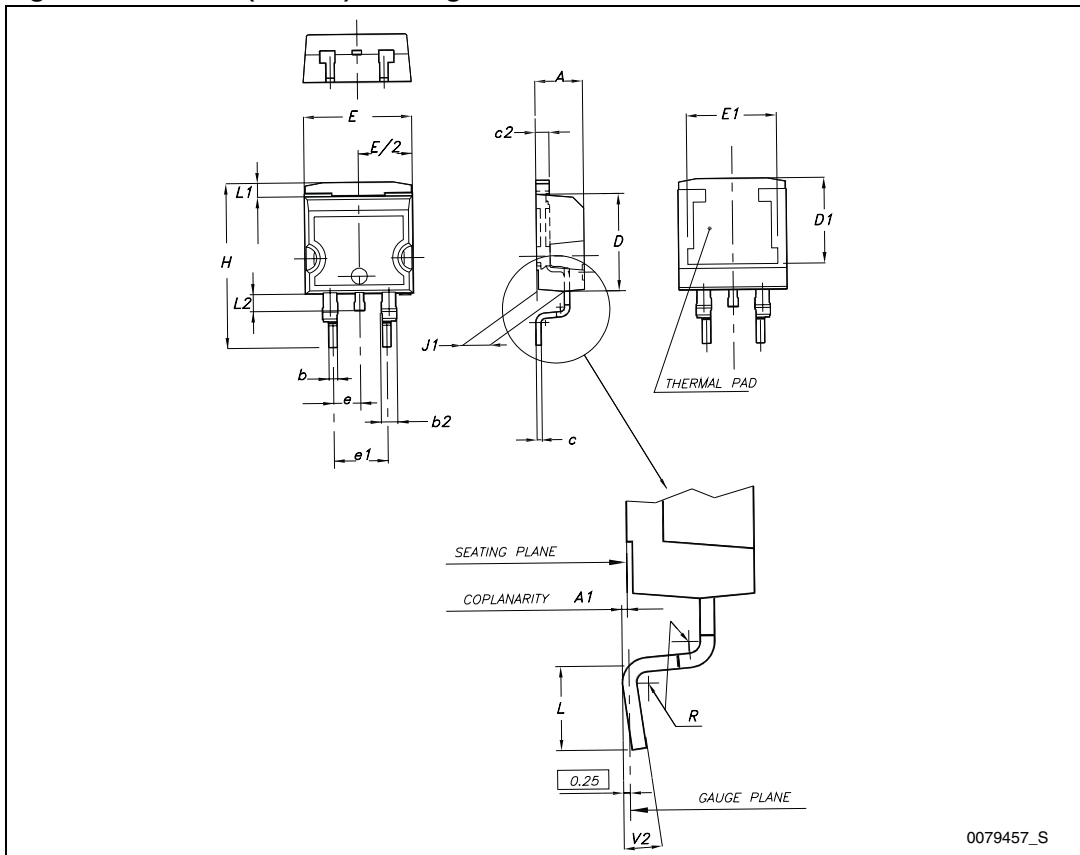
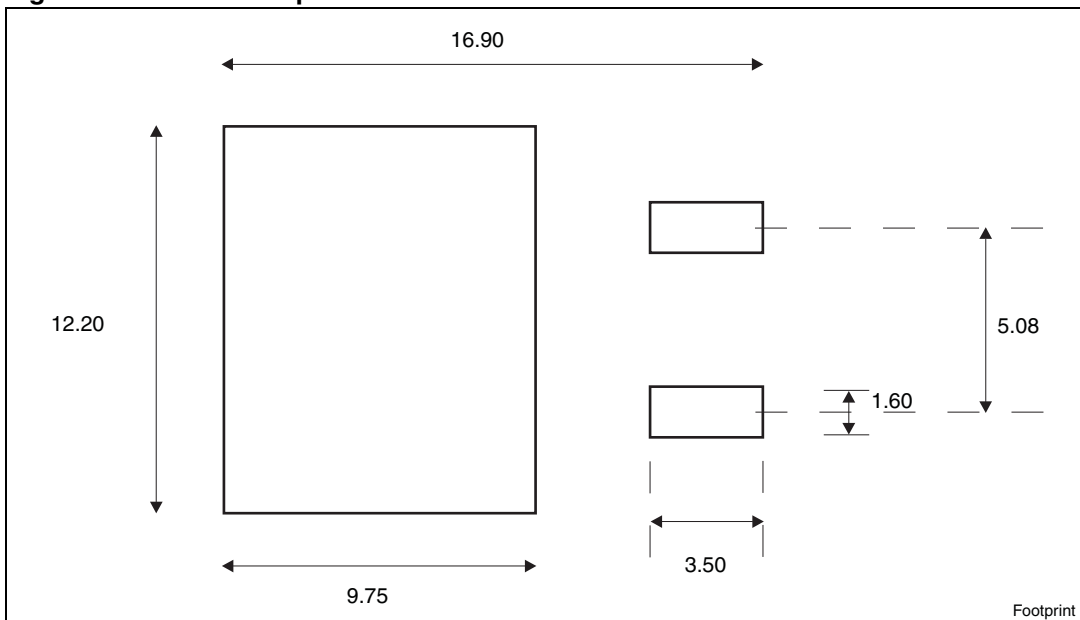


Figure 9. D<sup>2</sup>PAK footprint<sup>(a)</sup>

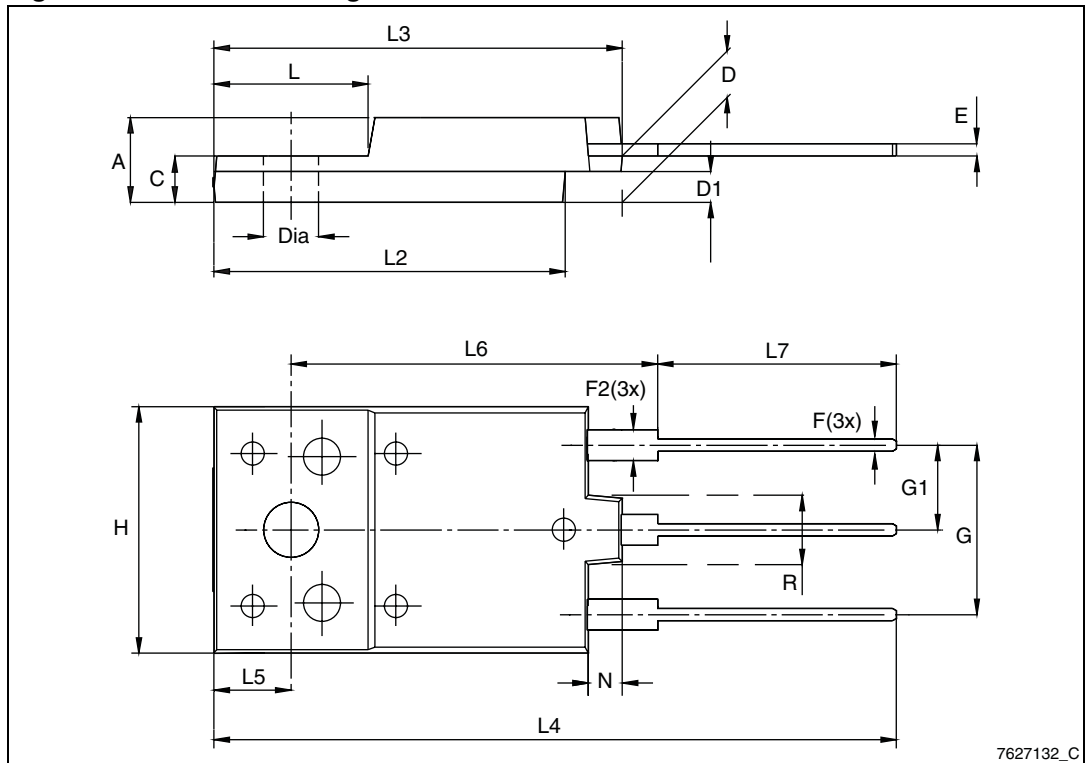


a. All dimensions are in millimeters

Table 10. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

Figure 10. TO-3PF drawing



7627132\_C

Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 11. TO-220 type A drawing

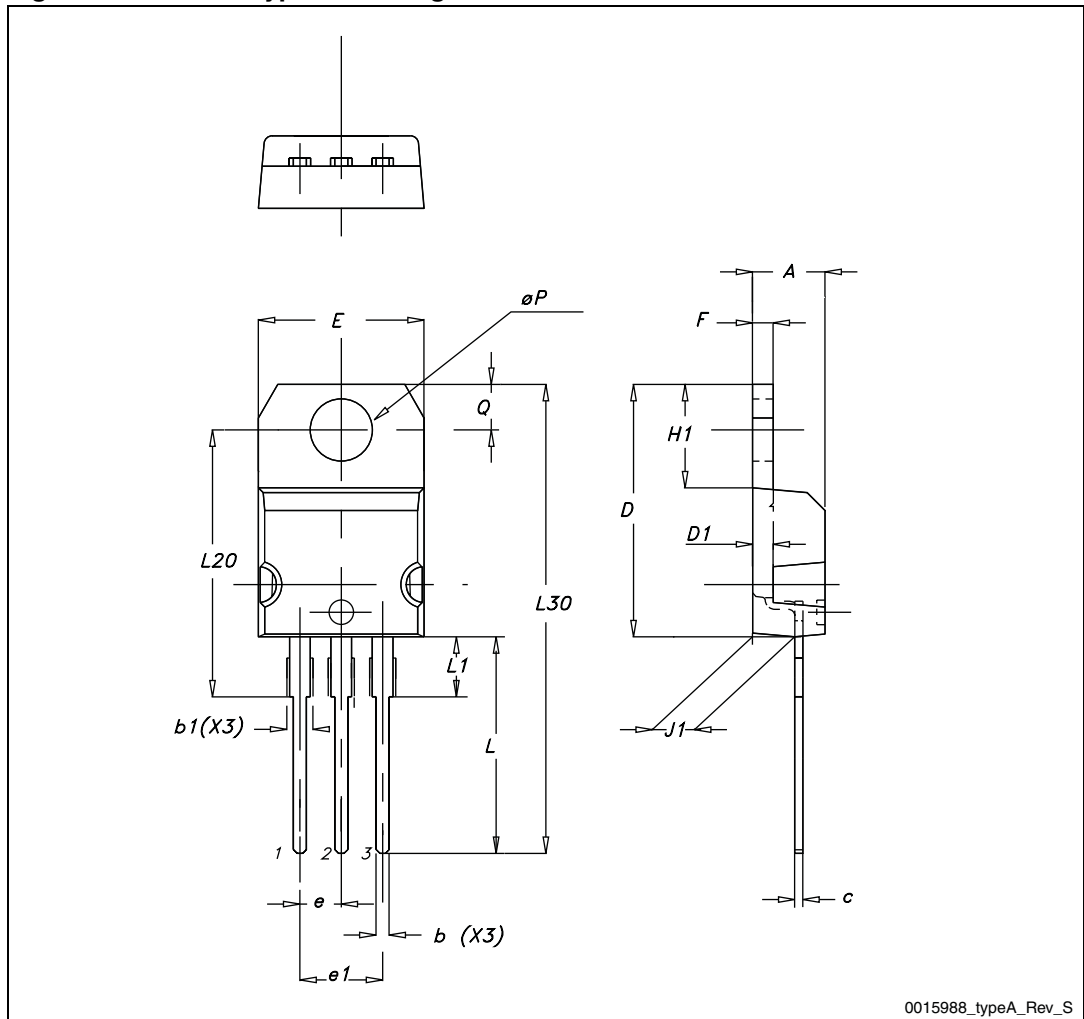
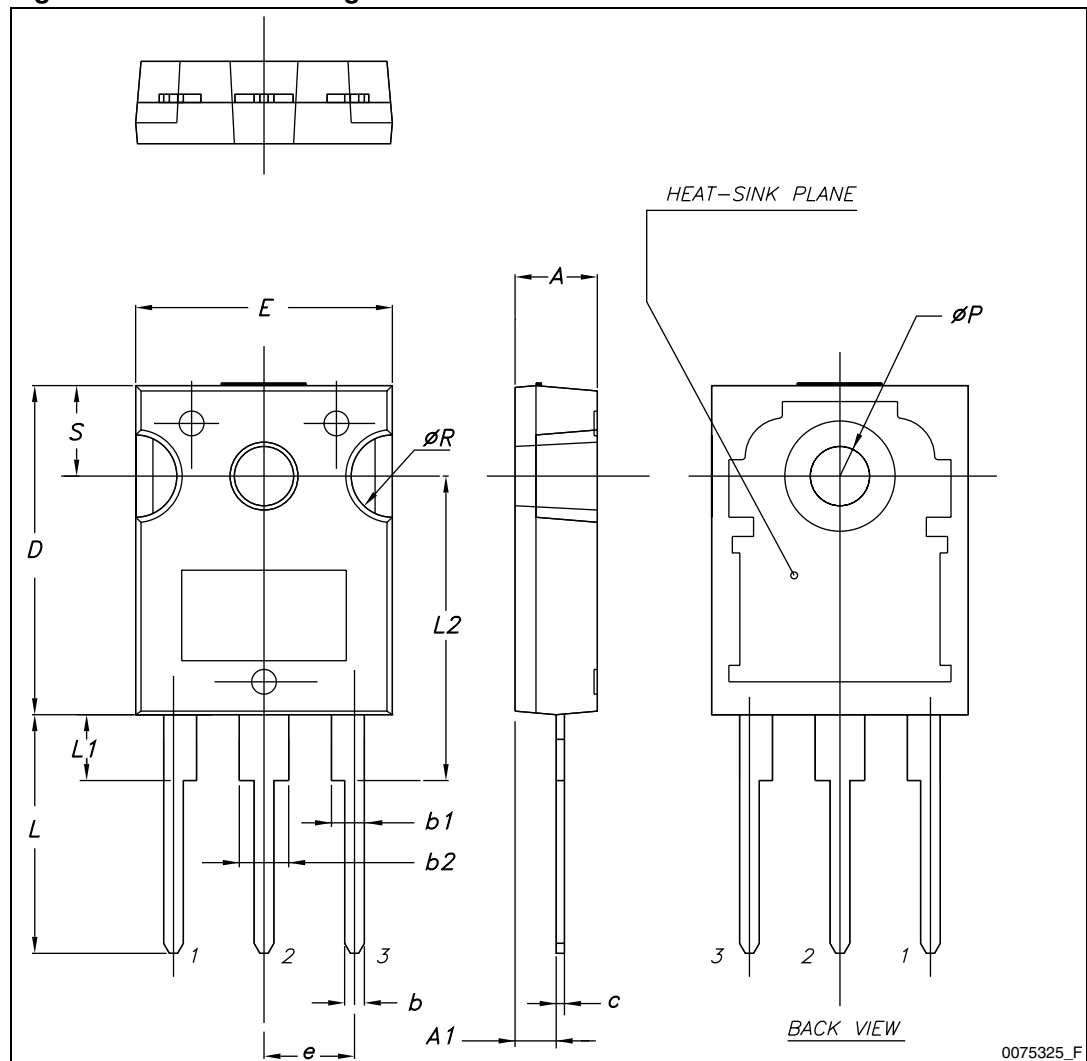


Table 12. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 12. TO-247 drawing



## 5 Packaging mechanical data

Table 13. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			



Figure 13. Tape

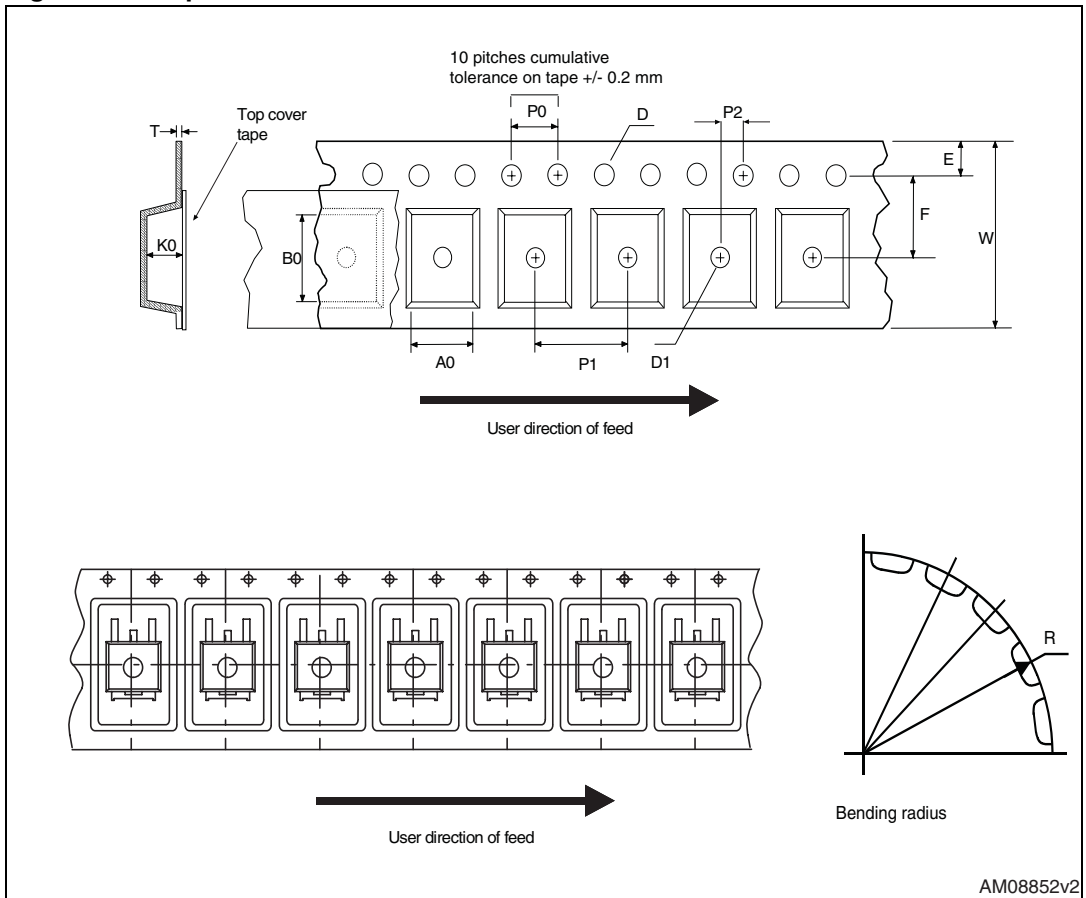
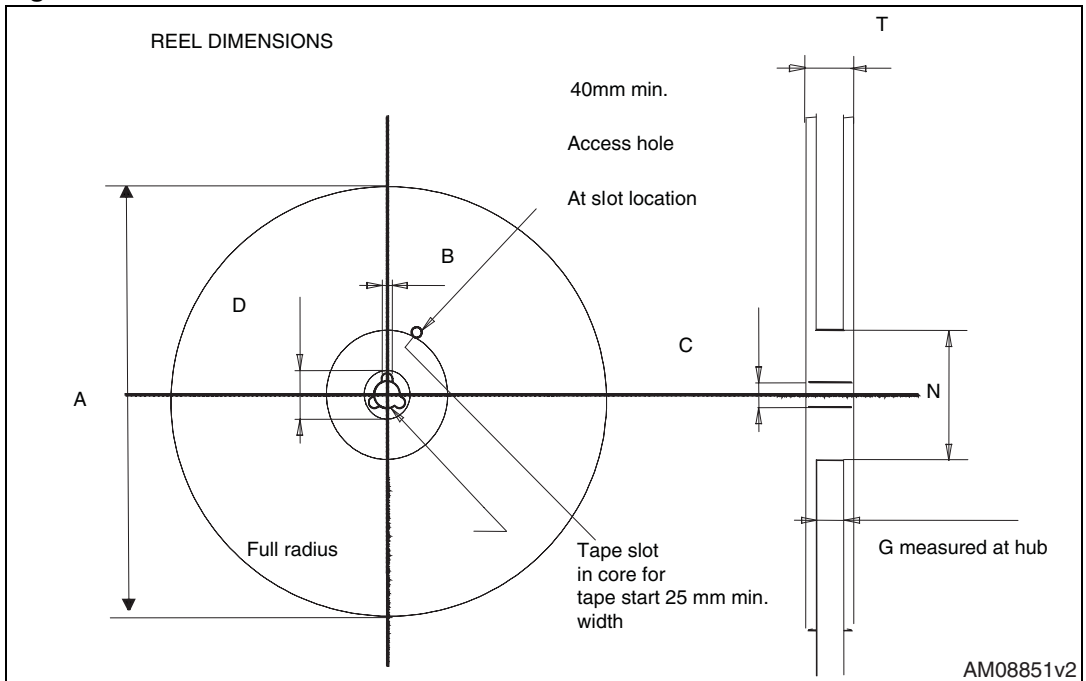


Figure 14. Reel



## 6 Revision history

Table 14. Document revision history

Date	Revision	Changes
23-Aug-2011	1	First release.

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