

STD7N80K5, STF7N80K5, STP7N80K5

Datasheet — preliminary data

N-channel 800 V, 0.95 Ω typ., 6 A Zener-protected SuperMESH[™] 5 Power MOSFET in a TO-220FP, DPAK and TO-220 packages

Features

Туре	V_{DSS}	R _{DS(on)} max	I _D	P _{TOT}
STD7N80K5				110 W
STF7N80K5	800 V	< 1.2 Ω	6 A	25 W
STP7N80K5				110 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

Switching applications

Description

These devices are N-channel Zener-protected Power MOSFETs realized in SuperMESH[™]5, a revolutionary avalanche-rugged very high voltage Power MOSFET technology based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1.	Device	summary

Order codes	Marking	Package	Packaging
STD7N80K5		DPAK	Tape and reel
STF7N80K5	7N80K5	TO-220FP	Tube
STP7N80K5		TO-220	Tube

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

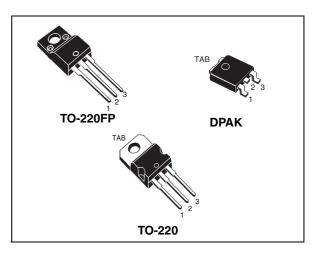
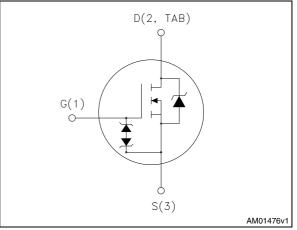
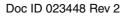


Figure 1. Internal schematic diagram



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1 Electrical ratings

Gumbal	Devenueter	Va	lue	11
Symbol	Parameter	DPAK, TO-220	TO-220FP	Unit
V _{GS}	Gate- source voltage	± 30		V
۱ _D	Drain current (continuous) at $T_C = 25 \ ^{\circ}C$	6 6 ⁽¹⁾		А
۱ _D	Drain current (continuous) at T_{C} = 100 °C	3.8 3.8 ⁽¹⁾		А
I _{DM} ⁽²⁾	Drain current (pulsed)	24	24 ⁽¹⁾	А
P _{TOT}	Total dissipation at $T_C = 25 \ ^{\circ}C$	110	25	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	TE	A	
E _{AS}	Single pulse avalanche energy (starting $T_J = 25 \text{ °C}, I_D=I_{AS}, V_{DD}= 50 \text{ V}$)	TE	mJ	
V _{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink $(t=1 s;T_C=25 °C)$		2500	v
dv/dt ⁽³⁾	Peak diode recovery voltage slope	TBD		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 te	o 150	°C

Table 2.Absolute maximum ratings

1. Limited by package.

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 6 \text{ A}, \text{ di/dt} \leq 100 \text{ A/}\mu\text{s}, V_{Peak} \leq V_{(BR)DSS}$

Table 3.Thermal data

Symbol	Parameter		Unit		
Symbol	Farameter	TO-220	DPAK	PAK TO-220FP	
Rthj-case	Thermal resistance junction-case max	1.14		5	
Rthj-amb	Thermal resistance junction-amb max	62.5		62.5	°C/W
Rthj-pcb ⁽¹⁾	Thermal resistance junction-pcb max		50		

1. When mounted on 1 inch² FR-4, 2 Oz copper board.



2 Electrical characteristics

 $(T_{CASE} = 25 \ ^{\circ}C \text{ unless otherwise specified}).$

	On/on states					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage (V _{GS} = 0)	I _D = 1 mA	800			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 800 V V _{DS} = 800 V, Tc=125 °C			1 50	μΑ μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20 V$			±10	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \ \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 3 A		0.95	1.2	Ω

Table 4. On/off states

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance			355		pF
C _{oss}	Output capacitance	V_{DS} =100 V, f=1 MHz, V_{GS} =0	-	30	-	pF
C _{rss}	Reverse transfer capacitance			1		pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0 \text{ to } 640 \text{ V}$	-	TBD	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	TBD	-	pF
R _G	Intrinsic gate resistance	f = 1MHz open drain	-	3	-	Ω
Qg	Total gate charge	V _{DD} = 640 V, I _D = 6 A		10		nC
Q _{gs}	Gate-source charge	V _{GS} =10 V	-	TBD	-	nC
Q _{gd}	Gate-drain charge	(see Figure 3)		TBD		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}



	e milening timee					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$\label{eq:VDD} \begin{array}{l} V_{\text{DD}} = 400 \; \text{V}, \; I_{\text{D}} = 3 \; \text{A}, \\ R_{\text{G}} = 4.7 \; \Omega \; V_{\text{GS}} = 10 \; \text{V} \\ \textit{(see Figure 5)} \end{array}$	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 6. Switching times

Table 7.Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM}	Source-drain current Source-drain current (pulsed)		-		6 24	A A
V _{SD} ⁽¹⁾	Forward on voltage	I_{SD} = 6 A, V_{GS} =0	-		1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 6 A, V _{DD} = 60 V di/dt = 100 A/µs, <i>(see Figure 4)</i>	-	TBD TBD TBD		ns μC Α
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 6 A,V _{DD} = 60 V di/dt=100 A/µs, Tj=150 °C <i>(see Figure 4)</i>	-	TBD TBD TBD		ns μC Α

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zen	er diode
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Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
BV _{GSO}	Gate-source breakdown voltage	lgs ± 1mA, (open drain)	30	-	-	V

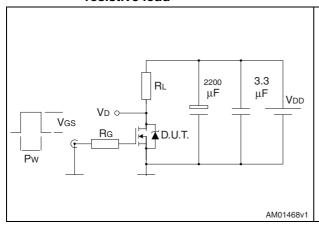
The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

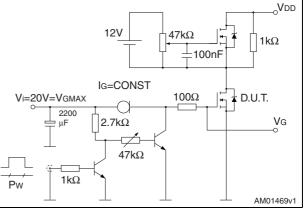


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3 Test circuits

Figure 2. Switching times test circuit for resistive load



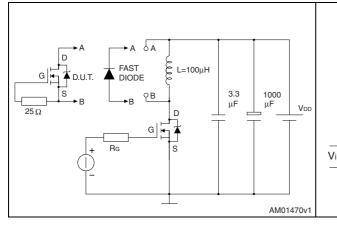


Gate charge test circuit

Figure 3.

Figure 4. Test circuit for inductive load switching and diode recovery times





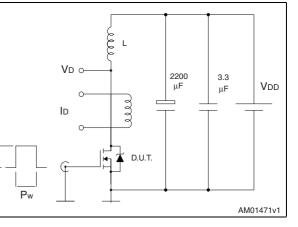
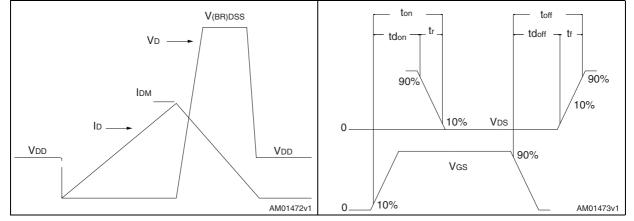




Figure 7. Switching time waveform



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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.



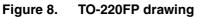
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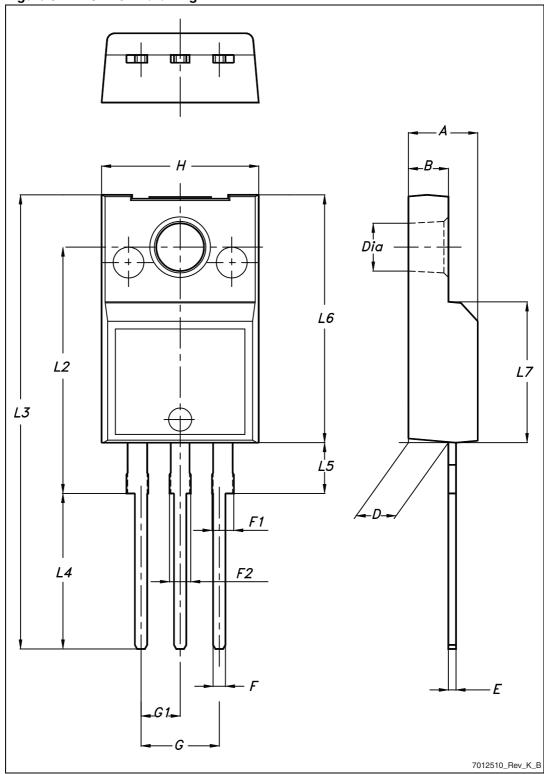
Dim.	mm			
	Min.	Тур.	Max.	
А	4.4		4.6	
В	2.5		2.7	
D	2.5		2.75	
E	0.45		0.7	
F	0.75		1	
F1	1.15		1.70	
F2	1.15		1.70	
G	4.95		5.2	
G1	2.4		2.7	
Н	10		10.4	
L2		16		
L3	28.6		30.6	
L4	9.8		10.6	
L5	2.9		3.6	
L6	15.9		16.4	
L7	9		9.3	
Dia	3		3.2	

Table 9.TO-220FP mechanical data

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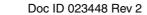




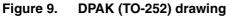
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	mm			
Dim.	Min.	Тур.	Max.	
A	2.20		2.40	
A1	0.90		1.10	
A2	0.03		0.23	
b	0.64		0.90	
b4	5.20		5.40	
С	0.45		0.60	
c2	0.48		0.60	
D	6.00		6.20	
D1		5.10		
E	6.40		6.60	
E1		4.70		
е		2.28		
e1	4.40		4.60	
Н	9.35		10.10	
L	1			
L1		2.80		
L2		0.80		
L4	0.60		1	
R		0.20		
V2	0°		8°	

Table 10. DPAK (TO-252) mechanical data







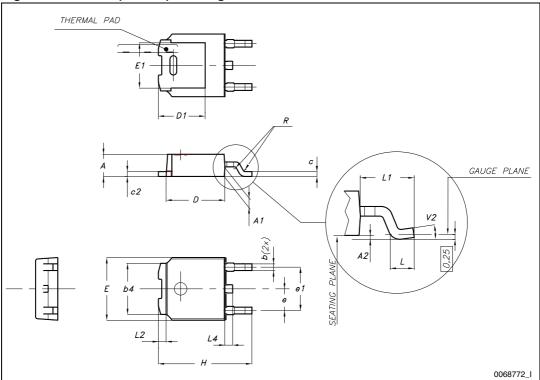
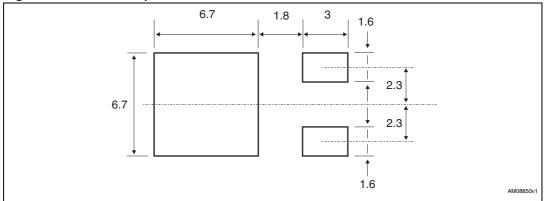


Figure 10. DPAK footprint^(a)



a. All dimensions are in millimeters



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Dim	mm				
Dim. —	Min.	Тур.	Max.		
A	4.40		4.60		
b	0.61		0.88		
b1	1.14		1.70		
с	0.48		0.70		
D	15.25		15.75		
D1		1.27			
E	10		10.40		
е	2.40		2.70		
e1	4.95		5.15		
F	1.23		1.32		
H1	6.20		6.60		
J1	2.40		2.72		
L	13		14		
L1	3.50		3.93		
L20		16.40			
L30		28.90			
ØР	3.75		3.85		
Q	2.65		2.95		

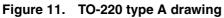
Table 11. TO-220 type A mechanical data

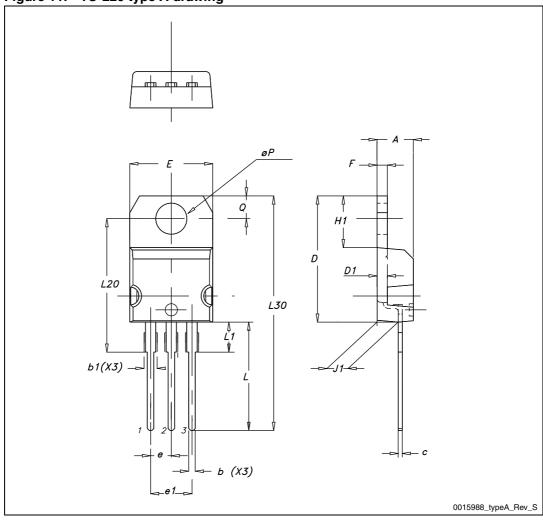


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5 Packaging information

Таре				Reel		
Dim.	r	ım	Dim	mm		
	Min.	Max.	— Dim.	Min.	Max.	
A0	6.8	7	А		330	
B0	10.4	10.6	В	1.5		
B1		12.1	С	12.8	13.2	
D	1.5	1.6	D	20.2		
D1	1.5		G	16.4	18.4	
Е	1.65	1.85	N	50		
F	7.4	7.6	Т		22.4	
K0	2.55	2.75				
P0	3.9	4.1		Base qty.	2500	
P1	7.9	8.1		Bulk qty.	2500	
P2	1.9	2.1				
R	40					
Т	0.25	0.35				
W	15.7	16.3				

Table 12. DPAK (TO-252) tape and reel mechanical data

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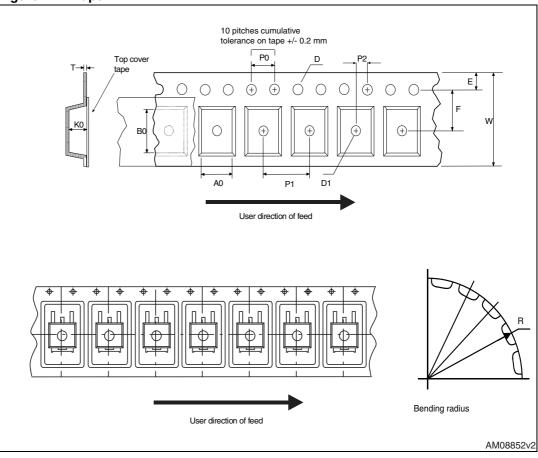
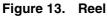
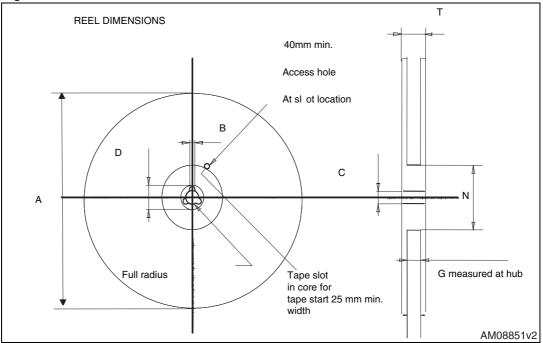


Figure 12. Tape







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6 Revision history

Table 13.Document revision history

Date	Revision	Changes	
17-Jul-2012	1	First release.	
17-Oct-2012	2	 Minor text changes in cover page Modified: title and I_D value in cover page 	

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