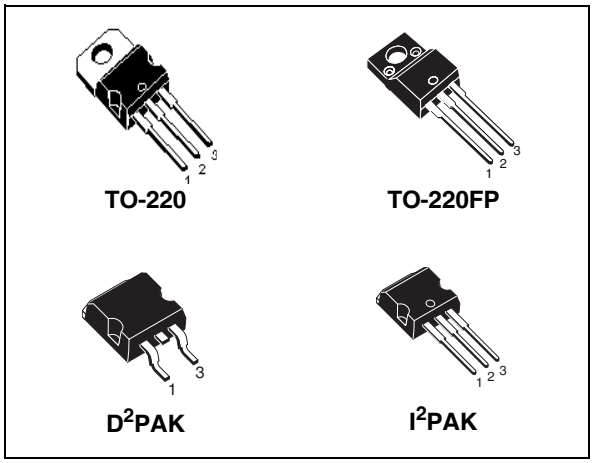
STB7NK80Z, STB7NK80Z-1
STP7NK80ZFP, STP7NK80Z

N-channel 800 V, 1.5 Ω, 5.2 A, TO-220,TO-220FP,D²PAK,I²PAK
Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STP7NK80Z	800V	< 1.8Ω	5.2A
STP7NK80ZFP	800V	< 1.8Ω	5.2A
STB7NK80Z	800V	< 1.8Ω	5.2A
STB7NK80Z-1	800V	< 1.8Ω	5.2A

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



Applications

- Switching application

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

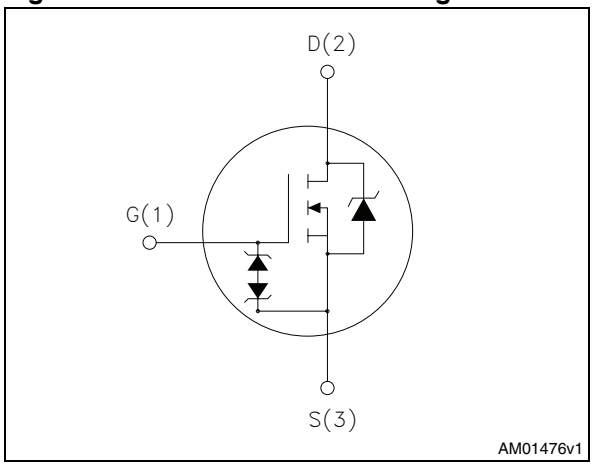


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB7NK80ZT4	B7NK80Z	D²PAK	Tape e reel
STB7NK80Z-1	B7NK80Z	I²PAK	Tube
STP7NK80Z	P7NK80Z	TO-220	
STP7NK80ZFP	P7NK80ZFP	TO-220FP	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-220	D^2PAK	I^2PAK	TO-220FP	
V_{DS}	Drain-source voltage (V_{GS} = 0)	800				V
V_{GS}	Gate- source voltage	± 30				V
I_D	Drain current (continuous) at T_C = 25 °C	5.2			5.2 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	3.3			3.3 (1)	A
I_{DM} (2)	Drain current (pulsed)	20.8			20.8(1)	A
P_{TOT}	Total dissipation at T_C = 25°C	125			30	W
	Derating factor	1			0.24	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	4000				V
dv/dt (3)	Peak diode recovery voltage slope	4.5				V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C= 25 °C)				2500	V
T_j T_{stg}	Max operating junction temperature Storage temperature	-55 to 150				°C °C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 5.2$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX.}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	D^2PAK	I^2PAK	TO-220FP	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1			4.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5				°C/W
T_l	Maximum lead temperature for soldering purpose	300				°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	5.2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D =1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero gate voltage Drain Current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C = 125 °C				1 50	µA µA
I_{GSS}	Gate-body leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 2.6 A		1.5	1.8	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2.6 A	-	5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1138 122 25		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{DS} =0 , V_{DS} = 0 to 640 V	-	50		pF
$t_{d(on)}$ t_r $t_{r(off)}$ t_r	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 400 V, I_D = 2.6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	20 12 45 20		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 640 V, I_D = 5.2 A, V_{GS} = 10 V (see *Figure 18*)	-	40 7 21	56	nC nC nC
$t_{r(Voff)}$ t_r t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 640 V, I_D = 5.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17*)	-	12 10 20		ns ns ns

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		5.2 20.8	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 5.2 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 5.2 A, di/dt = 100 A/µs V_{DD} = 50 V, Tj = 150°C (see *Figure 22*)	-	530 3.31 12.5		ns µC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Pulse width limited by safe operating area

Table 8. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	I_{GS}= ± 1mA (open drain)	30			V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK, I²PAK

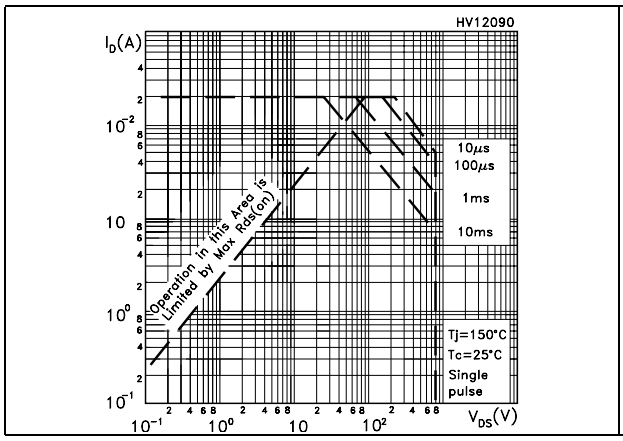


Figure 3. Thermal impedance for TO-220, D²PAK, I²PAK

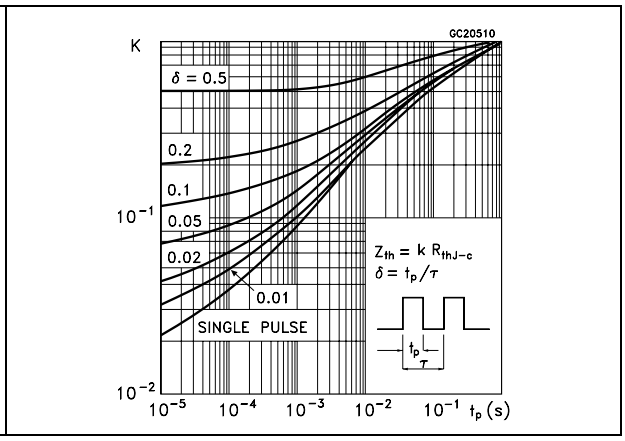


Figure 4. Safe operating area for TO-220FP

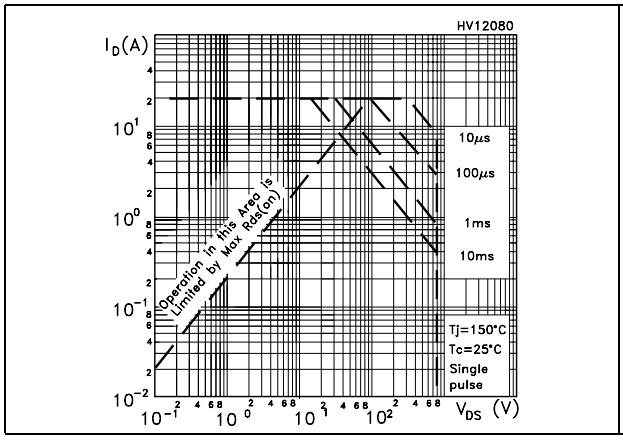


Figure 5. Thermal impedance for TO-220FP

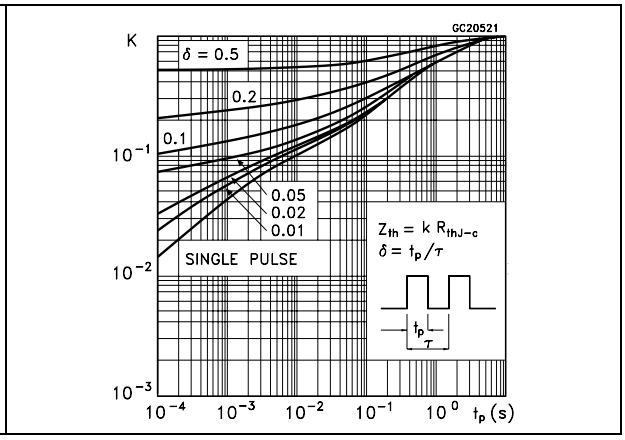


Figure 6. Output characteristics

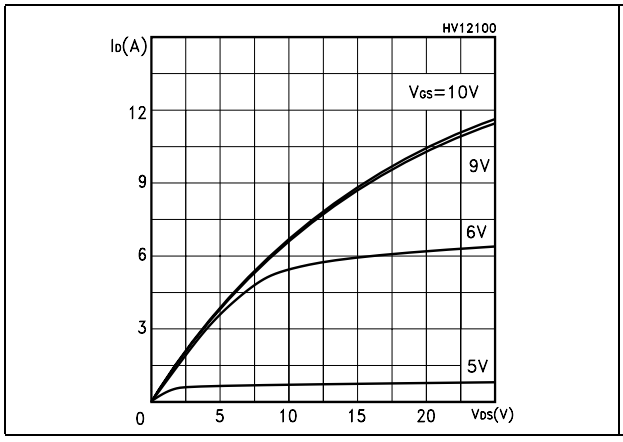


Figure 7. Transfer characteristics

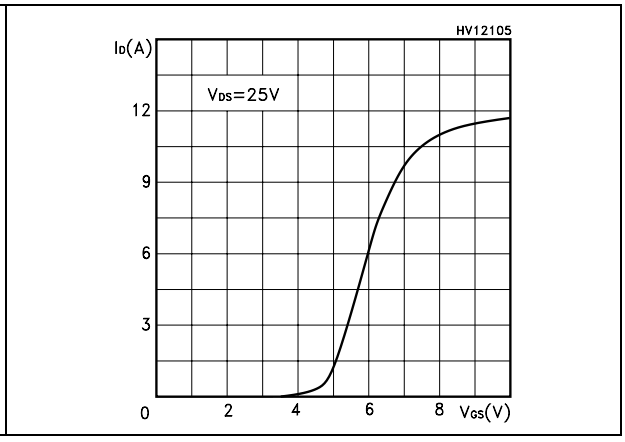


Figure 8. Transconductance

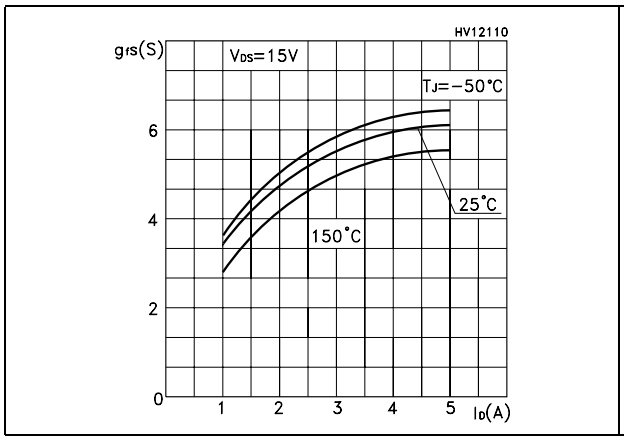


Figure 9. Static drain-source on resistance

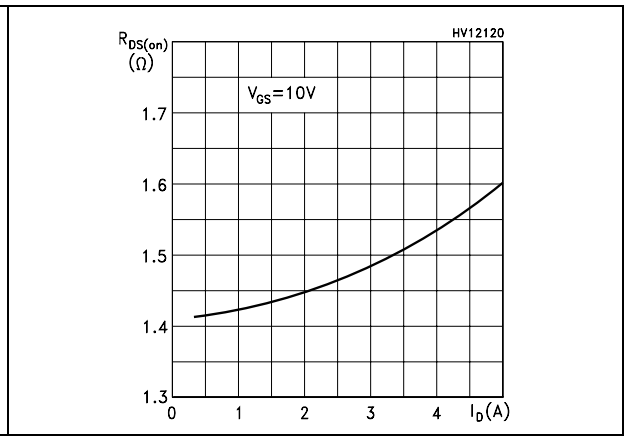


Figure 10. Gate charge vs gate-source voltage

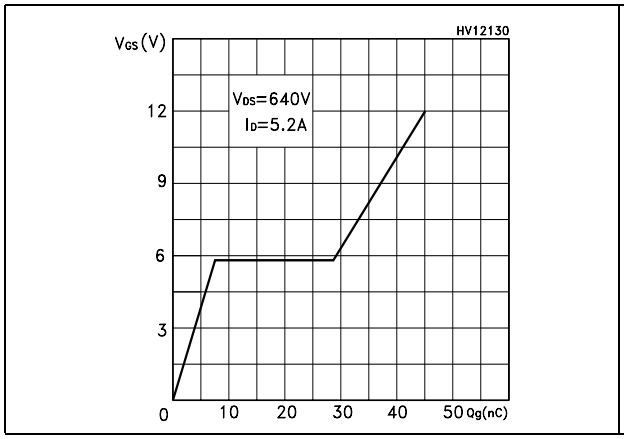


Figure 11. Capacitance variations

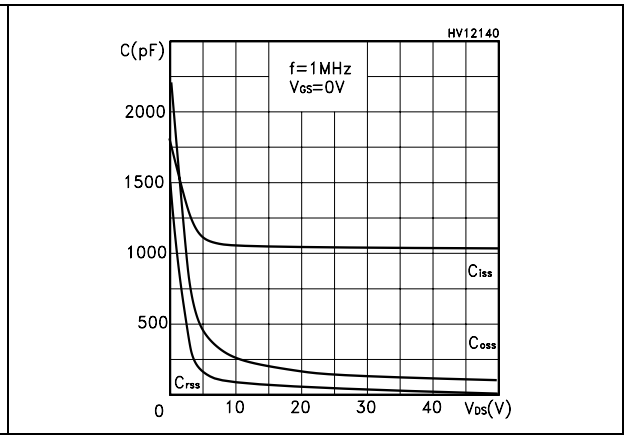


Figure 12. Normalized gate threshold voltage vs temperature

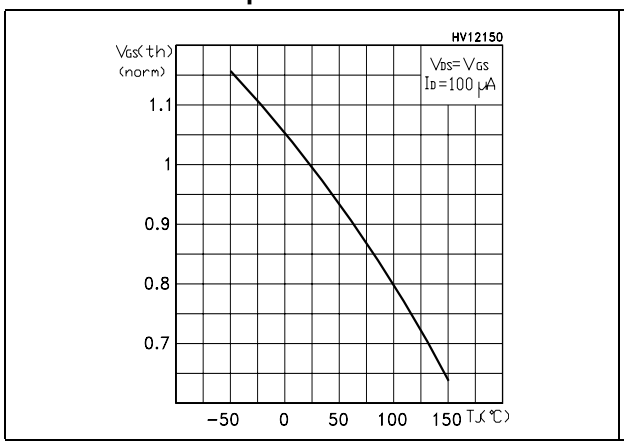


Figure 13. Normalized on resistance vs temperature

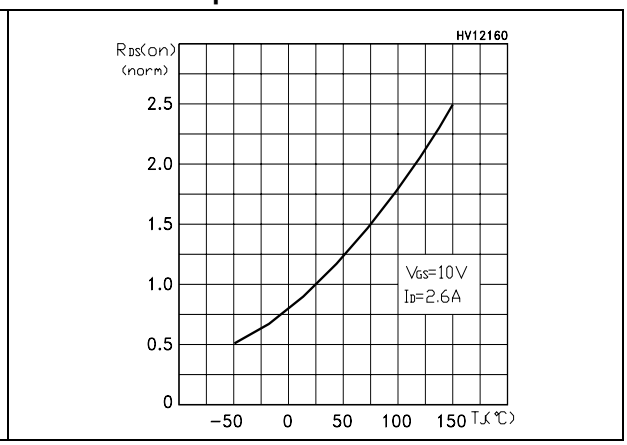


Figure 14. Source-drain diode forward characteristic

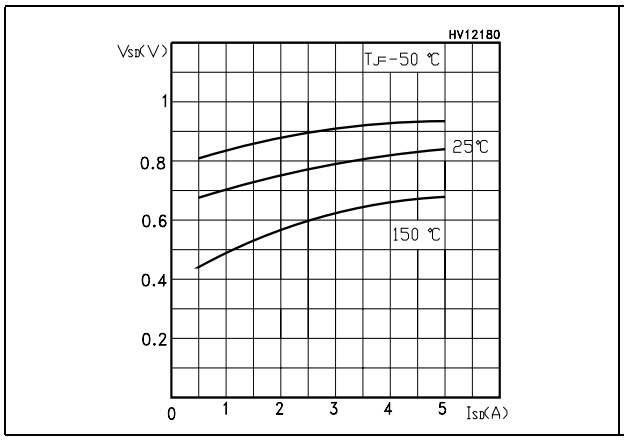


Figure 15. Normalized BVDSS vs temperature

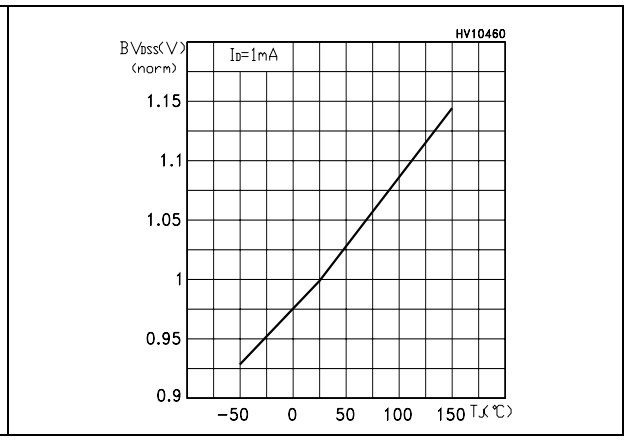
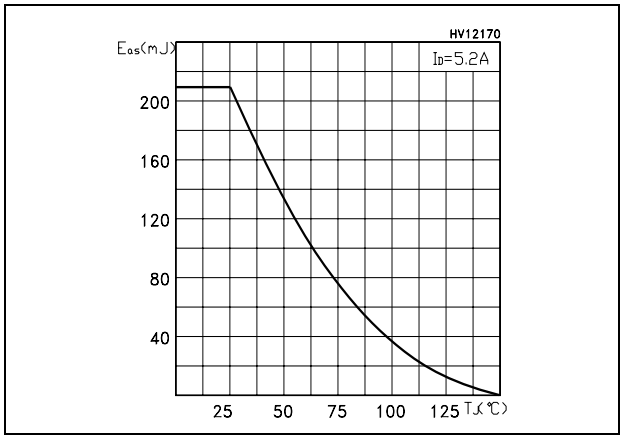


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load

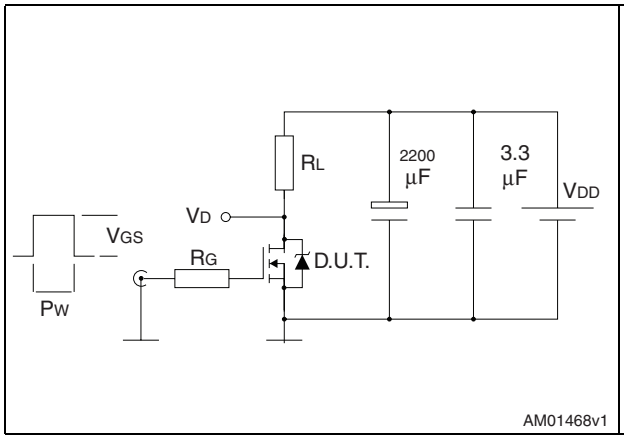


Figure 18. Gate charge test circuit

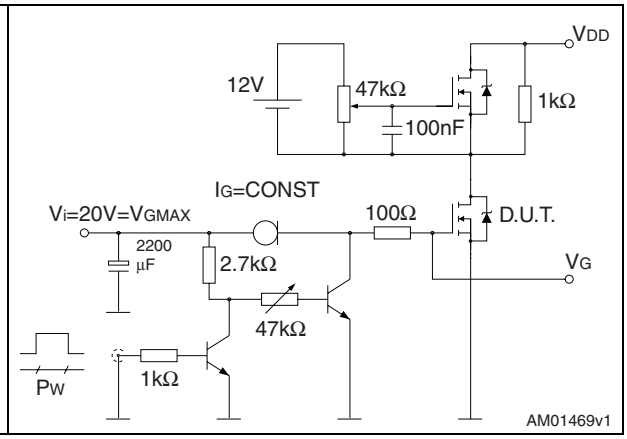


Figure 19. Test circuit for inductive load switching and diode recovery times

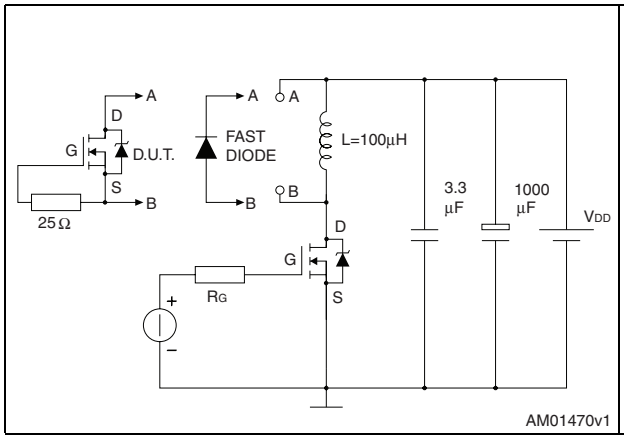


Figure 20. Unclamped inductive load test circuit

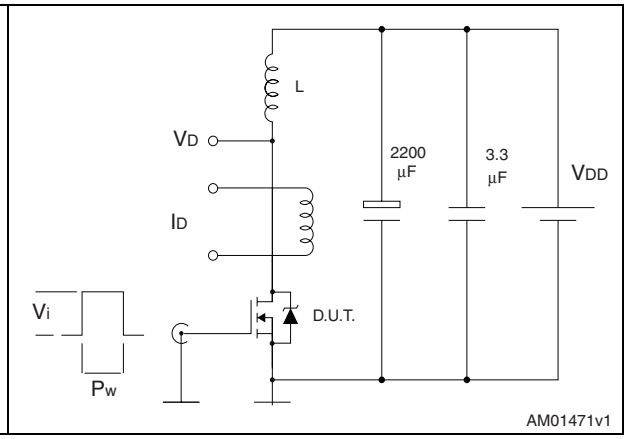


Figure 21. Unclamped inductive waveform

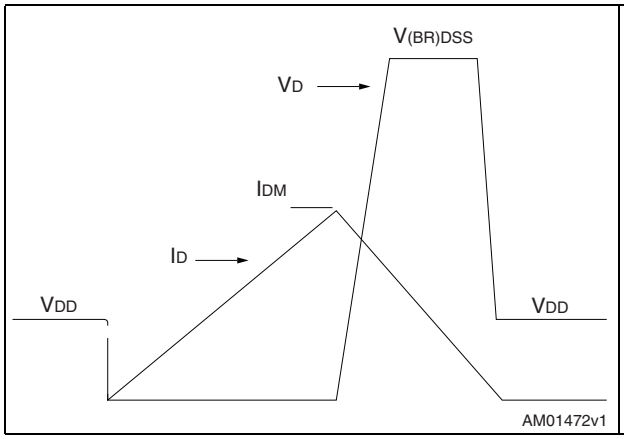
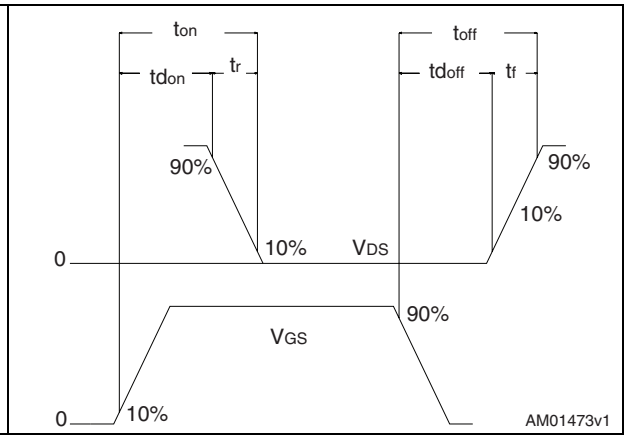


Figure 22. Switching time waveform



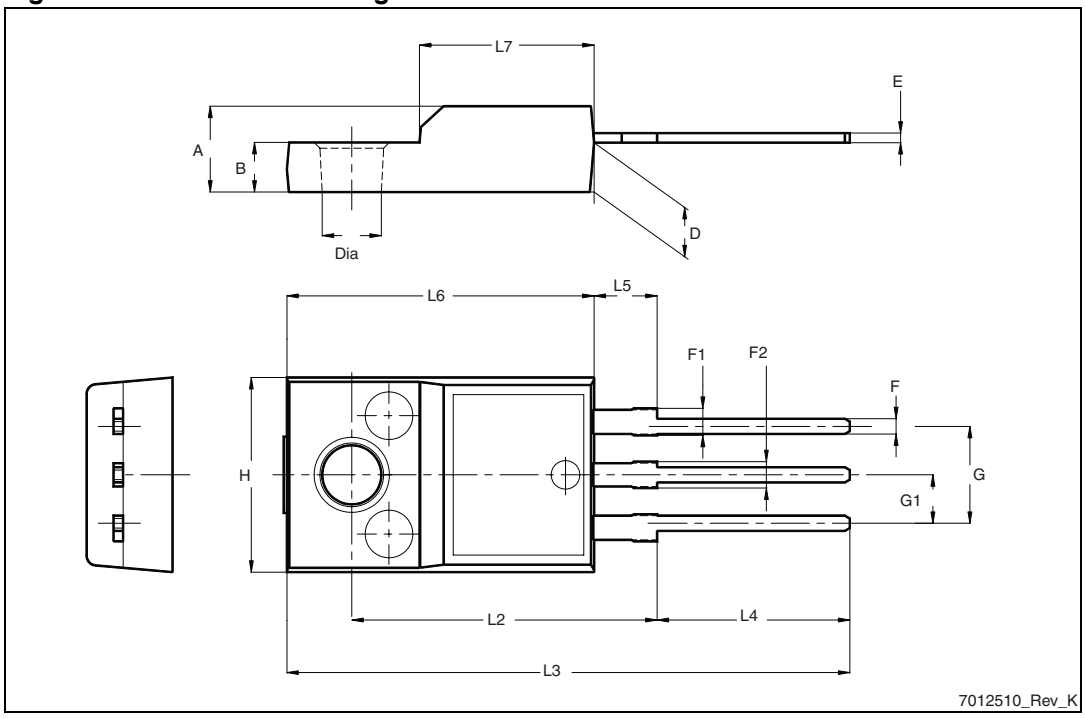
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

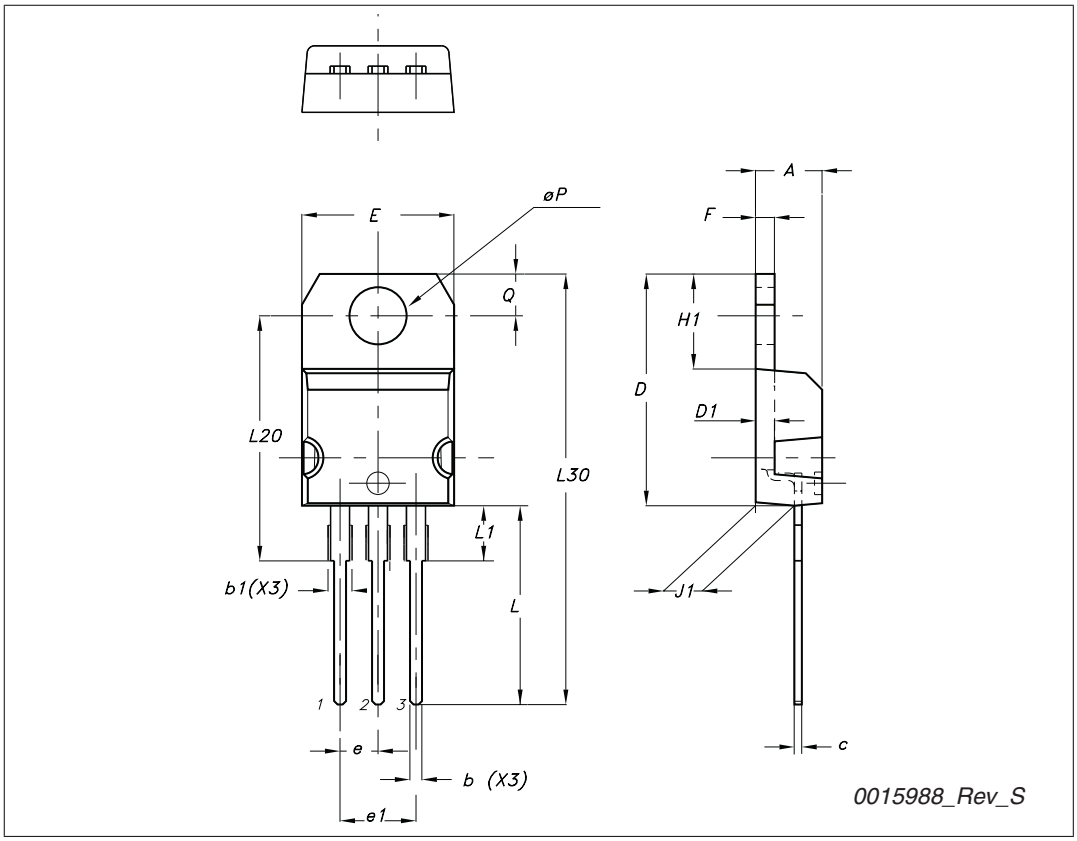
Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing



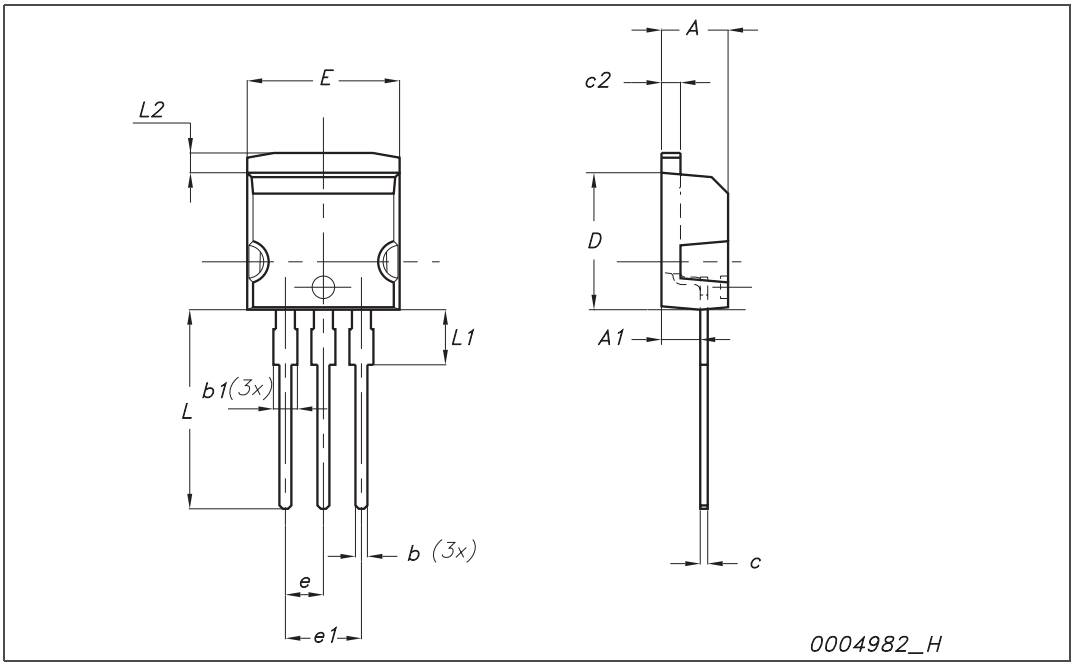
TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



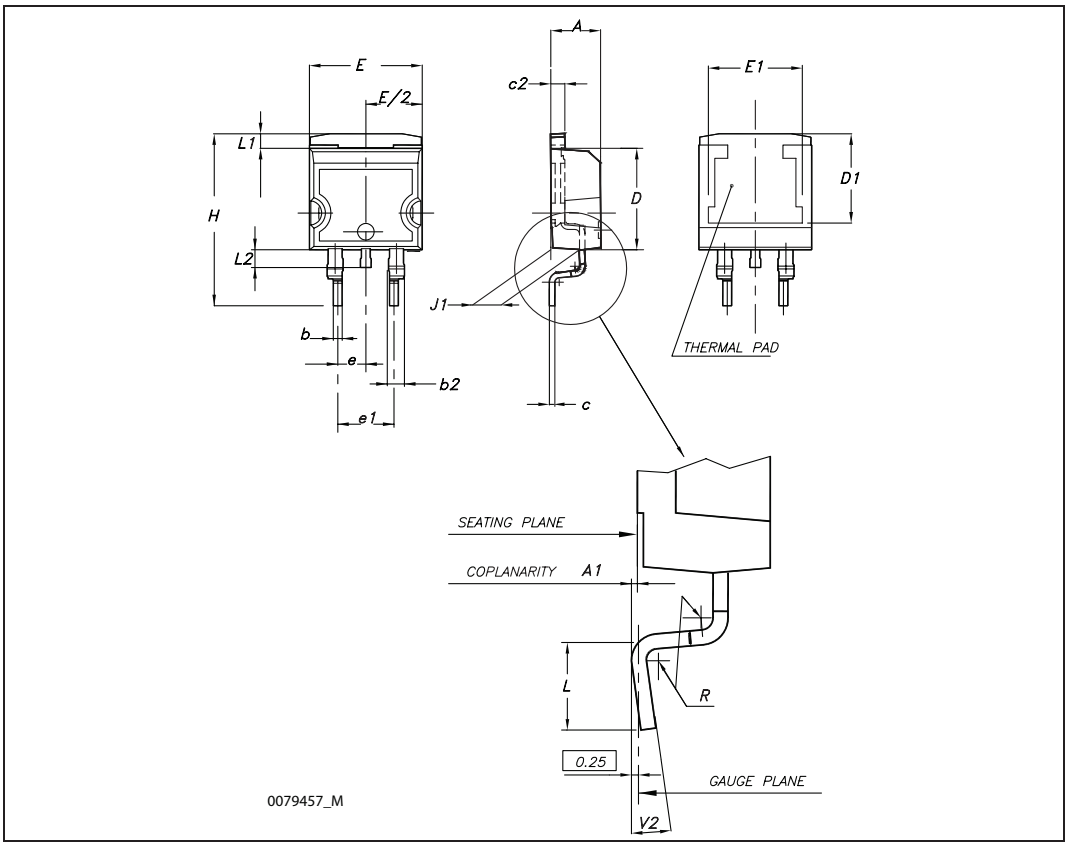
I²PAK (TO-262) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	2.40		2.72	0.094		0.107
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
c2	1.23		1.32	0.048		0.052
D	8.95		9.35	0.352		0.368
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
E	10		10.40	0.393		0.410
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L2	1.27		1.40	0.050		0.055



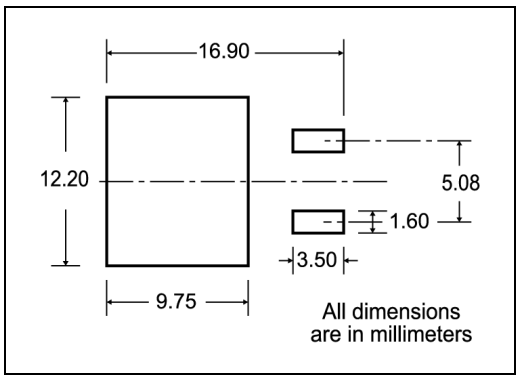
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

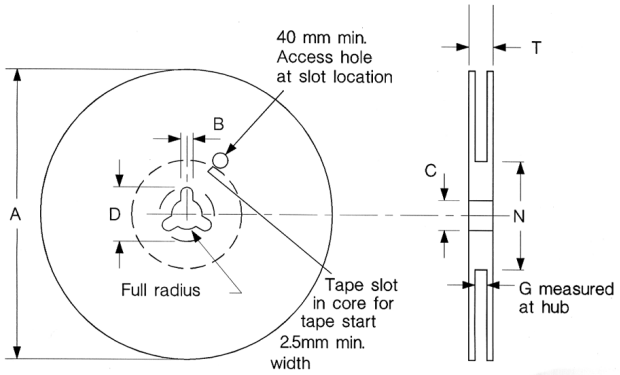


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



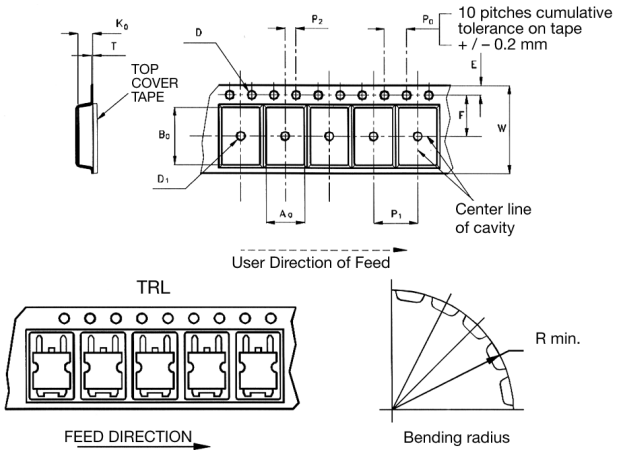
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956



* on sales type

6 Revision history

Table 10. Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete version
16-Aug-2006	4	New template, no content change
09-Oct-2006	5	Corrected order code
28-Mar-2010	6	Corrected *Table 1: Device summary*

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