STD8N80K5, STF8N80K5, STFI8N80K5, STP8N80K5, STU8N80K5

N-channel 800 V, 0.76 Ω typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFET in a DPAK, TO-220FP, I²PAKFP, TO-220 and IPAK

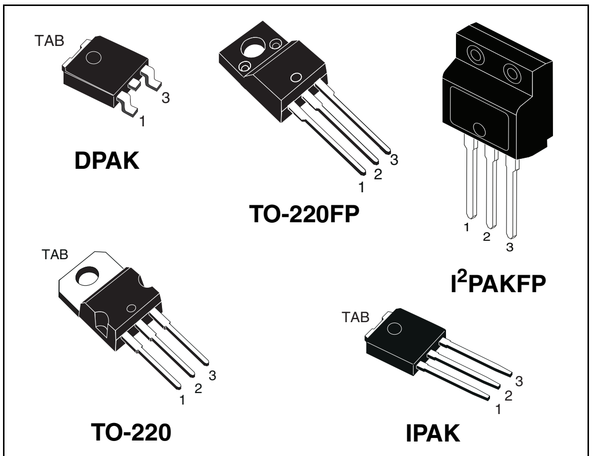
Datasheet — preliminary data

Features

Order codes	V_{DSS}	$R_{DS(on)}$max.	I_D	P_{TOT}
STD8N80K5	800 V	< 0.95 Ω	6 A	110 W
STF8N80K5			6 A (1)	25 W
STFI8N80K5			6 A	110 W
STP8N80K5				
STU8N80K5				

1. Limited by package.

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected



Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Figure 1. Internal schematic diagram

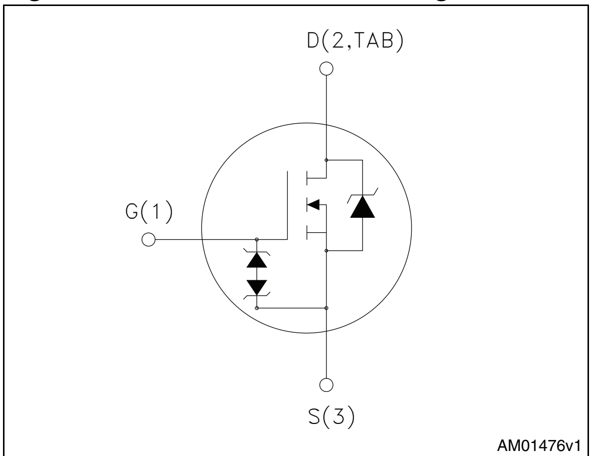


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD8N80K5	8N80K5	DPAK	Tape and reel
STF8N80K5		TO-220FP	Tube
STFI8N80K5		I²PAKFP	
STP8N80K5		TO-220	
STU8N80K5		IPAK	

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	I^2PAKFP TO-220FP	
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current T_C = 25 °C	6	6 (1)	A
I_D	Drain current T_C = 100 °C	4	4 (1)	A
I_{DM} (2)	Drain current (pulsed)	24	24 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	25	W
I_{AR} (3)	Max current during repetitive or single pulse avalanche	TBD		A
E_{AS} (4)	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	TBD		mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;T_C=25 °C)		2500	V
dv/dt (5)	Peak diode recovery voltage slope	4.5		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

1. Limited by package.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_{Jmax}.
4. Starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V
5. I_{SD} ≤ 6 A, di/dt ≤ 100 A/µs, V_{Peak} ≤ $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	DPAK	IPAK	I^2PAKFP TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max.	1.14			5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max.	62.5		100	62.5	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-pcb max.		50			°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 800 V, V_{DS} = 800 V, Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 3 A		0.76	0.95	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	450 30 1.6	-	pF pF pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 640 V	-	45	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	19	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 640 V, I_D = 6 A V_{GS} =10 V *(see Figure 3)*	-	13 3 7	-	nC nC nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 400 V, I_D = 3 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 5)*	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		6 24	A A
V_{SD}(1)	Forward on voltage	I_{SD}= 6 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 6 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 4)*	-	372 4 22		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 6 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C *(see Figure 4)*	-	522 5 20		ns µC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30	-		V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

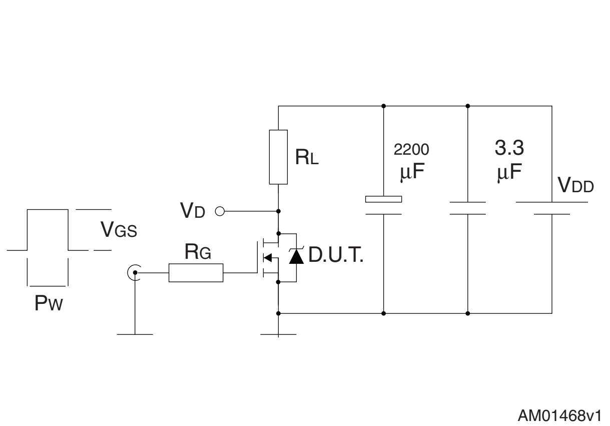


Figure 3. Gate charge test circuit

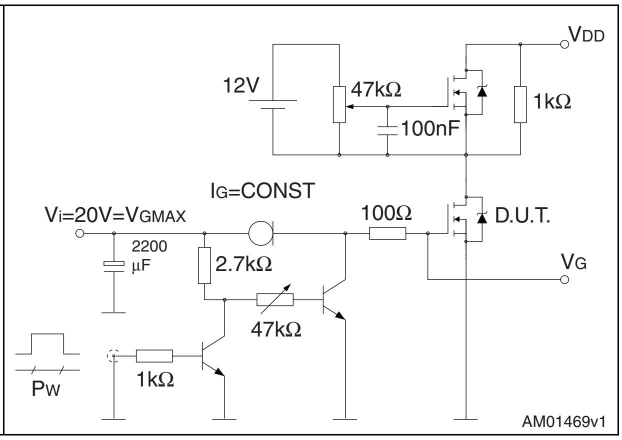


Figure 4. Test circuit for inductive load switching and diode recovery times

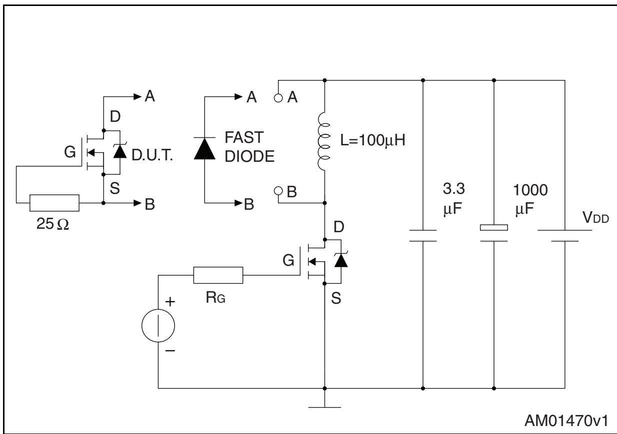


Figure 5. Unclamped inductive load test circuit

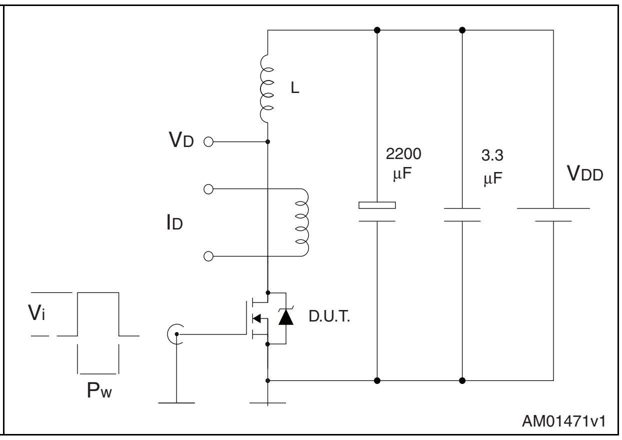


Figure 6. Unclamped inductive waveform

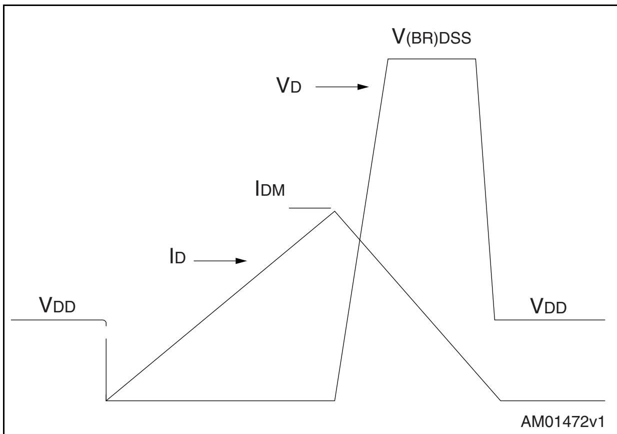
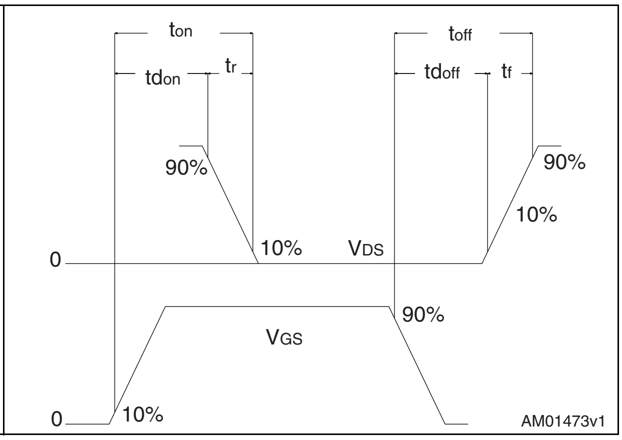


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 8. DPAK (TO-252) drawing

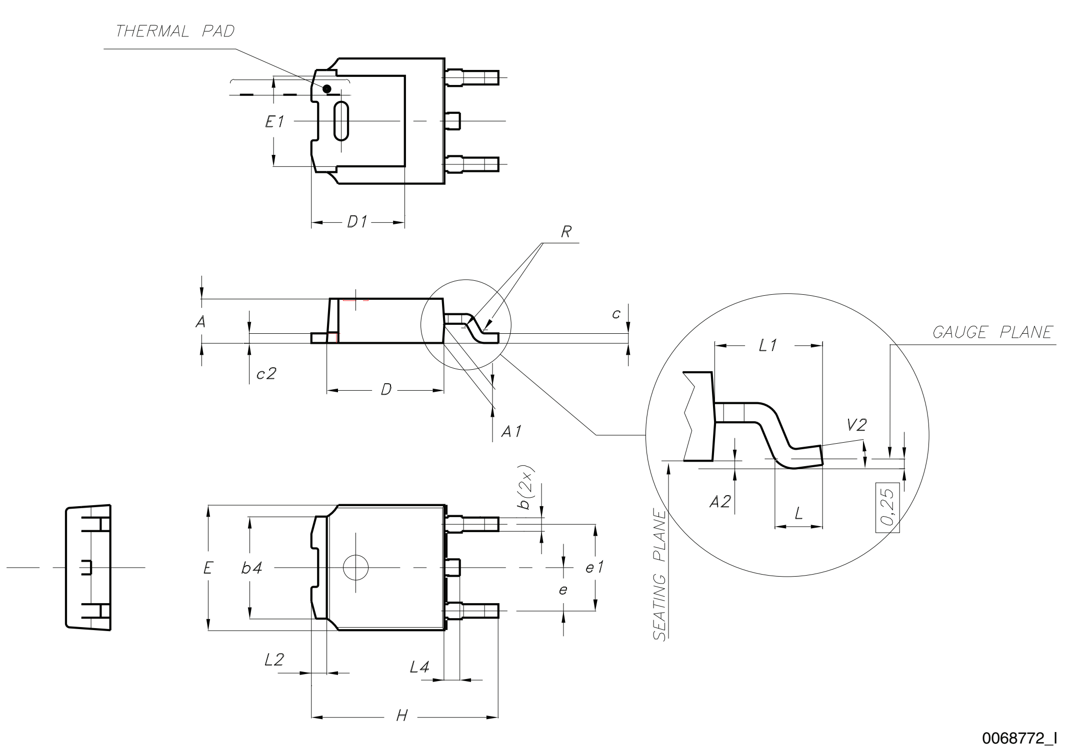
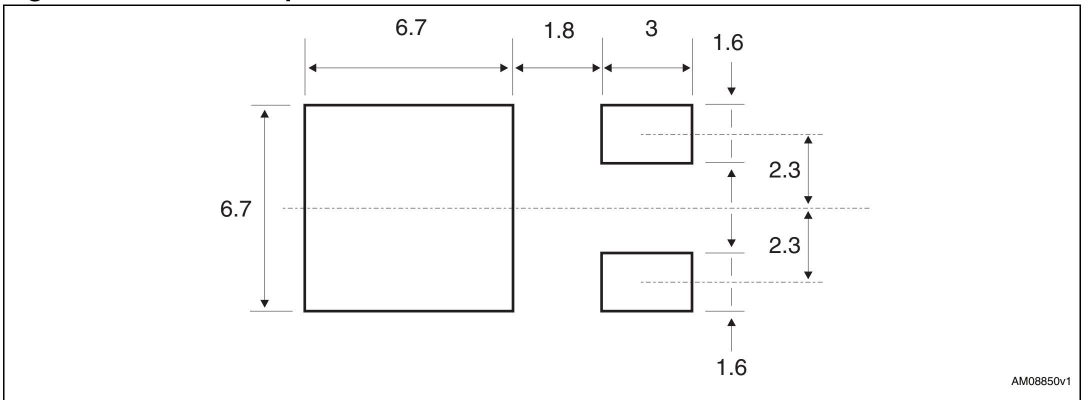


Figure 9. DPAK footprint[(a)]



a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 10. TO-220FP drawing

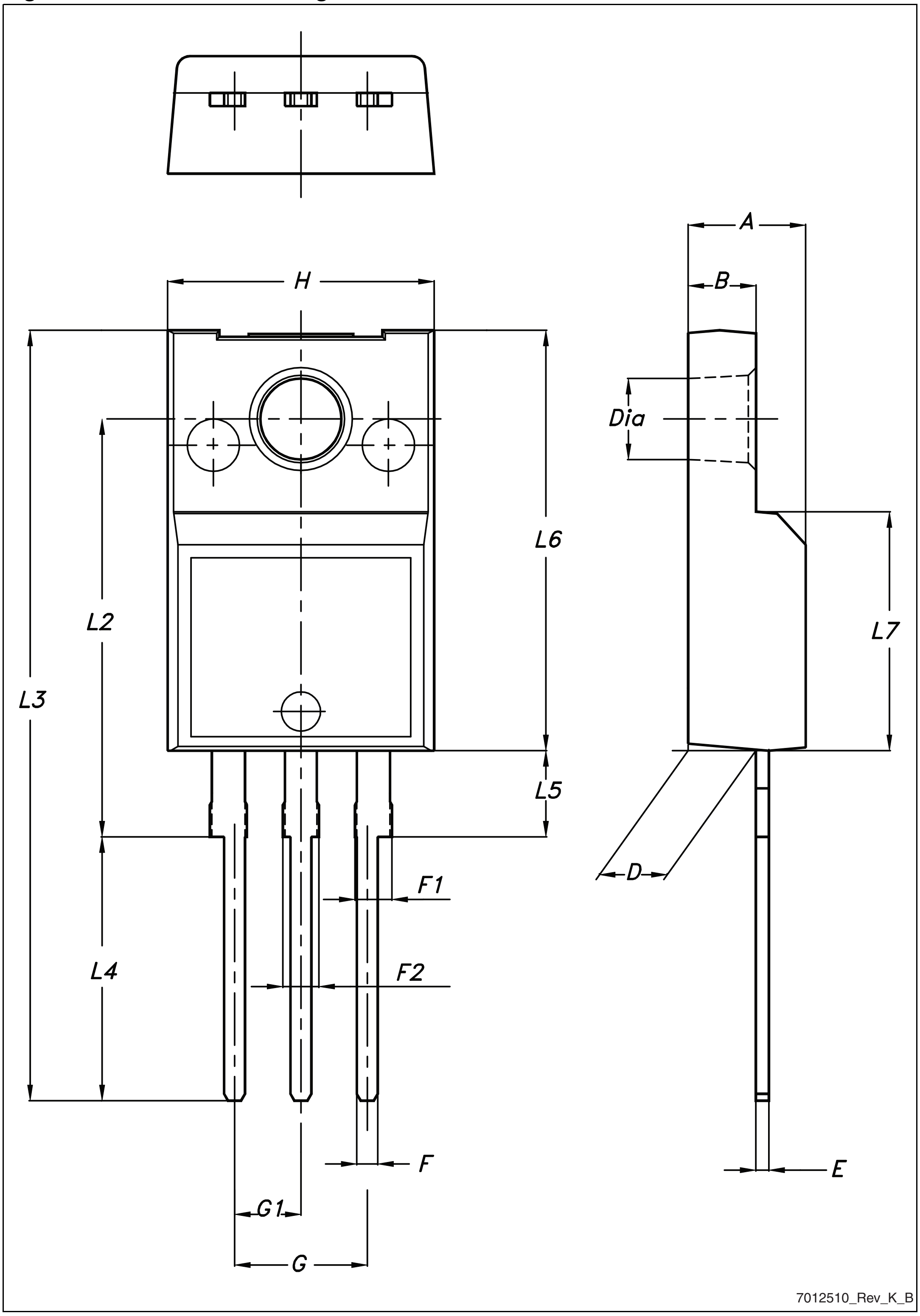


Table 11. I^2PAKFP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 11. I^2PAKFP drawing

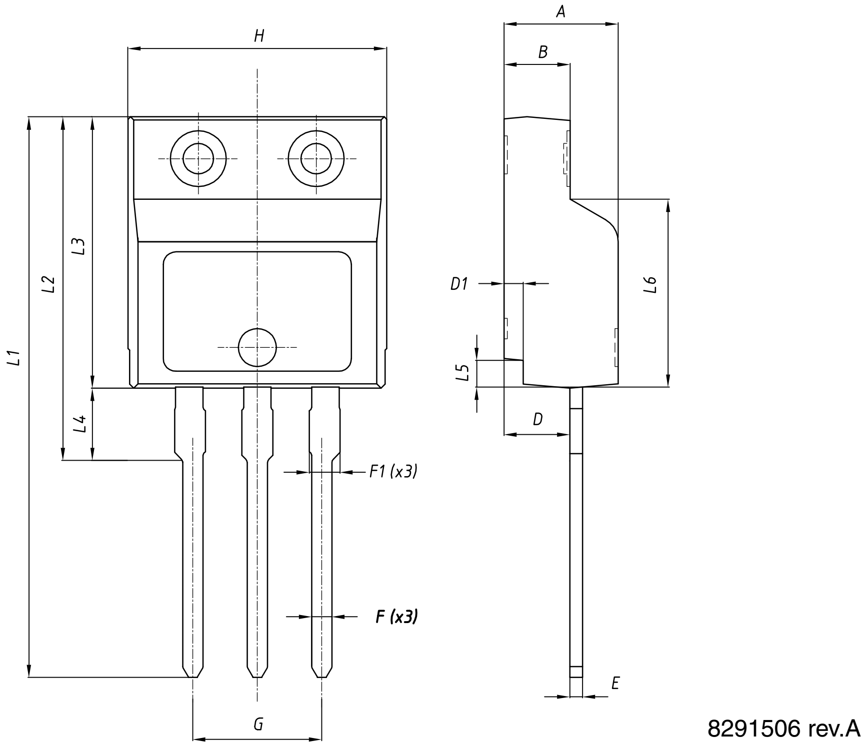


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 12. TO-220 type A drawing

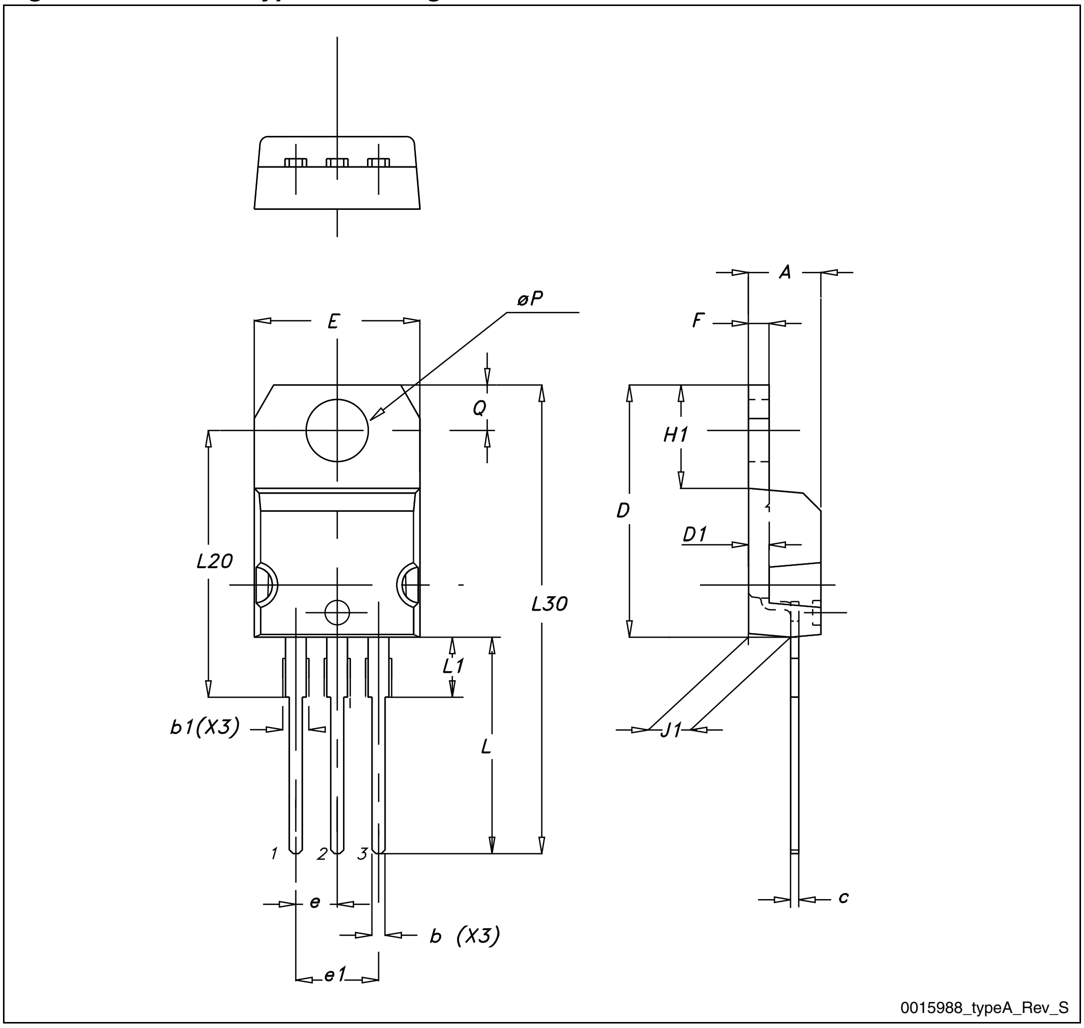
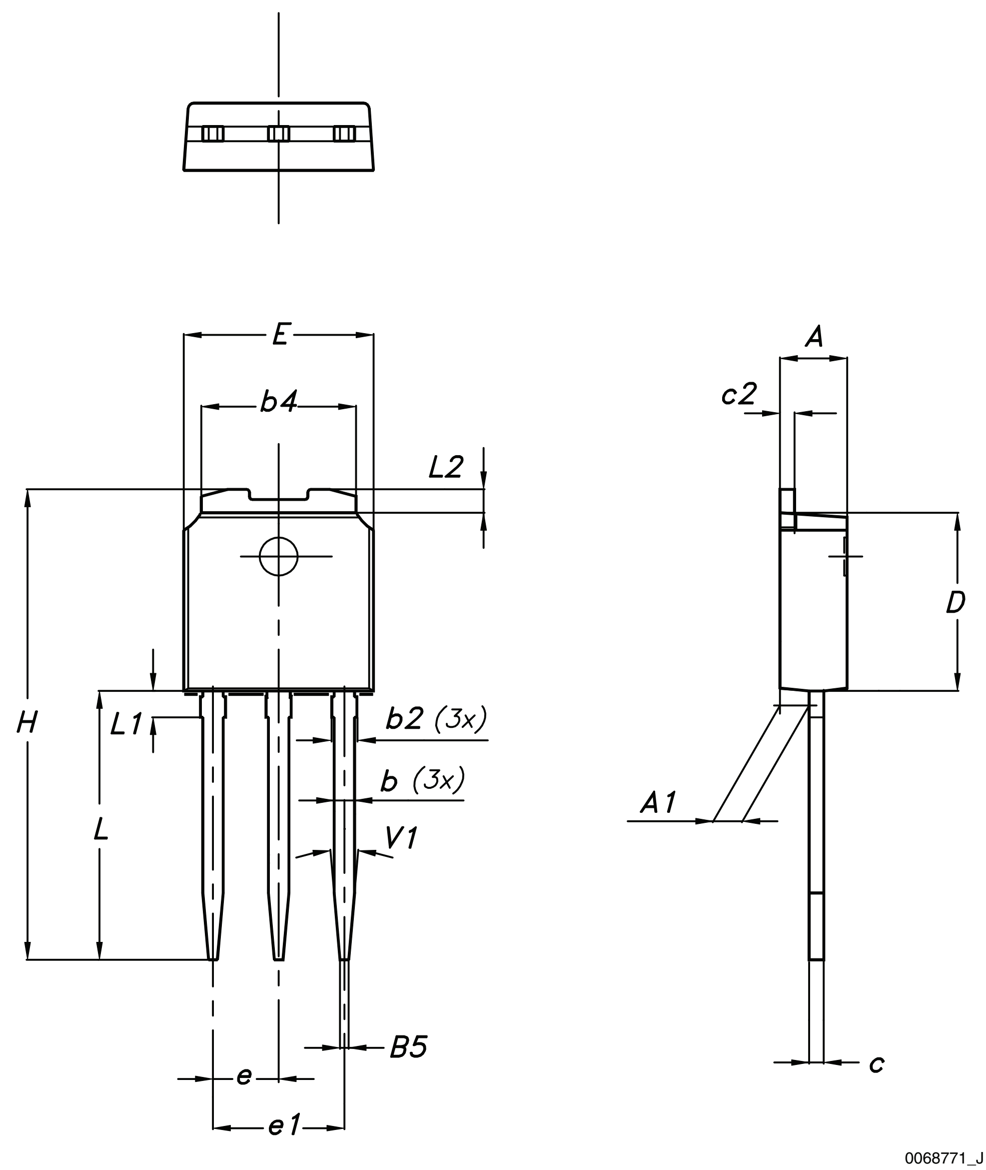


Table 13. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 13. IPAK (TO-251) drawing



5 Packaging mechanical data

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 14. Tape for DPAK (TO-252)

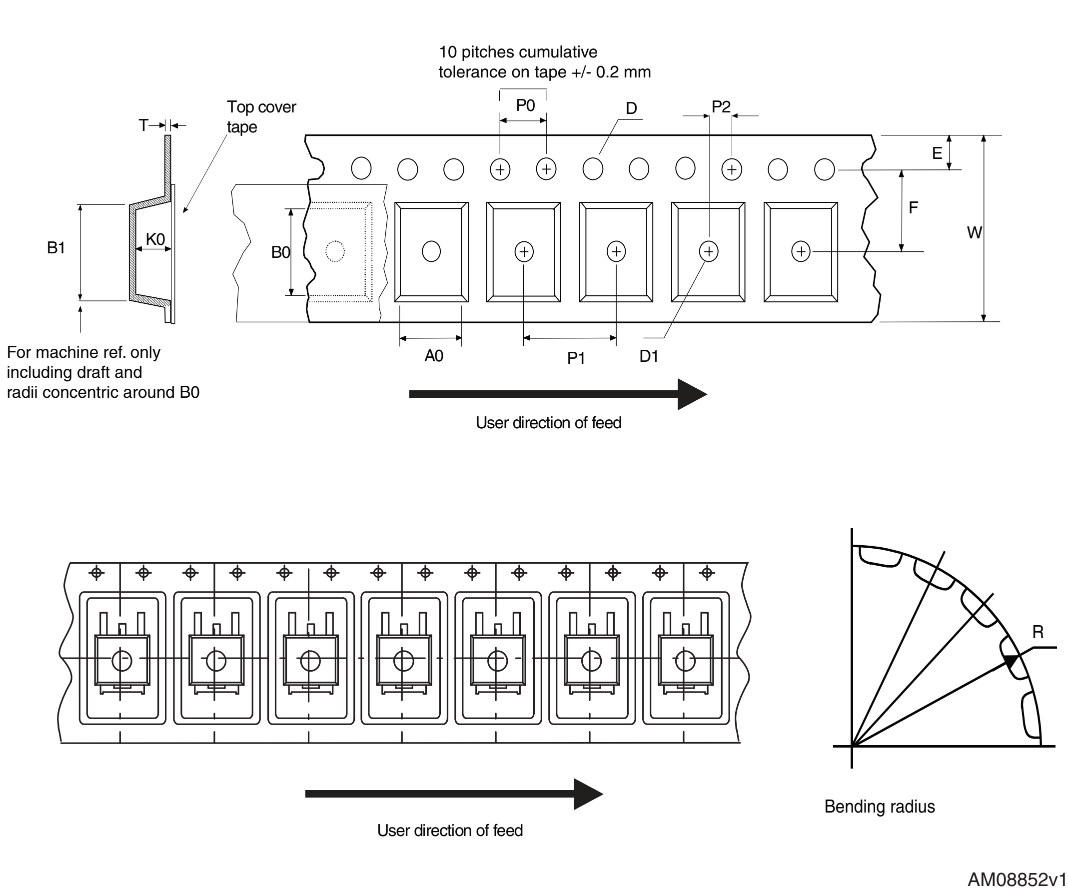
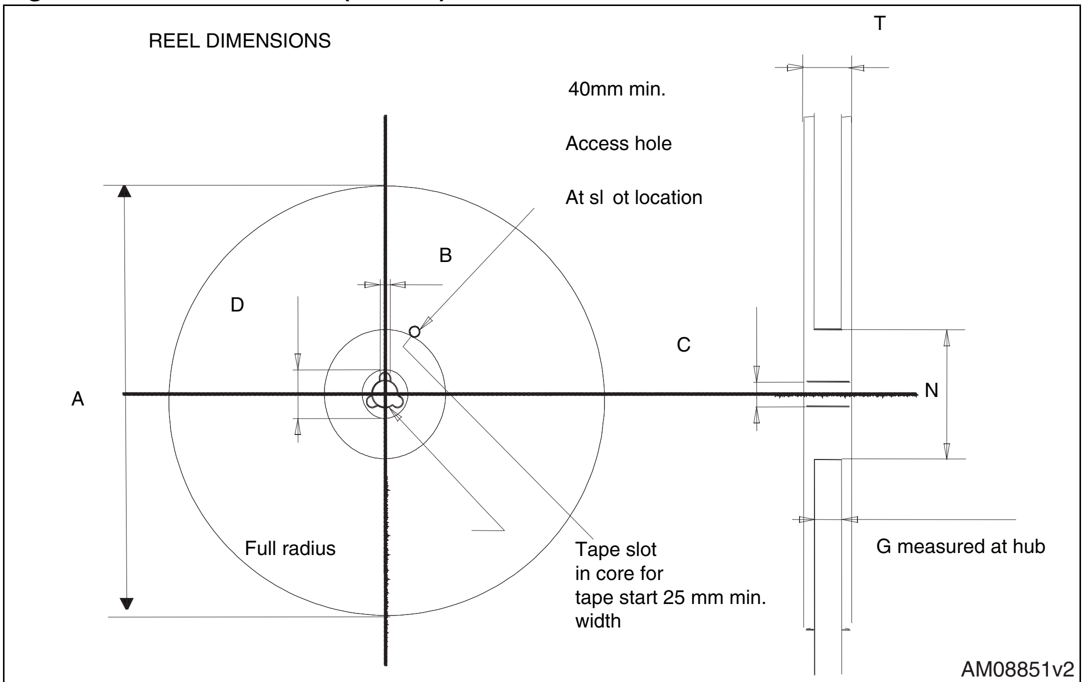


Figure 15. Reel for DPAK (TO-252)



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
06-Aug-2012	1	First release.
16-Oct-2012	2	– Minor text changes in cover page – Updatd: PTOT value for DPAK, TO-220 and IPAK in *Table 2*, $R_{thj\text{-}case}$ value for DPAK in *Table 3*, VSD value in *Table 7* – Deleted T_l in *Table 3* – Updated *Section 4: Package mechanical data* for DPAK and IPAK