



STD8N80K5, STF8N80K5, STFI8N80K5, STP8N80K5, STU8N80K5

N-channel 800 V, 0.76 Ω typ., 6 A Zener-protected SuperMESH™ 5 Power MOSFET in a DPAK, TO-220FP, I²PAKFP, TO-220 and IPAK

Datasheet — preliminary data

Features

Order codes	V _{DSS}	R _{DS(on)} max.	I _D	P _{TOT}
STD8N80K5	800 V	< 0.95 Ω	6 A	110 W
STF8N80K5			6 A ⁽¹⁾	25 W
STFI8N80K5			6 A	110 W
STP8N80K5			6 A	110 W
STU8N80K5			6 A	110 W

1. Limited by package.

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STD8N80K5	8N80K5	DPAK	Tape and reel
STF8N80K5		TO-220FP	Tube
STFI8N80K5		I ² PAKFP	
STP8N80K5		TO-220	
STU8N80K5		IPAK	

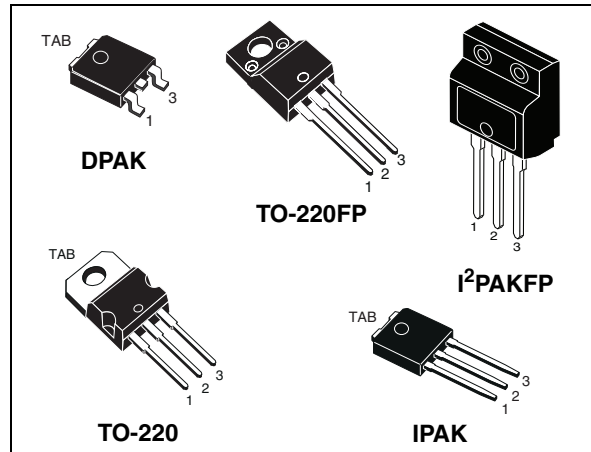
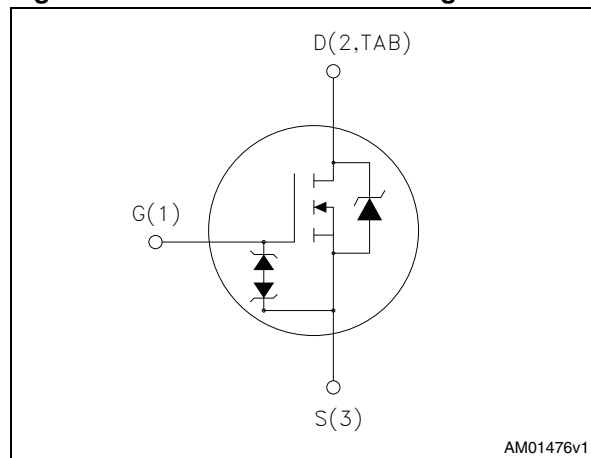


Figure 1. Internal schematic diagram



Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuits	6
4	Package mechanical data	7
5	Packaging mechanical data	17
6	Revision history	19

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK, TO-220, IPAK	I ² PAKFP TO-220FP	
V _{GS}	Gate-source voltage	± 30		V
I _D	Drain current T _C = 25 °C	6	6 ⁽¹⁾	A
I _D	Drain current T _C = 100 °C	4	4 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	24	24 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	25	W
I _{AR} ⁽³⁾	Max current during repetitive or single pulse avalanche	TBD		A
E _{AS} ⁽⁴⁾	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	TBD		mJ
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
dv/dt ⁽⁵⁾	Peak diode recovery voltage slope	4.5		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	- 55 to 150		°C

- Limited by package.
- Pulse width limited by safe operating area.
- Pulse width limited by T_{Jmax}.
- Starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V
- I_{SD} ≤ 6 A, di/dt ≤ 100 A/μs, V_{Peak} ≤ V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	DPAK	IPAK	I ² PAKFP TO-220FP	
R _{thj-case}	Thermal resistance junction-case max.	1.14			5	°C/W
R _{thj-amb}	Thermal resistance junction-amb max.	62.5		100	62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max.		50			°C/W

- When mounted on 1inch² FR-4 board, 2 oz Cu

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	800			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 800\text{ V}$, $V_{DS} = 800\text{ V}$, $T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$		0.76	0.95	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance			450		pF
C_{oss}	Output capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	30	-	pF
C_{rss}	Reverse transfer capacitance			1.6		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }640\text{ V}$	-	45	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			19		
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	7	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 6\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3)	-	13	-	nC
Q_{gs}	Gate-source charge			3		
Q_{gd}	Gate-drain charge			7		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 3\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 5)	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}	Source-drain current (pulsed)				24	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 4)	-	372		ns
Q_{rr}	Reverse recovery charge			4		μC
I_{RRM}	Reverse recovery current			22		A
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 4)	-	522		ns
Q_{rr}	Reverse recovery charge			5		μC
I_{RRM}	Reverse recovery current			20		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} \pm 1\text{ mA}$, (open drain)	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

3 Test circuits

Figure 2. Switching times test circuit for resistive load

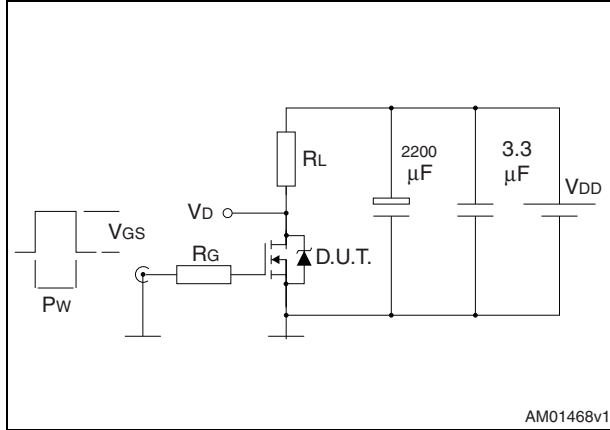


Figure 3. Gate charge test circuit

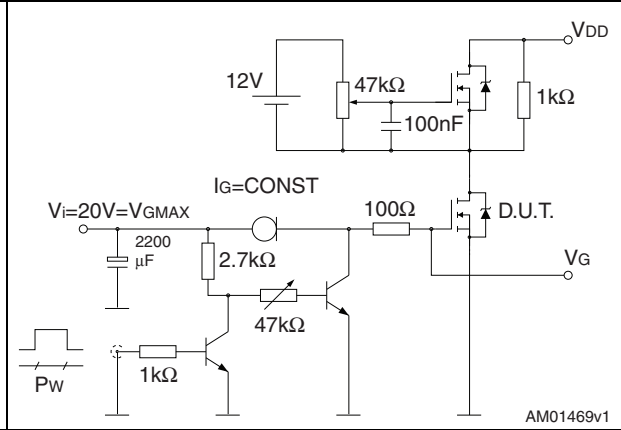


Figure 4. Test circuit for inductive load switching and diode recovery times

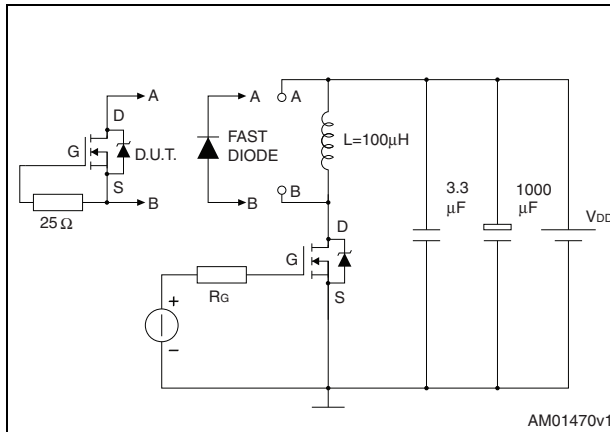


Figure 5. Unclamped inductive load test circuit

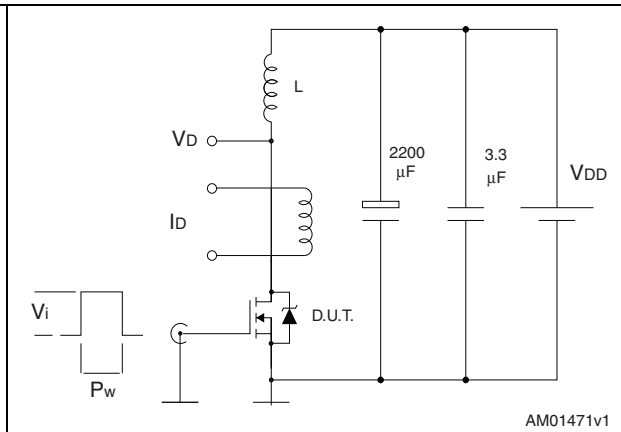


Figure 6. Unclamped inductive waveform

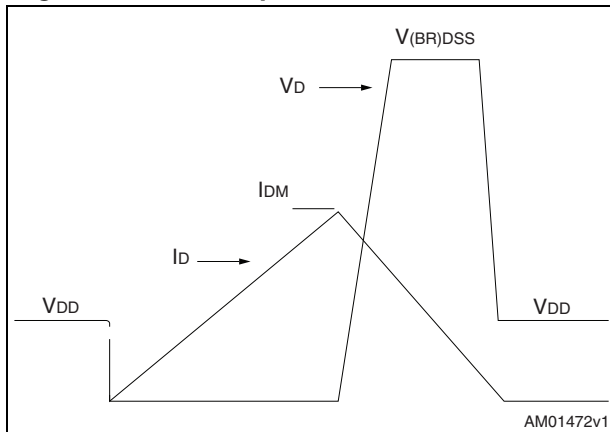
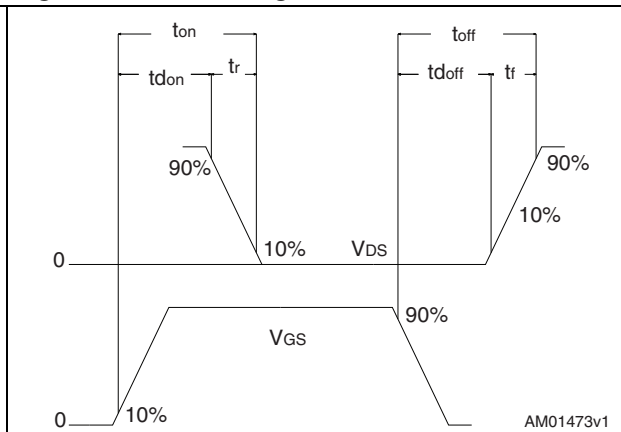


Figure 7. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 8. DPAK (TO-252) drawing

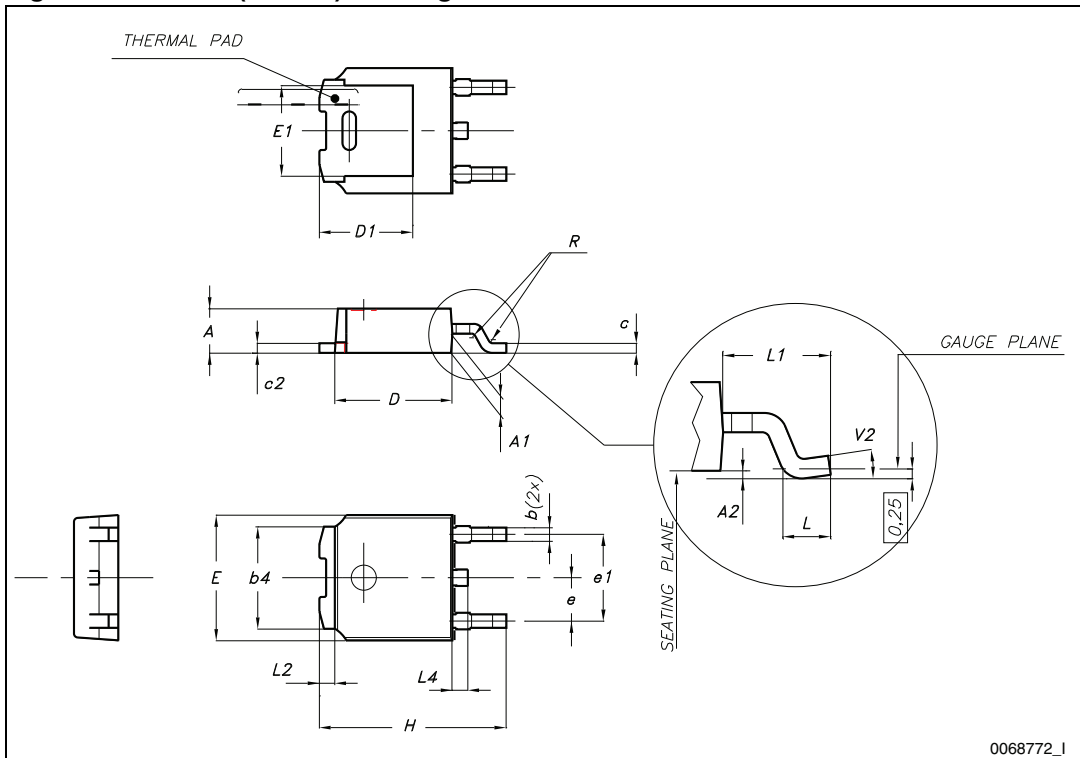
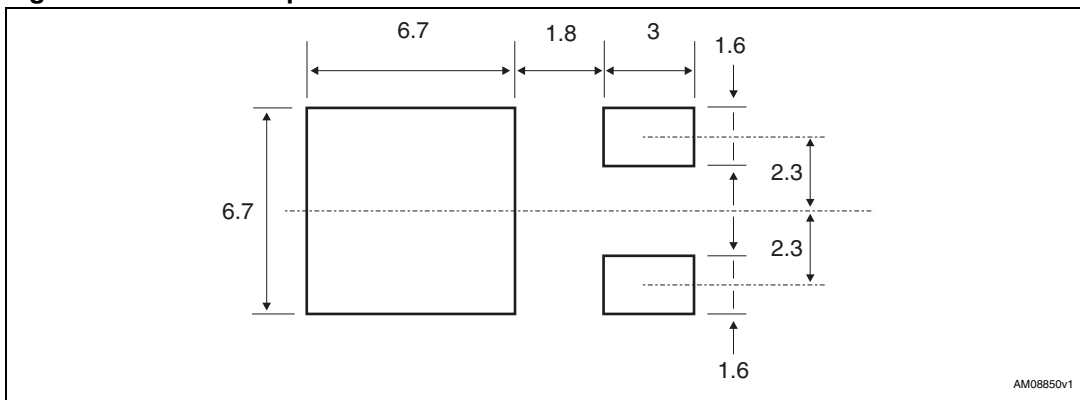


Figure 9. DPAK footprint(a)

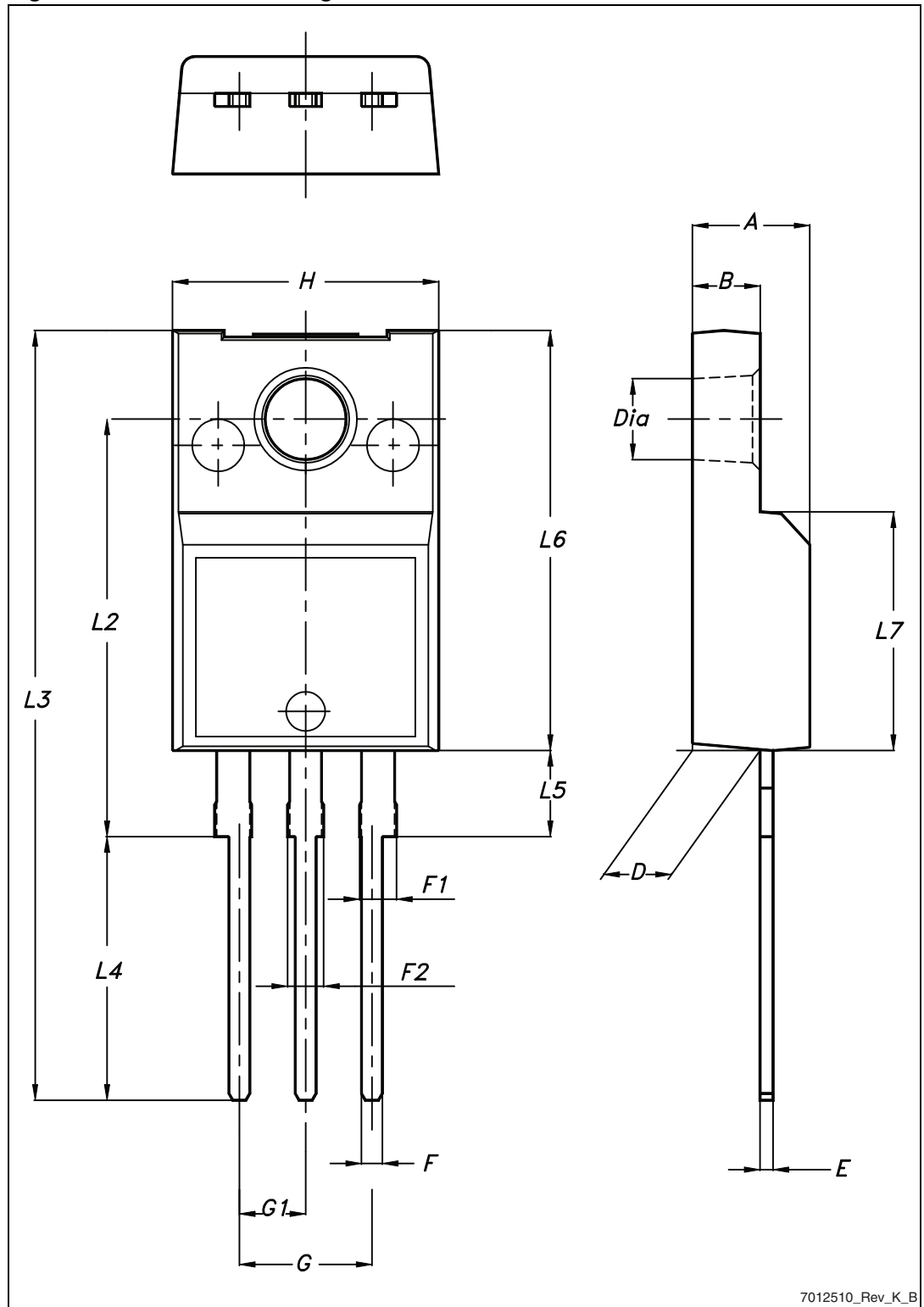


a. All dimensions are in millimeters

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 10. TO-220FP drawing



7012510_Rev_K_B

Table 11. I²PAKFP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 11. I²PAKFP drawing

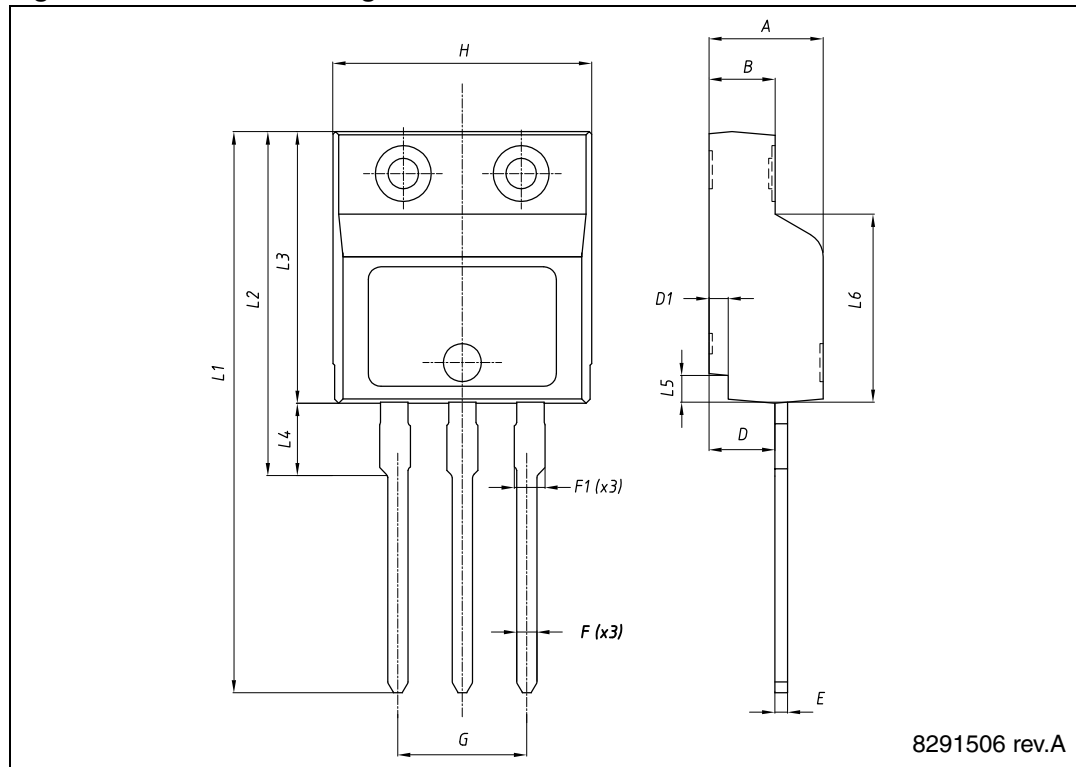


Table 12. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 12. TO-220 type A drawing

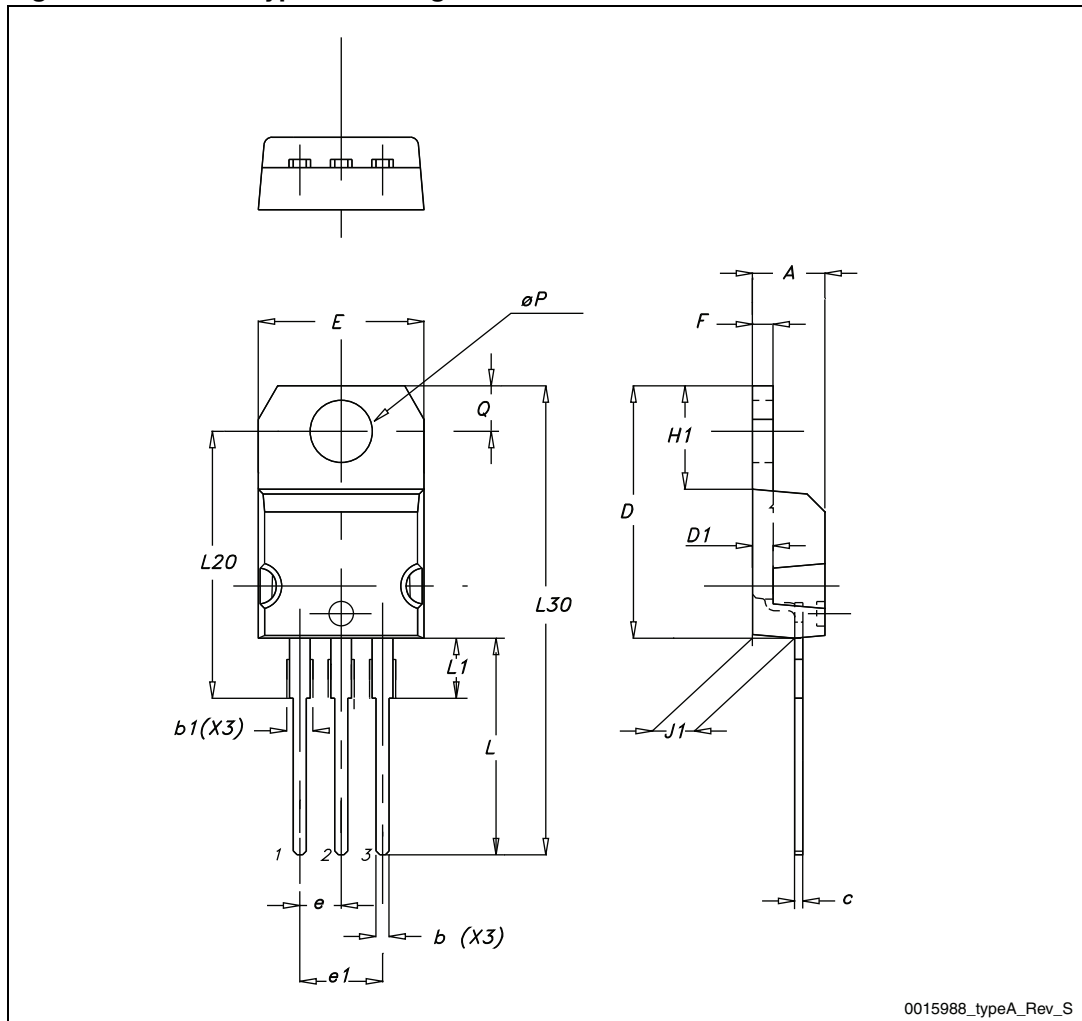
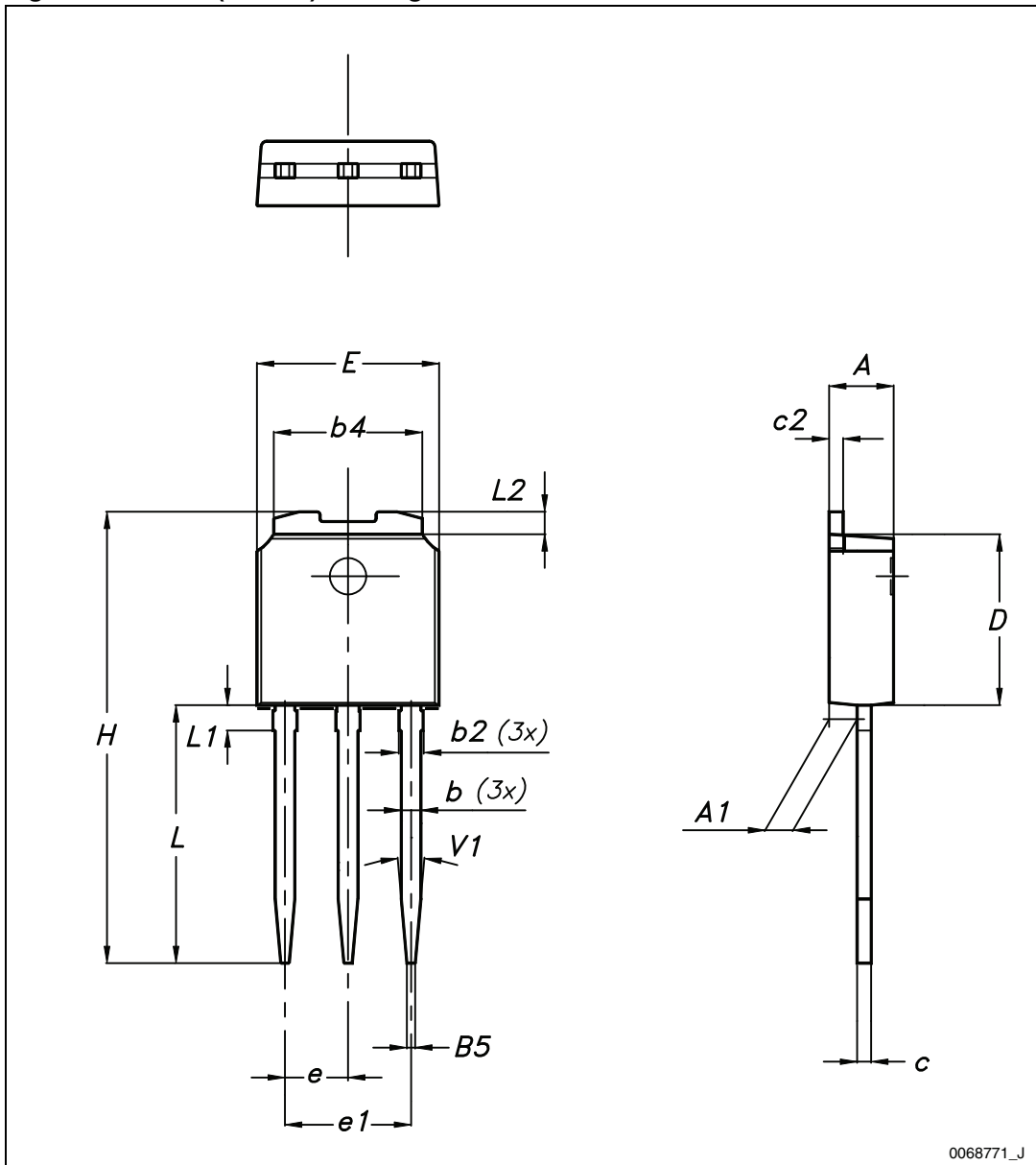


Table 13. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 13. IPAK (TO-251) drawing



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5 Packaging mechanical data

Table 14. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 14. Tape for DPAK (TO-252)

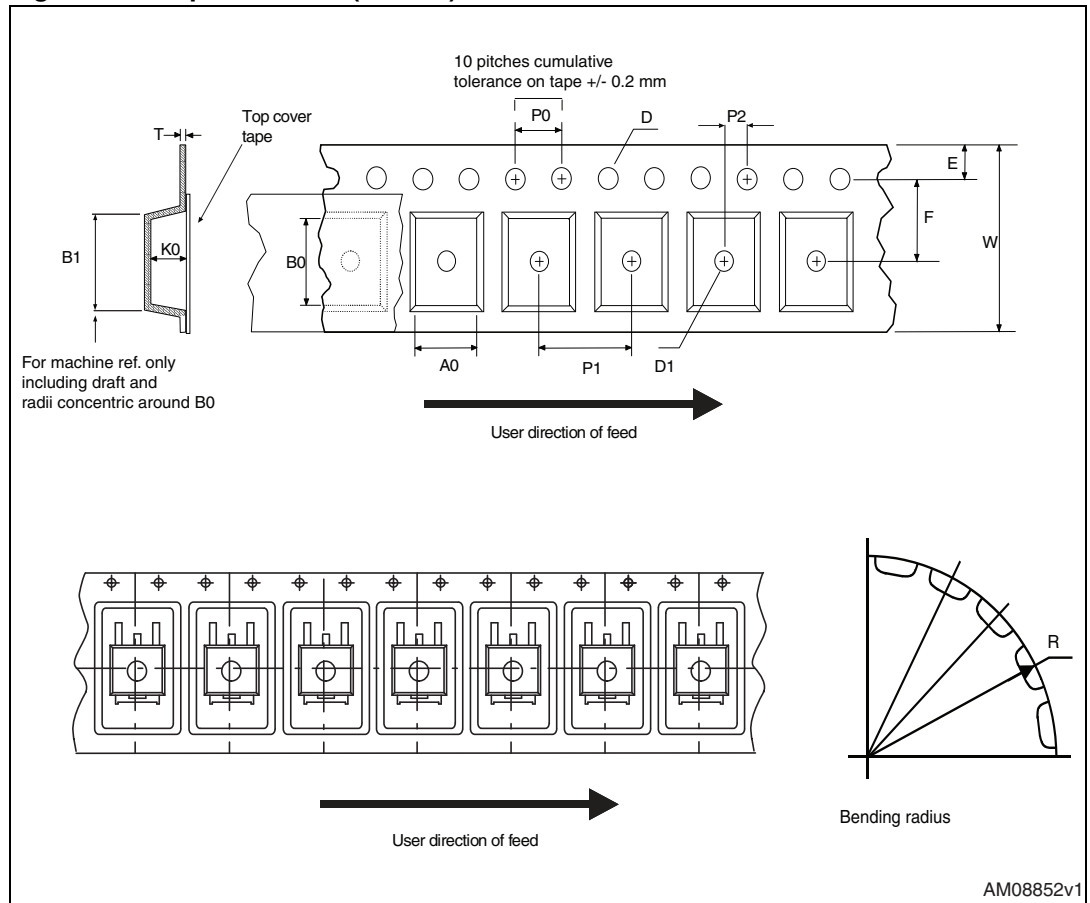
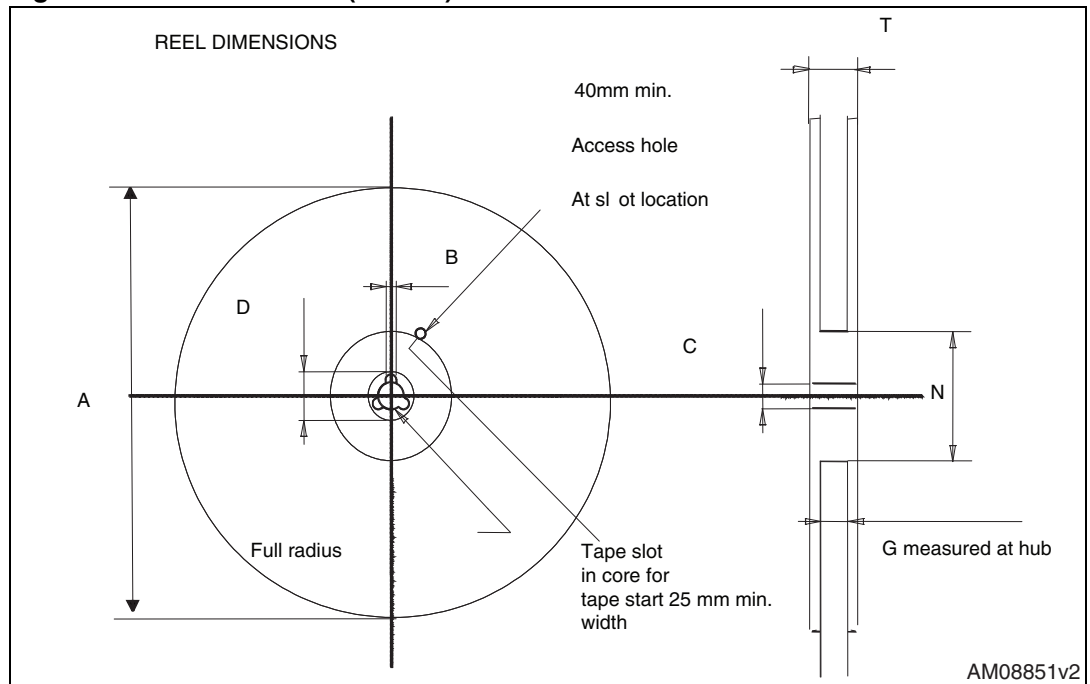


Figure 15. Reel for DPAK (TO-252)



6 Revision history

Table 15. Document revision history

Date	Revision	Changes
06-Aug-2012	1	First release.
16-Oct-2012	2	<ul style="list-style-type: none">– Minor text changes in cover page– Updated: PTOT value for DPAK, TO-220 and IPAK in Table 2, $R_{thj-case}$ value for DPAK in Table 3, VSD value in Table 7– Deleted T_1 in Table 3– Updated Section 4: Package mechanical data for DPAK and IPAK

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