



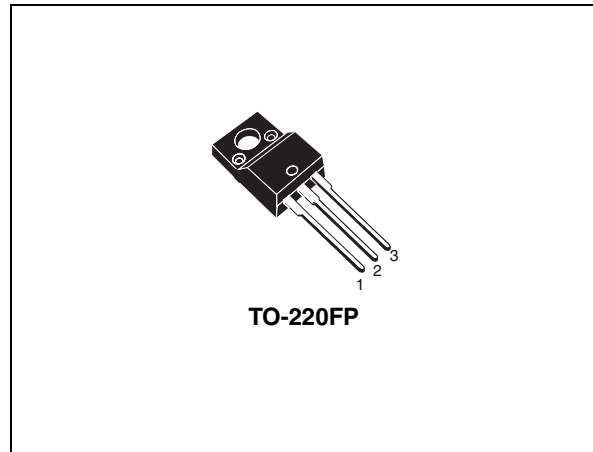
STF10N65K3

N-channel 650 V, 0.9 Ω , 10 A, TO-220FP
SuperMESH3™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D	P _w
STF10N65K3	650 V	< 1 Ω	10 A	35 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitances
- Improved diode reverse recovery characteristics
- Zener-protected



Application

- Switching applications

Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Figure 1. Internal schematic diagram

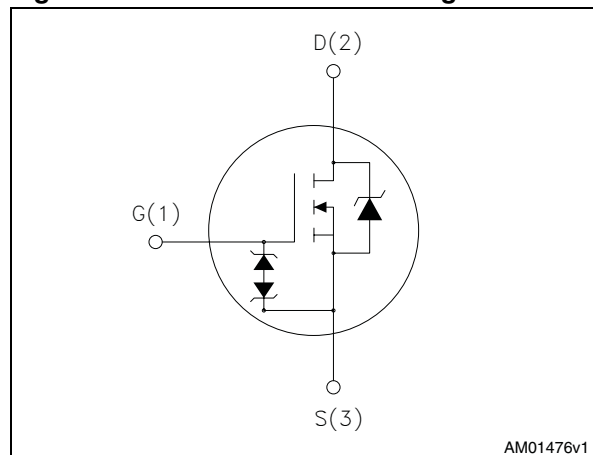


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF10N65K3	10N65K3	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	650	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	35	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	7.2	A
E_{AS}	Single pulse avalanche energy ⁽²⁾	212	mJ
	Derating factor	0.28	W/ $^\circ\text{C}$
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12	V/ns
$V_{ESD(G-S)}$	G-S ESD (HBM C=100 pF, R=1.5 k Ω)	2500	V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; $T_C=25\text{ }^\circ\text{C}$)	2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.
2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$
3. $I_{SD} \leq 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{Peak} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.57	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	650			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 650 V V _{DS} = 650 V, T _C = 125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3		4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 3.6 A			1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0	-	1180	-	pF
C _{oss}	Output capacitance			125		pF
C _{rss}	Reverse transfer capacitance			14		pF
C _{oss eq.}	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0	-	77	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	3	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 7.2 A, V _{GS} = 10 V (see Figure 16)	-	42	-	nC
Q _{gs}	Gate-source charge			7.4		nC
Q _{gd}	Gate-drain charge			23		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)		14.5		ns	
t_r	Rise time			14		ns	
$t_{d(off)}$	Turn-off-delay time				44		ns
t_f	Fall time				35		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				7.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28.8	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 20)		320		ns
Q_{rr}	Reverse recovery charge			2		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 20)		410		ns
Q_{rr}	Reverse recovery charge			2.9		μC
I_{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

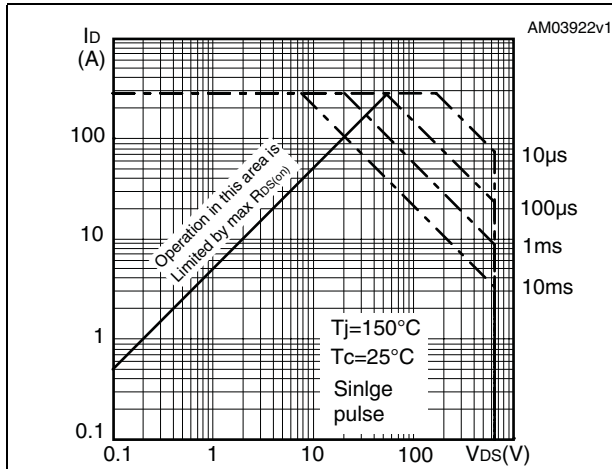


Figure 3. Thermal impedance

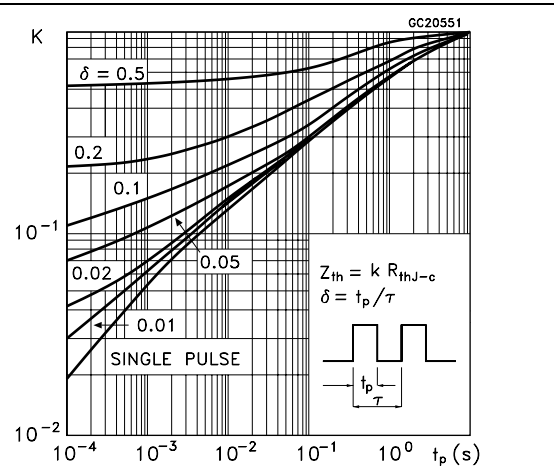


Figure 4. Output characteristics

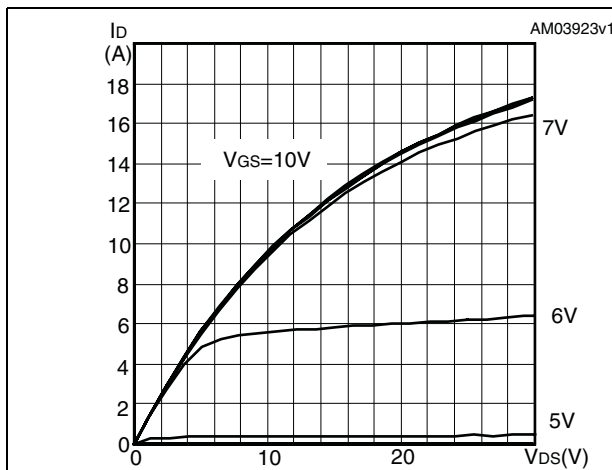


Figure 5. Transfer characteristics

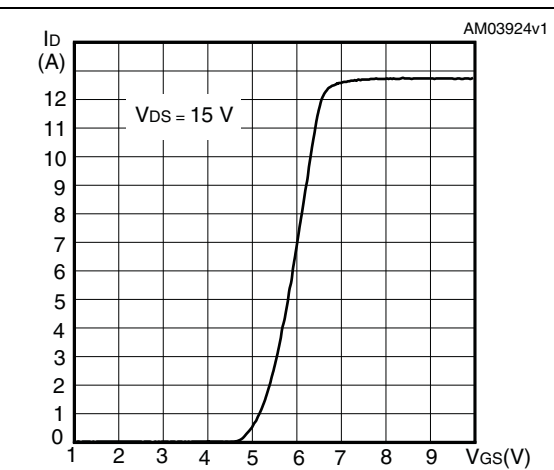


Figure 6. Normalized BV_{DSS} vs temperature

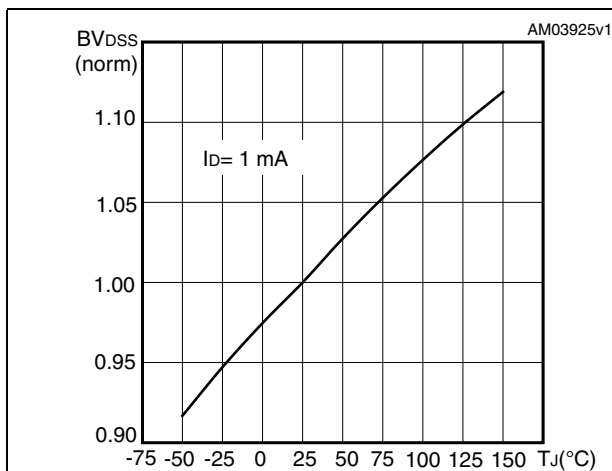


Figure 7. Static drain-source on resistance

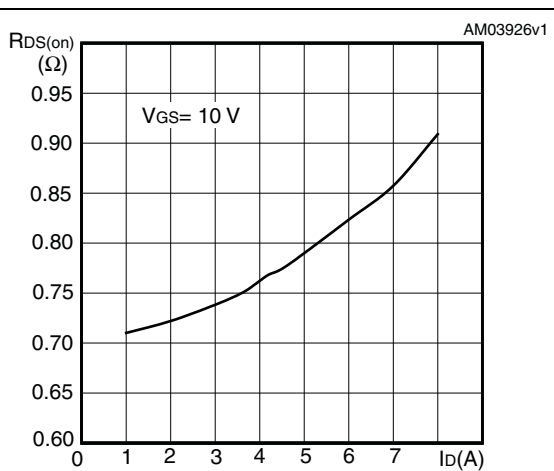


Figure 8. Output capacitance stored energy Figure 9. Capacitance variations

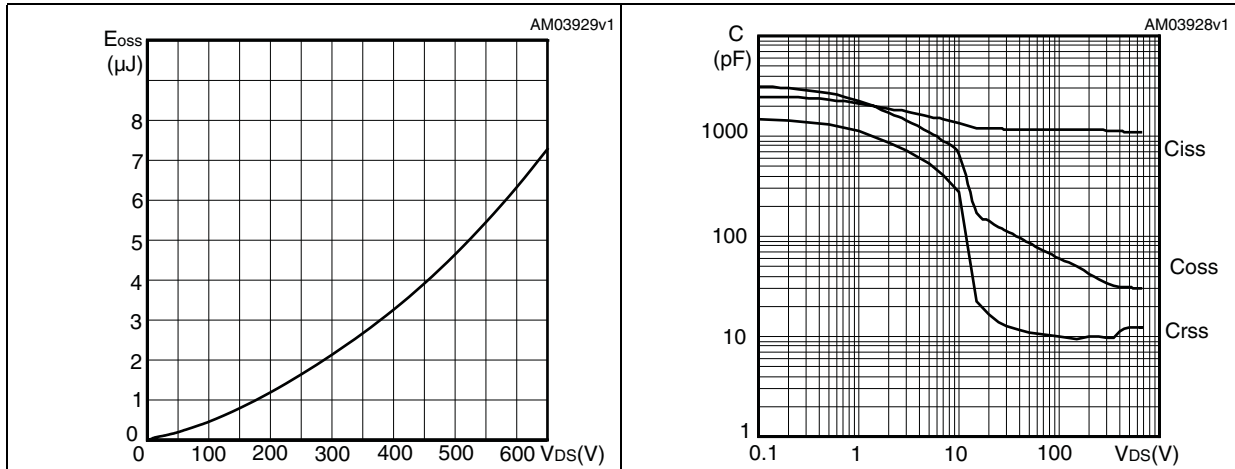


Figure 10. Gate charge vs gate-source voltage Figure 11. Normalized on resistance vs temperature

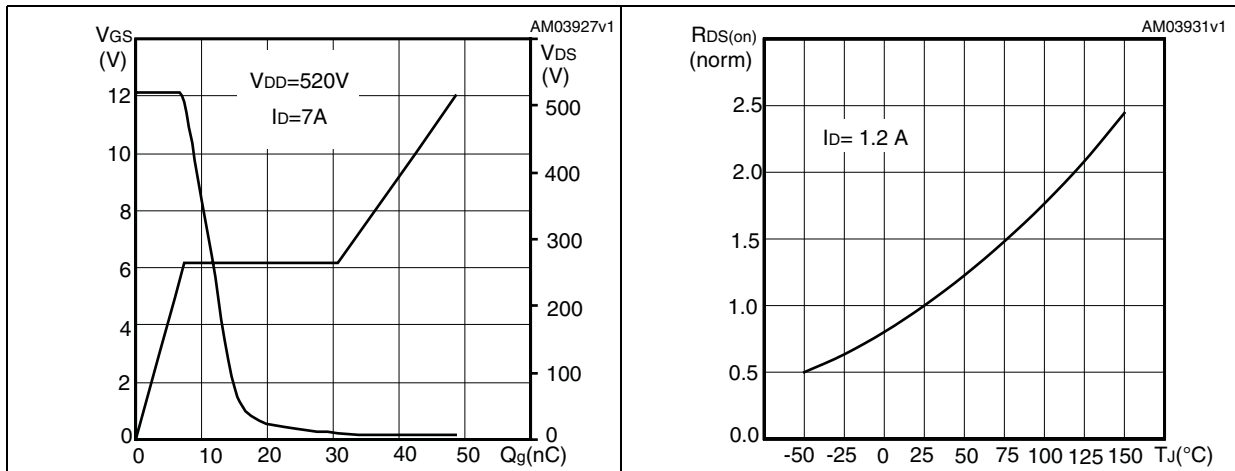


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Maximum avalanche energy vs temperature

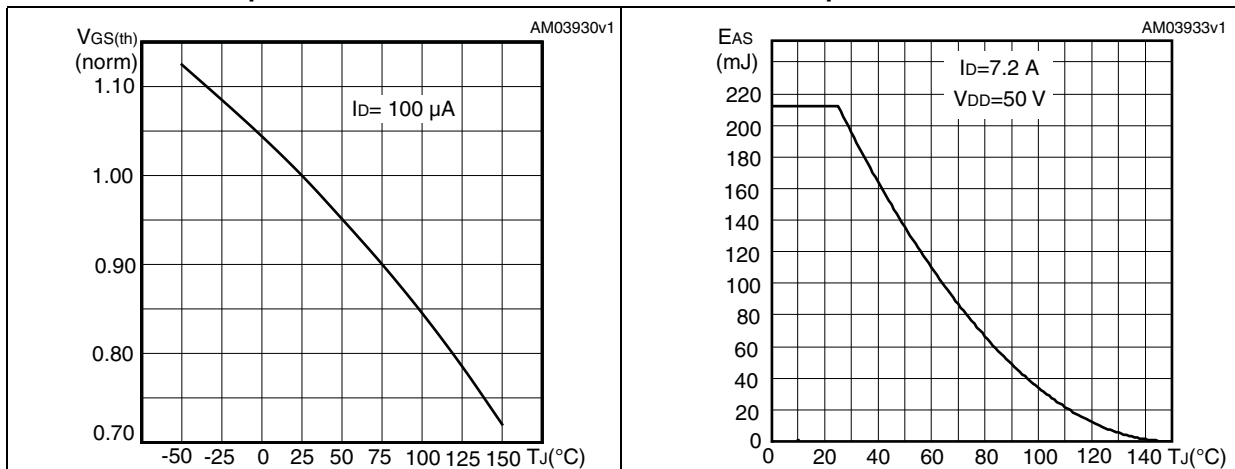
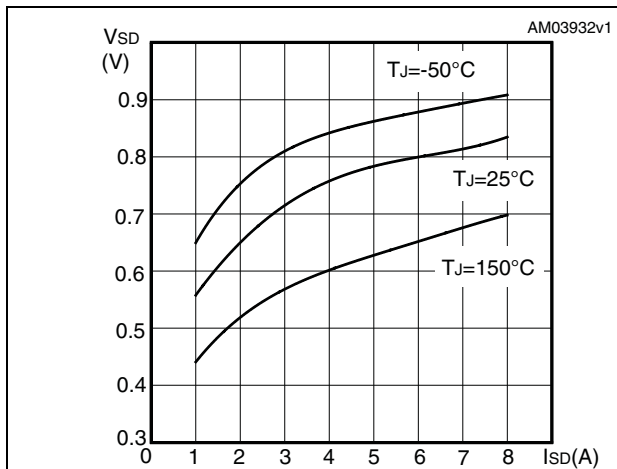


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

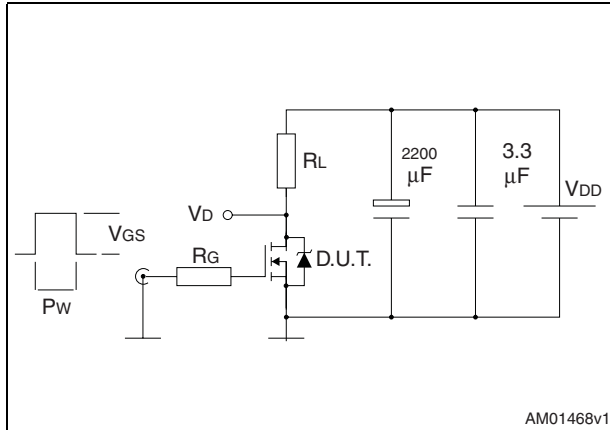


Figure 16. Gate charge test circuit

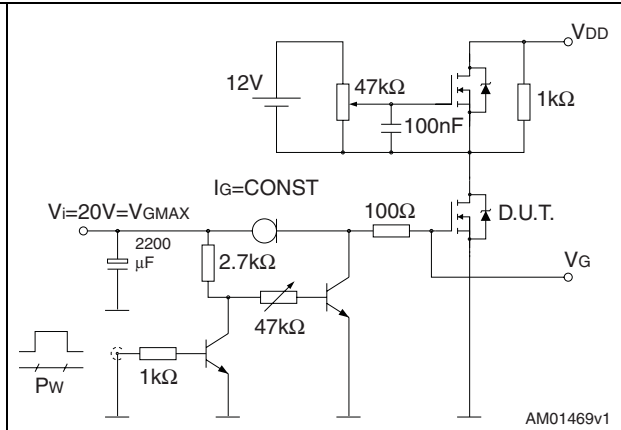


Figure 17. Test circuit for inductive load switching and diode recovery times

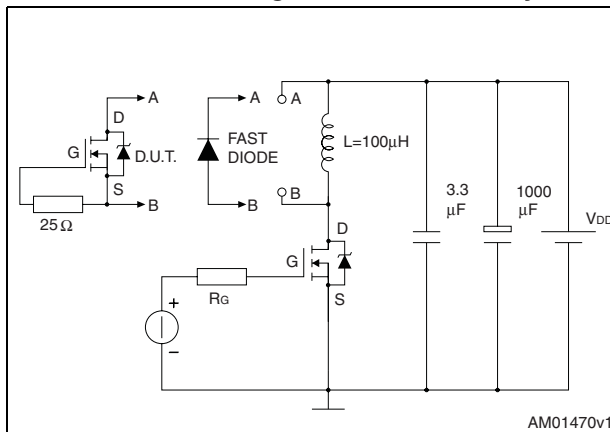


Figure 18. Unclamped inductive load test circuit

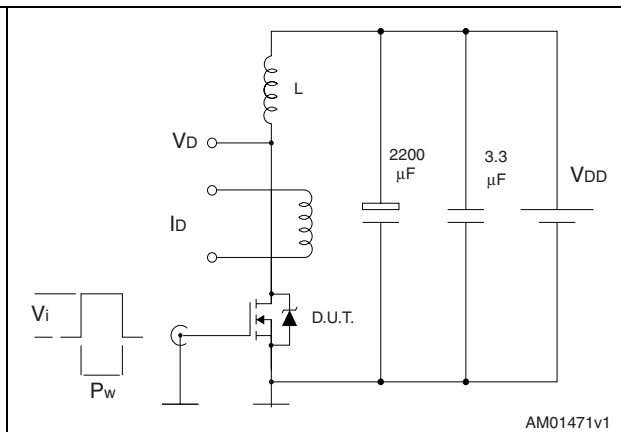


Figure 19. Unclamped inductive waveform

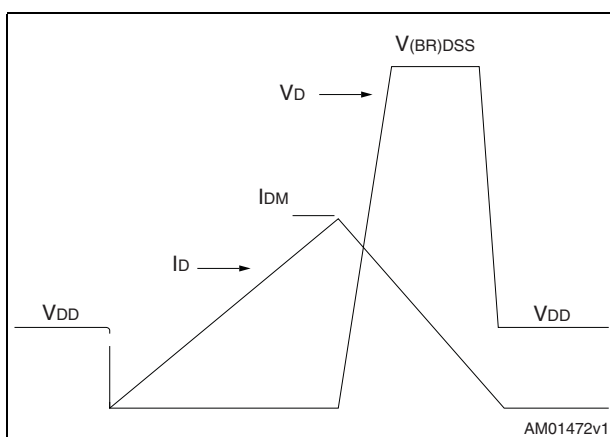
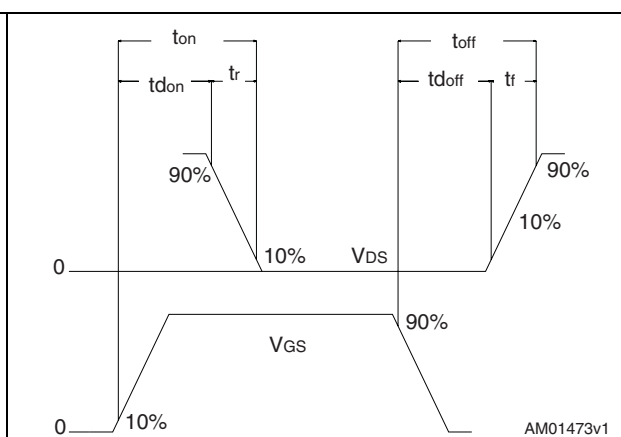


Figure 20. Switching time waveform



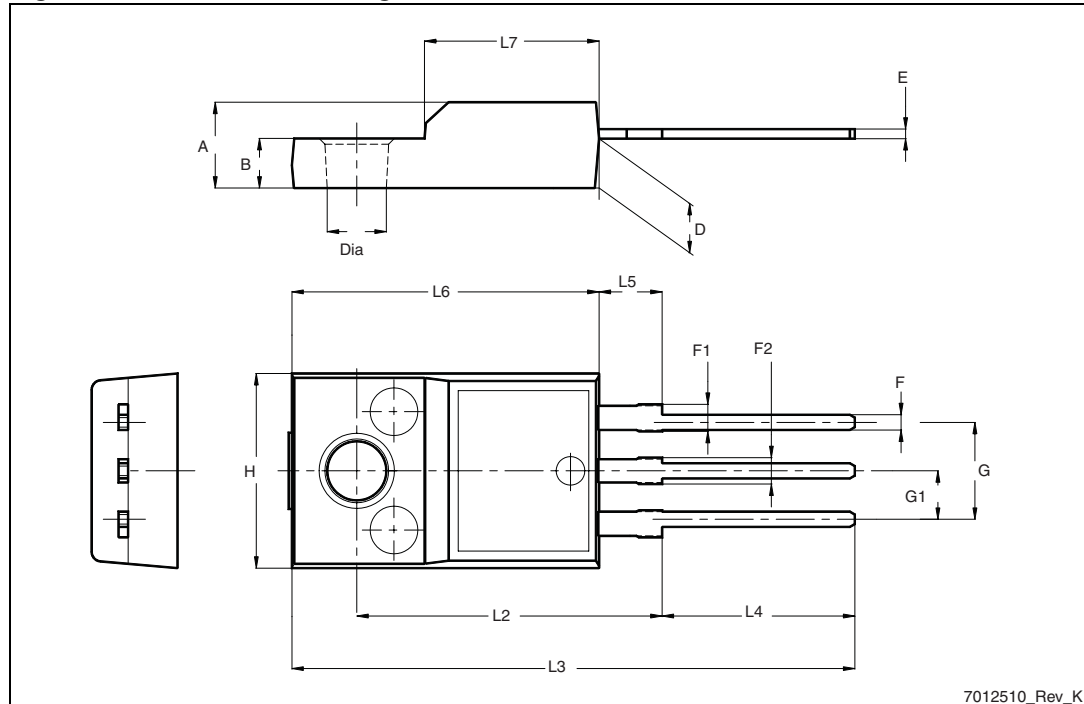
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 21. TO-220FP drawing



7012510_Rev_K

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
30-Jun-2009	1	First release
14-Nov-2011	2	Updated mechanical data and Section 2.1: Electrical characteristics (curves) . Minor text changes.

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