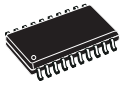
6 CHANNEL VOLUME CONTROLLER

1 FEATURES

- 6 CHANNEL INPUTS
- 6 CHANNEL OUTPUTS
- VOLUME ATTENUATION RANGE OF 0 TO -79dB
- VOLUME CONTROL IN 1.0dB STEPS
- 6 CHANNEL INDEPENDENT CONTROL
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

Figure 1. Package



SO-20

Table 1. Order Codes

Part Number	Package
TDA7448	SO-20
TDA744813TR	Tape & Reel

2 DESCRIPTION

The TDA7448 is a 6 channel volume controller for quality audio applications in Multi-Channels Audio Systems

Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

Figure 2. Block Diagram

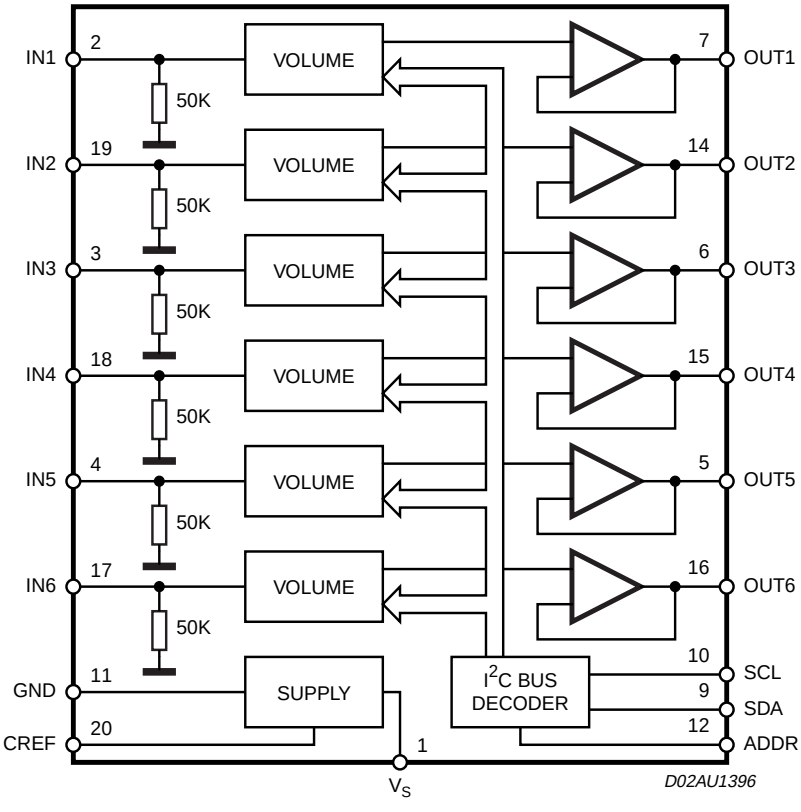


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	0 to 70	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

Figure 3. Pin Connection (Top view)

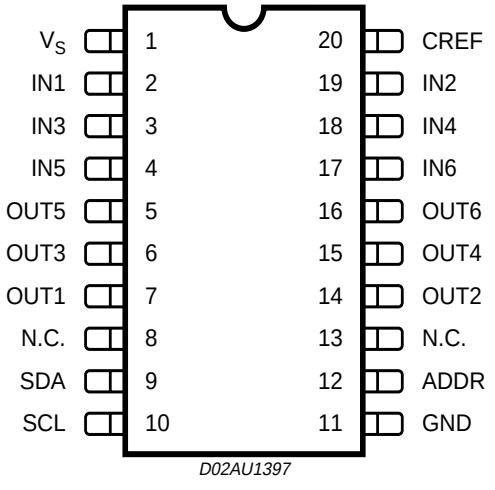


Table 3. Thermal Data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	thermal Resistance junction-pins	150	°C/W

Table 4. Quick Reference Data

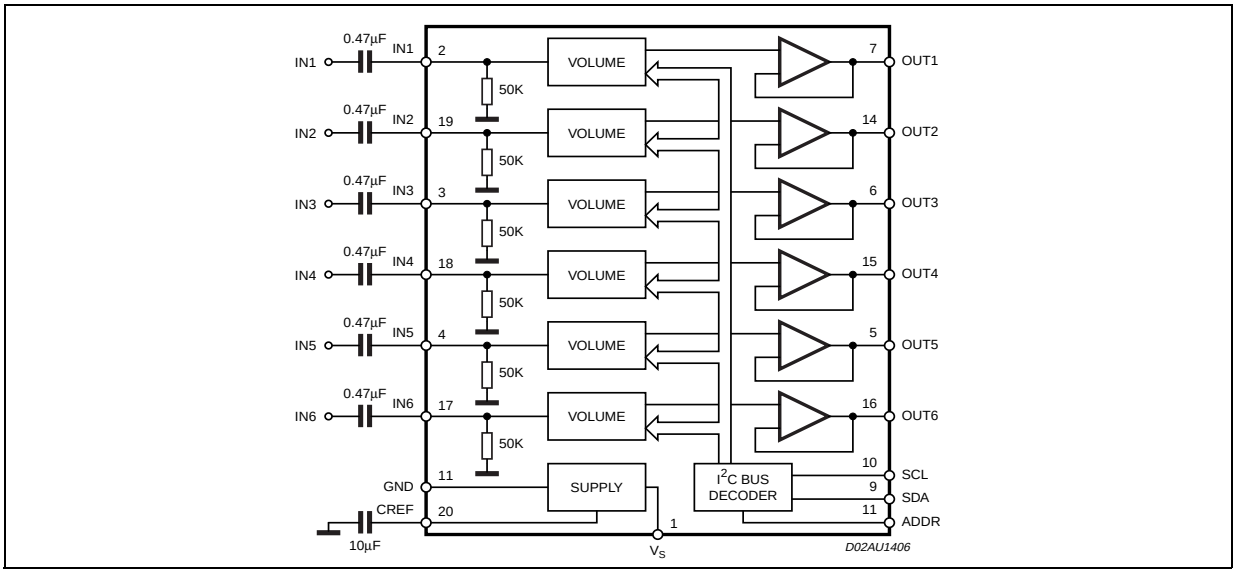
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	4.75	9	10	V
V_{CL}	Max Input Signal Handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f =1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio Vout = 1Vrms		100		dB
S_C	Channel Separation f = 1KHz		90		dB
	Volume Control (1dB step)	-79		0	dB
	Mute Attenuation		90		dB

Table 5. Electrical Characteristcs

(refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		4.75	9	10	V
I_S	Supply Current			7		mA
SVR	Ripple Rejection			80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		Vrms
S_{IN}	Input Separation	The selected input is grounded through a 2.2µ capacitor		90		dB
VOLUME CONTROL						
C_{RANGE}	Control Range			79		dB
A_{VMAX}	Max. Attenuation			79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	A_V = 0 to -24dB	-1	0	1	dB
		A_V = -24 to -79dB	-2.0	0	2.0	dB
E_T	Tracking Error	A_V = 0 to -24dB	-1	0	1	dB
		A_V = -24 to -79dB	-2	0	2	dB
V_{DC}	DC Step	adyacent attenuation steps	-3	0	3	mV
A_{mute}	Mute Attenuation			90		db
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	THD = 0.3%	2	2.5		Vrms
R_L	Output Load Resistance		2			KΩ
V_{DC}	DC Voltage Level			4.5		V
GENERAL						
E_{NO}	Output Noise	BW = 20Hz to 20KHz All gains = 0dB, Flat		10	15	µV
S/N	Signal to Noise Ratio	All gains = 0dB; V_O = 1Vrms		100		dB
S_C	Channel Separation left/Right		80	90		dB
THD	Distortion	A_V = 0; V_I = 1Vrms		0.01	0.1	%
BUS INPUT						
V_{II}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Achnowledge	I_O = 1.6mA		0.4	0.8	V

Figure 4. Test circuit



3 APPLICATION SUGGESTIONS

The volume control range is 0 to -79dB, by 1dB step resolution.

The very high resolution allows the implementation of systems free from any noise acoustical effect.

3.1 CREF

The suggested 10µF reference capacitor (CREF) value can be reduced to 4.7µF if the application requires faster power ON.

Figure 5. THD vs. frequency

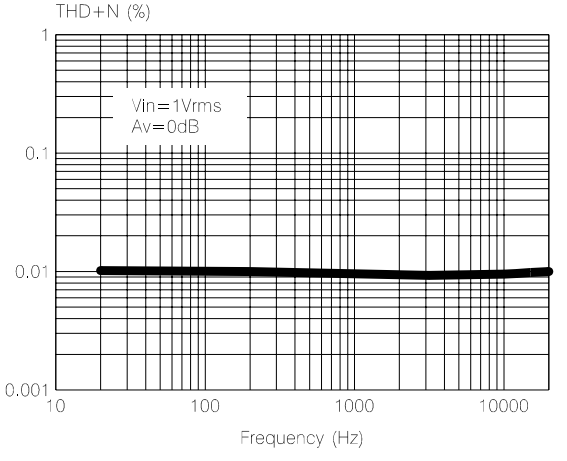


Figure 6. THD vs. R_{LOAD}

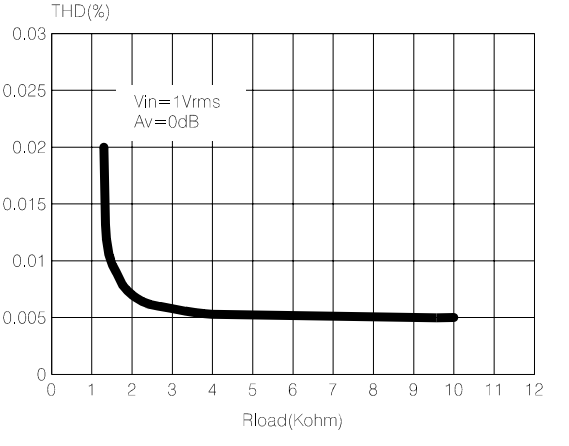
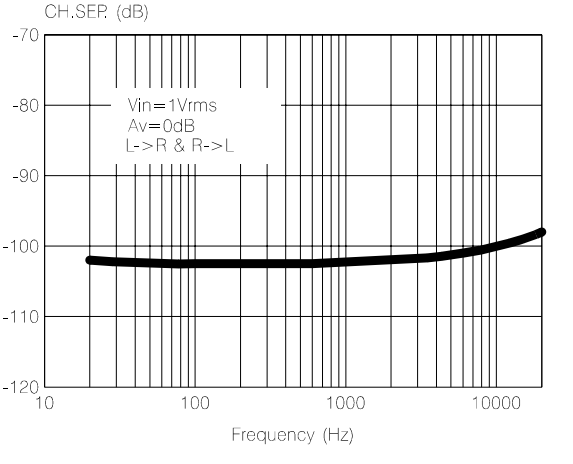


Figure 7. Channel separation vs. frequency



4 I²C BUS INTERFACE

Data transmission from microprocessor to the TDA7448 and vice versa takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

4.1 Data Validity

As shown in fig. 8, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

4.2 Start and Stop Conditions

As shown in fig. 9 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

4.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

4.4 Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 10). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

4.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking.

Figure 8. Data Validity on the I²CBUS

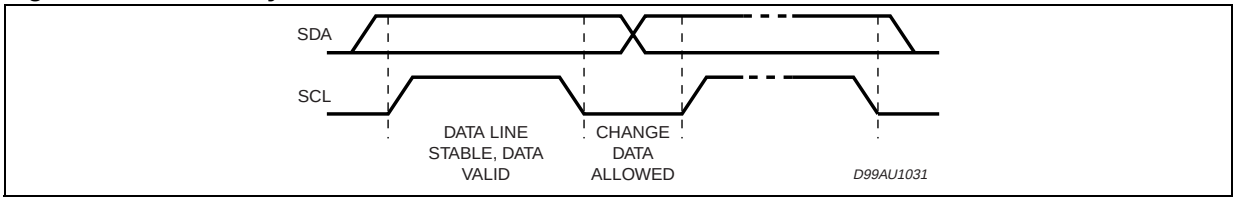


Figure 9. Timing Diagram of I²CBUS

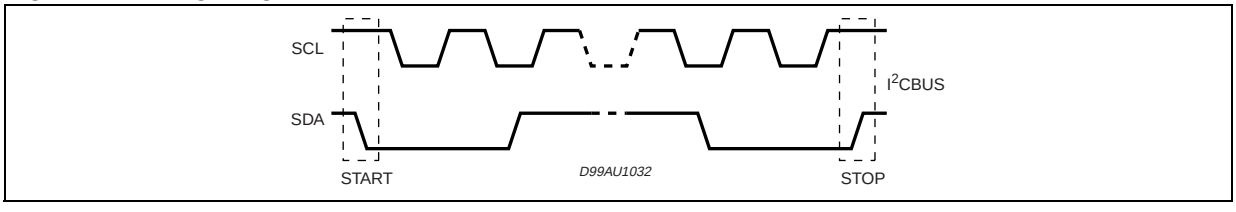
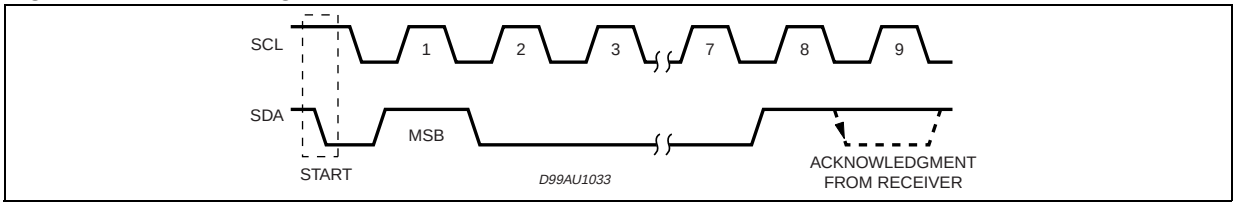


Figure 10. Acknowledge on the I²CBUS

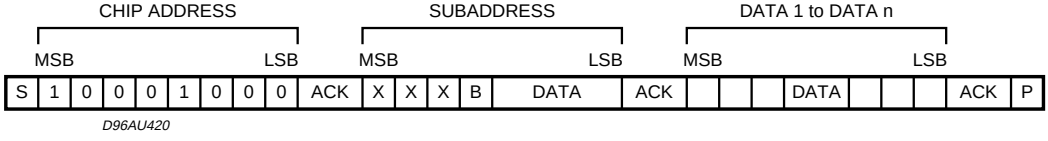


5 SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7448 address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P))

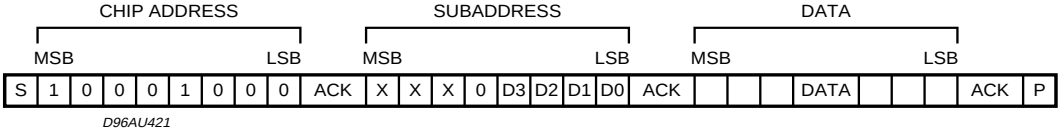


ACK = Acknowledge; S = Start; P = Stop; A = Address; B = Auto Increment

5.1 EXAMPLES

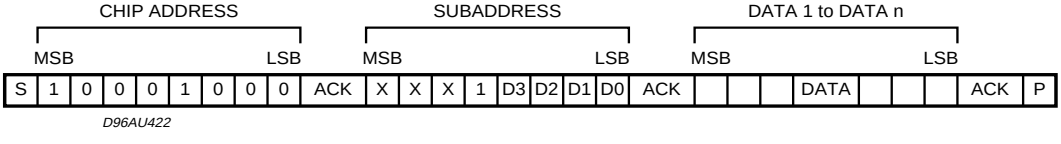
5.1.1 No Incremental Bus

The TDA7448 receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.



5.1.2 Incremental Bus

The TDA7448 receivea start conditions, the correct chip address, a subaddress with the B = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receivers the stop condition.



5.2 DATA BYTES

Address= 88 (HEX) (10001000): ADDR open; 8A (HEX) (10001010): connect to supply

Table 6. FUNCTION SELECTION: subaddress

MSB							LSB	SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	SPEAKER ATTENUATION OUT 1
X	X	X	B	0	0	0	1	SPEAKER ATTENUATION OUT 2
X	X	X	B	0	0	1	0	SPEAKER ATTENUATION OUT 3
X	X	X	B	0	0	1	1	SPEAKER ATTENUATION OUT 4
X	X	X	B	0	1	0	0	SPEAKER ATTENUATION OUT 5
X	X	X	B	0	1	0	1	SPEAKER ATTENUATION OUT 6
X	X	X	B	0	1	1	0	NOT USED”
X	X	X	B	0	1	1	1	NOT USED

B=1: INCREMENTAL BUS; ACTIVE
B=0: NO INCREMENTAL BUS
X= DON’T CARE

In Incremental Bus Mode, the three “not used” functions must be addressed in any case. For example to refresh “ Speaker Attenuation 3 = 0dB and Speaker Attenuation 6 = -40 dB”; the following bytes must be sent:

Table 7.

SUBADDRESS	XXX10010
SPEAKER ATTENUATION OUT 1	XXXXXXXX
SPEAKER ATTENUATION OUT 2	XXXXXXXX
SPEAKER ATTENUATION OUT 3	00000000
SPEAKER ATTENUATION OUT 4	XXXXXXXX
SPEAKER ATTENUATION OUT 5	XXXXXXXX
SPEAKER ATTENUATION OUT 6	00101111

Table 8. SPEAKER ATTENUATION SELECTION

MSB							LSB	SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
0	0	0	0	0				-0dB
0	0	0	0	1				-8dB
0	0	0	1	0				-16dB
0	0	0	1	1				-24dB
0	0	1	0	0				-32dB
0	0	1	0	1				-40dB
0	0	1	1	0				-48dB
0	0	1	1	1				-56dB
0	1							-64dB
1	0							-72dB
1	1							MUTE

value = 0 to -79dB and MUTE

Figure 11. PIN:20

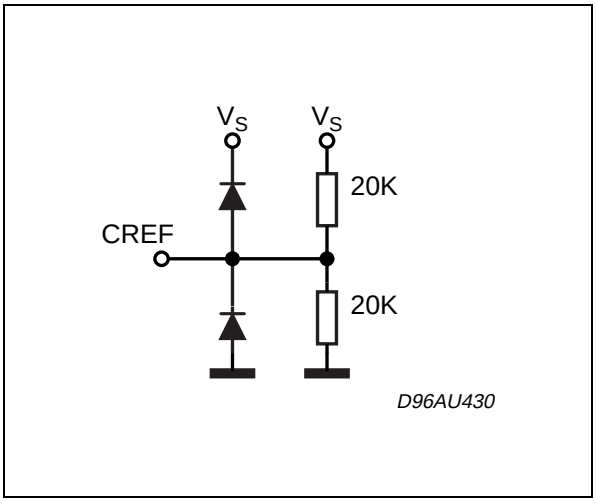


Figure 12. PINS: 5, 6, 7, 14, 15, 16

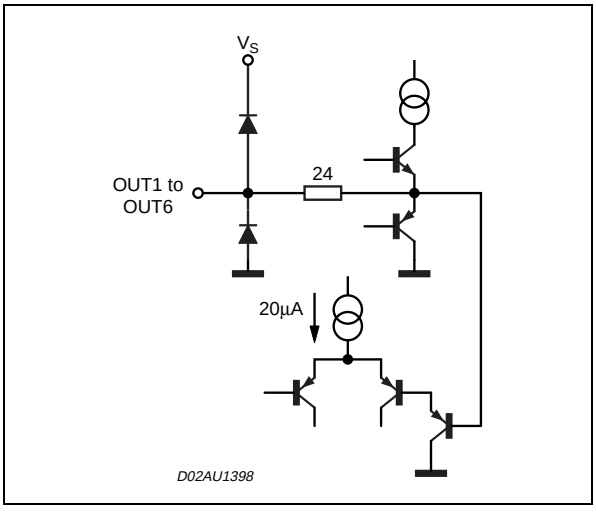


Figure 13. PINS: 2, 3, 4, 17, 18, 19

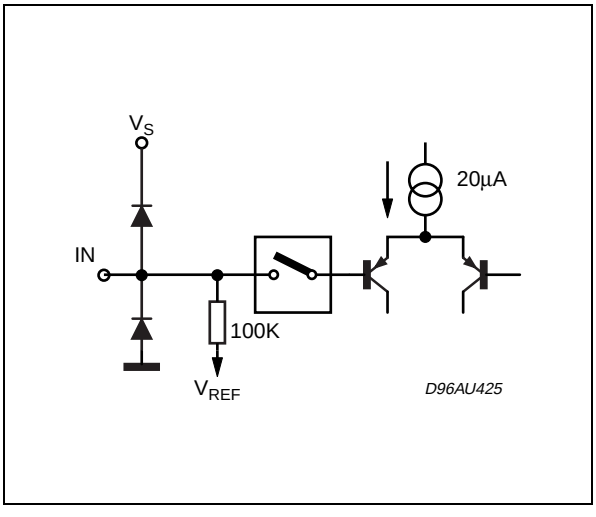


Figure 14. PINS: 10

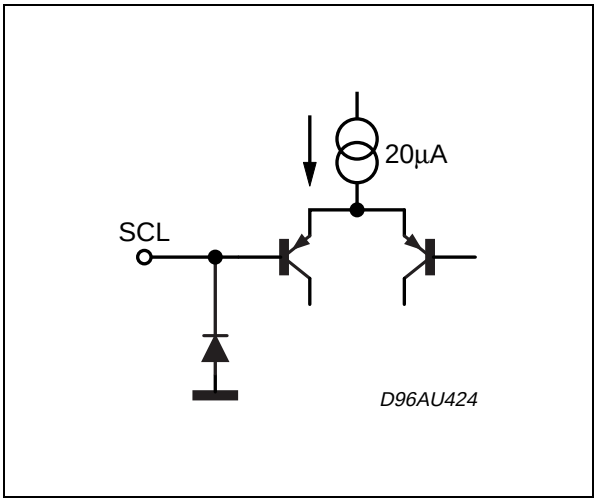


Figure 15. PINS: 9

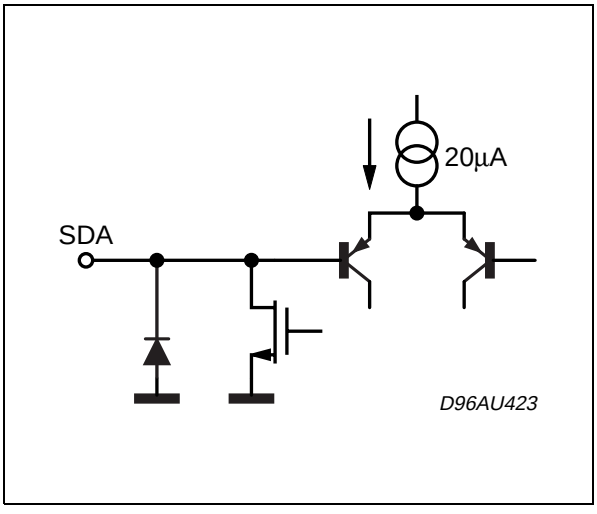


Figure 16. Test and Application Circuit

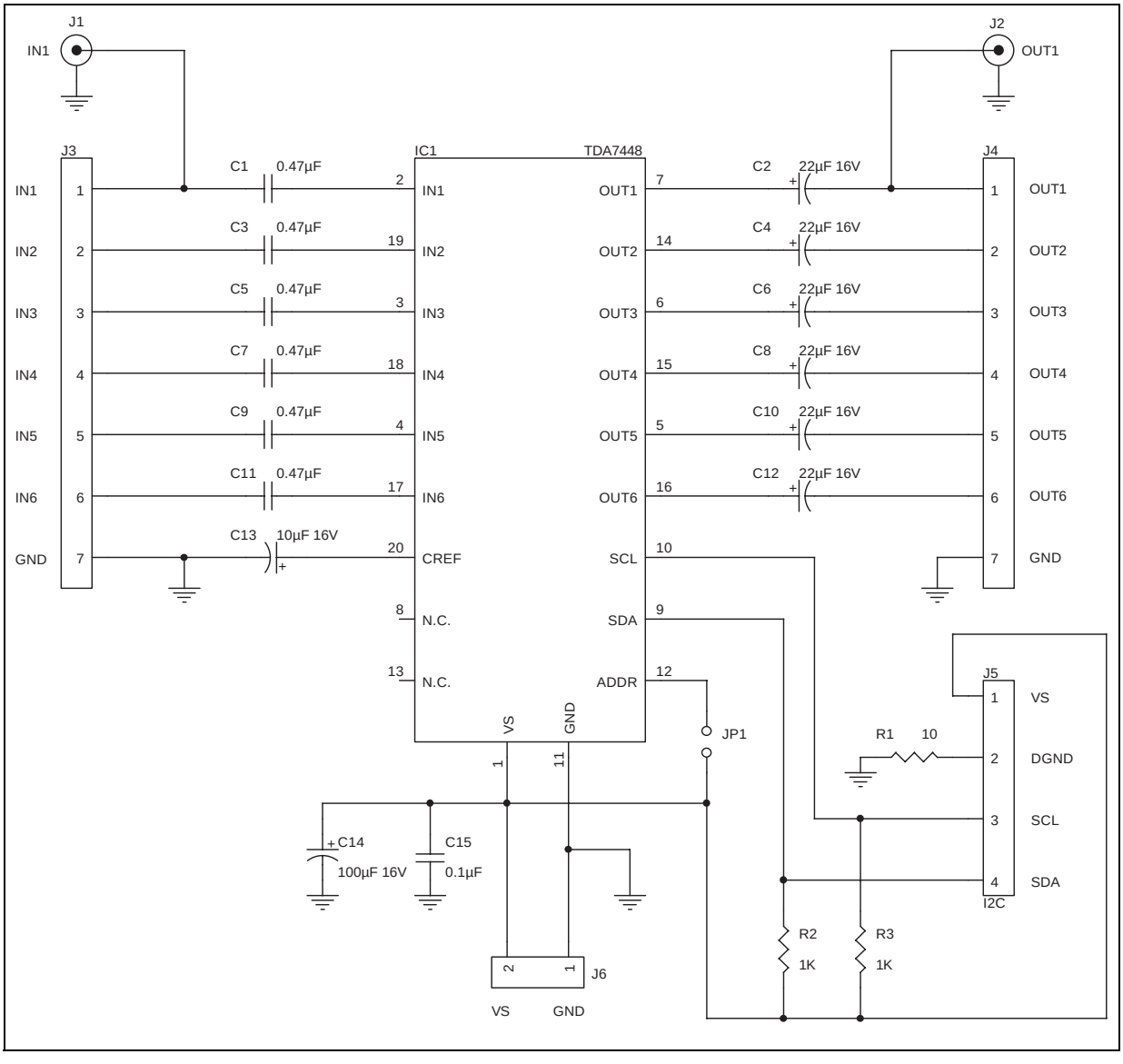


Figure 17. Component Layout (65 x 72mm)

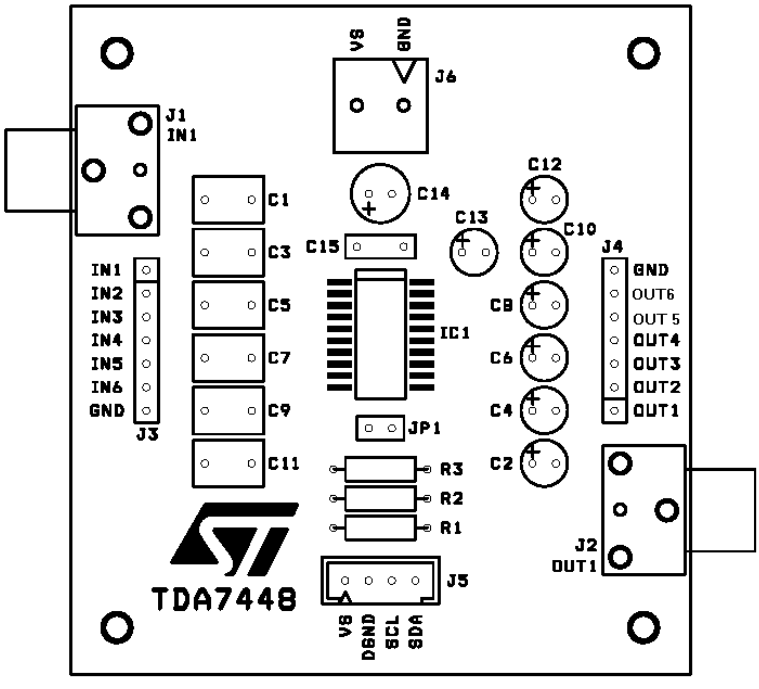


Figure 18. PC Board (Component side)

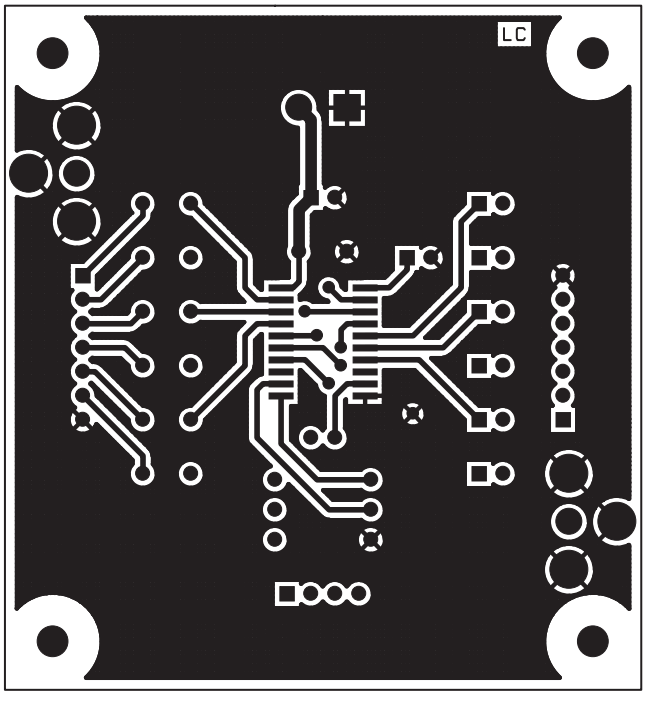


Figure 19. PC Board (Solder side)

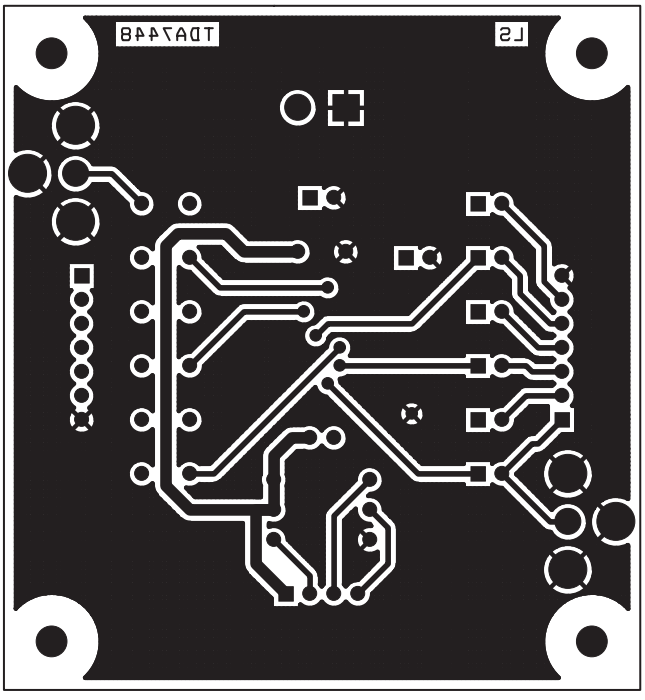
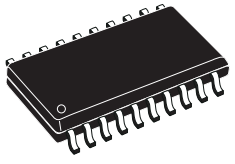


Figure 20. SO-20 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20

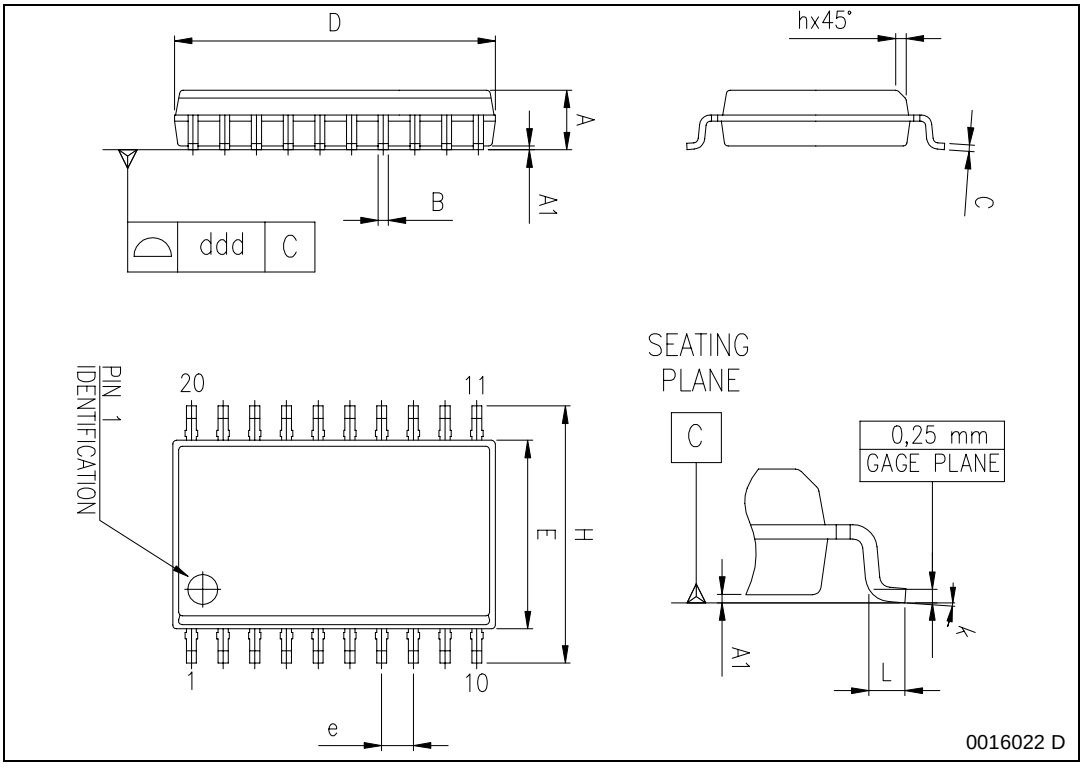


Table 9. Revision History

Date	Revision	Description of Changes
January 2004	1	First Issue
June 2004	3	Modified the style-sheet in compliance with the last revision of the “Corporate Technical Pubblications Design Guide”.