TS2012

Filter-free stereo 2x2.8W class D audio power amplifer

Features

- Operating range from V_{CC}=2.5V to 5.5V
- Standby mode active low
- Output power per channel : 1.35W @5V or 0.68W @ 3.6V into 8Ω with 1% THD+N max.
- Output power per channel : 2.2W @5V into 4Ω with 1% THD+N max.
- Four gains select : 6, 12, 18, 24 dB
- Low current consumption
- PSRR: 70dB typ @ 217Hz with 6dB gain.
- Fast start-up phase: 1ms
- Thermal shutdown protection
- QFN20 4x4mm lead-free package

Applications

- Cellular phone
- PDA
- Flat panel TV

Description

The TS2012 is a stereo fully differential class D power amplifier. Able to drive up to 1.35W into an 8Ω load at 5V per channel. It achieves outstanding efficiency compared to typical class AB audio amps.

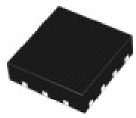
The device has four different gain settings utilizing two discrete pins: G0 and G1.

Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 1ms.

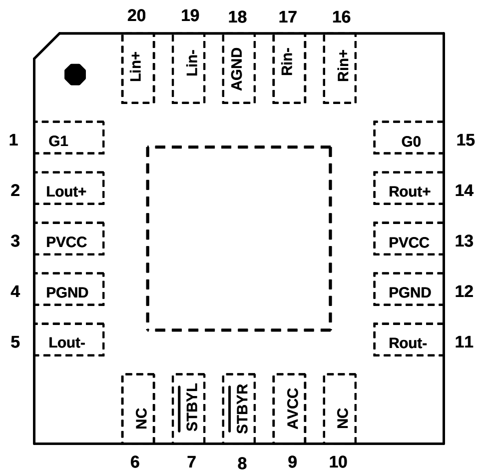
Two standby pins (active low) allow each channel to be switched off independently.

The TS2012 is available in a QFN20 package in 4x4 mm dimension.

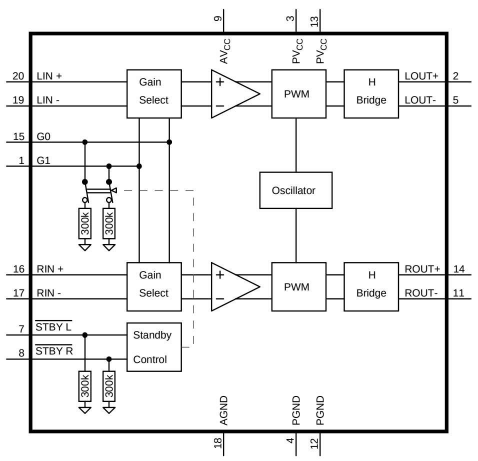
TS2012IQT - QFN20 (4x4)



Pin connections (top view)



Block diagram



Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_i	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	100	°C/W
P_d	Power dissipation	Internally limited(4)	
ESD	HBM: human body model(5)	2	kV
	MM: machine model(6)	200	V
Latch-up	Latch-up immunity	200	mA
V_{STBY}	Standby pin voltage maximum voltage	GND to V_{CC}	V
	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of the input signal must never exceed V_{CC} + 0.3V / GND - 0.3V.
3. The device is protected in case of over temperature by a thermal shutdown active @ 150°C.
4. Exceeding the power derating curves during a long period will cause abnormal operation.
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_I	Input voltage range	GND to V_{CC}	V
V_{ic}	Input common mode voltage[1]	GND+0.5V to V_{CC}-0.9V	V
V_{STBY}	Standby voltage input [2] Device ON Device in STANDBY[3]	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$	V
R_L	Load resistor	≥ 4	Ω
V_{IH}	GO, G1 - high level input voltage[4]	$1.4 \leq V_{IH} \leq V_{CC}$	V
V_{IL}	GO, G1 - low level input voltage	$GND \leq V_{IL} \leq 0.4$	V
R_{thja}	Thermal resistance junction to ambient [5]	40	°C/W

1. $I V_{oo} I \leq 40mV$ max with all differential gains except 24dB. For 24dB gain, input decoupling caps are mandatory.
2. Without any signal on V_{STBY}, the device is in standby (internal 300kΩ +/-20% pull-down resistor).
3. Minimum current consumption is obtained when V_{STBY} = GND.
4. Between G0, G1pins and GND, there is an internal 300kΩ (+/-20%) pull-down resistor. When pins are floating, the gain is 6 dB. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).
5. With 4-layer PCB.

2 Typical application

Figure 1. Typical application schematics

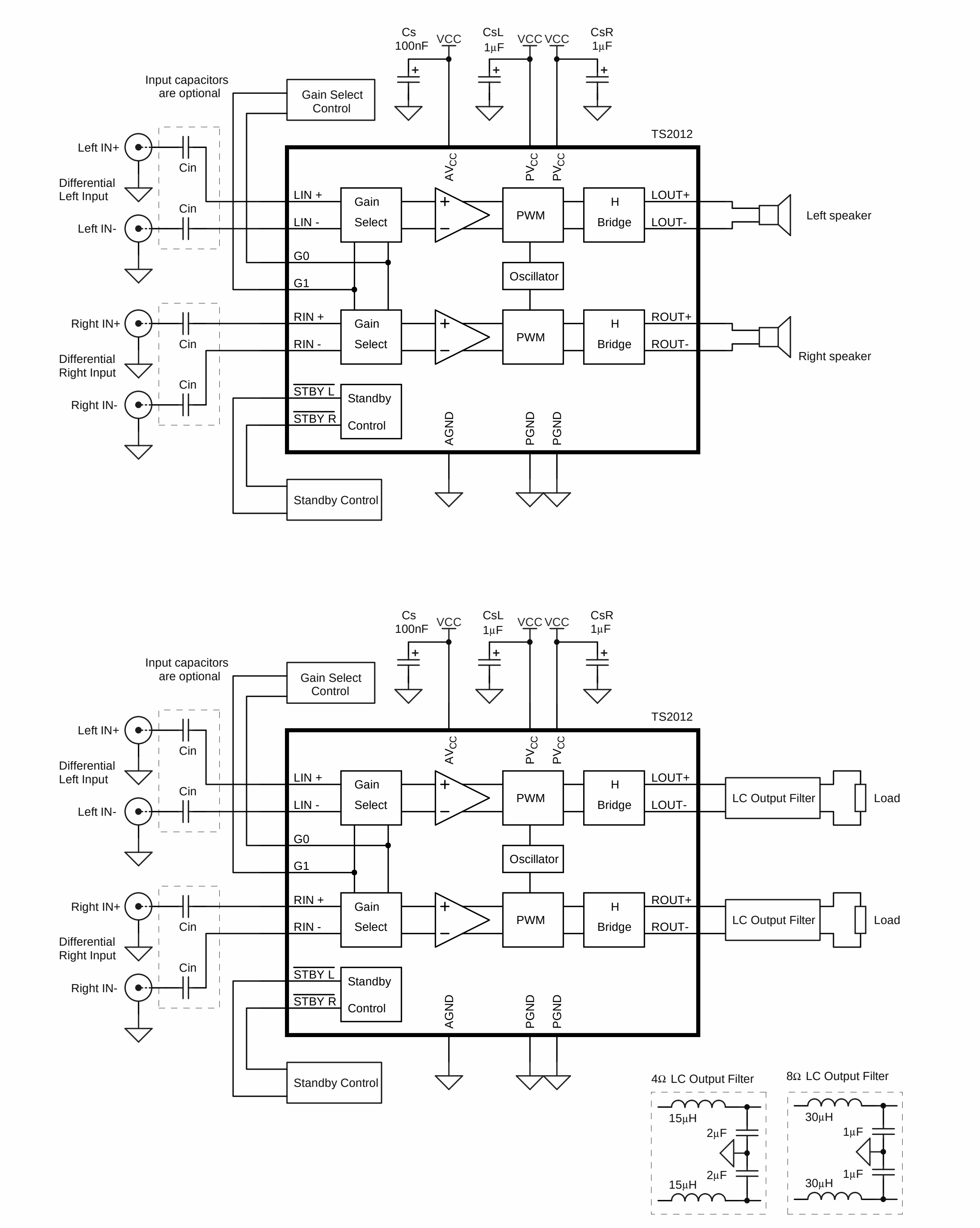


Table 3. External component descriptions

Components	Functional description
C_S, C_{SL}, C_{SR}	Supply capacitor that provides power supply filtering.
C_{in}	Input coupling capacitors (optional) that block the DC voltage at the amplifier input terminal. The capacitors also form a high pass filter with Z_{in} ($F_{cl} = 1 / (2 \times \pi \times Z_{in} \times C_{in})$).

Table 4. Pin descriptions

Pin number	Pin name	Pin description
1	G1	Gain select pin (MSB)
2	Lout+	Left channel positive output
3	PVCC	Power supply
4	PGND	Power ground
5	Lout-	Left channel negative output
6	NC	No internal connection
7	STBYL	Standby pin (active low) for left channel output
8	STBYR	Standby pin (active low) for right channel output
9	AVCC	Analog supply
10	NC	No internal connection
11	Rout-	Right channel negative output
12	PGND	Power ground
13	PVCC	Power supply
14	Rout+	Right channel positive output
15	G0	Gain select pin (LSB)
16	Rin+	Right channel positive differential input
17	Rin-	Right channel negative differential input
18	AGND	Analog ground
19	Lin-	Left channel negative differential input
20	Lin+	Left channel positive differential input
	Thermal pad	Connect the thermal pad of the QFN package to PCB ground

3 Electrical characteristics

3.1 Electrical characteristic tables

Table 5. V_{CC} = +5V, GND = 0V, V_{ic}=2.5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameters and test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, both channels		5	8	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND		0.2	2	µA
V_{oo}	Output offset voltage Floating inputs, G = 6dB, R_L = 8Ω			25	mV
P_o	Output power THD + N = 1% max, f = 1kHz, R_L = 4Ω THD + N = 1% max, f = 1kHz, R_L = 8Ω THD + N = 10% max, f = 1kHz, R_L = 4Ω THD + N = 10% max, f = 1kHz, R_L = 8Ω		 2.2 1.35 2.8 1.65		W
THD + N	Total harmonic distortion + noise P_o = 0.8W, G = 6dB, f =1kHz, R_L = 8Ω		0.07		%
Efficiency	Efficiency per channel P_o = 2.2W, R_L = 4Ω +15µH P_o = 1.25 W, R_L = 8Ω+15µH		 81 89		%
PSRR	Power supply rejection ratio with inputs grounded C_{in}=1µF (1),f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp}		70		dB
Crosstalk	Channel separation P_o = 0.9W, G = 6dB, f =1kHz, R_L = 8Ω		90		dB
CMRR	Common mode rejection ratio C_{in}=1µF, f = 217Hz, R_L = 8Ω, Gain=6dB, Δ_{VICM} = 200mV_{pp}		70		dB
Gain	Gain value G1 = G0 = V_{IL} G1 = V_{IL} & G0 = V_{IH} G1 = V_{IH} & G0 = V_{IL} G1 = G0 = V_{IH}	 5.5 11.5 17.5 23.5	 6 12 18 24	 6.5 12.5 18.5 24.5	dB
Z_{in}	Single ended input impedance All gains, refered to ground	24	30	36	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) P_o = 1.3W, G = 6dB, R_L = 8Ω		99		dB
t_{WU}	Wake-up time		1	3	ms
t_{STBY}	Standby time		1		ms

Table 5. V_{CC} = +5V, GND = 0V, V_{ic}=2.5V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameters and test conditions	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=8Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=24dB) A-weighted (Filterless, G=24dB) Unweighted (with LC output filter, G=24dB) A-weighted (with LC output filter, G=24dB)		 63 35 60 35 115 72 109 71		μV_{RMS}

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.

Table 6. V_{CC} = +3.6V, GND = 0V, V_{ic}=1.8V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, both channels		3.3	6.5	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND		0.2	2	µA
V_{oo}	Output offset voltage Floating inputs, G = 6dB, R_L = 8Ω			25	mV
P_o	Output power THD + N = 1% max, f = 1kHz, R_L = 4Ω THD + N = 1% max, f = 1kHz, R_L = 8Ω THD + N = 10% max, f = 1kHz, R_L = 4Ω THD + N = 10% max, f = 1kHz, R_L = 8Ω		 1.15 0.68 1.3 0.9		W
THD + N	Total harmonic distortion + noise P_o = 0.4W, G = 6dB, f =1kHz, R_L = 8Ω		0.05		%
Efficiency	Efficiency per channel P_o = 1.15W, R_L = 4Ω +15µH P_o = 0.68W, R_L = 8Ω+15µH		 80 88		%
PSRR	Power supply rejection ratio with inputs grounded C_{in}=1µF [(1)],f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp}		70		dB
Crosstalk	Channel separation P_o = 0.5W, G = 6dB, f =1kHz, R_L = 8Ω		90		
CMRR	Common mode rejection ratio C_{in}=1µF, f = 217Hz, R_L = 8Ω, Gain=6dB, Δ_{VICM} = 200mV_{pp}		70		dB
Gain	Gain value G1 = G0 = V_{IL} G1 = V_{IL} & G0 = V_{IH} G1 = V_{IH} & G0 = V_{IL} G1 = G0 = V_{IH}	 5.5 11.5 17.5 23.5	 6 12 18 24	 6.5 12.5 18.5 24.5	dB
Z_{in}	Single ended input impedance All gains, referred to ground	24	30	36	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) P_o = 0.65W, G = 6dB, R_L = 8Ω		96		dB
t_{WU}	Wake-up time		1	3	ms
t_{STBY}	Standby time		1		ms

Table 6. V_{CC} = +3.6V, GND = 0V, V_{ic}=1.8V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=4Ω Unweighted (Filterless, G=6dB) A-weighted (Filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (Filterless, G=24dB) A-weighted (Filterless, G=24dB) Unweighted (with LC output filter, G=24dB) A-weighted (with LC output filter, G=24dB)		 58 34 55 34 111 70 105 69		μV_{RMS}

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.

Table 7. V_{CC} = +2.5V, GND = 0V, V_{ic}=1.25V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply current No input signal, no load, both channels		2.8	4	mA
I_{STBY}	Standby current No input signal, V_{STBY} = GND		0.2	2	µA
V_{oo}	Output offset voltage Floating inputs, G = 6dB, R_L = 8Ω			25	mV
P_o	Output power THD + N = 1% max, f = 1kHz, R_L = 4Ω THD + N = 1% max, f = 1kHz, R_L = 8Ω THD + N = 10% max, f = 1kHz, R_L = 4Ω THD + N = 10% max, f = 1kHz, R_L = 8Ω		 0.53 0.32 0.75 0.45		W
THD + N	Total harmonic distortion + noise P_o = 0.2W, G = 6dB, f =1kHz, R_L = 8Ω		0.04		%
Efficiency	Efficiency per channel P_o = 0.53W, R_L = 4Ω +15µH P_o = 0.32W, R_L = 8Ω+15µH		 80 88		%
PSRR	Power supply rejection ratio with inputs grounded C_{in}=1µF [(1)],f = 217Hz, R_L = 8Ω, Gain=6dB, V_{ripple} = 200mV_{pp}		70		dB
Crosstalk	Channel separation P_o = 0.2W, G = 6dB, f =1kHz, R_L = 8Ω		90		
CMRR	Common mode rejection ratio C_{in}=1µF, f = 217Hz, R_L = 8Ω, Gain=6dB, Δ_{VICM} = 200mV_{pp}		70		dB
Gain	Gain value G1 = G0 = V_{IL} G1 = V_{IL} & G0 = V_{IH} G1 = V_{IH} & G0 = V_{IL} G1 = G0 = V_{IH}	 5.5 11.5 17.5 23.5	 6 12 18 24	 6.5 12.5 18.5 24.5	dB
Z_{in}	Single ended input impedance All gains, refered to ground	24	30	36	kΩ
F_{PWM}	Pulse width modulator base frequency	190	280	370	kHz
SNR	Signal to noise ratio (A-weighting) P_o = 0.3W, G = 6dB, R_L = 8Ω		93		dB
t_{WU}	Wake-up time		1	3	ms
t_{STBY}	Standby time		1		ms

Table 7. V_{CC} = +2.5V, GND = 0V, V_{ic}=1.25V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_N	Output voltage noise f = 20Hz to 20kHz, R_L=8Ω Unweighted (filterless, G=6dB) A-weighted (filterless, G=6dB) Unweighted (with LC output filter, G=6dB) A-weighted (with LC output filter, G=6dB) Unweighted (filterless, G=24dB) A-weighted (filterless, G=24dB) Unweighted (with LC output filter, G=24dB) A-weighted (with LC output filter, G=24dB)		 57 34 54 33 110 71 104 69		μV_{RMS}

1. Dynamic measurements - 20*log(rms(V_{out})/rms(V_{ripple})). V_{ripple} is the superimposed sinus signal to V_{CC} @ f = 217Hz.

3.2 Electrical characteristic curves

The graphs shown in this section use the following abbreviations:

- R_L+ 15µH or 30µH = pure resistor + very low series resistance inductor
- Filter = LC output filter (1µF+30µH for 4Ω and 0.5µF+60µH for 8Ω)

All measurements are done with C_{SL}=C_{SR}=1µF and C_S=100nF (see *Figure 2*), except for the PSRR where $C_{SL,R}$ is removed (see *Figure 3*).

Figure 2. Test diagram for measurements

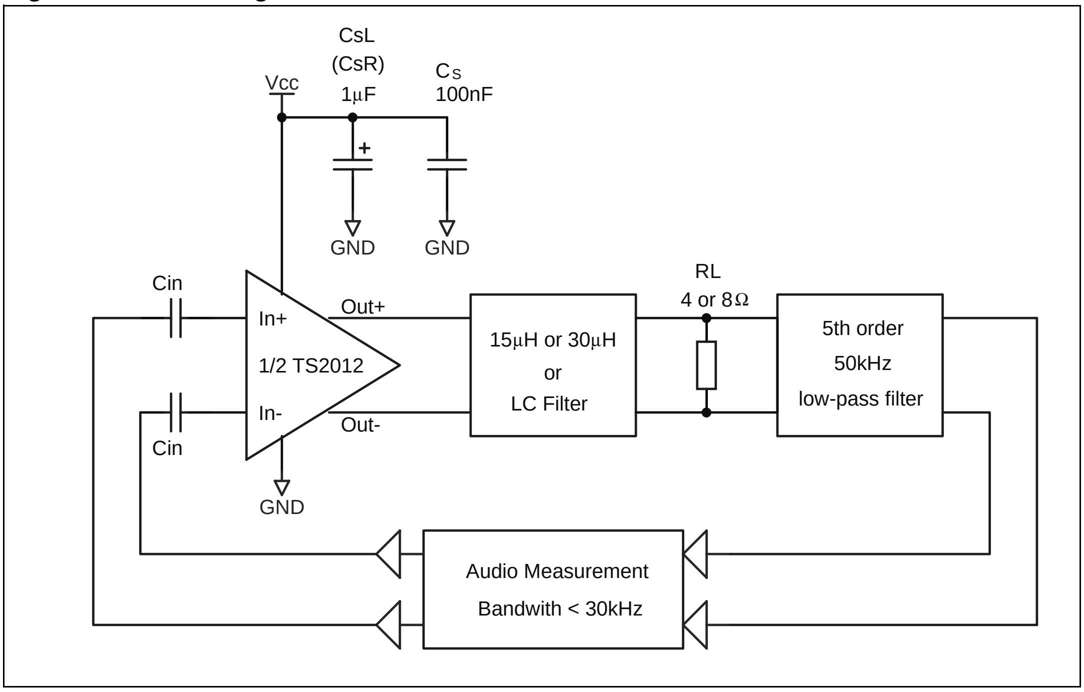


Figure 3. Test diagram for PSRR measurements

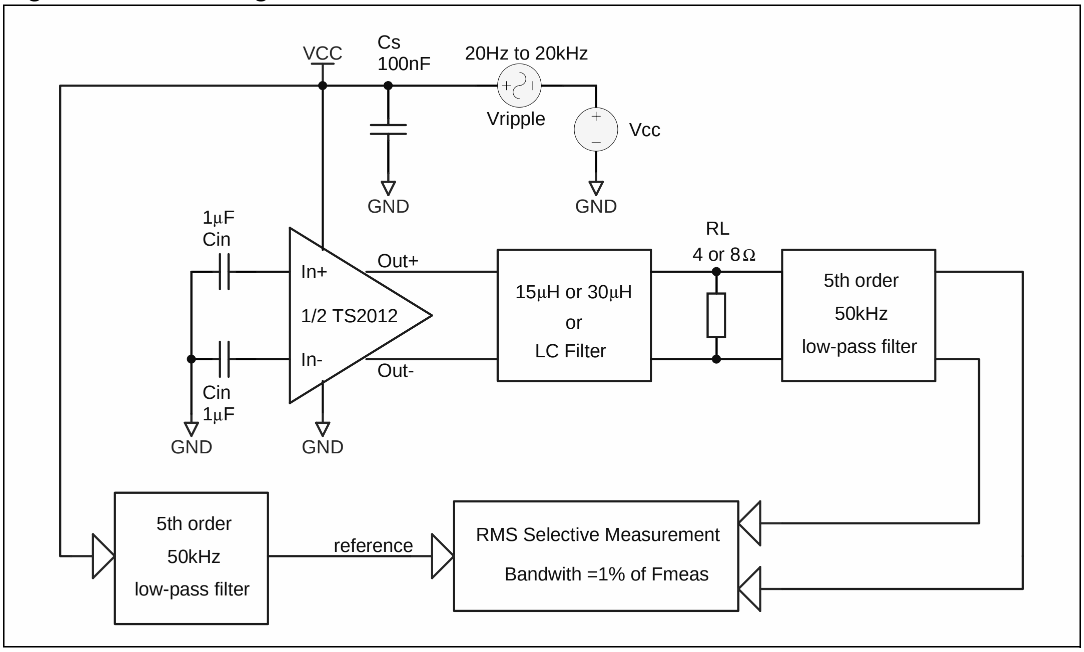


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Figure 4. Current consumption vs. power supply voltage

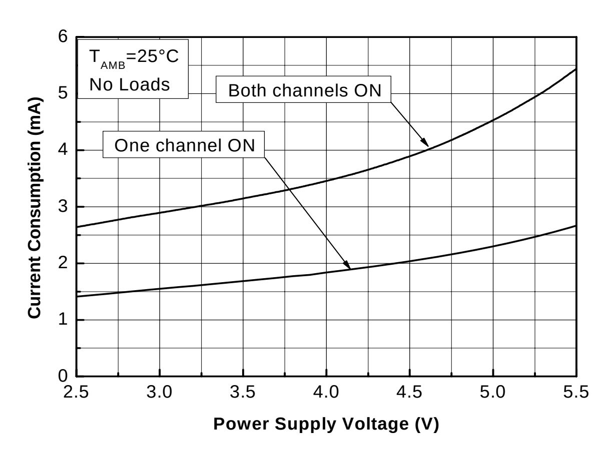


Figure 5. Current consumption vs. standby voltage (one channel)

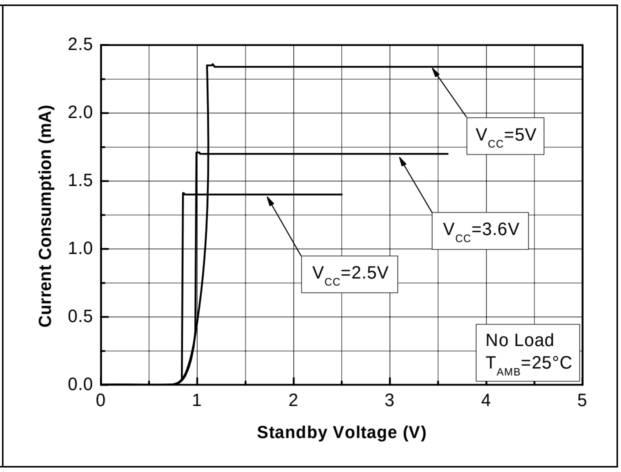


Figure 6. Efficiency vs. output power

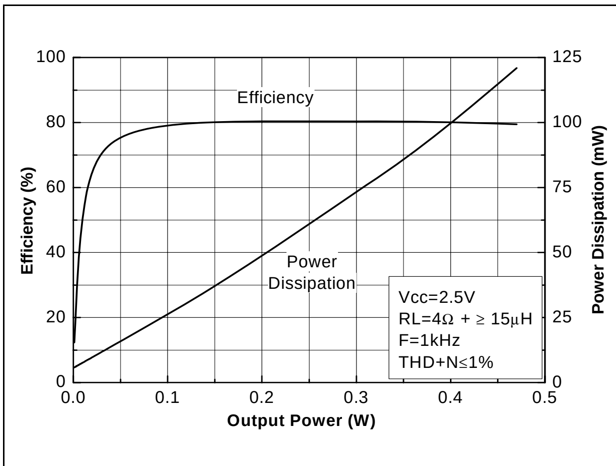


Figure 7. Efficiency vs. output power

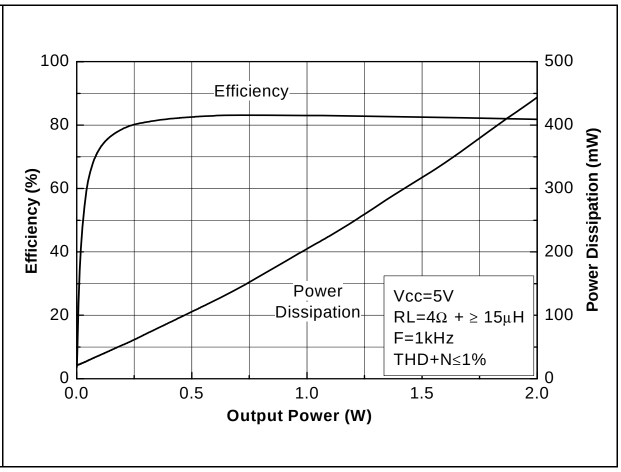


Figure 8. Efficiency vs. output power

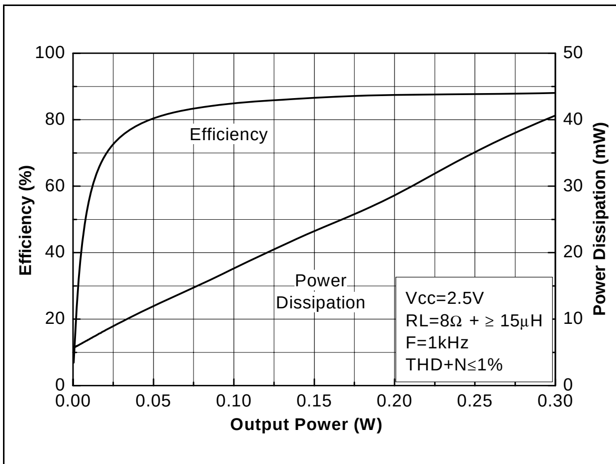


Figure 9. Efficiency vs. output power

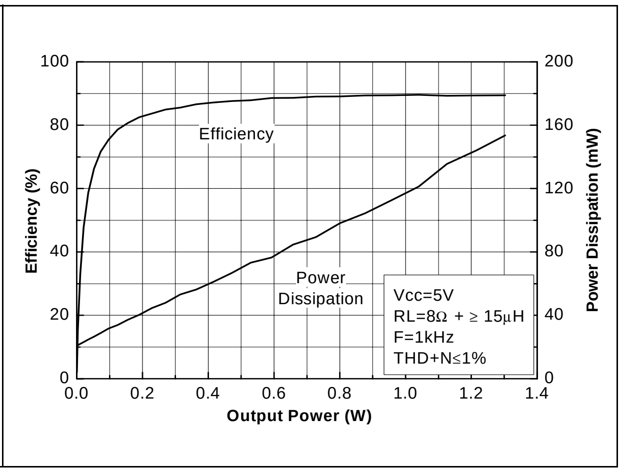


Figure 10. Output power vs. power supply voltage

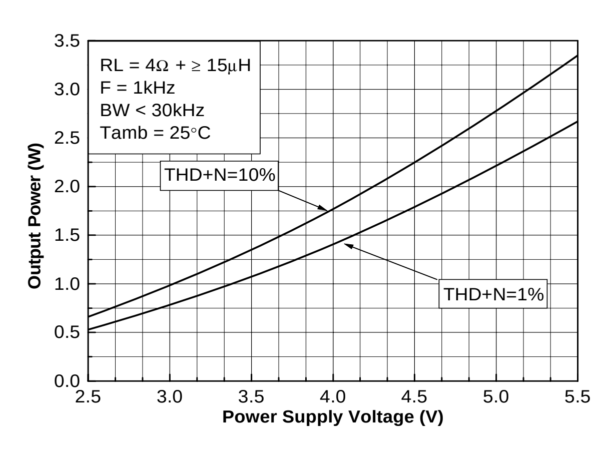


Figure 11. Output power vs. power supply voltage

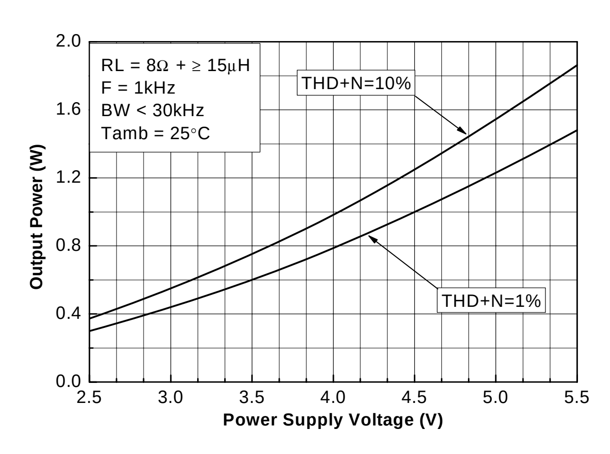


Figure 12. PSRR vs. common mode input voltage

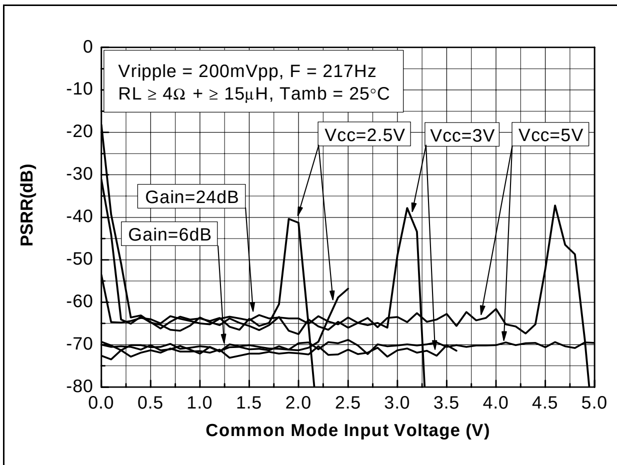


Figure 13. PSRR vs. frequency

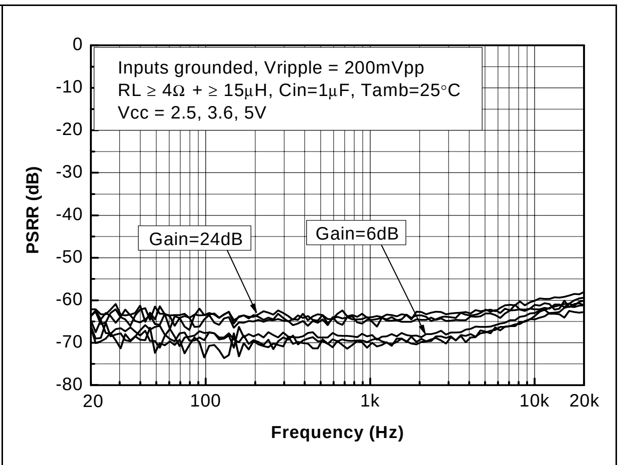


Figure 14. CMRR vs. common mode input voltage

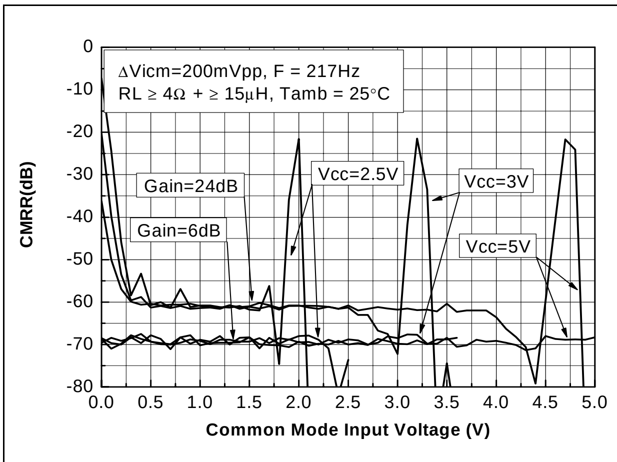


Figure 15. CMRR vs. frequency

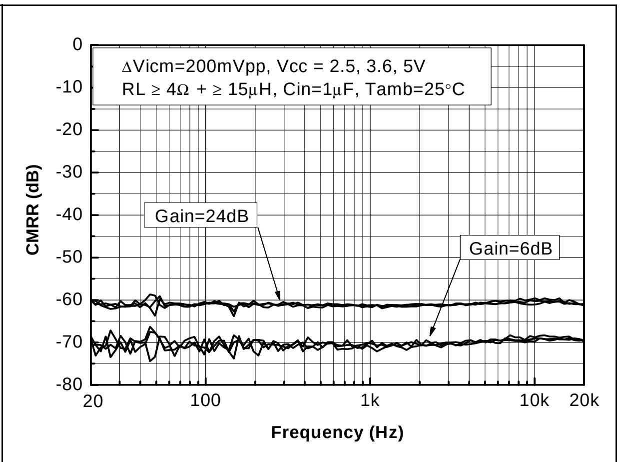


Figure 16. Gain vs. frequency

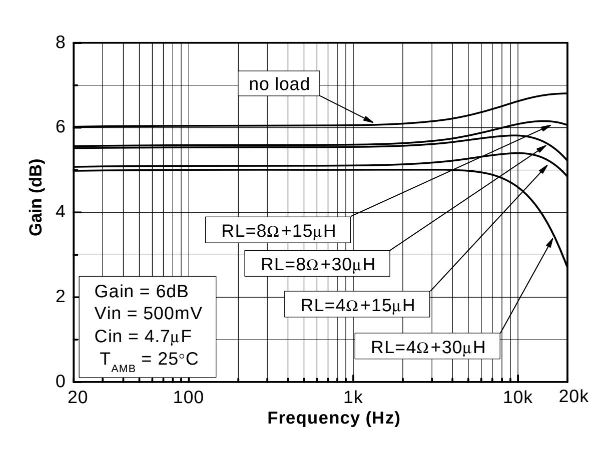


Figure 17. Gain vs. frequency

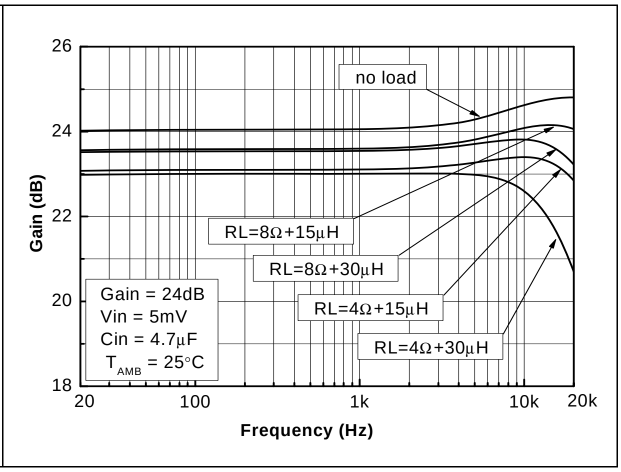


Figure 18. THD+N vs. output power

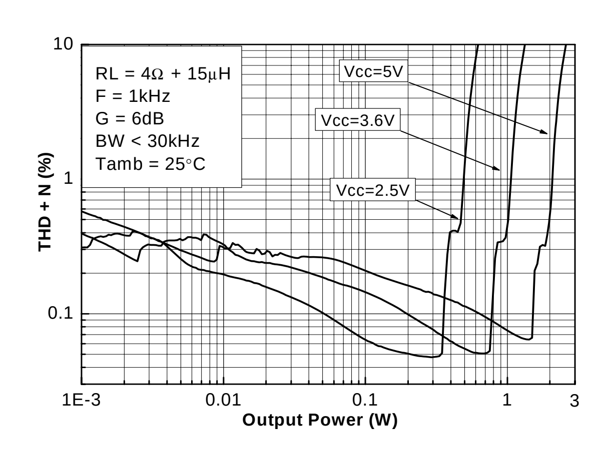


Figure 19. THD+N vs. output power

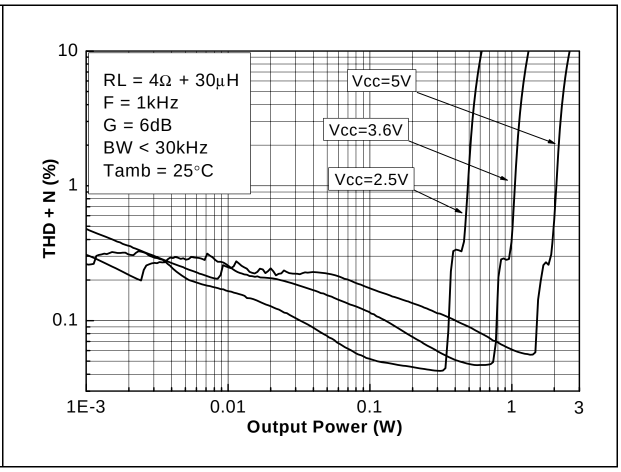


Figure 20. THD+N vs. output power

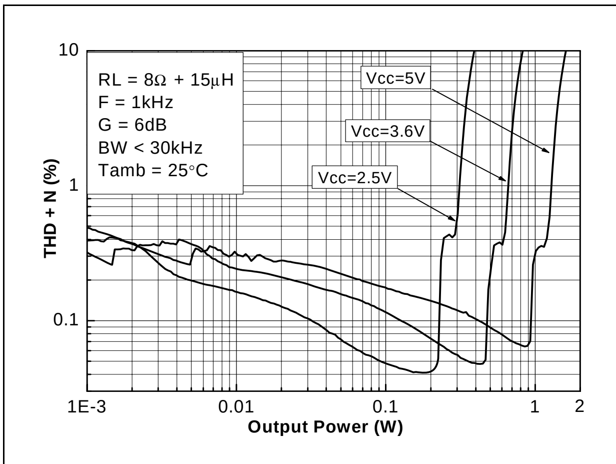


Figure 21. THD+N vs. output power

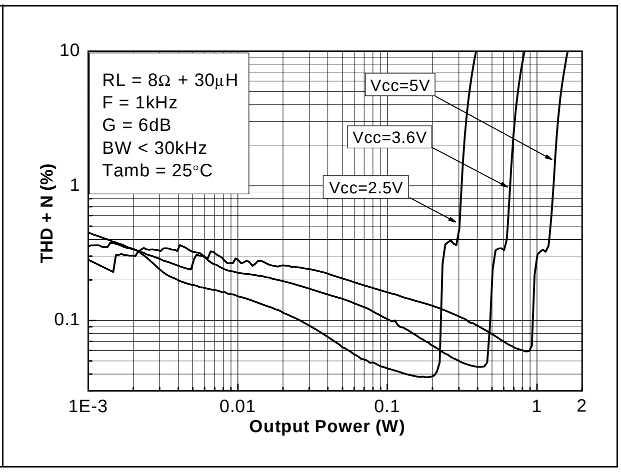


Figure 22. THD+N vs. output power

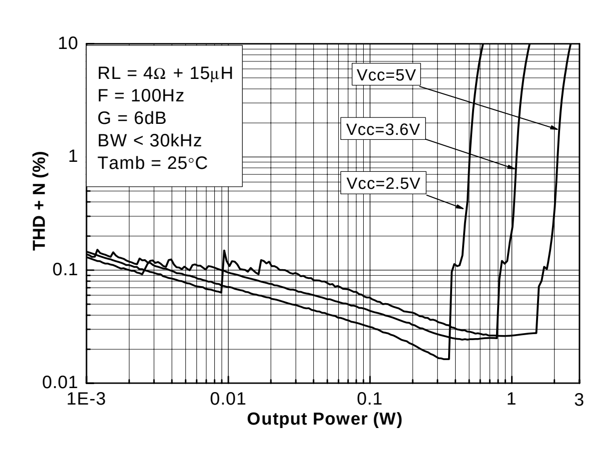


Figure 23. THD+N vs. output power

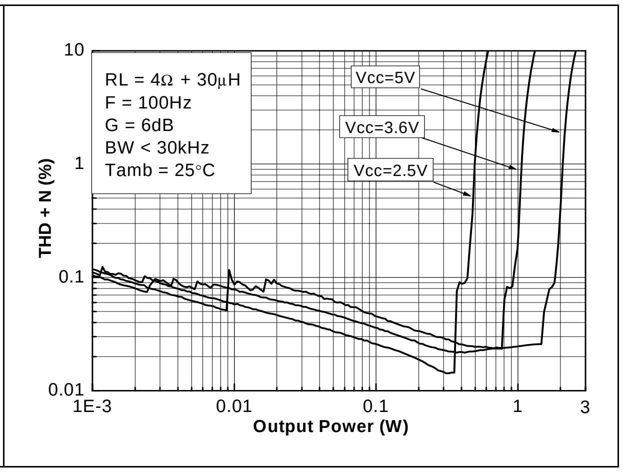


Figure 24. THD+N vs. output power

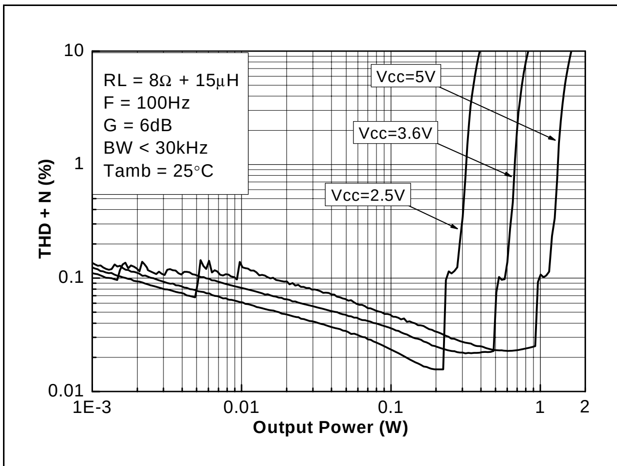


Figure 25. THD+N vs. output power

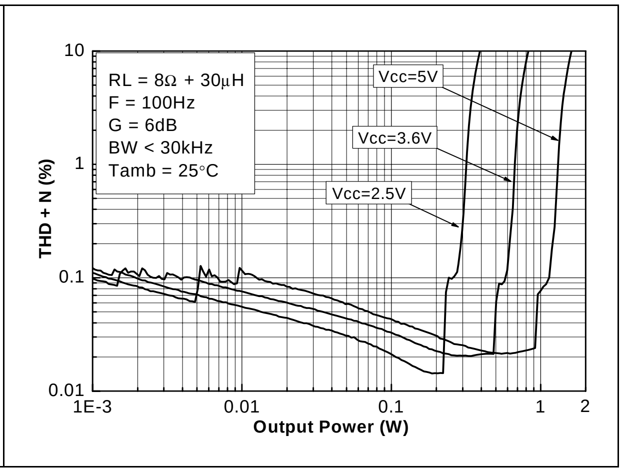


Figure 26. THD+N vs. frequency

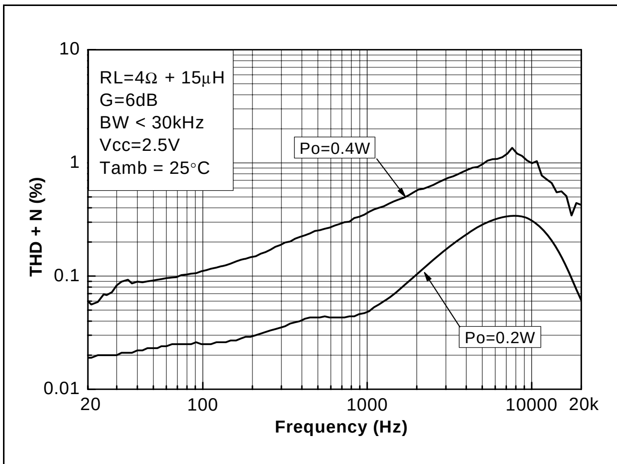


Figure 27. THD+N vs. frequency

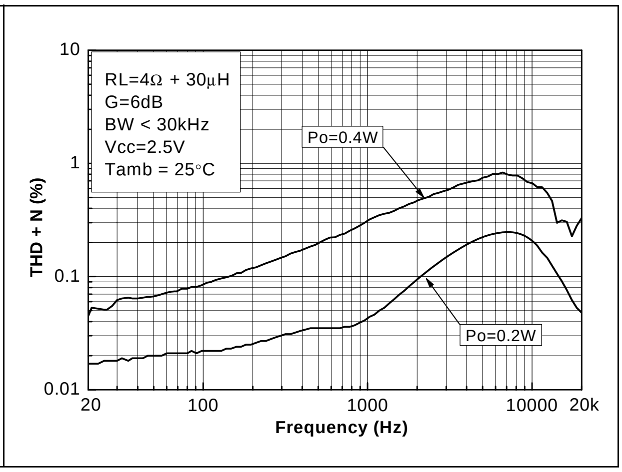


Figure 28. THD+N vs. frequency

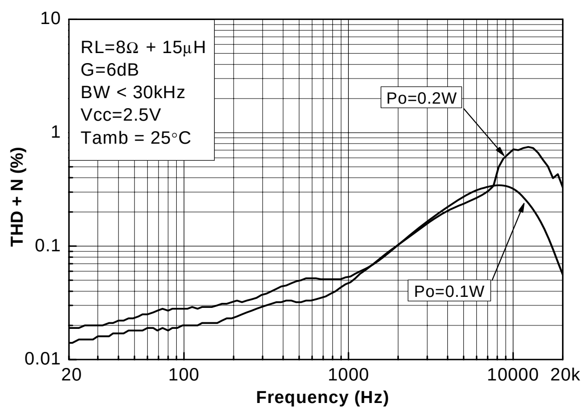


Figure 29. THD+N vs. frequency

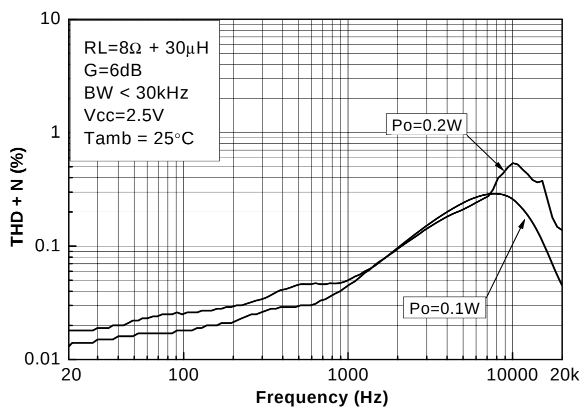


Figure 30. THD+N vs. frequency

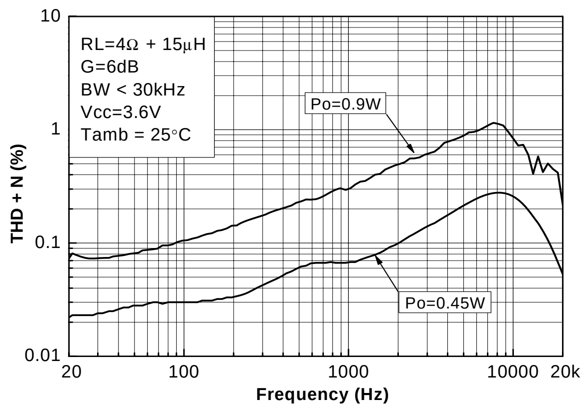


Figure 31. THD+N vs. frequency

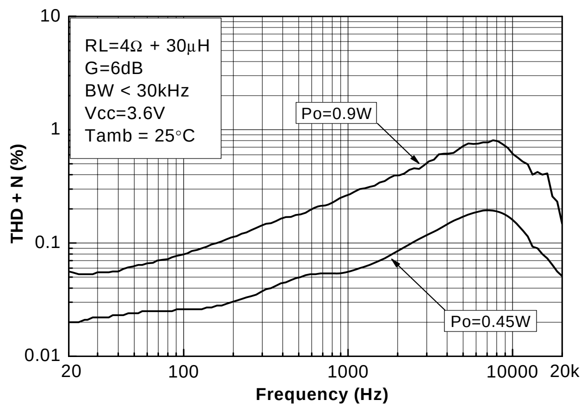


Figure 32. THD+N vs. frequency

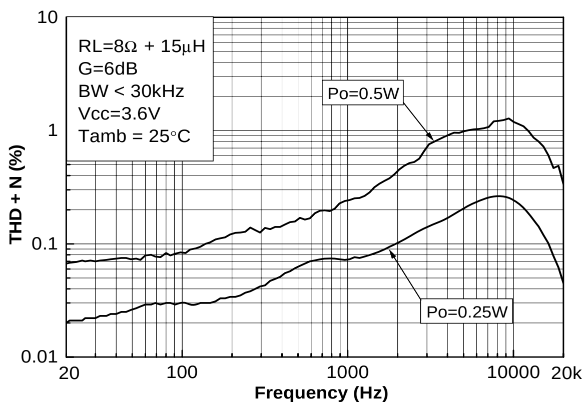


Figure 33. THD+N vs. frequency

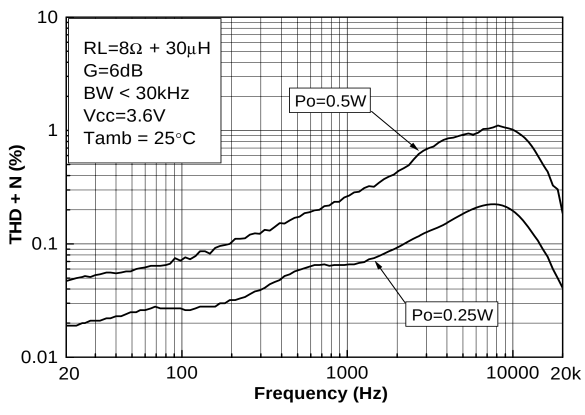


Figure 34. THD+N vs. frequency

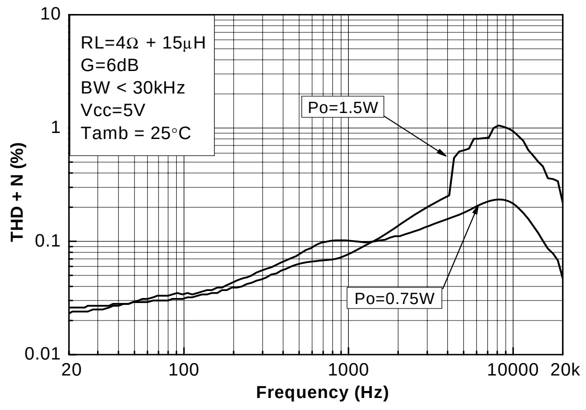


Figure 35. THD+N vs. frequency

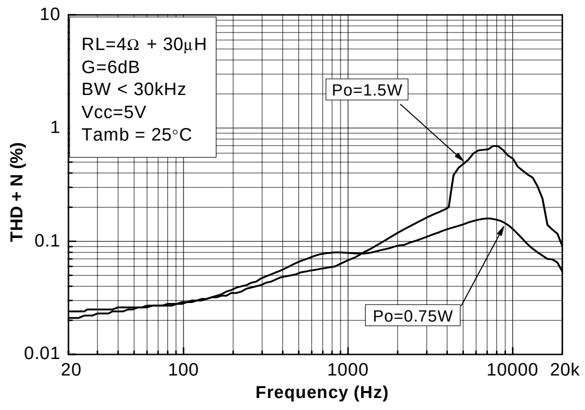


Figure 36. THD+N vs. frequency

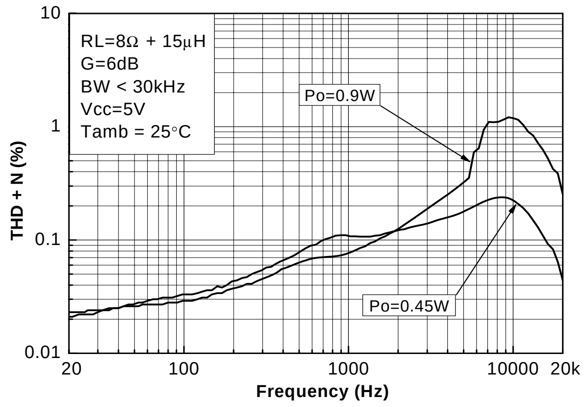


Figure 37. THD+N vs. frequency

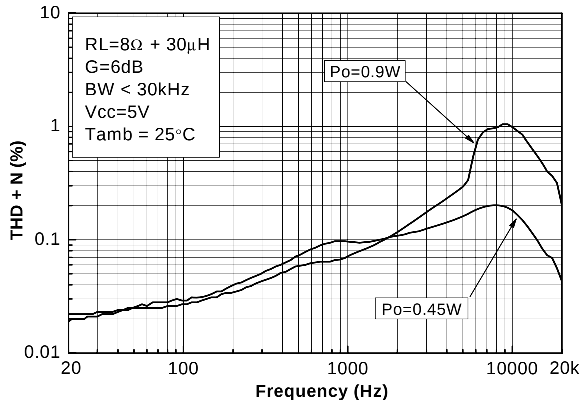


Figure 38. Crosstalk vs. frequency

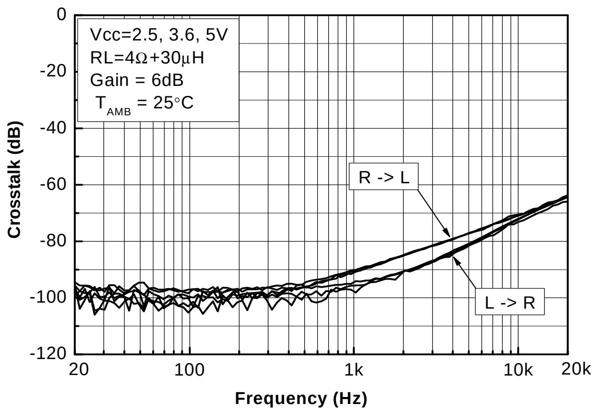


Figure 39. Crosstalk vs. frequency

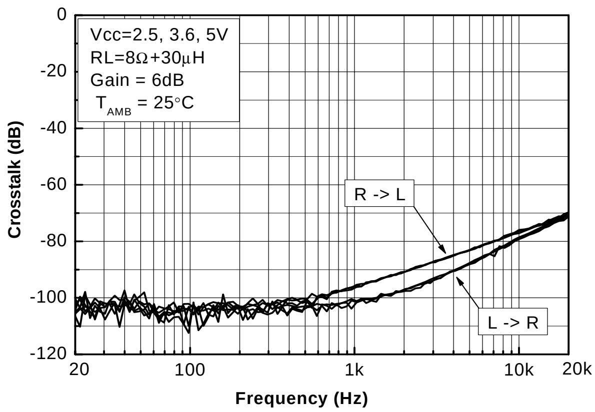


Figure 40. Crosstalk vs. frequency

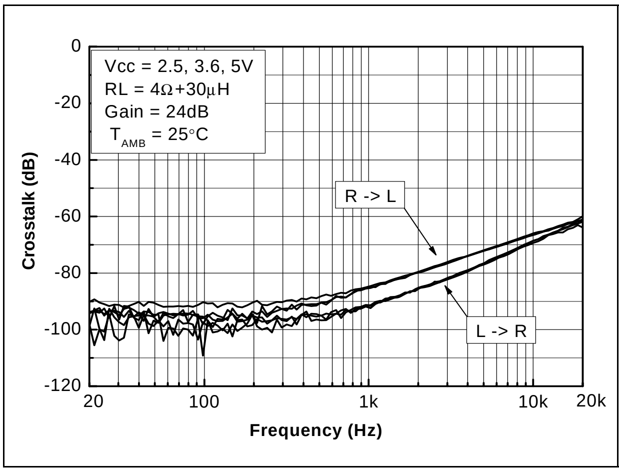


Figure 41. Crosstalk vs. frequency

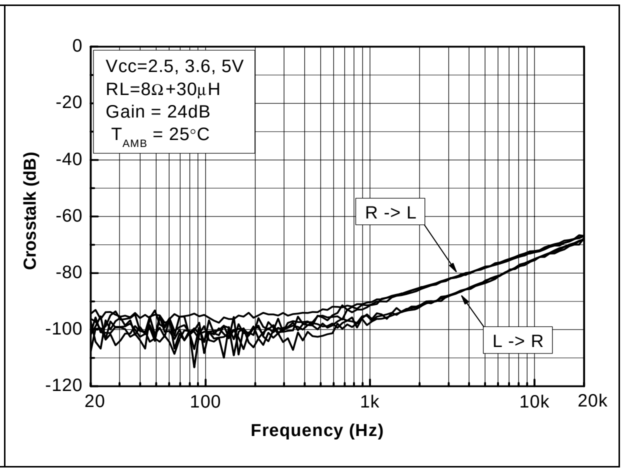


Figure 42. Power derating curves

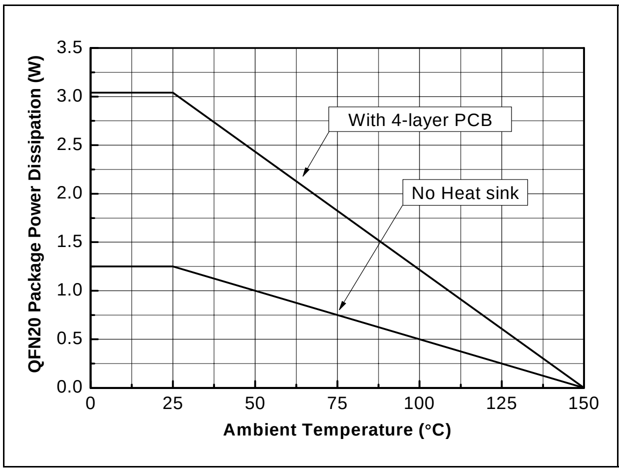


Figure 43. Startup and shutdown phase V_{CC}=5V, G=6dB, C_{in}=1µF, inputs grounded

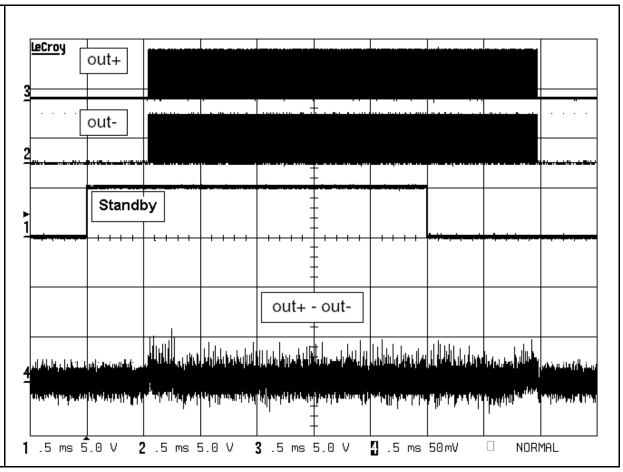
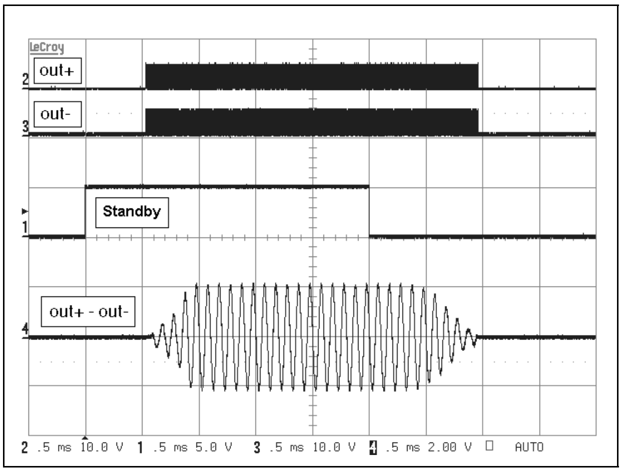


Figure 44. Startup and shutdown phase V_{CC}=5V, G=6dB, C_{in}=1µF, V_{in}=2V_{pp}, F=10kHz



4 Application information

4.1 Differential configuration principle

The TS2012 is a monolithic fully-differential input/output class D power amplifier. The TS2012 also includes a common-mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially compared with a single-ended topology, the output is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- High PSRR (power supply rejection ratio)
- High common mode noise rejection
- Virtually zero pop without additional circuitry, giving a faster start-up time compared with conventional single-ended input amplifiers
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required thanks to common mode feedback loop

4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to 6, 12 18, 24 dB depending on the logic level of the G0 and G1 pins, as shown in *Table 9*.

Table 9. Gain settings with G0 and G1 pins

G1	G0	Gain (dB)	Gain (V/V)
0	0	6	2
0	1	12	4
1	0	18	8
1	1	24	16

Note: Between pins G0, G1 and GND there is an internal 300kΩ(+/-20%) resistor. When the pins are floating, the gain is 6 dB. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).

4.3 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{ic} limitation of the input stage (see *Table 2: Operating conditions on page 4*), the common mode feedback loop can fulfil its role only within the defined range.

4.4 Low frequency response

If a low frequency bandwidth limitation is required, it is possible to use input coupling capacitors. In the low frequency region, the input coupling capacitor C_{in} starts to have an effect. C_{in} forms, with the input impedance Z_{in}, a first order high-pass filter with a -3dB cut-off frequency (see *Table 5* to *Table 7*):

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

So, for a desired cut-off frequency F_{CL} C_{in} is calculated as follows:

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

with F_{CL} in Hz, Z_{in} in Ω and C_{in} in F.

The input impedance Z_{in} is for the whole power supply voltage range, typically 30kΩ. There is also a tolerance around the typical value (see *Table 5* to *Table 7*). You can also calculate the tolerance of the F_{CL}:

- $F_{CLmax} = 1.103 \cdot F_{CL}$
- $F_{CLmin} = 0.915 \cdot F_{CL}$

4.5 Decoupling of the circuit

Power supply capacitors, referred to as C_S,C_{SL},C_{SR} are needed to correctly bypass the TS2012.

The TS2012 has a typical switching frequency of 280kHz and output fall and rise time about 5ns. Due to these very fast transients, careful decoupling is mandatory.

A 1µF ceramic capacitor between each PVCC and PGND and also between AVCC and AGND is enough, but they must be located very close to the TS2012 in order to avoid any extra parasitic inductance created by a long track wire. Parasitic loop inductance, in relation with di/dt, introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, a TS2012 breakdown.

In addition, even if a ceramic capacitor has an adequate high frequency ESR value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1µF/6.3V capacitor used at 5V, loses about 50% of its value. With a power supply voltage of 5V, the decoupling value, instead of 1µF, could be reduced to 0.5µF. As C_S has particular influence on the THD+N in the medium to high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots which can be problematic if they reach the power supply AMR value (6V).

4.6 Wake-up time (t_{wu})

When the standby is released to set the device ON, there is a delay of 1ms typically. The TS2012 has an internal digital delay that mutes the outputs and releases them after this time in order to avoid any pop noise.

Note: The gain increases smoothly (see Figure 44) from the mute to the gain selected by the G1 and G0 pin (Section 4.2).

4.7 Shutdown time

When the standby command is set, the time required to set the output stage considered into high impedance and to put the internal circuitry in shutdown mode, is typically 1ms. This time is used to decrease the gain and avoid any pop noise during shutdown.

Note: The gain decreases smoothly until the outputs are muted (see Figure 44).

4.8 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300kΩ (+-/20%) resistor. This resistor forces the TS2012 to be in shutdown when the shutdown input is left floating.

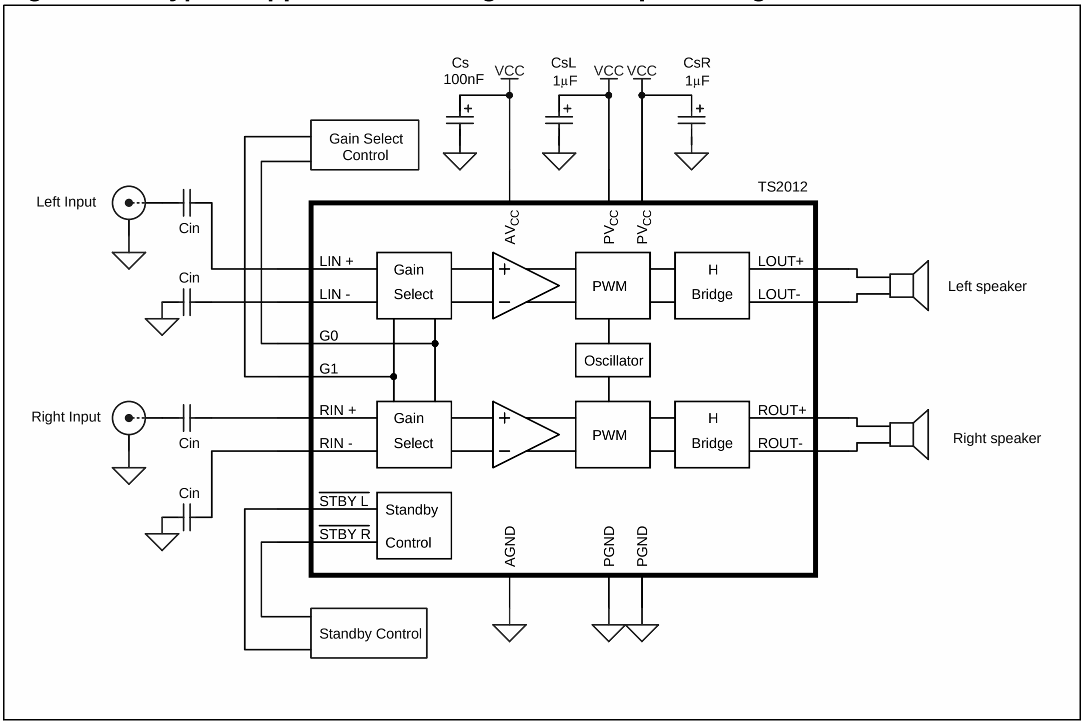
However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not 0V.

With a 0.4V shutdown voltage pin for example, you must add 0.4V/300kΩ=1.3µA in typical (0.4V/240kΩ=1.66µA in maximum for each shutdown pin) to the standby current specified in Table 5 to Table 7. Of course, this current will be provided by the external control device for standby pins.

4.9 Single-ended input configuration

It is possible to use the TS2012 in a single-ended input configuration. However, input coupling capacitors are mandatory in this configuration. The schematic diagram in Figure 45 shows a typical single-ended input application.

Figure 45. Typical application for single-ended input configuration



4.10 Output filter considerations

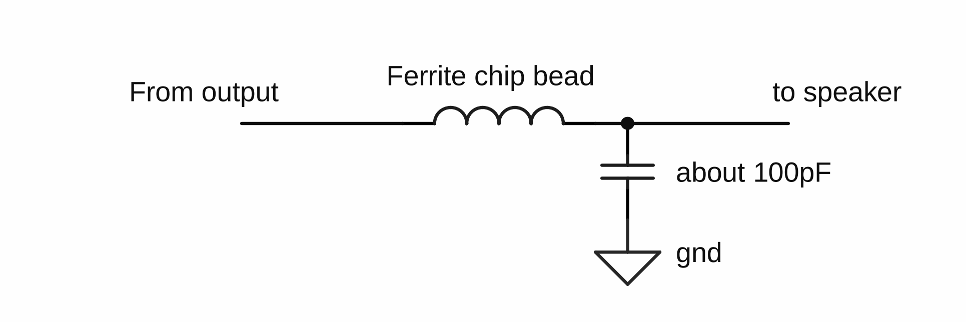
The TS2012 is designed to operate without an output filter. However, due to very sharp transients on the TS2012 output, EMI radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS2012 outputs and loudspeaker terminal are long (typically more than 50mm, or 100mm in both directions, to the speaker terminals). As the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow:

- Reduce, as much as possible, the distance between the TS2012 output pins and the speaker terminals.
- Use a ground plane for “shielding” sensitive wires.
- Place, as close as possible to the TS2012 and in series with each output, a ferrite bead with a rated current of minimum 2.5A and impedance greater than 50Ω at frequencies above 30MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow extra footprint to place, if necessary, a capacitor to short perturbations to ground (see *Figure 46*).

Figure 46. Ferrite chip bead placement



In the case where the distance between the TS2012 output and the speaker terminals is too long, it is possible to have low frequency EMI issues due to the fact that the typical operating frequency is 280kHz. In this configuration, it is necessary to use the output filter represented in *Figure 1 on page 5* as close as possible to the TS2012.

5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 47. QFN20 package mechanical drawing

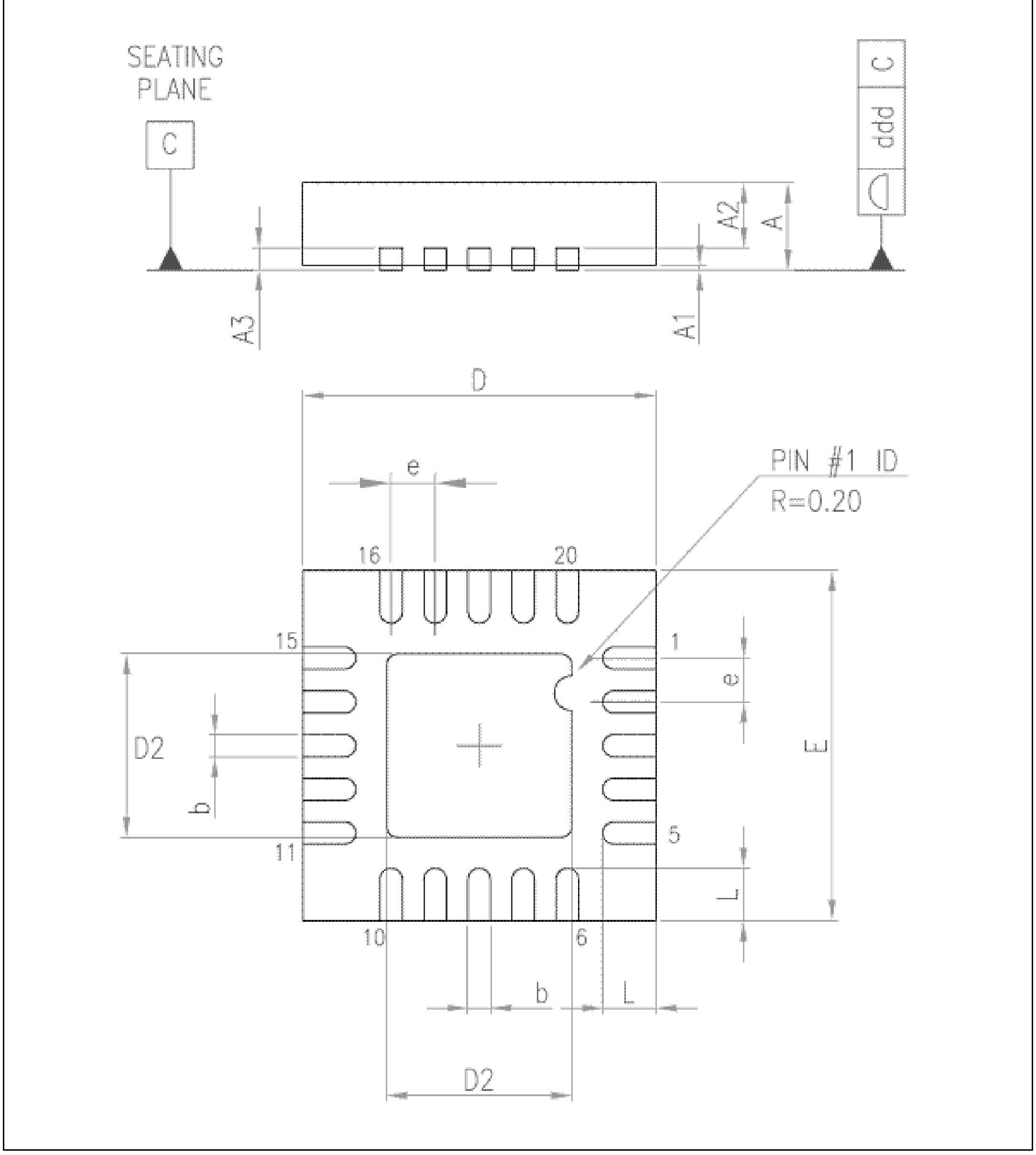
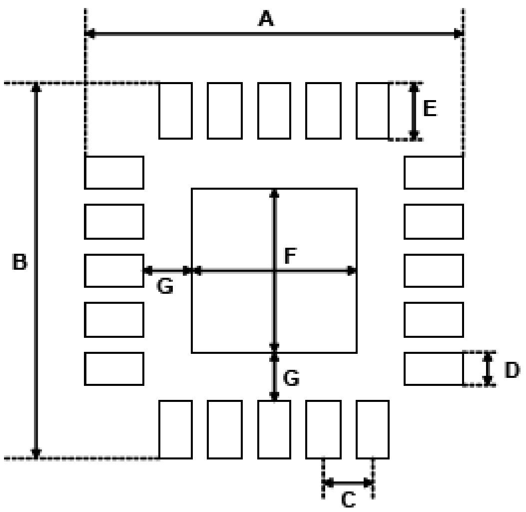


Table 10. QFN20 package mechanical data

Ref	Dimensions in mm		
	Min	Typ	Max
A	0.8	0.9	1
A1		0.02	0.05
A2		0.65	1
A3		0.25	
b	0.18	0.23	0.3
D	3.85	4	4.15
D2		2.6	
E	3.85	4	4.15
E2		2.6	
e	0.45	0.5	0.55
L	0.3	0.4	0.5
ddd			0.08

Figure 48. QFN20 package footprint



FOOTPRINT DATA (mm)	
A	4.55
B	4.55
C	0.50
D	0.35
E	0.65
F	2.45
G	0.40

Note: The QFN20 package has an exposed pad E2 x D2. For enhanced thermal performance, the exposed pad must be soldered to a copper area on the PCB, acting as a heatsink. This copper area can be electrically connected to pin 4, 12, 18 (PGND, AGND) or left floating.

6 Ordering information

Table 11. Order code

Part number	Temperature range	Package	Packaging	Marking
TS2012IQT	-40°C to +85°C	QFN20	Tape & reel	K12

7 Revision history

Table 12. Document revision history

Date	Revision	Changes
17-Dec-2007	1	First release.