TSH95

High-speed low-power quad operational amplifier with dual standby position

Features

- Low supply current: 4.5 mA
- High speed: 150 MHz - 110 V/µs
- Unity gain stability
- Low offset voltage: 4 mV
- Low noise 4.2 nV/√Hz
- Specified for 600 Ω and 150 Ω loads
- High video performances:
  - differential gain: 0.03%
  - differential phase: 0.07°
  - gain flatness: 6 MHz, 0.1 dB max. at 10 db gain

Applications

- Video buffers
- A/D converter drivers

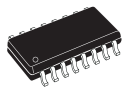
Description

The TSH95 is a low-power, high-frequency quad operational amplifier designated for high-quality video processing. The device offers an excellent speed consumption ratio with 4.5 mA per amplifier for a 150 MHz bandwidth.

A high slew rate and low noise also make it suitable for high-quality audio applications.

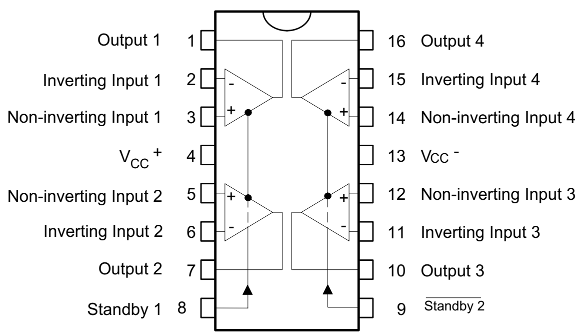
The TSH95 offers two separate complementary STANDBY pins**:** STANDBY 1 acting on operators 1 and 2, and STANDBY 2 acting on operators 3 and 4.

These pins reduce the consumption of the corresponding operators and put the output in a high impedance state.



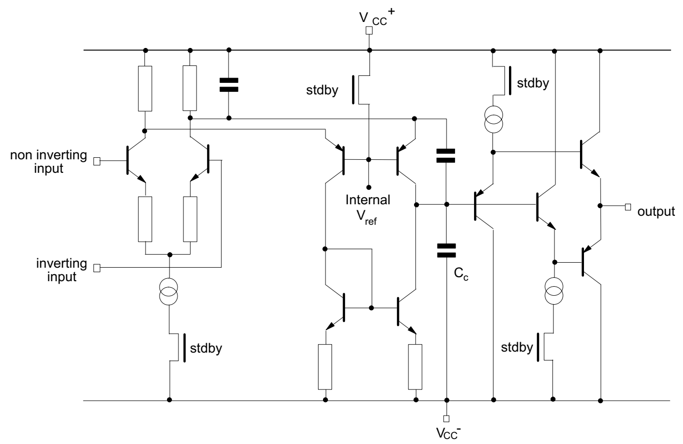
D
SO16
(Plastic micropackage)

Pin connections (top view)



1 Schematic diagram

Figure 1. Schematic diagram



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	14	V
V_{id}	Differential input voltage (2)	±5	V
V_i	Input voltage (3)	-0.3 to 12	V
T_{oper}	Operating free-air temperature range	-40 to +125	°C
T_{stg}	Storage temperature range	-65 to +150	°C
ESD	CDM: charged device model(4) HBM: human body model(5) MM: machine model(6)	1.5 2 200	kV kV V

1. All voltages values, except differential voltage, are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3 V.
4. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
5. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	7 to 12	V
V_{ic}	Common mode input voltage range	V_{CC}^- +2 to V_{CC}^+ -1	V

3 Electrical characteristics

Table 3. $V_{CC}+ = 5$ V, $V_{CC}- = -5$ V, pin 8 connected to 0 V, pin 9 connected to $V_{CC}+$, $T_{amb} = 25°$ C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage $V_{ic} = V_o = 0$ V $T_{min.} \leq T_{amb} \leq T_{max.}$			4 6	mV
I_{io}	Input offset current $T_{min.} \leq T_{amb} \leq T_{max.}$		1	2 5	µA
I_{ib}	Input bias current $T_{min.} \leq T_{amb} \leq T_{max.}$		5	15 20	µA
I_{CC}	Supply current (per amplifier, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		4.5	6 8	mA
CMR	Common-mode rejection ratio $V_{ic} = -3$ V to +4 V, $V_o = 0$ V $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
SVR	Supply voltage rejection ratio $V_{CC} = \pm 5$ V to ± 3 V $T_{min.} \leq T_{amb} \leq T_{max.}$	60 50	75		dB
Avd	Large signal voltage gain $R_L = 10$ kΩ, Vo = ±2.5 V $T_{min.} \leq T_{amb} \leq T_{max.}$	57 54	70		dB
V_{OH}	High level output voltage $V_{id} = 1$ V $R_L = 600$ Ω $R_L = 150$ Ω $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 150$ Ω	3 2.5 2.4	3.5 3		V
V_{OL}	Low level output voltage $V_{id} = 11$ V $R_L = 600$ Ω $R_L = 150$ Ω $T_{min.} \leq T_{amb} \leq T_{max.}$ $R_L = 150$ Ω		-3.5 -2.8	-3 -2.5 -2.4	V
I_o	Output short circuit current Vid = ±1 V Source Sink $T_{min.} \leq T_{amb} \leq T_{max.}$ Source Sink	20 20 15 15	36 40		mA
GBP	Gain bandwidth product $A_{VCL} = 100$, $R_L = 600$ Ω, $C_L = 15$ pF, f = 7.5 MHz	90	150		MHz
f_T	Transition frequency		90		MHz
SR	Slew rate $V_{in} = -2$ to +2 V, $R_L = 600$ Ω, $C_L = 15$ pF	62	110		V/µs
e_n	Equivalent input voltage noise $R_s = 50$ Ω, f = 1 kHz		4.2		nV/√Hz
ϕm	Phase margin $A_{VM} = +1$		35		Degrees
V_{O1}/V_{O2}	Channel separation f = 1 MHz to 10 MHz		65		dB
Gf	Gain flatness f = DC to 6 MHz, $A_{VCL} = 10$ dB			0.1	dB
THD	Total harmonic distortion f = 1 kHz, $V_o = \pm 2.5$ V, $R_L = 600$ Ω		0.01		%

Table 3. $V_{CC}+$ = 5 V, $V_{CC}-$ = -5 V, pin 8 connected to 0 V, pin 9 connected to $V_{CC}+$, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔG	Differential gain f = 3.58 MHz, A_{VCL} = +2, R_L = 150 Ω		0.03		%
Δφ	Differential phase f = 3.58 MHz, A_{VCL} = +2, R_L = 150 Ω		0.07		Degree

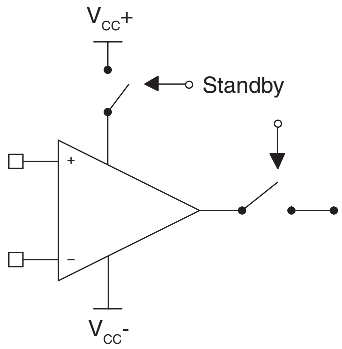
Table 4. Standby mode: $V_{CC}+$ = 5 V, $V_{CC}-$ = -5 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SBY}	Pin 8/9 threshold voltage for STANDBY mode	V_{CC}^{+} -2.2	V_{CC}+ -1.6	V_{CC}+ - 1.0	V
$I_{CC\ SBY}$	Total consumption: Pin 8 (Standby 1) = 0, Pin 9 ($\overline{\text{Standby 2}}$) = 0 Pin 8 (Standby 1) = 0, Pin 9 ($\overline{\text{Standby 2}}$) = 1 Pin 8 (Standby 1) = 0, Pin 9 ($\overline{\text{Standby 2}}$) = 0		 9.4 9.4 0.8		mA
I_{sol}	Input/output isolation (f = 1 MHz to 10 MHz)		70		dB
t_{ON}	Time from Standby mode to Active mode		200		ns
t_{OFF}	Time from Active mode to Standby mode		200		ns
I_D	Standby driving current		2		pA
I_{OL}	Output leakage current		20		pA
I_{IL}	Input leakage current		20		pA

Table 5. Standby control pin status

Logic input		Status	
Standby 1	**Standby 2**	**Op-amps 1 and 2**	**Op-amps 2 and 3**
0	0	Enable	Standby
0	1	Enable	Enable
1	0	Standby	Standby
1	1	Standby	Enable

Figure 2. Standby position



To put the device in standby, a logic level must be applied on the standby MOS input. Since ground is a virtual level for the device, the threshold voltage has been referred to V_{CC+} at V_{CC+} -1.6 V typical.

In standby mode, the output goes into high impedance in 200 ns. Note that all maximum ratings must still be followed in this mode. This mode leads to a swing limitation while using the device in a signal multiplexing configuration with followers; the differential input voltage must not exceed ±5 V, limiting the input swing to 2.5 Vpp.

4 Application information

Figure 3. Signal multiplexing

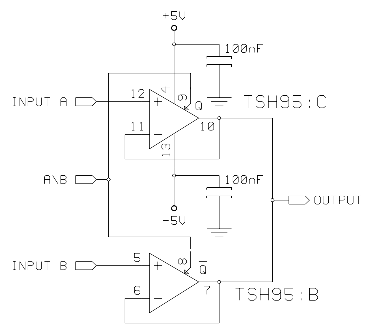
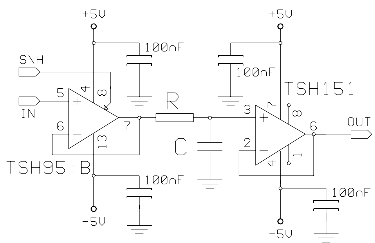


Figure 4. Sample and hold



4.1 Printed circuit layout recommendations

As with any high-frequency device, a few rules must be observed when designing the PCB so as to maximize performance.

From the most to the least important points:

- Each power supply lead must be bypassed to ground with a 10 nF ceramic capacitor and a 10 µF capacitor placed very close to the device.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible, especially for the inputs, in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease the time constant with parasitic capacitance.
- Choose the smallest-possible component sizes (SMD).
- Decrease the capacitor load at the output to avoid degrading the circuit's stability and cause oscillation. You can also add a serial resistor to minimize its influence.

Figure 5. Large signal follower response

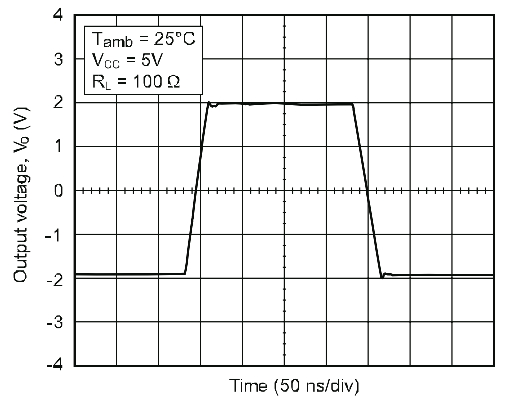


Figure 6. Static open-loop voltage gain

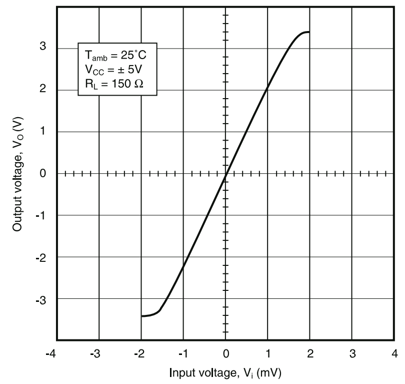


Figure 7. Input offset voltage drift versus temperature

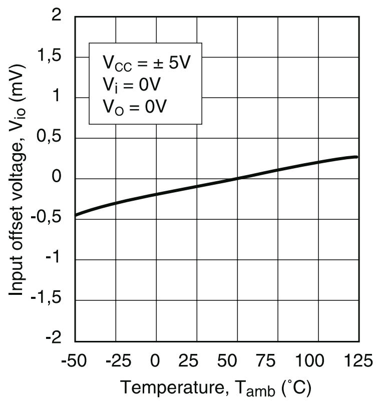


Figure 8. Small signal follower response

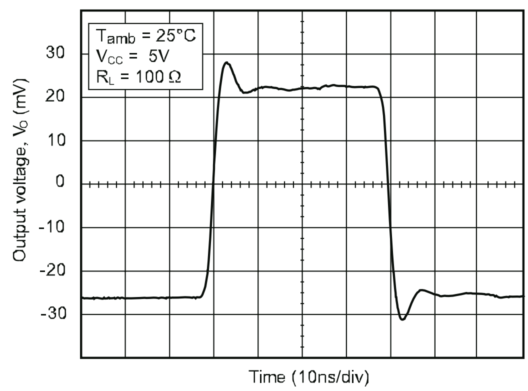


Figure 9. Closed-loop frequency response and phase shift

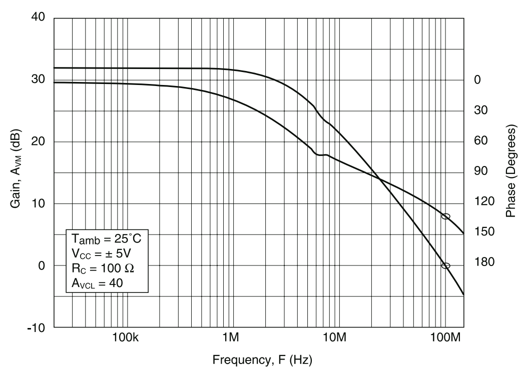


Figure 10. Closed-lop frequency response

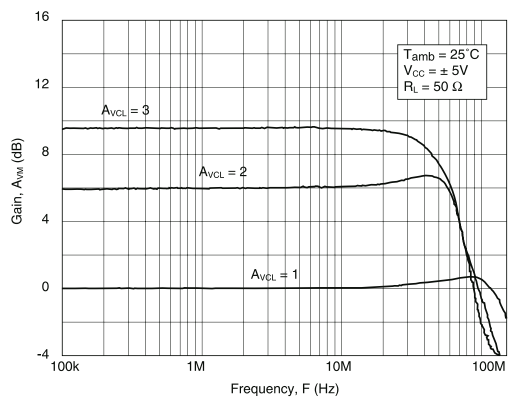


Figure 11. Audio bandwidth frequency response & phase shift (TSH95 vs standard 15 MHz audio op-amp)

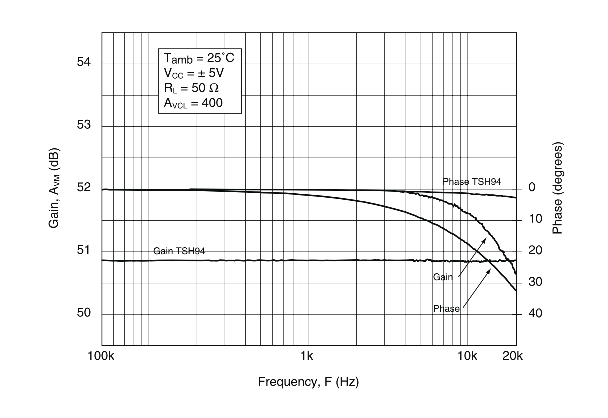


Figure 12. Gain flatness and phase shift vs. frequency

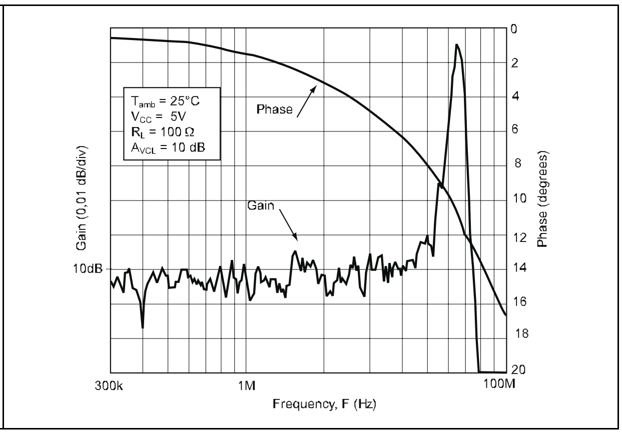


Figure 13. Crosstalk isolation vs. frequency (SO-16 package)

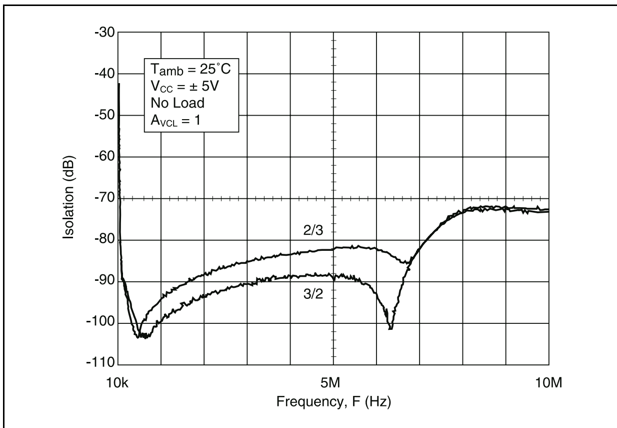


Figure 14. Crosstalk isolation vs. frequency (SO-16 package)

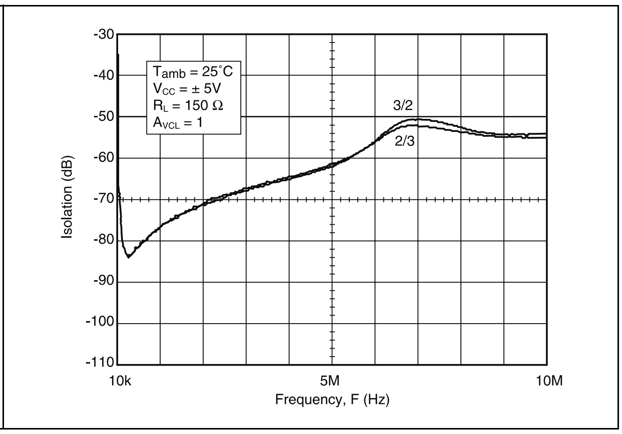


Figure 15. Input/output isolation in standby mode (SO-16 package)

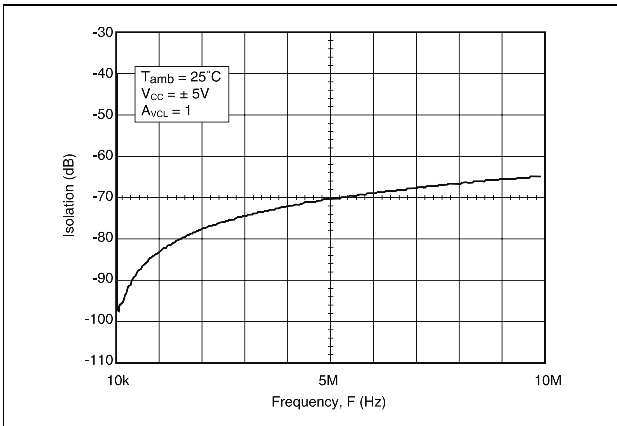


Figure 16. Standby switching

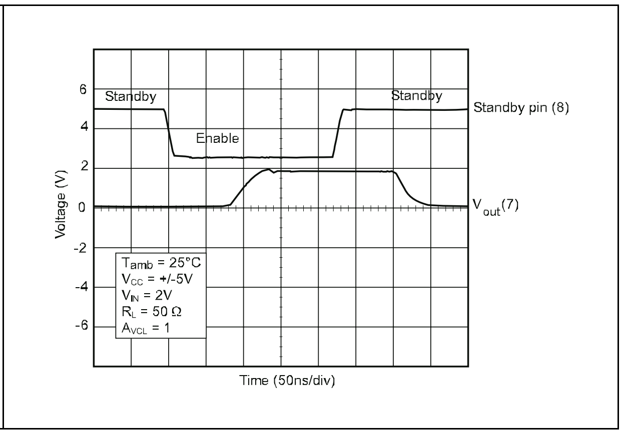


Figure 17. Signal multiplexing

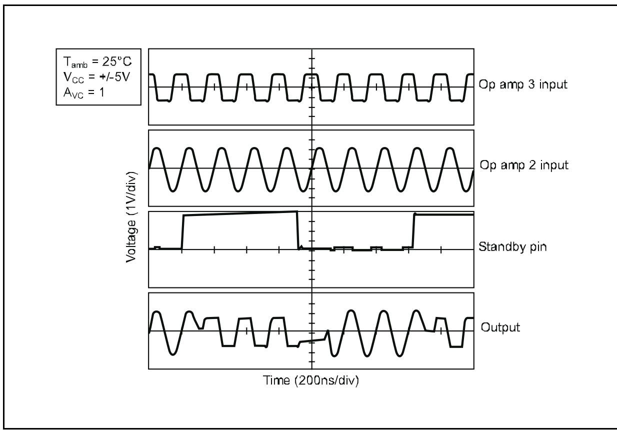


Figure 18. Differential input impedance versus frequency

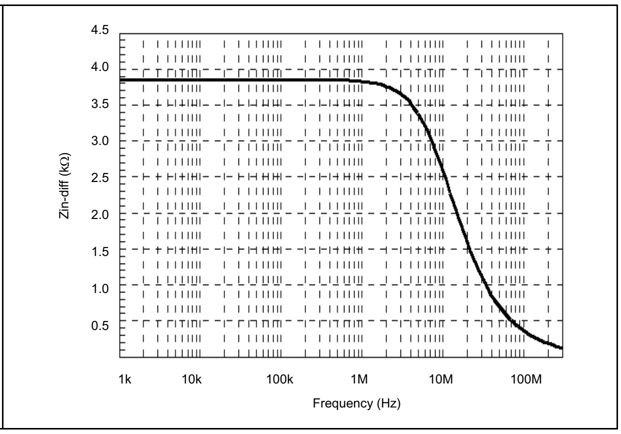
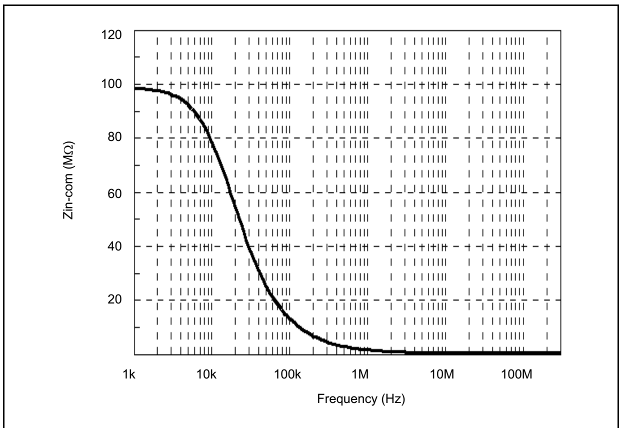


Figure 19. Common input impedance versus frequency



5 Macromodel information

The information below applies to the TSH95I.

```
** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
* 6 STANDBY
.SUBCKT TSH95 1 3 2 4 5 6 (analog)
*********************************************************
**************** switch ******************
.SUBCKT SWITCH 20 10 IN OUT COM
.MODEL DIDEAL D N=0.1 IS=1E-08
DP IN 1 DIDEAL 400E-12
DN OUT 2 DIDEAL 400E-12
EP 1 OUT COM 10 2
EN 2 IN COM 10 2
RFUIT1 IN 1 1E+09
RFUIT2 OUT 2 1E+09
RCOM COM 0 1E+12
.ENDS SWITCH
**************** inverter *****************
.SUBCKT INV 20 10 IN OUT
.MODEL DIDEAL D N=0.1 IS=1E-08
RP1 20 15 1E+09
RN1 15 10 1E+09
RIN IN 10 1E+12
RIP IN 20 1E+12
DPINV OUT 20 DIDEAL 400E-12
DNINV 10 OUT DIDEAL 400E-12
GINV 0 OUT IN 15 -6.7E-7
CINV 0 OUT 210f
```

```
.ENDS INV
***************** AOP *********************
.MODEL MDTH D IS=1E-8 KF=1.809064E-15
CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E-01
RIN 15 16 2.600000E-01
RIS 11 15 3.645298E-01
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 1314DC 0
FPOL 13 5 VSTB 1E+03
CPS 11 15 2.986990E-10
DINN 17 13 MDTH 400E-12
VIN 17 5 2.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 1.000000E+00
FCP 4 5 VOFP 3.500000E+00
FCN 5 4 VOFN 3.500000E+00
ISTB0 4 5 130UA
FIBP 2 5 VOFP 1.000000E-02
FIBN 5 1 VOFN 1.000000E-02
* AMPLIFYING STAGE
FIP 5 19 VOFP 2.530000E+02
FIN 5 19 VOFN 2.530000E+02
RG1 19 120 3.160721E+03
XCOM1 4 0 120 5 COM SWITCH
RG2 19 121 3.160721E+03
```

```
XCOM2 4 0 4 121 COM SWITCH
CC 19 5 2.00000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 1.504000E+03
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 1.400000E+03
VINM 5 27 5.000000E+01
*********** ZP **********
RZP1 5 80 1E+06
RZP2 4 80 1E+06
GZP 5 82 19 80 2.5E-05
RZP2H 83 4 10000
RZP1H 83 82 80000
RZP2B 84 5 10000
RZP1B 82 84 80000
LZPH 4 83 3.535e-02
LZPB 84 5 3.535e-02
**************************
EOUT26 2382 51
VOUT 23 5 0
ROUT 26 103 35
COUT 103 5 30.000000E-12
XCOM 4 0 103 3 COM SWITCH
DOP 19 25 MDTH 400E-12
VOP 4 25 2.361965E+00
DON 24 19 MDTH 400E-12
VON 24 5 2.361965E+00
********** STAND BY ********
RMI1 4 111 1E+7
```

```
RMI2 0 111 2E+7
RONOFF 6 60 1K
CONOGG 60 0 10p
RSTBIN 60 0 1E+12
ESTBIN 106 0 6 0 1
ESTBREF 106 107 111 0 1
DSTB1 107 108 MDTH 400E-12
VSTB 108 109 0
ISTB 109 0 1U
RSTB 109 110 1
DSTB2 0 110 MDTH 400E-12
XINV 4 0 6 COM INV
.ENDS
```

Table 6. Electrical characteristics with V_{CC} = ±5 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 600 Ω	3.2	V/mV
I_{CC}	No load/amplifier	5.2	mA
V_{icm}		-3 to 4	V
V_{OH}	R_L = 600 Ω	+3.6	V
V_{OL}	R_L = 600 Ω	-3.6	V
I_{sink}	V_o = 0 V	40	mA
I_{source}	V_o = 0 V	40	mA
GBP	R_L = 600 Ω, C_L = 15 pF	147	MHz
SR	R_L = 600 Ω, C_L = 15 pF	110	V/µs
φm	R_L = 600 Ω, C_L = 15 pF	42	Degrees

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

6.1 SO-16 package information

Figure 20. SO-16 package mechanical drawing

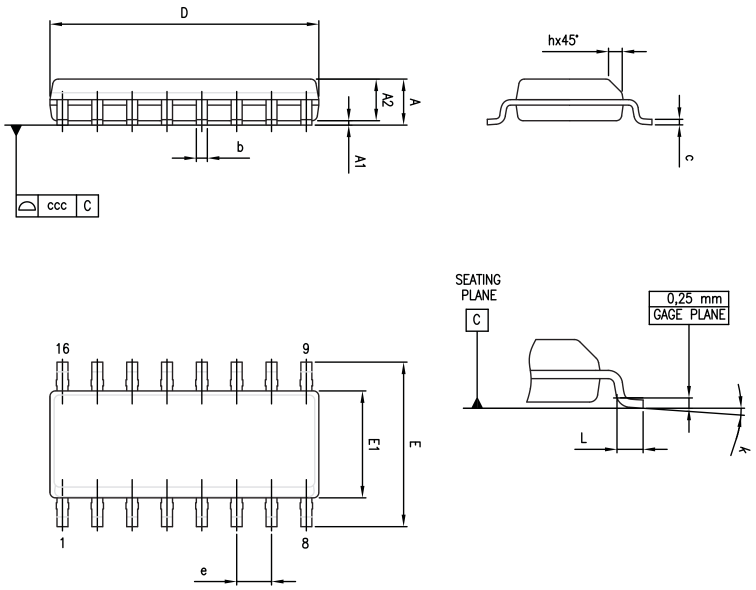


Table 7. SO-16 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.31		0.51	0.012		0.020
c	0.17		0.25	0.007		0.010
D(1)	9.80	9.90	10.00	0.386	0.390	0.394
E	5.80	6.00	6.20	0.228	0.236	0.244
E1(2)	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0		8			
ccc			0.10			0.004

1. Does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs not to exceed 0.15 mm in total.
2. Does not include interlead flash or protrusions. Interlead flash or protrusions not to exceed 0.25 mm per side.

7 Ordering information

Table 8. Order codes

<table>
<tr><th>Part number</th><th>Temperature range</th><th>Package</th><th>Packing</th><th>Marking</th></tr>
<tr><td>TSH95ID</td><td rowspan="4">-40° C to +125° C</td><td rowspan="2">SO-16</td><td rowspan="4">Tube or
Tape & reel</td><td rowspan="2">TSH95I</td></tr>
<tr><td>TSH95IDT</td></tr>
<tr><td>TSH95IYD(1)</td><td rowspan="2">SO-16
(Automotive grade)</td><td rowspan="2">TSH95IY</td></tr>
<tr><td>TSH95IYDT(1)</td></tr>
</table>

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q 002 or equivalent are on-going.

8 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Nov-2000	1	Initial release.
27-Aug-2009	2	Document format updated. Updated SO-16 package information in *Chapter 6*. Added automotive grade order codes in *Table 8*.