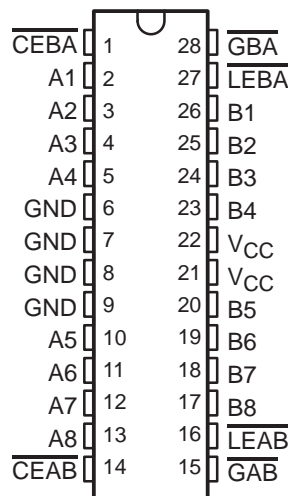


# 74ACT11543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS136 – D3608, JULY 1990 – REVISED APRIL 1993

- Inputs Are TTL-Voltage Compatible
- 3-State True Outputs
- Back-to-Back Registers for Storage
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C

DW PACKAGE  
(TOP VIEW)



## description

This 8-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ( $\overline{LEAB}$  or  $\overline{LEBA}$ ) and output enable ( $\overline{GAB}$  or  $\overline{GBA}$ ) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable ( $\overline{CEAB}$ ) input must be low in order to enter data from A or to output data to B. Having  $\overline{CEAB}$  low and  $\overline{LEAB}$  low makes the A-to-B latches transparent; a subsequent low-to-high transition of  $\overline{LEAB}$  puts the A latches in the storage mode. With  $\overline{CEAB}$  and  $\overline{GAB}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B-to-A is similar, but requires the use of  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{GBA}$  inputs.

The 74ACT11543 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS			LATCH STATUS A TO B†	OUTPUT BUFFERS B1 THRU B8
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{GAB}$		
H	X	X	Storing	Z
X	H		Storing	
X		H		Z
L	L	L	Transparent	Current A Data
L	H	L	Storing	Previous‡ A Data

† A-to-B data flow is shown: B-to-A flow control is the same except uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{GBA}$ .

‡ Data present before low-to-high transition of  $\overline{LEAB}$ .

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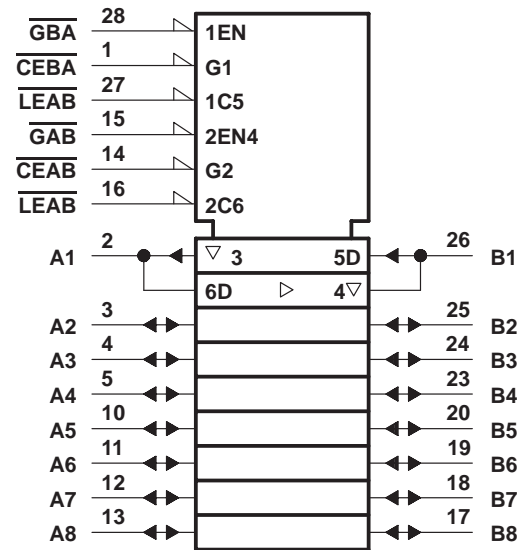
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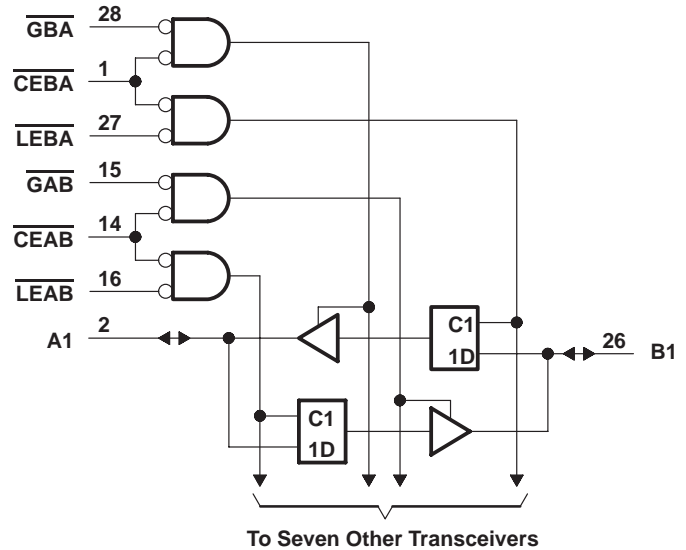
# 74ACT11543 OCTAL REGISTERED TRANSCEIVER WITH 3-STATE OUTPUTS

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 200$ mA
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$V_I$ Input voltage	0		$V_{CC}$	V
$V_O$ Output voltage	0		$V_{CC}$	V
$I_{OH}$ High-level output current			-24	mA
$I_{OL}$ Low-level output current			24	mA
$\Delta t/\Delta v$ Input transition rise or fall rate	0		10	ns/V
$T_A$ Operating free-air temperature	-40		85	°C

**74ACT11543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = – 50 μA	4.5 V	4.4			4.4	V	
		5.5 V	5.4			5.4		
	I <sub>OH</sub> = – 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
I <sub>OH</sub> = – 75 mA†	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	I <sub>OL</sub> = 24 mA	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
	I <sub>OL</sub> = 75 mA†	5.5 V				1.65		
I <sub>I</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.1	± 1	μA
I <sub>OZ</sub>	A or B ports‡	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			± 0.5	± 5	μA
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			8	80	μA
ΔI <sub>CC</sub> §		One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			0.9	1	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			4.5		pF
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			12		pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

‡ For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}$ low	4		4		ns
t <sub>su</sub>	Setup time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	2.5		2.5	ns
		Data before $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	3		3	
t <sub>h</sub>	Hold time	Data after $\overline{\text{LEAB}}$ or $\overline{\text{LEBA}}\uparrow$	2		2	ns
		Data after $\overline{\text{CEAB}}$ or $\overline{\text{CEBA}}\uparrow$	1.5		1.5	

**74ACT11543**  
**OCTAL REGISTERED TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

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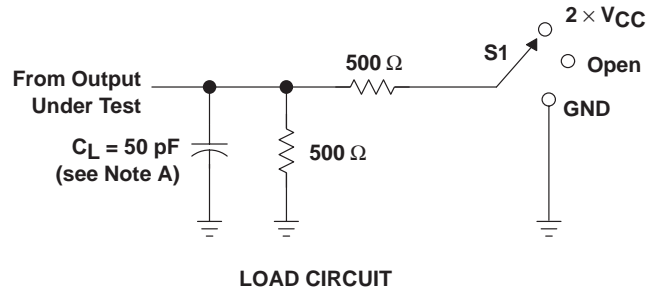
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	B or A	3.5	6.2	9.1	3.5	10.2	ns
t <sub>PHL</sub>			3.2	6.5	10.8	3.2	12.1	
t <sub>PLH</sub>	$\overline{\text{LEBA}}$ or $\overline{\text{LEAB}}$	A or B	3	6.1	10.1	3	11.2	ns
t <sub>PHL</sub>			3.7	7.2	11.7	3.7	13.2	
t <sub>PZH</sub>	$\overline{\text{CEBA}}$ or $\overline{\text{CEAB}}$	A or B	3.5	6.7	11.1	3.5	12.2	ns
t <sub>PZL</sub>			3.2	8.4	13.4	3.2	16	
t <sub>PHZ</sub>	CEBA or CEAB	A or B	4.8	7.3	10.1	4.8	11	ns
t <sub>PLZ</sub>			5.1	7.5	10.3	5.1	11.1	
t <sub>PZH</sub>	$\overline{\text{GBA}}$ or $\overline{\text{GAB}}$	A or B	3.3	6.4	10.5	3.3	11.5	ns
t <sub>PZL</sub>			3	8	12.8	3	15.3	
t <sub>PHZ</sub>	$\overline{\text{GBA}}$ or $\overline{\text{GAB}}$	A or B	4.6	6.9	9.6	4.6	10.4	ns
t <sub>PLZ</sub>			5	7.1	9.8	5	10.5	

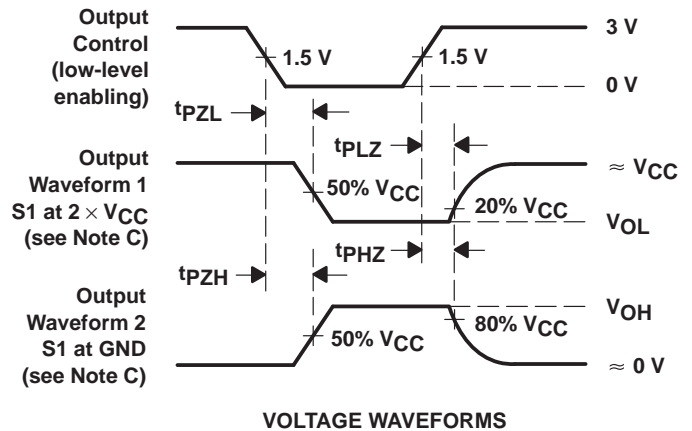
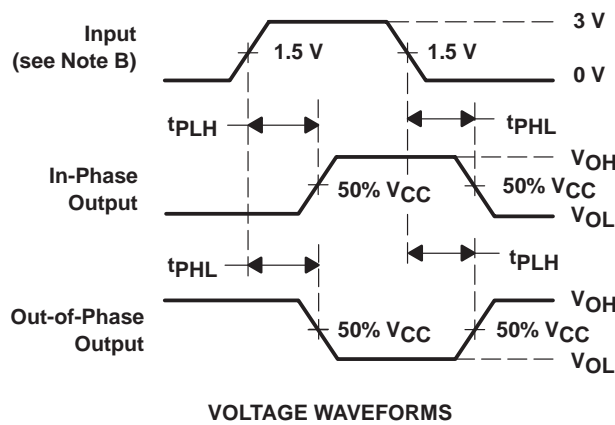
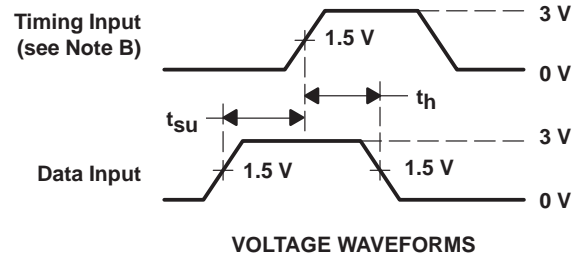
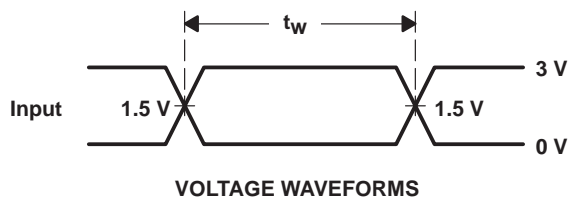
operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	47	pF
		Outputs disabled	13	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74ACT11543DWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11543DWRE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11543DWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT11543NT	OBSOLETE	PDIP	NT	28		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

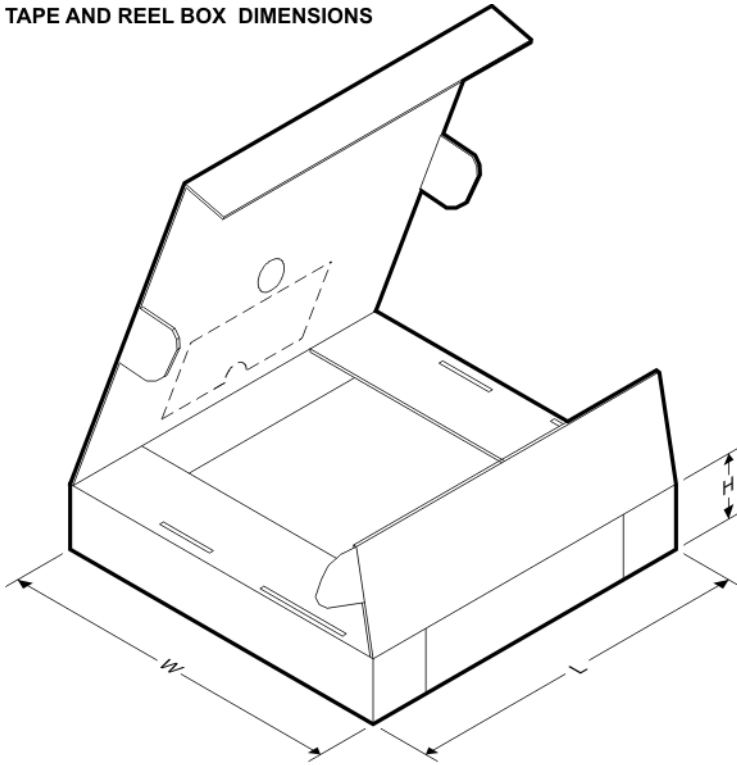


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT11543DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1



**TAPE AND REEL BOX DIMENSIONS**

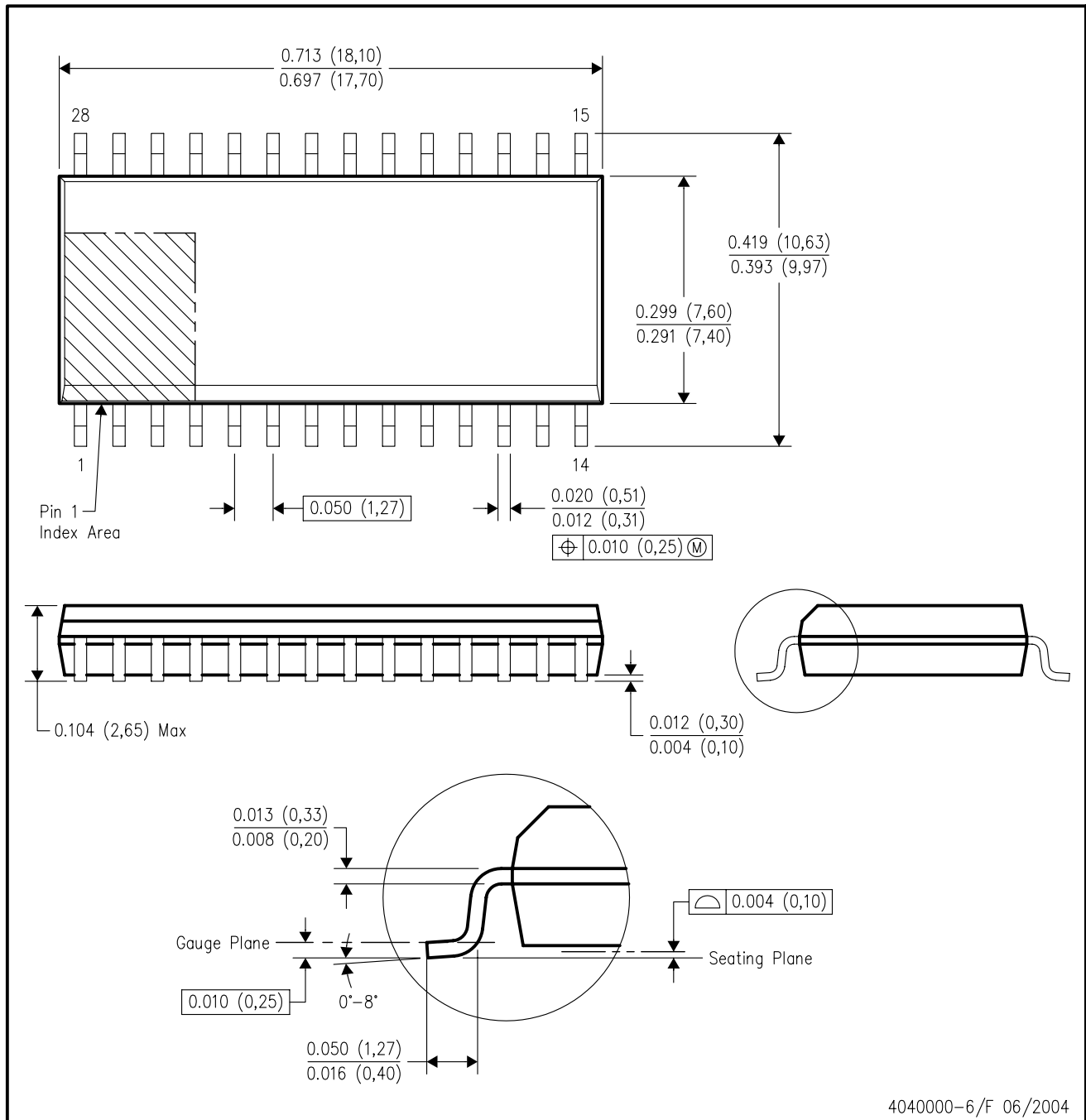


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT11543DWR	SOIC	DW	28	1000	346.0	346.0	49.0

DW (R-PDSO-G28)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

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