



10-Bit, 40MHz Sampling ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- HIGH SNR: 60dB
- HIGH SFDR: 72dBFS
- LOW POWER: 190mW
- INTERNAL/EXTERNAL REFERENCE OPTION
- SINGLE-ENDED OR FULLY DIFFERENTIAL ANALOG INPUT
- PROGRAMMABLE INPUT RANGE
- LOW DNL: 0.5LSB
- SINGLE +5V SUPPLY OPERATION

- +3V OR +5V LOGIC I/O COMPATIBLE (ADS825)
- POWER DOWN: 20mW
- SSOP-28 PACKAGE

APPLICATIONS

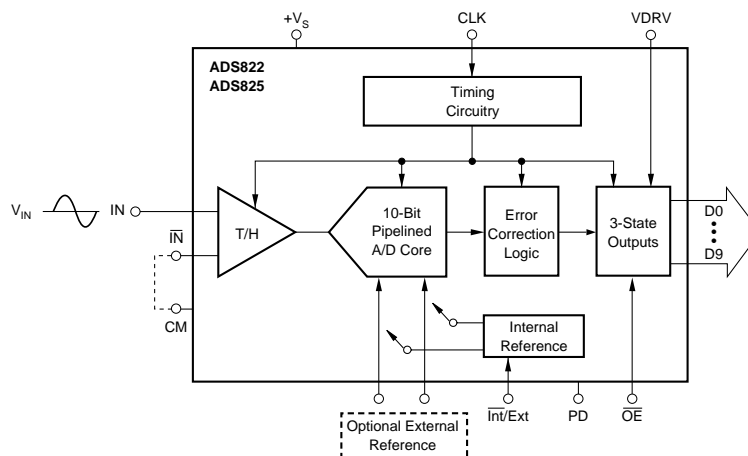
- MEDICAL IMAGING
- TEST EQUIPMENT
- COMPUTER SCANNERS
- COMMUNICATIONS
- VIDEO DIGITIZING

DESCRIPTION

The ADS822 and ADS825 are pipeline, CMOS Analog-to-Digital Converters (ADC) that operate from a single +5V power supply. These converters provide excellent performance with a single-ended input and can be operated with a differential input for added spurious performance. These high-performance converters include a 10-bit quantizer, high-bandwidth track-and-hold, and a high-accuracy internal reference. They also allow for the user to disable the internal reference and utilize external references. This external reference option provides excellent gain and offset matching when used in multichannel applications, or in applications where full-scale range adjustment is required.

The ADS822 and ADS825 employ digital error correction techniques to provide excellent differential linearity for demanding imaging applications. Its low distortion and high SNR give the extra margin needed for medical imaging, communications, video, and test instrumentation. The ADS822 and ADS825 offer power dissipation of 190mW and also provide a power-down mode, thus reducing power dissipation to only 20mW. The ADS825 is +3V or +5V logic I/O compatible.

The ADS822 and ADS825 are specified at a maximum sampling frequency of 40MSPS and a single-ended input range of 1.5V to 3.5V. The ADS822 and ADS825 are available in an SSOP-28 package and are pin-for-pin compatible with the 10-bit, 60MSPS ADS823 and ADS826, and the 10-bit, 75MSPS ADS828, providing an upgrade path to higher sampling frequencies.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | |
|----------------------------|-----------------------------------|
| +V _S | +6V |
| Analog Input | -0.3V to (+V _S + 0.3V) |
| Logic Input | -0.3V to (+V _S + 0.3V) |
| Case Temperature | +100°C |
| Junction Temperature | +150°C |
| Storage Temperature | +150°C |

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DEMO BOARD ORDERING INFORMATION

| PRODUCT | DEMO BOARD |
|---------|-------------|
| ADS822E | DEM-ADS822E |



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR ⁽¹⁾ | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|-----------------------------------|-----------------------------|-----------------|-----------------|---------------------------|
| ADS822 | SSOP-28 | DB | -40°C to +85°C | ADS822E | ADS822E | Rails, |
| " | " | " | " | " | ADS822E/1K | Tape and Reel, 1000 |
| ADS825 | SSOP-28 | DB | -40°C to +85°C | ADS825E | ADS825E | Rails, |
| " | " | " | " | " | ADS825E/1K | Tape and Reel, 1000 |

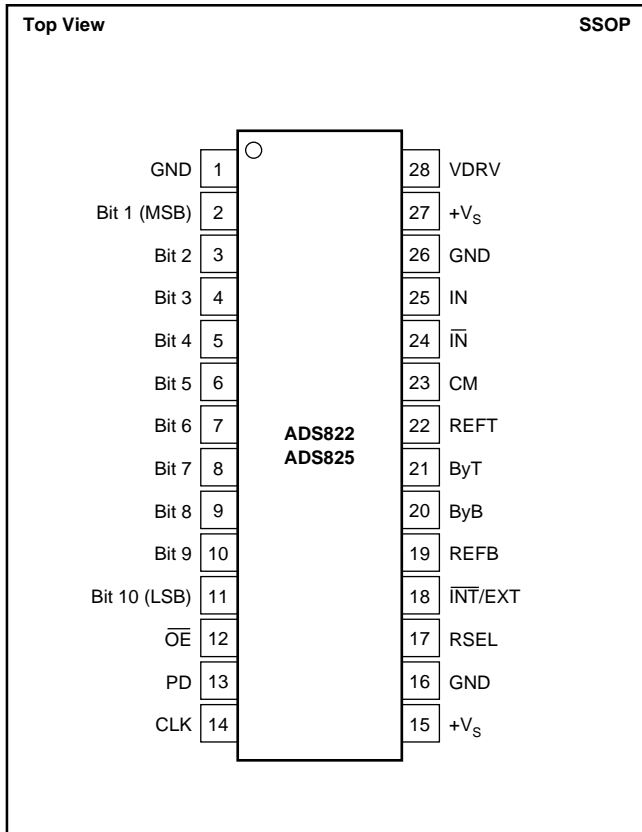
NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz and, external reference, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS822E | | | ADS825E ⁽¹⁾ | | | UNITS |
|--|---------------------------|---------|------------|------|------------------------|------------|-----|---------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| RESOLUTION | | | 10 | | | 10 | | Bits |
| SPECIFIED TEMPERATURE RANGE | Ambient Air | | -40 to +85 | | | -40 to +85 | | °C |
| ANALOG INPUT | | | | | | | | |
| Standard Single-Ended Input Range | 2Vp-p | 1.5 | | 3.5 | * | | * | V |
| Optional Single-Ended Input Range | 1Vp-p | 2 | | 3 | * | | * | V |
| Common-Mode Range | | | 2.5 | | | * | | V |
| Optional Differential Input Range | 2Vp-p | 2 | | 3 | * | | * | V |
| Analog Input Bias Current | | | 1 | | | * | | μA |
| Input Impedance | | | 1.25 5 | | | * | | MΩ pF |
| Track-Mode Input Bandwidth | -3dBFS Input | | 300 | | | * | | MHz |
| CONVERSION CHARACTERISTICS | | | | | | | | |
| Sample Rate | | 10k | | 40M | * | | * | Samples/s |
| Data Latency | | | 5 | | | * | | Clk Cyc |
| DYNAMIC CHARACTERISTICS | | | | | | | | |
| Differential Linearity Error (largest code error) | | | | | | | | |
| f = 1MHz | | | ±0.25 | ±1.0 | | * | * | LSB |
| f = 10MHz | | | ±0.5 | | | * | * | LSB |
| No Missing Codes | | | Tested | | | Tested | | |
| Integral Nonlinearity Error, f = 1MHz | | | ±0.5 | ±2.0 | | * | * | LSBs |
| Spurious-Free Dynamic Range ⁽²⁾ | Referred to Full-Scale | | | | | | | |
| f = 1MHz | | | 72 | | | 71 | | dBFS ⁽³⁾ |
| f = 10MHz | | 63 | 66 | | 60 | 65 | | dBFS |
| 2-Tone Intermodulation Distortion ⁽⁴⁾ | | | | | | | | |
| f = 9.5MHz and 9.9MHz (-7dB each tone) | Referred to Full-Scale | | -67 | | | * | | dBc |
| Signal-to-Noise Ratio (SNR) | Referred to Full-Scale | | | | | | | |
| f = 1MHz | | | 60 | | | * | | dB |
| f = 10MHz | | 57 | 60 | | * | * | | dB |
| Signal-to-(Noise + Distortion) (SINAD) | Referred to Full-Scale | | | | | | | |
| f = 1MHz | | | 59 | | | * | | dB |
| f = 10MHz | | 56 | 58 | | * | * | | dB |
| Effective Number of Bits ⁽⁵⁾ , f = 1MHz | | | 9.5 | | | * | | Bits |
| Output Noise | Input Tied to Common-Mode | | 0.2 | | | * | | LSBs rms |
| Aperture Delay Time | | | 3 | | | * | | ns |
| Aperture Jitter | | | 1.2 | | | * | | ps rms |
| Overvoltage Recovery Time | | | 2 | | | * | | ns |
| Full-Scale Step Acquisition Time | | | 5 | | | * | | ns |

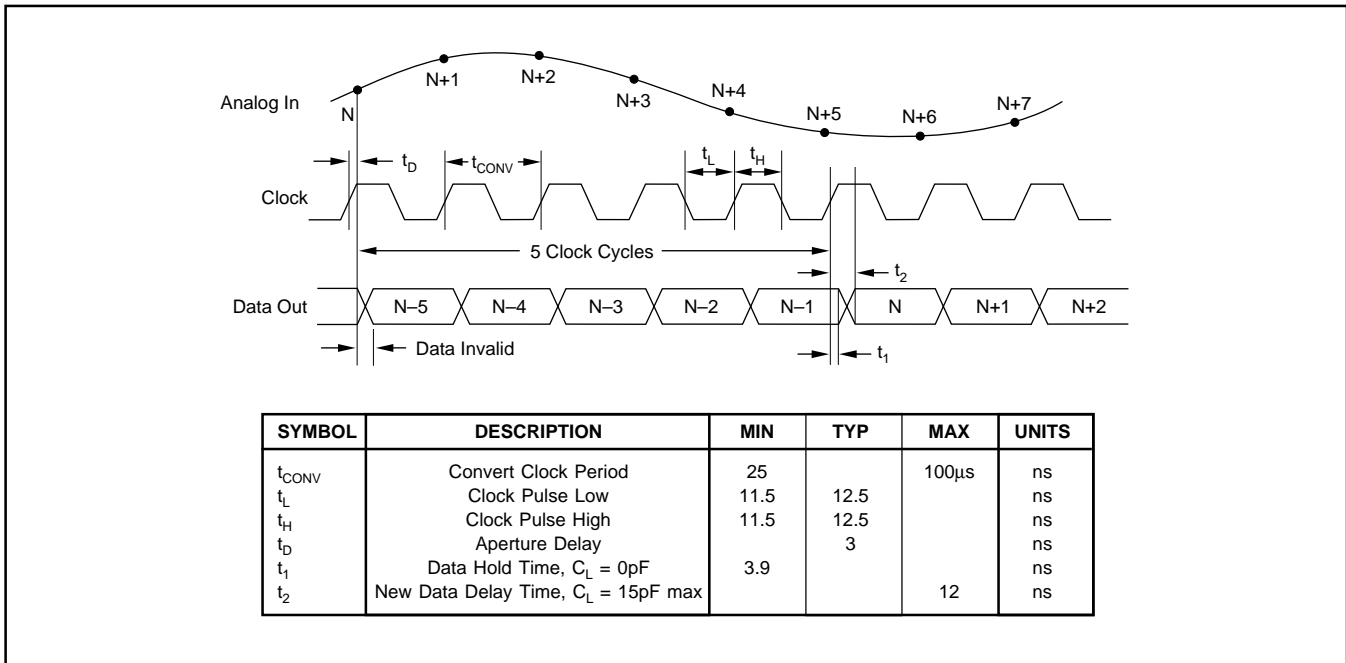
PIN CONFIGURATION



PIN DESCRIPTIONS

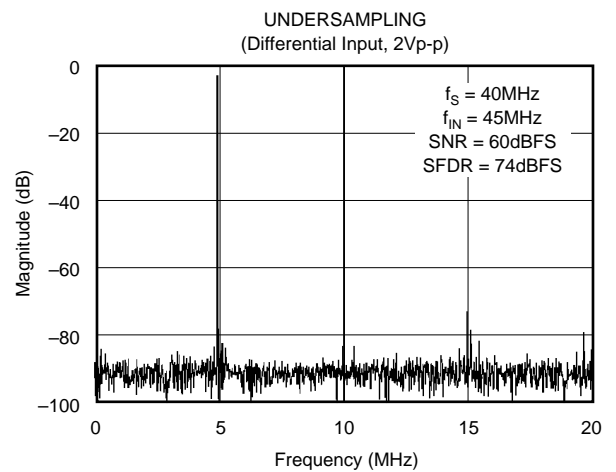
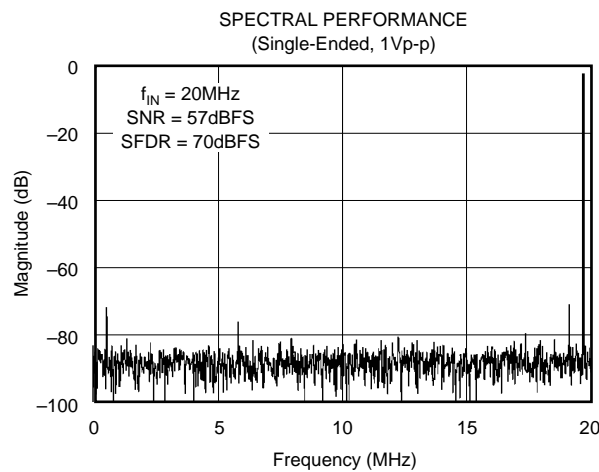
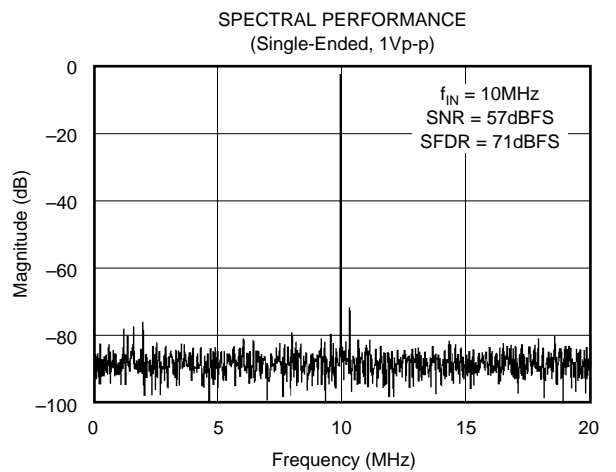
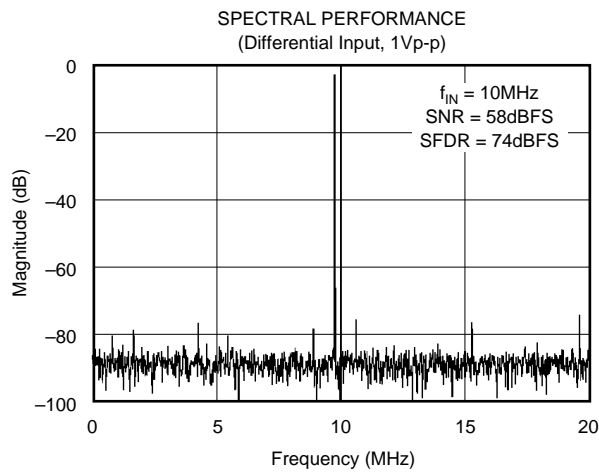
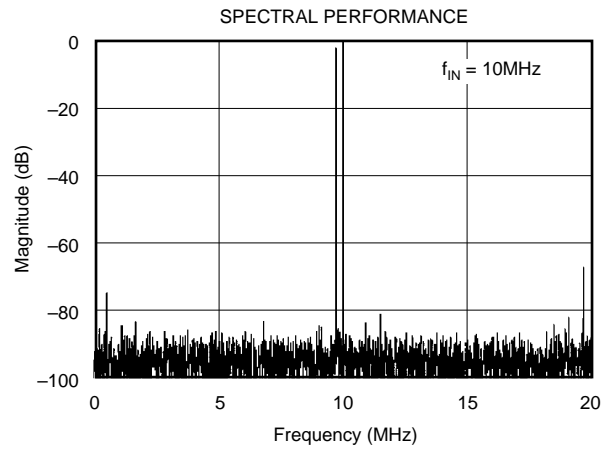
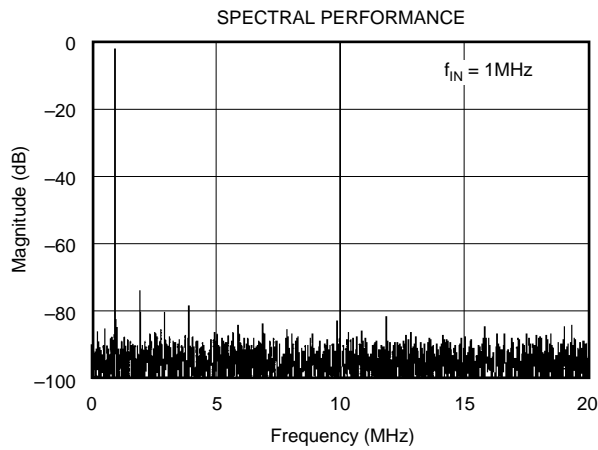
| PIN | DESIGNATOR | DESCRIPTION |
|-----|------------|---|
| 1 | GND | Ground |
| 2 | Bit 1 | Data Bit 1 (D9) (MSB) |
| 3 | Bit 2 | Data Bit 2 (D8) |
| 4 | Bit 3 | Data Bit 3 (D7) |
| 5 | Bit 4 | Data Bit 4 (D6) |
| 6 | Bit 5 | Data Bit 5 (D5) |
| 7 | Bit 6 | Data Bit 6 (D4) |
| 8 | Bit 7 | Data Bit 7 (D3) |
| 9 | Bit 8 | Data Bit 8 (D2) |
| 10 | Bit 9 | Data Bit 9 (D1) |
| 11 | Bit 10 | Data Bit 10 (D0) (LSB) |
| 12 | OE | Output Enable. HI = high impedance state LO = normal operation (internal pull-down resistor) |
| 13 | PD | Power Down. HI = enable; LO = disable |
| 14 | CLK | Convert Clock Input |
| 15 | +Vs | +5V Supply |
| 16 | GND | Ground |
| 17 | RSEL | Input Range Select. HI = 2V; LO = 1V |
| 18 | INT/EXT | Reference Select. HI = external, LO = internal |
| 19 | REFB | Bottom Reference |
| 20 | ByB | Bottom Ladder Bypass |
| 21 | ByT | Top Ladder Bypass |
| 22 | REFT | Top Reference |
| 23 | CM | Common-Mode Voltage Output |
| 24 | IN | Complementary Input (-) |
| 25 | IN | Analog Input (+) |
| 26 | GND | Analog Ground |
| 27 | +Vs | +5V Supply |
| 28 | VDRV | Output Logic Driver Supply Voltage |

TIMING DIAGRAM



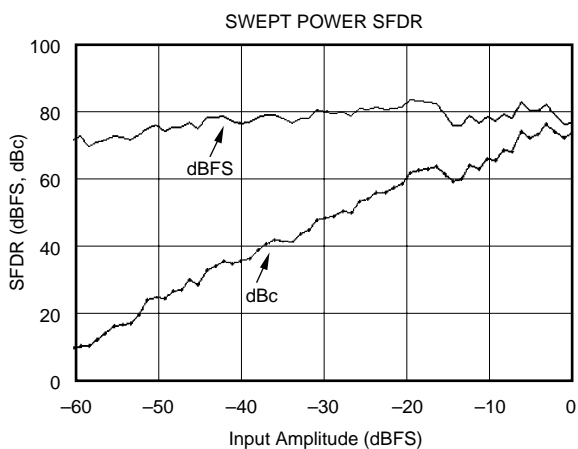
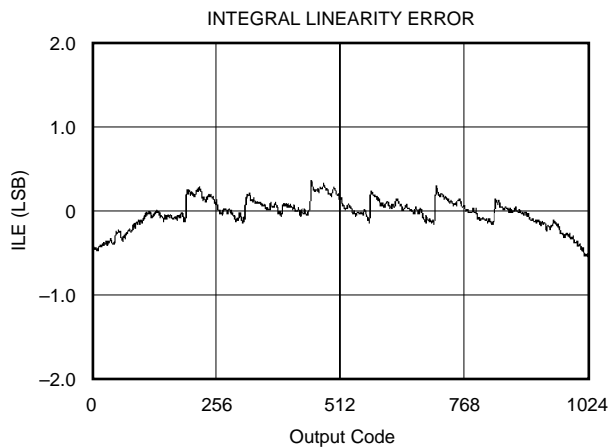
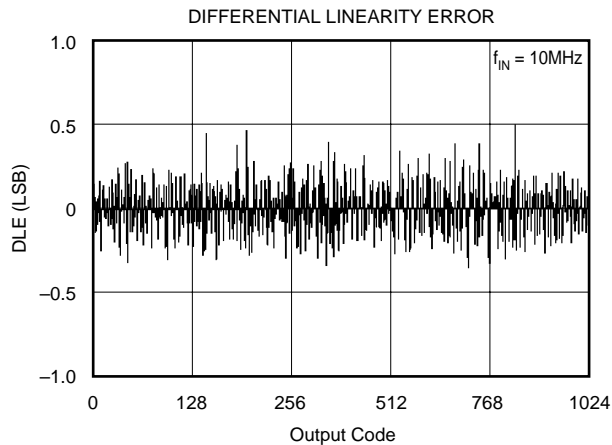
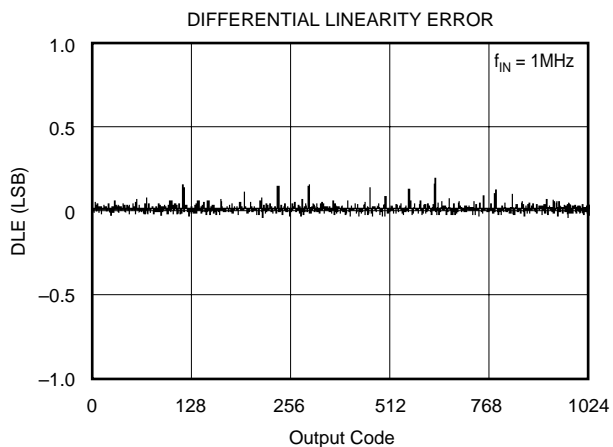
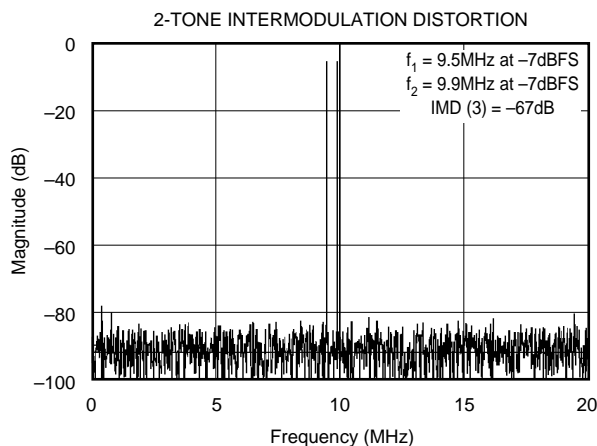
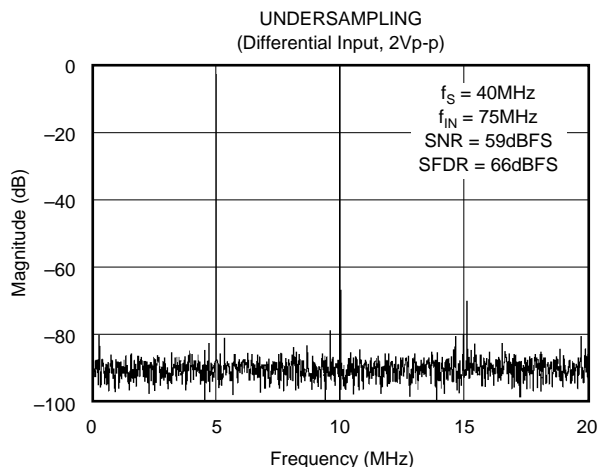
ELECTRICAL CHARACTERISTICS

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.



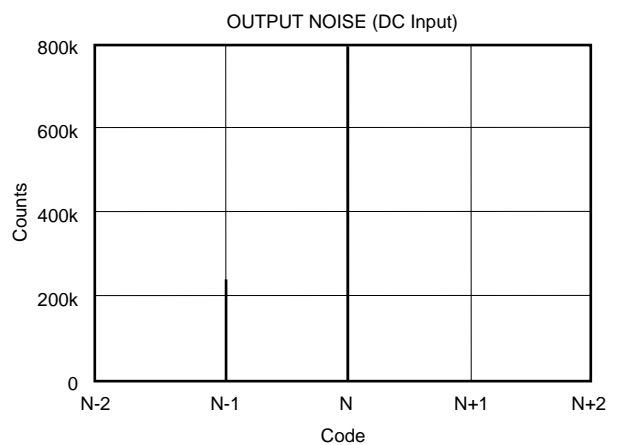
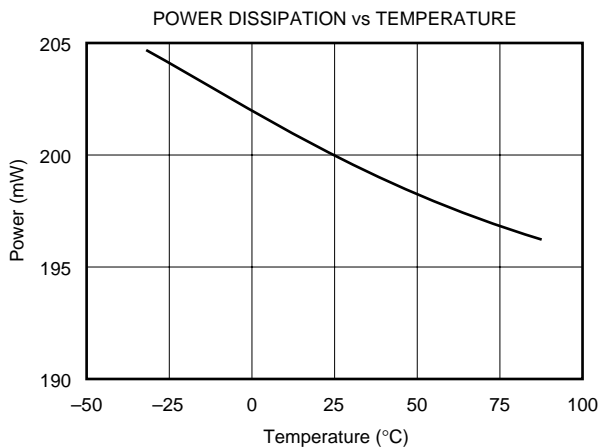
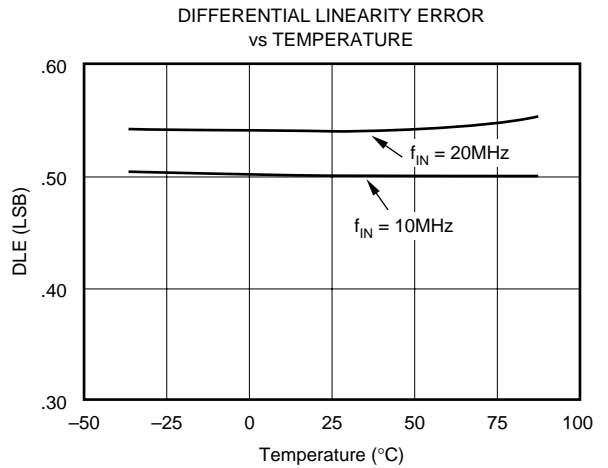
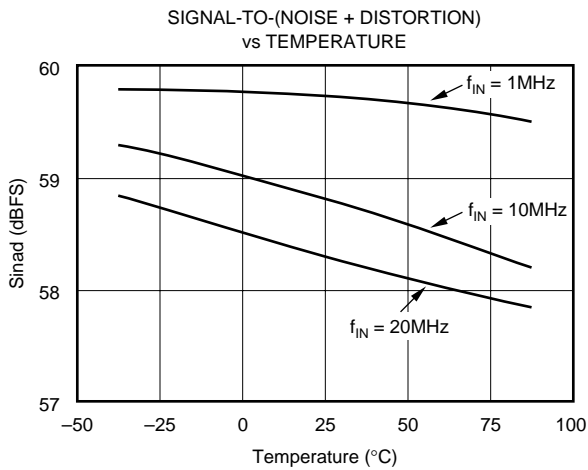
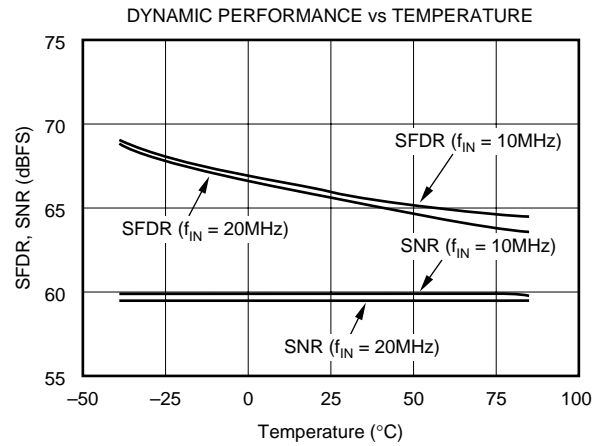
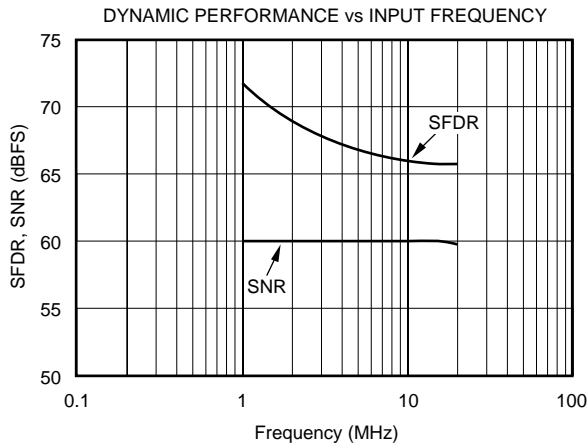
ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.



ELECTRICAL CHARACTERISTICS (Cont.)

At T_A = full specified temperature range, V_S = +5V, single-ended input range = 1.5V to 3.5V, sampling rate = 40MHz, and external reference, unless otherwise noted.



APPLICATION INFORMATION

THEORY OF OPERATION

The ADS822 and ADS825 are high-speed CMOS ADCs which employ a pipelined converter architecture consisting of nine internal stages. Each stage feeds its data into the digital error correction logic ensuring excellent differential linearity and no missing codes at the 10-bit level. The output data becomes valid on the rising clock edge (see Timing Diagram). The pipeline architecture results in a data latency of 5 clock cycles.

The analog inputs of the ADS822 and ADS825 are differential track-and-hold, as shown in Figure 1. The differential topology, along with tightly matched capacitors, produce a high level of AC performance while sampling at very high rates.

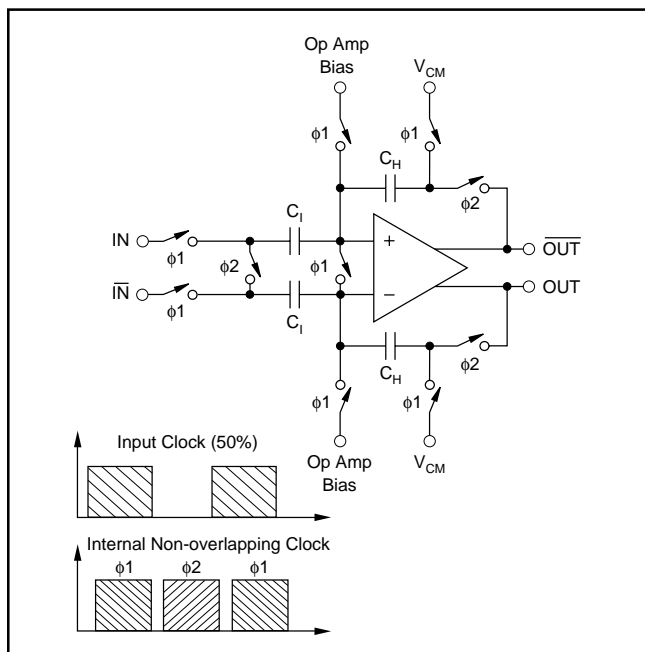


FIGURE 1. Simplified Circuit of Input Track-and-Hold with Timing Diagram.

The ADS822 and ADS825 allow their analog inputs to be driven either single-ended or differentially. The typical configuration for the ADS822 and ADS825 is the single-ended mode in which the input track-and-hold performs a single-ended-to-differential conversion of the analog input signal.

Both inputs (IN, \bar{IN}) require external biasing using a common-mode voltage that is typically at the mid-supply level ($+V_S/2$).

The following application discussion focuses on the single-ended configuration. Typically, its implementation is easier to achieve and the rated specifications for the ADS822 and ADS825 are characterized using the single-ended mode of operation.

DRIVING THE ANALOG INPUT

The ADS822 and ADS825 achieve excellent AC performance either in the single-ended or differential mode of operation.

The selection for the optimum interface configuration will depend on the individual application requirements and system structure. For example, communications applications often process a band of frequencies that do not include DC, whereas in imaging applications, the previously restored DC level must be maintained correctly up to the ADC. Features on the ADS822 and ADS825, such as the input range select (RSEL pin) or the option for an external reference, provide the needed flexibility to accommodate a wide range of applications. In any case, the ADS822 and ADS825 should be configured such that the application objectives are met while observing the headroom requirements of the driving amplifier in order to yield the best overall performance.

INPUT CONFIGURATIONS

AC-Coupled, Single-Supply Interface

See Figure 2 for the typical circuit for an AC-coupled analog input configuration of the ADS822 and ADS825 while all components are powered from a single +5V supply.

With the RSEL pin connected HI, the full-scale input range is set to 2Vp-p. In this configuration, the top and bottom references (REFT, REFB) provide an output voltage of +3.5V and +1.5V, respectively. Two resistors ($2 \times 1.62k\Omega$) are used to create a common-mode voltage (V_{CM}) of approximately +2.5V to bias the inputs of the driving amplifier A1. Using the OPA680 on a single +5V supply, its ideal common-mode point is at +2.5V which coincides with the recommended common-mode input level for the ADS822 and ADS825. This obviates the need of a coupling capacitor between the amplifier and the converter. Even though the OPA680 has an AC gain of +2, the DC gain is only +1 due to the blocking capacitor at resistor R_G .

The addition of a small series resistor (R_S) between the output of the op amp and the input of the ADS822 and ADS825 will be beneficial in almost all interface configurations. This will decouple the op amp's output from the capacitive load and avoid gain peaking, which can result in increased noise. For best spurious and distortion performance, the resistor value should be kept below 100 Ω . Furthermore, the series resistor in combination with the 10pF capacitor establishes a passive low-pass filter limiting the bandwidth for the wideband noise, thus helping improve the SNR performance.

AC-Coupled, Dual Supply Interface

The circuit provided in Figure 3 illustrates typical connections for the analog input in case the selected amplifier operates on dual supplies. This might be necessary to take full advantage of very low distortion operational amplifiers, like the OPA642. The advantage is that the driving amplifier can be operated with a ground-referenced bipolar signal swing. This will keep the distortion performance at its lowest, since the signal range stays within the linear region of the op amp and sufficient headroom to the supply rails can be maintained. By capacitively coupling the single-ended signal to the input of the ADS822 and ADS825, its common-mode requirements can easily be satisfied with two resistors connected between the top and bottom references.

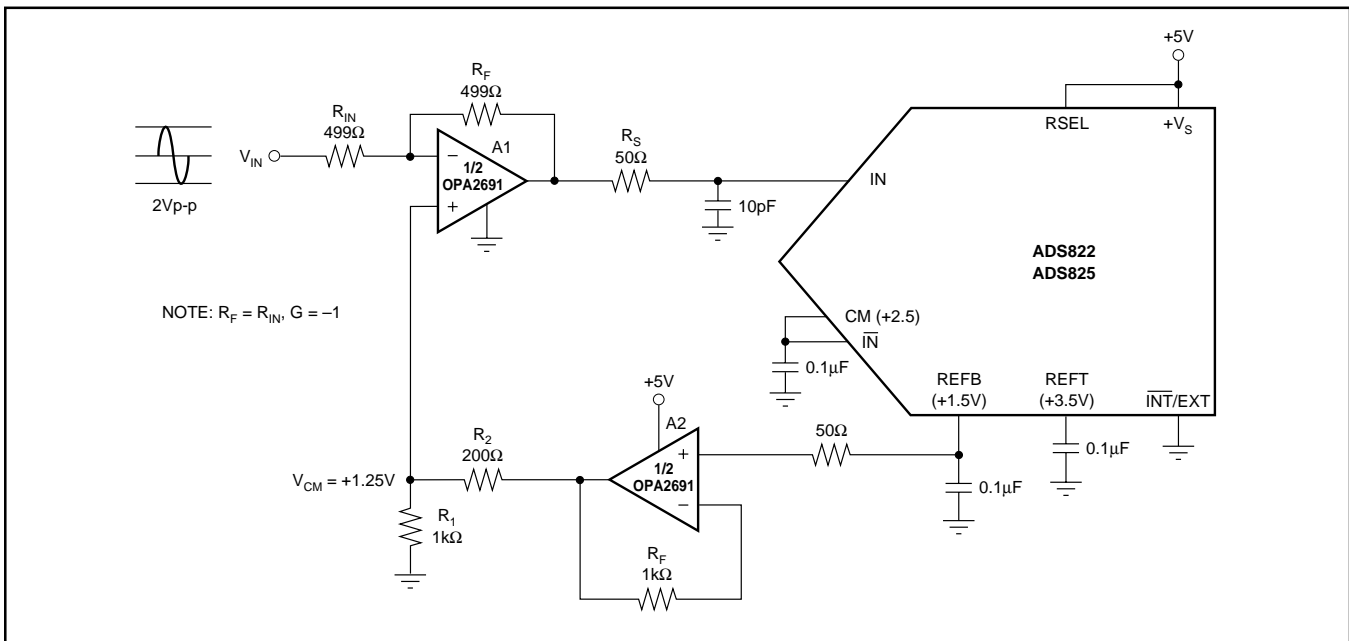


FIGURE 4. DC-Coupled Interface Circuit with Dual Current-Feedback Amplifier OPA2681.

SINGLE-ENDED-TO-DIFFERENTIAL CONFIGURATION (Transformer Coupled)

If the application requires a signal conversion from a single-ended source to feed the ADS822 and ADS825 differentially, a RF transformer might be a good solution. The selected transformer must have a center tap in order to apply the common-mode DC voltage necessary to bias the converter inputs. AC-grounding the center tap will generate the differential signal swing across the secondary winding. Consider a step-up transformer to take advantage of a signal amplification without the introduction of another noise source. Furthermore, the reduced signal swing from the source may lead to an improved distortion performance.

The differential input configuration may provide a noticeable advantage of achieving good SFDR performance over a wide range of input frequencies. In this mode, both inputs of the ADS822 and ADS825 see matched impedances, and the differential signal swing can be reduced to half of the swing required for single-ended drive. Figure 5 shows the schematic for the suggested transformer-coupled interface circuit.

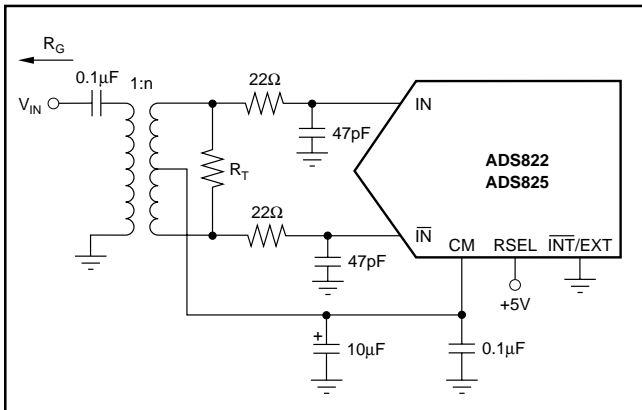


FIGURE 5. Transformer Coupled Input.

The component values of the R-C low-pass may be optimized depending on the desired roll-off frequency. The resistor across the secondary side (R_T) should be calculated using the equation $R_T = n^2 \cdot R_G$ to match the source impedance (R_G) for good power transfer and Voltage Standing Wave Ratio (VSWR).

REFERENCE OPERATION

Figure 6 depicts the simplified model of the internal reference circuit. The internal blocks are the bandgap voltage reference, the drivers for the top and bottom references, and the

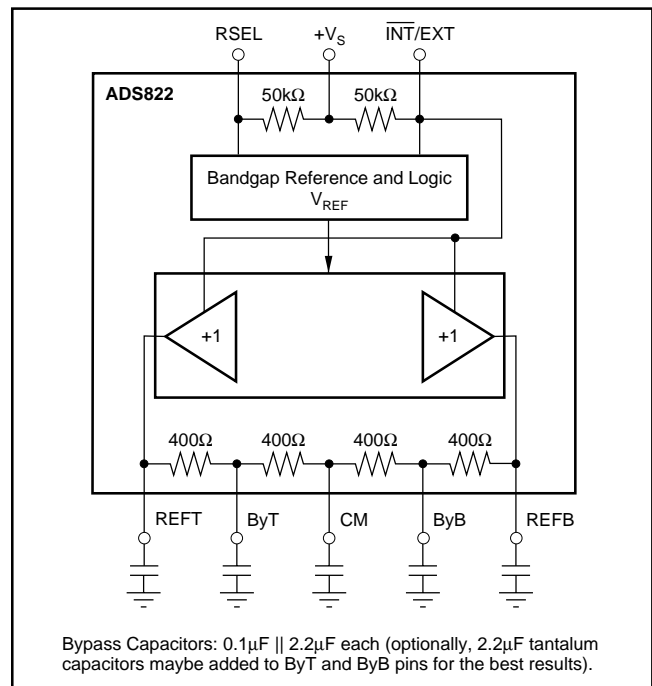


FIGURE 6. Equivalent Reference Circuit with Recommended Reference Bypassing.

resistive reference ladder. The bandgap reference circuit includes logic functions that allows setting the analog input swing of the ADS822 and ADS825 to either a 1Vp-p or 2Vp-p full-scale range simply by tying the RSEL pin to a Low or High potential, respectively. While operating the ADS822 in the external reference mode, the buffer amplifiers for the REFT and REFB are disconnected from the reference ladder.

As shown, the ADS822 and ADS825 have internal 50kΩ pull-up resistors at the range select pin (RSEL) and reference select pin ($\overline{\text{INT}}/\text{EXT}$). Leaving these pins open configures the ADS822 and ADS825 for a 2Vp-p input range and external reference operation. Setting the ADS822 and ADS825 up for internal reference mode requires bringing the $\overline{\text{INT}}/\text{EXT}$ pin Low.

The reference buffers can be utilized to supply up to 1mA (sink and source) to external circuitry. The resistor ladders of the ADS822 and ADS825 are divided into several segments and have two additional nodes, ByT and ByB, which are brought out for external bypassing only (see Figure 6). To ensure proper operation with any reference configurations, it is necessary to provide solid bypassing at all reference pins in order to keep the clock feedthrough to a minimum. All bypassing capacitors should be located as close to their respective pins as possible.

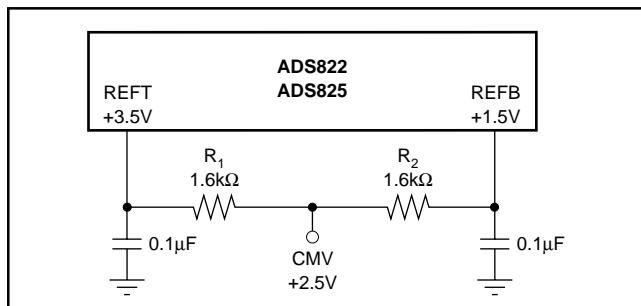


FIGURE 7. Alternative Circuit to Generate CM Voltage.

The common-mode voltage available at the CM pin may be used as a bias voltage to provide the appropriate offset for the driving circuitry. However, care must be taken not to appreciably load this node, which is not buffered and has a high impedance. An alternative way of generating a common-mode voltage is given in Figure 7. Here, two external precision resistors (tolerance 1% or better) are located between the top and bottom reference pins. The common-mode voltage, CMV, will appear at the midpoint.

EXTERNAL REFERENCE OPERATION

For even more design flexibility, the internal reference can be disabled and an external reference voltage be used. The utilization of an external reference may be considered for applications requiring higher accuracy, improved temperature performance, or a wide adjustment range of the converter's full-scale range. Especially in multichannel applications, the use of a common external reference has the benefit of obtaining better matching of the full-scale range between converters.

The external references can vary as long as the value of the external top reference REFT_{EXT} stays within the range of ($V_S - 1.25\text{V}$) and ($\text{REFB} + 0.8\text{V}$), and the external bottom reference REFB_{EXT} stays within 1.25V and ($\text{REFT} - 0.8\text{V}$) (See Figure 8).

DIGITAL INPUTS AND OUTPUTS

Clock Input Requirements

Clock jitter is critical to the SNR performance of high-speed, high-resolution ADCs. Clock jitter leads to aperture jitter (t_A), which adds noise to the signal being converted. The ADS822 and ADS825 samples the input signal on the rising edge of the CLK input. Therefore, this edge should have the lowest possible jitter. The jitter noise contribution to total SNR is given by

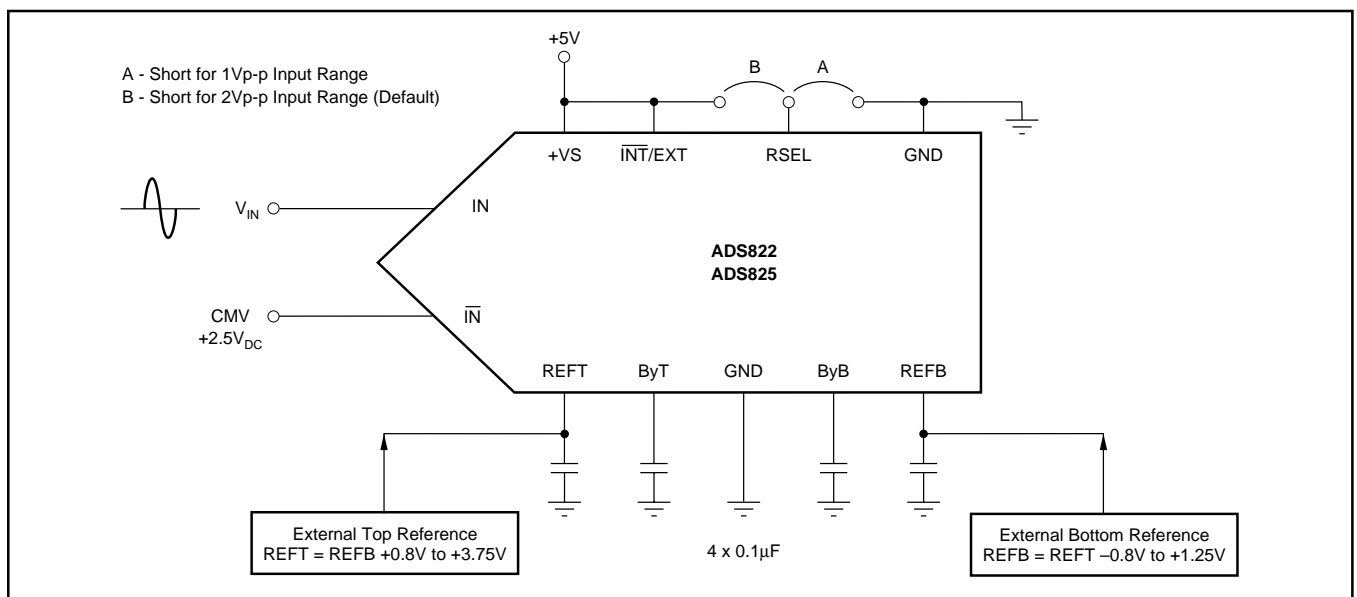


FIGURE 8. Configuration Example for External Reference Operation.

the following equation. If this value is near your system requirements, input clock jitter must be reduced.

$$\text{Jitter SNR} = 20 \log \frac{1}{2\pi f_{IN} t_A} \text{ rms signal to rms noise}$$

where: f_{IN} is input signal frequency
 t_A is rms clock jitter

Particularly in undersampling applications, special consideration should be given to clock jitter. The clock input should be treated as an analog input in order to achieve the highest level of performance. Any overshoot or undershoot of the clock signal may cause degradation of the performance. When digitizing at high sampling rates, the clock should have 50% duty cycle ($t_H = t_L$), along with fast rise and fall times of 2ns or less. The clock input of the ADS825 can be driven with either 3V or 5V logic levels. Using low-voltage logic (3V) may lead to improved AC performance of the converter.

Digital Outputs

The output data format of the ADS822 and ADS825 are in positive Straight Offset Binary code, as shown in Tables I and II. This format can easily be converted into the Binary Two's Complement code by inverting the MSB.

It is recommended to keep the capacitive loading on the data lines as low as possible ($\leq 15\text{pF}$). Higher capacitive loading will cause larger dynamic currents as the digital outputs are changing. Those high current surges can feed back to the analog portion of the ADS822 and ADS825 and affect the performance. If necessary, external buffers or latches close to the converter's output pins may be used to minimize the capacitive loading. They also provide the added benefit of isolating the ADS822 and ADS825 from any digital noise activities on the bus coupling back high frequency noise.

| SINGLE-ENDED INPUT ($\overline{IN} = \text{CMV}$) | STRAIGHT OFFSET BINARY (SOB) |
|--|---------------------------------|
| +FS -1LSB ($\overline{IN} = \text{REFT}$) | 11 1111 1111 |
| +1/2 Full Scale | 11 0000 0000 |
| Bipolar Zero ($\overline{IN} = \text{CMV}$) | 10 0000 0000 |
| -1/2 Full Scale | 01 0000 0000 |
| -FS ($\overline{IN} = \text{REFB}$) | 00 0000 0000 |

TABLE I. Coding Table for Single-Ended Input Configuration with \overline{IN} Tied to the Common-Mode Voltage (CMV).

| DIFFERENTIAL INPUT | STRAIGHT OFFSET BINARY (SOB) |
|--|---------------------------------|
| +FS -1LSB ($\overline{IN} = +3\text{V}$, $\overline{\overline{IN}} = +2\text{V}$) | 11 1111 1111 |
| +1/2 Full Scale | 11 0000 0000 |
| Bipolar Zero ($\overline{IN} = \overline{\overline{IN}} = \text{CMV}$) | 10 0000 0000 |
| -1/2 Full Scale | 01 0000 0000 |
| -FS ($\overline{IN} = +2\text{V}$, $\overline{\overline{IN}} = +3\text{V}$) | 00 0000 0000 |

TABLE II. Coding Table for Differential Input Configuration and 2Vp-p Full-Scale Range.

Digital Output Driver (VDRV)

The ADS822 features a dedicated supply pin for the output logic drivers, VDRV, which are not internally connected to the other supply pins. Setting the voltage at VDRV to +5V or +3V, the ADS822 and ADS825 produce corresponding logic levels and can directly interface to the selected logic family. The output stages are designed to supply sufficient current to drive a variety of logic families. However, it is recommended to use the ADS822 and ADS825 with +3V logic supply. This will lower the power dissipation in the output stages due to the lower output swing and reduce current glitches on the supply line which may affect the AC-performance of the converter. In some applications, it might be advantageous to decouple the VDRV pin with additional capacitors or a pi filter.

GROUNDING AND DECOUPLING

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer PC boards are recommended for best performance since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. The ADS822 and ADS825 should be treated as analog components. Whenever possible, the supply pins should be powered by the analog supply. This will ensure the most consistent results, since digital supply lines often carry high levels of noise which otherwise would be coupled into the converter and degrade the achievable performance. All ground connections on the ADS822 and ADS825 are internally joined together obviating the design of split ground planes. The ground pins (1, 16, 26) should directly connect to an analog ground plane which covers the PC board area around the converter. While designing the layout, it is important to keep the analog signal traces separated from any digital lines to prevent noise coupling onto the analog signal path. Due to their high sampling rates, the ADS822 and ADS825 generate high frequency current transients, and noise (clock feedthrough) that are fed back into the supply and reference lines. This requires that all supply and reference pins are sufficiently bypassed. Figure 9 shows the recommended decoupling scheme for the ADS822 and ADS825. In most cases, $0.1\mu\text{F}$ ceramic chip capacitors at each pin are adequate to keep the impedance low over a wide frequency range. Their effectiveness largely depends on the proximity to the individual supply pin. Therefore, they should be located as close to the supply pins as possible. In addition, a larger bipolar capacitor ($1\mu\text{F}$ to $22\mu\text{F}$) should be placed on the PC board in proximity of the converter circuit.

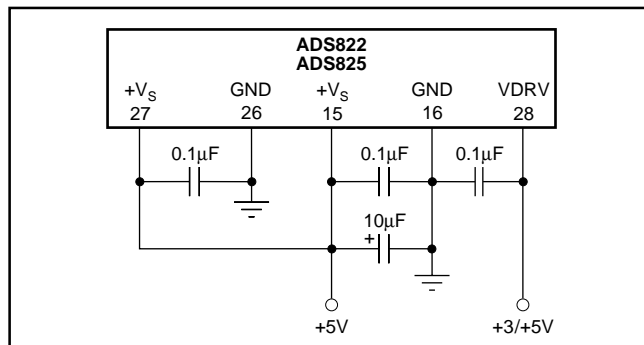
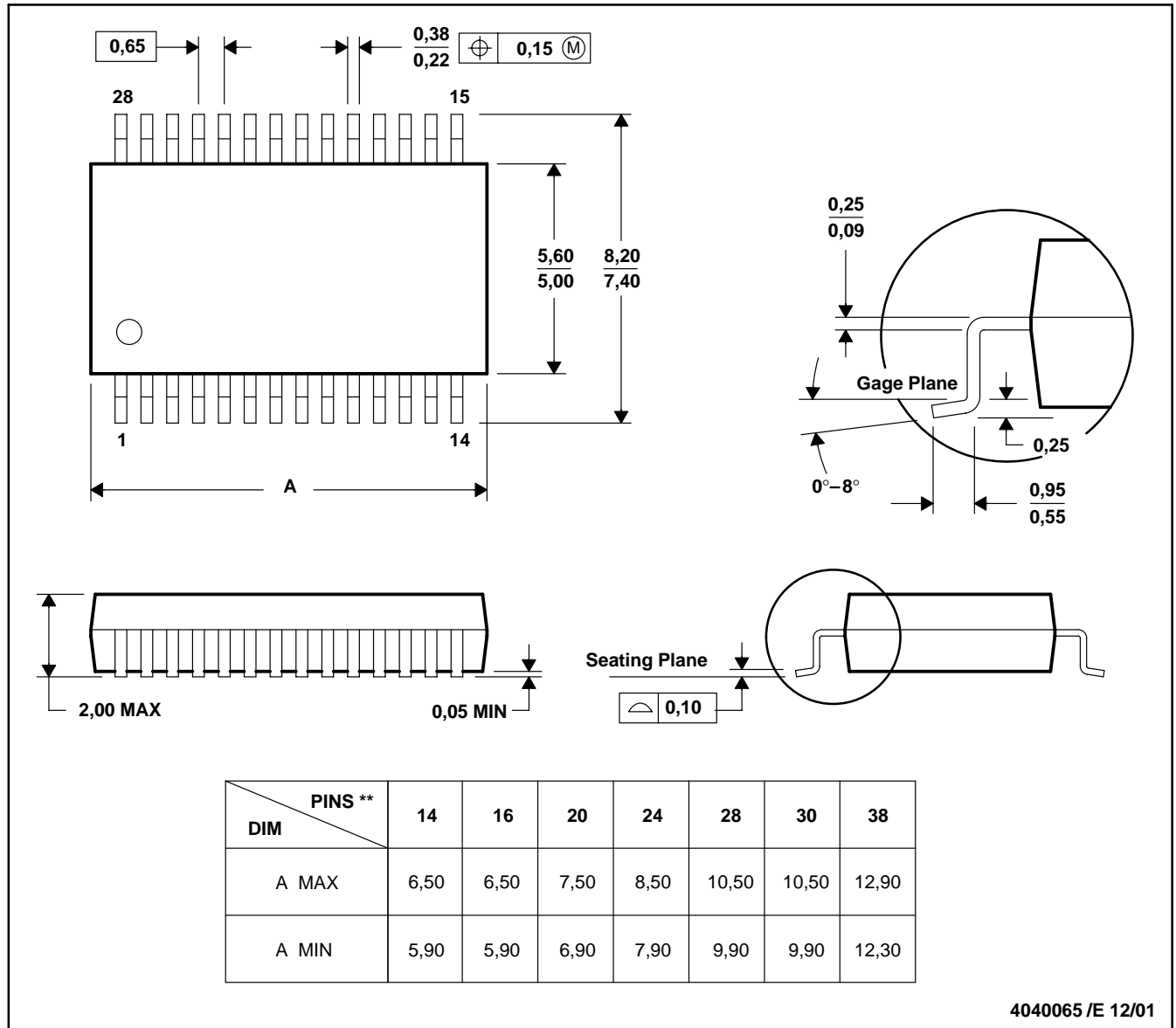


FIGURE 9. Recommended Bypassing for the Supply Pins.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| ADS822E | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS822E/1K | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS822E/1KG4 | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS822EG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS825E | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS825E/1K | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS825E/1KG4 | ACTIVE | SSOP | DB | 28 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| ADS825EG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



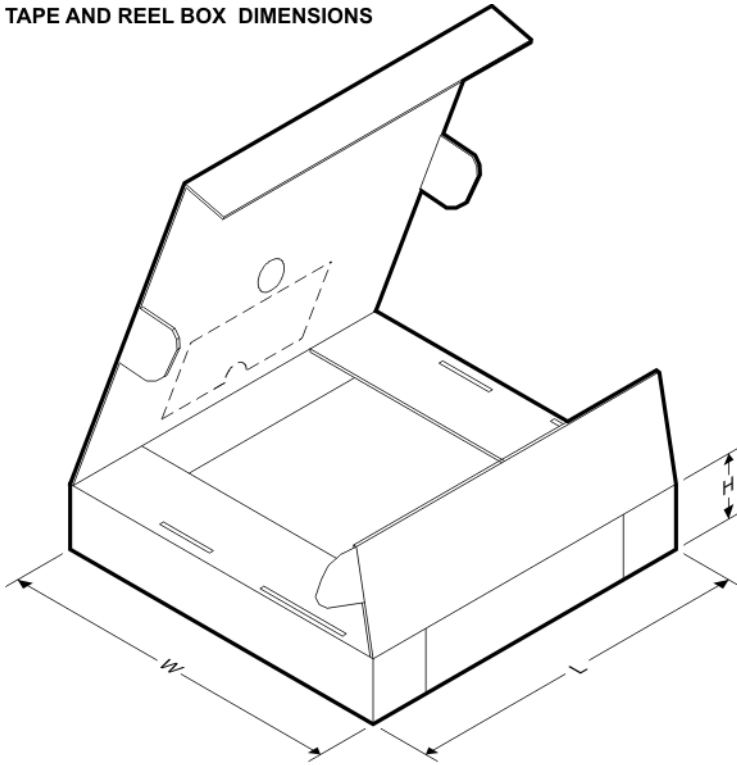
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS822E/1K | SSOP | DB | 28 | 1000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| ADS825E/1K | SSOP | DB | 28 | 1000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS822E/1K | SSOP | DB | 28 | 1000 | 346.0 | 346.0 | 33.0 |
| ADS825E/1K | SSOP | DB | 28 | 1000 | 346.0 | 346.0 | 33.0 |

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

| | |
|-----------------------------|--|
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| RF/IF and ZigBee® Solutions | www.ti.com/lprf |

Applications

| | |
|--------------------|--|
| Audio | www.ti.com/audio |
| Automotive | www.ti.com/automotive |
| Broadband | www.ti.com/broadband |
| Digital Control | www.ti.com/digitalcontrol |
| Medical | www.ti.com/medical |
| Military | www.ti.com/military |
| Optical Networking | www.ti.com/opticalnetwork |
| Security | www.ti.com/security |
| Telephony | www.ti.com/telephony |
| Video & Imaging | www.ti.com/video |
| Wireless | www.ti.com/wireless |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

www.BDTIC.com/TI/