

www.ti.com SLAS628-MARCH 2009

18-BIT, 1-MSPS, PSEUDO-BIPOLAR DIFFERENTIAL SAR ADC WITH ON-CHIP ADC DRIVER (OPA) AND 4-CHANNEL DIFFERENTIAL MULTIPLEXER

FEATURES

- 1.0-MHz Sample Rate, Zero Latency at Full Speed
- 18-Bit Resolution
- Supports Pseudo-Bipolar Differential Input Range: -4 V to +4 V with 2-V Common-Mode
- Built-In Four Channel, Differential Ended Multiplexer; with Channel Count Selection and Auto/Manual Mode
- On-Board Differential ADC Driver (OPA)
- Buffered Reference Output to Level Shift Bipolar ±4-V Input with External Resistance Divider
- Reference/2 Output to Set Common-Mode for External Signal Conditioner
- 18-/16-/8-Bit Parallel Interface
- SNR: 98.4dB Typ at 2-kHz I/P
- THD: -119dB Typ at 2-kHz I/P
- Power Dissipation: 331.25 mW at 1 MSPS Including ADC Driver
- Internal Reference
- Internal Reference Buffer
- 64-Pin QFN Package

APPLICATIONS

- Medical Imaging/CT Scanners
- Automated Test Equipment
- High-Speed Data Acquisition Systems
- High-Speed Closed-Loop Systems

DESCRIPTION

The ADS8284 is a high-performance analog system-on-chip (SoC) device with an 18-bit, 1-MSPS A/D converter, 4-V internal reference, an on-chip ADC driver (OPA), and a 4-channel differential multiplexer. The channel count of the multiplexer and auto/manual scan modes of the device are user selectable.

ADS8284

The ADC driver is designed to leverage the very high noise performance of the differential ADC at optimum power usage levels.

The ADS8284 outputs a buffered reference signal for level shifting of a ± 4 -V bipolar signal with an external resistance divider. A $V_{ref}/2$ output signal is available to set the common-mode of a signal conditioning circuit. The device also includes an 18-/16-/8-bit parallel interface.

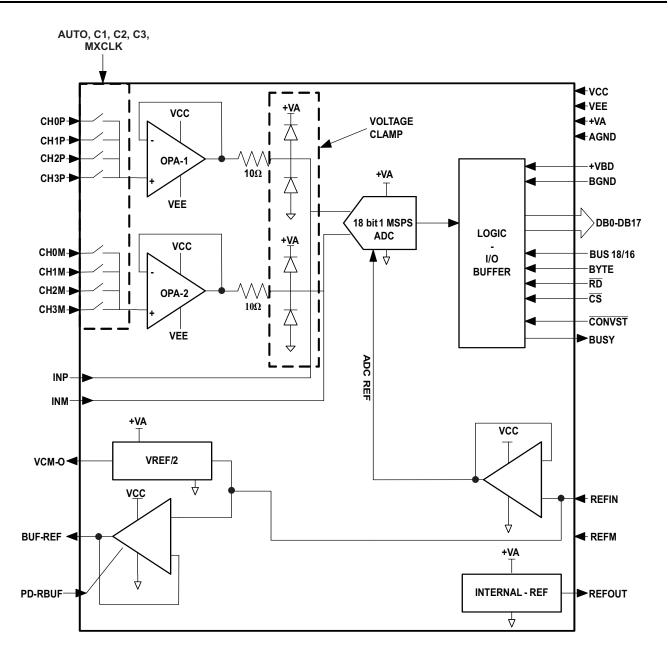
The ADS8284 is available in a 9 mm x 9 mm, 64-pin QFN package and is characterized from -40°C to 85°C.

HIGH-SPEED SAR CONVERTER FAMILY

TYPE/SPEED	500 kHz	~600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381		ADS8481				
To-Bit FSeudo-Dill		ADS8380 (s)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (s)		ADS8284	ADS8484			
16-Bit Pseudo-Bipolar, Fully Dill				ADS8482				
	ADS8327	ADS8370 (s)	ADS8371	ADS8471	ADS8401	ADS8411		
16-Bit Pseudo-Diff	ADS8328				ADS8405	ADS8410 (s)		
	ADS8319							
16-Bit Pseudo-Bipolar, Fully Diff	ADS8318	ADS8372 (s)		ADS8472	ADS8402	ADS8412		ADS8422
To-bit Eseudo-Bipolai, Fully Dill				ADS8254	ADS8406	ADS8413 (s)		
14-Bit Pseudo-Diff					ADS7890 (s)		ADS7891	
12-Bit Pseudo-Diff				ADS7886		ADS7883		ADS7881









www.ti.com SLAS628-MARCH 2009



NSTRUMENTS

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY					
ADS8284IB	±2.5	+1.5/–1	18				ADS8284IBRGCT	250					
AD36264IB	±2.5	+1.5/-1	10	10	10	10	10	10		RGC	−40°C to	ADS8284IBRGCR	2000
ADS8284I	±4.5	+1.5/–1	18	64-pin QFN	RGC	85°C	ADS8284IRGCT	250					
AD30204I	±4.5	+1.5/-1	10				ADS8284IRGCR	2000					

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
CH(i) to AGND (both P and M	nputs)	VEE-0.3 to VCC + 0.3	V
VCC to VEE		-0.3 to 18	V
+VA to AGND		-0.3 to 7	V
+VBD to BDGND		-0.3 to 7	V
ADC control digital input voltag	e to GND	-0.3 to (+VBD + 0.3)	V
ADC control digital output to G	ND	-0.3 to (+VBD + 0.3)	V
Multiplexer control digital input	voltage to GND	-0.3 to (+VA + 0.3)	V
Power control digital input volta	ge to GND	-0.3 to (+VCC + 0.3)	V
Operating temperature range		-40 to 85	°C
Storage temperature range		-65 to 150	°C
Junction temperature (T _J max)		150	°C
OFN poekage	Power dissipation	(T _J Max–T _A)/ θJA	
QFN package	θJA Thermal impedance	86	°C/W
	Vapor phase (60 sec)	215	°C
Lead temperature, soldering	Infrared (15 sec)	220	°C

⁽¹⁾ Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SLAS628-MARCH 2009 www.ti.com



SPECIFICATIONS

 $T_{A} = -40^{\circ}C \text{ to } 85^{\circ}C, \ VCC = 5 \ \text{V}, \ \text{VEE} = -5 \ \text{V}, \ \text{+VA} = 5 \ \text{V}, \ \text{+VBD} = 5 \ \text{V} \ \text{or } 3.3 \ \text{V}, \ V_{ref} = 4 \ \text{V}, \ f_{SAMPLE} = 1 \ \text{MSPS} \ \text{(unless the leaves of the leaves o$ otherwise noted)

Full-scale input voltage at multiplexer input (**) Absolute input range at multiplexer input (**) Absolute input range at multiplexer input (**) Absolute input range at multiplexer input (**) Absolute input common-mode voltage CH(I)P + CH(I)M] / 2	PARA	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Absolute input range at multiplexer input CH (i) -0.2 V _{rel} + 0.2 V v _{rel} + 0.	ANALOG INPUT			+				
Input common-mode voltage ICH(I)P + CH(I)MI / 2	Full-scale input voltage at m	nultiplexer input ⁽¹⁾	CH(i)P-CH(i)M	-V _{ref}		V_{ref}	V	
System Performance	Absolute input range at mul	tiplexer input	CH (i)	-0.2		V_{ref} + 0.2	V	
Resolution	Input common-mode voltage	Э	[CH(i)P + CH(i)M] /2	(V _{ref})/2 - 0.2	(V _{ref})/2		٧	
ADS8284IB ADS8	SYSTEM PERFORMANCE			·				
ADS8284	Resolution				18		Bits	
ADS8284 18		ADS8284IB		18				
ADS8284 ADS8284 AL 18-bit level -4.5	No missing codes	ADS8284I		18			Bits	
ADS8284	(2)	ADS8284IB		-2.5	±1.25	2.5	(2)	
ADS8284I	Integral linearity (2)	ADS8284I		-4.5	±1.5	4.5	LSB (5)	
ADS8284IB		ADS8284IB		-1	±0.6	1.5	(0)	
Offset error ADS8284I — 0.5 ±0.05 0.5 mV Gain error ⁽⁴⁾ ADS8284IB ADS8284I External reference — 0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 −0.1 ±0.025 0.1 0.1 −0.1 ±0.025 0.1 0.1 −0.1 ±0.025 0.1 0.1 68 680 ns 0.8 <	Differential linearity	ADS8284I	At 18-bit level	-1	±0.6	1.5	LSB ⁽³⁾	
AD\$8284I		ADS8284IB		-0.5	±0.05	0.5		
ADS82841 External reference	Offset error	ADS8284I		-0.5	±0.05	0.5	mV	
ADS82841 External reference		ADS8284IB		-0.1	±0.025	0.1		
At 3FFF0H output code. For +VA or VCC, VEE variation of 0.5 V individually 80	Gain error ⁽⁴⁾	ADS8284I	External reference				%FS	
ADS2841	DC power supply rejection ratio						dB	
Acquisition time	SAMPLING DYNAMICS		,					
+VDB = 3 V 625 650 ns +VBD = 5 V 320 350 ns +VDB = 3 V 320 320 350 ns +VDB = 3 V 320 320 320 320 320 +VDB = 3 V 320 320 320 +VDB = 3			+VBD = 5 V		625	650	ns	
Acquisition time +VBD = 5 V	Conversion time		+VDB = 3 V		625	650	ns	
+VDB = 3 V 320 350 MMz			+VBD = 5 V	320			ns	
Aperture delay Aperture jitter Settling time to 0.5 LSB For ADC only For OPA (OP1, OP2) + mux For OPA (OP1, OP2) + mux For OPA (OP1, OP2) + mux For ADC only DYNAMIC CHARACTERISTICS Total harmonic distortion (THD) (6) ADS8284IB AD	Acquisition time		+VDB = 3 V	320	350			
Aperture jitter	Maximum throughput rate					1.0	MHz	
Aperture jitter	Aperture delay				4		ns	
For ADC only	-				5		ps	
For OPA (OP1, OP2) + mux 700			For ADC only		150		-	
Total harmonic distortion (THD) Signal-to-noise ratio (SNR) ADS8284I	Settling time to 0.5 LSB		For OPA (OP1, OP2) + mux		700			
ADS8284	Over voltage recovery				150		ns	
ADS8284 B VIN = 4 Vpp at 2 kHz -119 dB ADS8284 B VIN = 4 Vpp at 10 kHz -105 dB ADS8284 B VIN = 4 Vpp at 100 kHz -100 dB ADS8284 B VIN = 4 Vpp at 100 kHz -100 dB ADS8284 B VIN = 4 Vpp at 2 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 10 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 10 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 10 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 10 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 10 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 100 kHz 98.4 dB ADS8284 B VIN = 4 Vpp at 100 kHz 99.5 dB ADS8284 B VI	DYNAMIC CHARACTERIS	TICS	· · · · · · · · · · · · · · · · · · ·				1	
ADS8284IB ADS828		ADS8284I			-119			
ADS8284 B		ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz		-119		dB	
(THD) (5) ADS8284IB ADS8284II ADS8284II ADS8284IB ADS8284IB ADS8284IB ADS8284IB ADS8284II ADS8284IB ADS8284II ADS8284IB	Total harmonic distortion	ADS8284I			-105			
AD\$8284IB	(THD) ⁽⁵⁾	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		-105		dB	
ADS8284I V _{IN} = 4 V _{pp} at 2 kHz ADS8284IB ADS8284IB ADS8284I ADS8284IB V _{IN} = 4 V _{pp} at 10 kHz ADS8284IB ADS8284II ADS8284IB V _{IN} = 4 V _{pp} at 100 kHz, dB		ADS8284I	V – 4 V at 100 kHz		-100			
ADS8284I		ADS8284IB	$\frac{\sqrt{N} - 4\sqrt{pp} \text{ at 100 kHz}}{\text{LoPWR} = 0}$				dB	
ADS8284IB								
ADS8284I V _{IN} = 4 V _{pp} at 100 kHz, ADS8284I V _{IN} = 4 V _{pp} at 100 kHz, dB			$V_{IN} = 4 V_{pp}$ at 2 kHz	97.5			dB	
Signal-to-noise ratio (SNR) ADS8284IB V _{IN} = 4 V _{pp} at 10 kHz V _{IN} = 4 V _{pp} at 100 kHz, dB								
ADS8284I V _{IN} = 4 V _{pp} at 100 kHz, 95	Signal-to-noise ratio (SNR)		$V_{IN} = 4 V_{pp}$ at 10 kHz				dB	
T P V V P P Q P Q P Q P Q P Q P Q P Q P Q			V = 4 V at 100 kHz					
		ADS8284IB	$v_{IN} = 4 v_{pp}$ at 100 kHz, LoPWR = 0		97		dB	

- (1) Ideal input span, does not include gain or offset error.
- (2) This is endpoint INL, not best fit.
- LSB means least significant bit.
- Calculated on the first nine harmonics of the input frequency.
- (5) Measured relative to acutal measured reference.



SPECIFICATIONS (continued)

 $T_A = -40$ °C to 85°C, VCC = 5 V, VEE = -5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, $V_{ref} = 4$ V, $f_{SAMPLE} = 1$ MSPS (unless otherwise noted)

PARAI	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	ADS8284I	$V_{IN} = 4 V_{pp}$ at 2 kHz		98.3		dB
	ADS8284IB	VIN = 4 Vpp at 2 Ki i2		98.3		uБ
Signal-to-noise + distortion	ADS8284I	V = 4 V of 10 kHz		97.2		٩D
(SINAD)	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		97.2		dB
	ADS8284I	$V_{IN} = 4 V_{pp}$ at 100 kHz,		93.8		٦D
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 100 kHz, LoPWR = 0		95.23		dB
	ADS8284I			121		
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 2 kHz		121		dB
Spurious free dynamic	ADS8284I			106		
range (SFDR)	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 10 kHz		106		dB
	ADS8284I	V _W = 4 V at 100 kHz		101		
	ADS8284IB	$V_{IN} = 4 V_{pp}$ at 100 kHz, LoPWR = 0		101		dB
-3dB small signal bandwidth	n			8		MHz
VOLTAGE REFERENCE IN	IPUT (REFIN)					
Reference voltage at REFIN			3.0	4.096	+VA - 0.8	V
Reference input current ⁽⁶⁾	7 101			1	1	μА
INTERNAL REFERENCE C	OUTPUT (REFOUT)					r
Internal reference start-up ti	-	From 95% (+VA), with 1-μF storage capacitor			120	ms
Reference voltage range, V _{ref}		The state (* 11 7), that is particularly corporate.	4.081	4.096	4.111	V
Source current		Static load			10	μА
Line regulation		+VA = 4.75 V to 5.25 V		60		μV
Drift		I _O = 0		±6		PPM/°C
BUFFERED REFERENCE	OUTPUT (BUE-REE)	10 - 0				111111
Output current	oon or (bor KEI)	REFIN = 4 V, at 85°C		70		mA
REFERENCE/2 OUTPUT (\	/CMO)	NET IIV = 4 V, at 65 C		70		111/ (
Output current	, cmo,	REFIN = 4 V, at +85°C		50		μА
ANALOG MULTIPLEXER		NET IIV - 4 V, at 100 O				μιτ
Number of channels					4	
Channel to channel crosstal	l l	100 kHz i/p		-95		dB
Channel selection	N.	Auto sequencer with selection of channel count or		-93		uБ
		manual selection through control lines				
DIGITAL INPUT-OUTPUT						
ADC CONTROL PINS						
Logic Family-CMOS						
	V _{IH}	I _{IH} = 5 μA	+V _{BD} -1		$+V_{BD} + 0.3$	V
Logic level	V _{IL}	I _{IL} = 5 μA	0.3		0.8	V
Ü	V _{OH}	I _{OH} = 2 TTL loads	+V _{BD} -0.6		+V _{BD}	V
	V _{OL}	I _{OL} = 2 TTL loads	0		0.4	V
MULTIPLEXER CONTROL	PINS					
Logic Family - CMOS						
Logic level	I _{IH}	$I_{IH} = 5 \mu A$	2.3		+VA +0.3	V
	I _{IL}	$I_{IL} = 5 \mu A$	-0.3		0.8	V
POWER CONTROL PINS						
Logic Family - CMOS						
Logic lovel	V _{IH}	$I_{IH} = 5 \mu A$	2.3		+VA +0.3	V
Logic level	V _{IL}	I _{IL} = 5 μA	-0.3		0.8	V
POWER SUPPLY REQUIR	EMENTS					



SPECIFICATIONS (continued)

 $T_A = -40$ °C to 85°C, VCC = 5 V, VEE = -5 V, +VA = 5 V, +VBD = 5 V or 3.3 V, $V_{ref} = 4$ V, $f_{SAMPLE} = 1$ MSPS (unless otherwise noted)

PARA	METER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	+VBD		2.7	3.3	5.25	V
D	+VA		4.75	5	5.25	V
Power supply voltage	VCC		4.75	5	7.5	V
	VEE		-7.5	-5	-3	V
ADC driver positive supply (VCC) current (for OP1 and OP2 together)		VCC = +5, VEE = -5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		11.65		mA
ADC driver negative supply OP1 together)	(VEE) current (for OP1 and	VCC= +5V, CH0 - CH3 p and m inputs shorted to each other and connected to 2V		9.6		mA
+VA supply current, 1-MHz	sample rate			45	50	mA
Reference buffer (BUF-REF	supply current (VCC to	VCC= +5, PD-RBUF = 0, Quiescent current		8		mA
GND)		VCC = 5, PD-RBUF = 1 ⁽⁷⁾		10		μΑ
TEMPERATURE RANGE						
Operating free-air			-40		85	°C

⁽⁷⁾ PD-RBUF = 1 powers down the reference buffer (BUF-REF), note that it does not 3-state the BUF-REF output.



TIMING REQUIREMENTS

All specifications typical at -40° C to 85° C, +VA = +VBD = 5 V (1) (2) (3)

	PARAMETER	MIN	TYP	MAX	UNIT
t _(CONV)	Conversion time			650	ns
t _(ACQ)	Acquisition time	320			ns
t _(HOLD)	Sample capacitor hold time			25	ns
t _{pd1}	CONVST low to BUSY high			40	ns
t _{pd2}	Propagation delay time, end of conversion to BUSY low			15	ns
t _{pd3}	Propagation delay time, start of convert state to rising edge of BUSY			15	ns
t _{w1}	Pulse duration, CONVST low	40			ns
t _{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t _{w2}	Pulse duration, CONVST high	20			ns
	CONVST falling edge jitter			10	ps
t _{w3}	Pulse duration, BUSY signal low	t _(ACQ) min			ns
t _{w4}	Pulse duration, BUSY signal high			650	ns
t _{h1}	Hold time, first data bus transition (RD low, or CS low for read cycle, or BYTE or BUS18/16 input changes) after CONVST low	40			ns
t _{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t _{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t _{w5}	Pulse duration, RD low	50			ns
t _{en}	Enable time, \overline{RD} low (or \overline{CS} low for read cycle) to data valid			20	ns
t _{d2}	Delay time, data hold from RD high	5			ns
t _{d3}	Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid	10		20	ns
t _{w6}	Pulse duration, RD high	20			ns
t _{w7}	Pulse duration, CS high	20			ns
t _{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t _{pd4}	Propagation delay time, BUSY falling edge to next \overline{RD} (or \overline{CS} for read cycle) falling edge	0			ns
t _{d4}	Delay time, BYTE edge to BUS18/16 edge skew	0			ns
t _{su3}	Setup time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t _{h3}	Hold time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t _{dis}	Disable time, RD high (CS high for read cycle) to 3-stated data bus			20	ns
t _{d5}	Delay time, BUSY low to MSB data valid delay			0	ns
t _{d6}	Delay time, CS rising edge to BUSY falling edge	50			ns
t _{d7}	Delay time, BUSY falling edge to CS rising edge	50			ns
t _{su5}	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/16 transition setup time, from BUS18/16 to next BUS18/16.	50			ns
t _{su(ABORT)}	Setup time from the <u>falling edge</u> of \overline{CONVST} (used to start the valid conversion) to the next falling edge of \overline{CONVST} (when $\overline{CS} = 0$ and \overline{CONVST} are used to abort) or to the next falling edge of \overline{CS} (when \overline{CS} is used to abort).	60		550	ns

⁽¹⁾ All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. (2) See timing diagrams.

All timing are measured with 20 pF equivalent loads on all data bits and BUSY pins.

SLAS628-MARCH 2009 www.ti.com



TIMING REQUIREMENTS

All specifications typical at -40°C to 85°C, +VA = 5 V +VBD = 3 V $^{(1)}$ $^{(2)}$ $^{(3)}$

	PARAMETER	MIN	TYP	MAX	UNIT
t _(CONV)	Conversion time			650	ns
t _(ACQ)	Acquisition time	320			ns
t _(HOLD)	Sample capacitor hold time			25	ns
t _{pd1}	CONVST low to BUSY high			40	ns
t _{pd2}	Propagation delay time, end of conversion to BUSY low			25	ns
t _{pd3}	Propagation delay time, start of convert state to rising edge of BUSY			25	ns
t _{w1}	Pulse duration, CONVST low	40			ns
t _{su1}	Setup time, $\overline{\text{CS}}$ low to $\overline{\text{CONVST}}$ low	20			ns
t _{w2}	Pulse duration, CONVST high	20			ns
	CONVST falling edge jitter			10	ps
t _{w3}	Pulse duration, BUSY signal low	t _(ACQ) min			ns
t _{w4}	Pulse duration, BUSY signal high	, ,		650	ns
t _{h1}	Hold time, first data bus transition (RD low, or CS low for read cycle, or BYTE or BUS18/16 input changes) after CONVST low	40			ns
t _{d1}	Delay time, $\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low	0			ns
t _{su2}	Setup time, $\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high	0			ns
t _{w5}	Pulse duration, RD low	50			ns
t _{en}	Enable time, \overline{RD} low (or \overline{CS} low for read cycle) to data valid			30	ns
t _{d2}	Delay time, data hold from RD high	5			ns
t _{d3}	Delay time, BUS18/16 or BYTE rising edge or falling edge to data valid	10		30	ns
t _{w6}	Pulse duration, RD high	20			ns
t _{w7}	Pulse duration, CS high	20			ns
t _{h2}	Hold time, last $\overline{\text{RD}}$ (or $\overline{\text{CS}}$ for read cycle) rising edge to $\overline{\text{CONVST}}$ falling edge	50			ns
t _{pd4}	Propagation delay time, BUSY falling edge to next \overline{RD} (or \overline{CS} for read cycle) falling edge	0			ns
t _{d4}	Delay time, BYTE edge to BUS18/16 edge skew	0			ns
t _{su3}	Setup time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t _{h3}	Hold time, BYTE or BUS18/16 transition to RD falling edge	10			ns
t _{dis}	Disable time, RD high (CS high for read cycle) to 3-stated data bus			30	ns
t _{d5}	Delay time, BUSY low to MSB data valid delay			0	ns
t _{d6}	Delay time, $\overline{\text{CS}}$ rising edge to BUSY falling edge	50			ns
t _{d7}	Delay time, BUSY falling edge to $\overline{\text{CS}}$ rising edge	50			ns
t _{su5}	BYTE transition setup time, from BYTE transition to next BYTE transition, or BUS18/16 transition setup time, from BUS18/16 to next BUS18/16.	50			ns
t _{su(ABORT)}	Setup time from the <u>falling edge</u> of \overline{CONVST} (used to start the valid conversion) to the next falling edge of \overline{CONVST} (when $\overline{CS} = 0$ and \overline{CONVST} are used to abort) or to the next falling edge of \overline{CS} (when \overline{CS} is used to abort).	70		550	ns

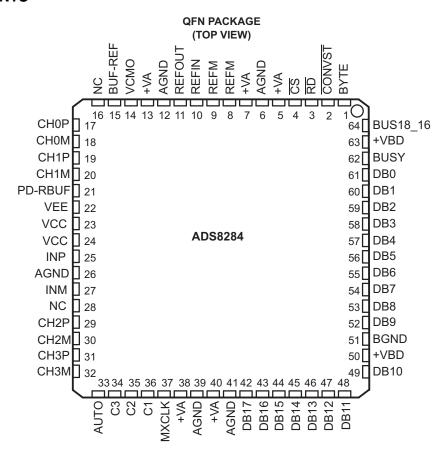
- (1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
- (2) See timing diagrams.
- (3) All timing are measured with 20-pF equivalent loads on all data bits and BUSY pins.

MULTIPLEXER TIMING REQUIREMENTS

VCC = 4.75 V to 7.5 V, VEE = -3 V to -7.5 V

		MIN	TYP	MAX	UNIT
t _{su6}	Setup time C1, C2 or C3 to MXCLK rising edge			600	ns
t _{d8}	Multiplexer and driver settle time (from MXCLK rising edge to CONVST falling edge)	600			ns

PIN ASSIGNMENTS



PIN FUNCTIONS

	PIN	I/O	DESCRIPTION
NO	NAME	1/0	DESCRIPTION
MULTIP	LEXER INPUT	PINS	
17	CH0P	I	Non-inverting analog input for differential multiplexer channel number 0. Device performance is optimized for $50-\Omega$ source impedance at this input.
18	СНОМ	I	Inverting analog input for differential multiplexer channel number 0. Device performance is optimized for 50-Ω source impedance at this input.
19	CH1P	ı	Non-inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50-Ω source impedance at this input.
20	CH1M	I	Inverting analog input for differential multiplexer channel number 1. Device performance is optimized for 50-Ω source impedance at this input.
29	CH2P	Non-inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50-Ω sou impedance at this input.	
30	CH2M	I	Inverting analog input for differential multiplexer channel number 2. Device performance is optimized for 50-Ω source impedance at this input.
31	СНЗР	I	Non-inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50 ohm source impedance at this input.
32	СНЗМ	I	Inverting analog input for differential multiplexer channel number 3. Device performance is optimized for 50-Ω source impedance at this input.
ADC IN	PUT PINS		
25	INP	- 1	ADC Non inverting input., connect 1-nF capacitor across INP and INM
27	INM	I	ADC Inverting input, connect 1-nF capacitor across INP and INM
REFERI	ENCE INPUT/	OUTPU	T PINS
8, 9	REFM	- 1	Reference ground.
10	REFIN	- 1	Reference Input. Add 0.1-μF decoupling capacitor between REFIN and REFM.
11	REFOUT	0	Reference Output. Add 1-μF capacitor between the REFOUT pin and REFM pin when internal reference is used.



PIN FUNCTIONS (continued)

	PIN PIN								
NO	NAME	I/O			DESCR	RIPTION			
14	VCMO	0	This pin outputs REFIN	I/2 and can be used t	o set common-mod	e voltage of differenti	al analog inputs		
15	BUF-REF	0		his pin outputs REFIN/2 and can be used to set common-mode voltage of differential analog inputs. uffered reference output. Useful to level shift bipolar signals using external resistors.					
	CONTROL PI		Danoica forciones car	out. Obordi to lovoi di	iii bipolai oigilalo ac	onig external redictors	,		
21	PD-RBUF	1	High on this pin powers	down the reference	huffer (BLIE-REE)				
	LEXER CONTI	POI DII		down the reference	bullet (BOT RET).				
33	AUTO	1	High level on this pin s	elects auto mode for	multiplexer scanning	a. Low level selects r	nanual mode of mul	Itinlexer scanning	
			In auto mode (AUTO =		·			1 0	
34	C3	I	not care in manual mod		01 001001101110 10001	to one on noing dag	o or wind t	50 = 1. The pin is do	
35	C2	_	Acts as multiplexer add multiplexer channel (ch			. In auto mode (AUTo	O = 1) C2 and C1 s	elect the last	
36	C1	I	Acts as multiplexer add multiplexer channel (ch				TO = 1) C2 and C1	select the last	
37	MXCLK	I	Multiplexer channel is so output can be connected					de. Device BUSY	
ADC DA	TA BUS								
40.40				8-BIT BUS		16-BIT	BUS	18-BIT BUS	
42-49, 52-61	Data Bus		BYTE = 0	BYTE = 1	BYTE = 1	BYTE = 0	BYTE = 0	BYTE = 0	
			BUS18/16 = 0	BUS18/16 = 0	BUS18/16 = 1	BUS18/16 = 0	BUS18/16 = 1	BUS18/16 = 0	
42	DB17	0	D17 (MSB)	D9	All ones	D17 (MSB)	All ones	D17 (MSB)	
43	DB16	0	D16	D8	All ones	D16	All ones	D16	
44	DB15	0	D15	D7	All ones	D15	All ones	D15	
45	DB14	0	D14	D6	All ones	D14	All ones	D14	
46	DB13	0	D13	D5	All ones	D13	All ones	D13	
47	DB12	0	D12	D4	All ones	D12	All ones	D12	
48	DB11	0	D11	D3	D1	D11	All ones	D11	
49	DB10	0	D10	D2	D0 (LSB)	D10	All ones	D10	
52	DB9	0	D9	All ones	All ones	D9	All ones	D9	
53	DB8	0	D8	All ones	All ones	D8	All ones	D8	
54	DB7	0	D7	All ones	All ones	D7	All ones	D7	
55	DB6	0	D6	All ones	All ones	D6	All ones	D6	
56	DB5	0	D5	All ones	All ones	D5	All ones	D5	
57	DB4	0	D4	All ones	All ones	D4	All ones	D4	
58	DB3	0	D3	All ones	All ones	D3	D1	D3	
59	DB2	0	D2	All ones	All ones	D2	D0 (LSB)	D2	
60	DB1	0	D1	All ones	All ones	D1	All ones	D1	
61	DB0	0	D0 (LSB)	All ones	All ones	D0 (LSB)	All ones	D0 (LSB)	
ADC CO	NTROL PINS								
62	BUSY	0	Status output. This pin	is held high when de	vice is converting.				
64	BUS18_16	ı	Bus size select input. U	Ised for selecting 18-	bit or 16-bit wide bu	us transfer. Refer to A	DC DATA BUS des	scription above.	
1	BYTE	I	Byte Select Input. Used						
2	CONVST	Ι	Convert start. This inpu	it is active low and ca	ın act independent o	of the CS input.			
3	RD	Ι	Synchronization pulse	for the parallel output	-				
4	CS	I	Chip select.						
DEVICE	POWER SUPI	PLIES							
22	VEE		Negative supply for OPA (OP1, OP2)						
23, 24	VCC		Positive supply for OPA	A (OP1, OP2, BUF-R	EF)				
5, 7, 13, 38, 40	+VA		Analog power supply.						
6, 12, 26, 39, 41	AGND		Analog ground.						
50, 63	+VBD		Digital power supply fo	r ADC bus.					



PIN FUNCTIONS (continued)

	PIN	1/0	DESCRIPTION				
NO	NAME	1/0	DESCRIPTION				
51	BGND		igital ground for ADC bus interface digital supply.				
NOT CO	NNECTED PI	IS					
16, 28	NC		onnection.				

DEVICE OPERATION AND TIMING DIAGRAMS

The ADS8284 is analog system-on-chip (SoC) device. The device includes a multiplexer, a differential input/differential output ADC driver and differential input high-performance ADC, an additional internal reference, a buffered reference output, and a REF/2 output.

Figure 1 shows the basic operation of the device (including all elements). Subsequent sections describe the detailed timings of the individual blocks of the device (primarily the multiplexer and ADC).

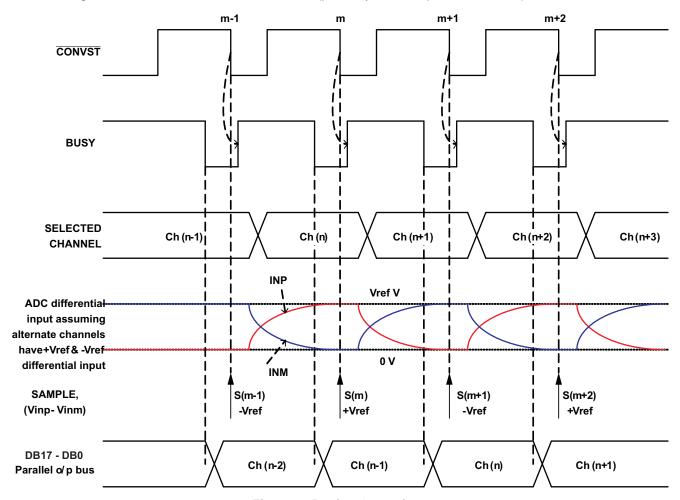


Figure 1. Device Operation

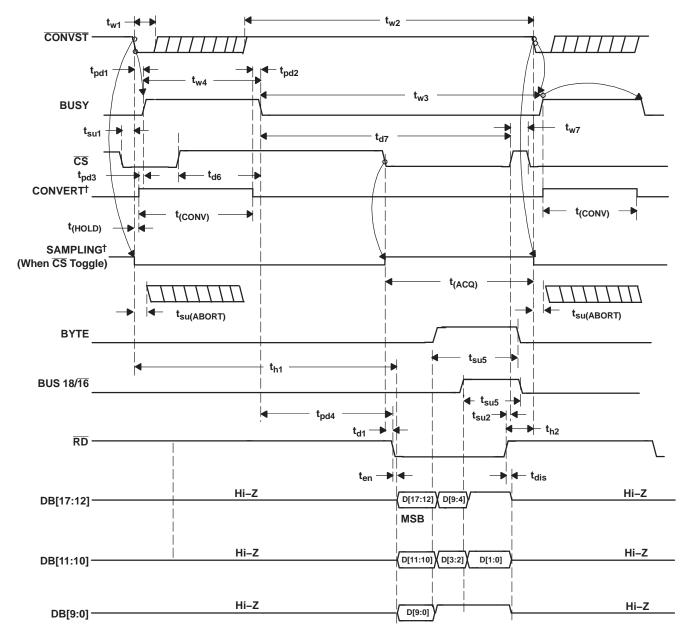
As shown in the diagram, the device can be controlled with only one (CONVST) digital input. On the falling edge of CONVST, the BUSY output of the device goes high. A high level on BUSY indicates the device has sampled the signal and it is converting the sample into its digital equivalent. After the conversion is complete, the BUSY output falls to a logic low level and the device output data corresponding to the recently converted sample is available for reading.

SLAS628-MARCH 2009 www.ti.com



It is recommended (not mandatory) to short the BUSY output of the device to the MXCLK input. The device selects a new channel at every rising edge of MXCLK. The multiplexer is differential. The multiplexer and ADC driver are designed to settle to the 18-bit level before sampling; even at the maximum conversion speed.

ADC control and timing: The timing diagrams in this section describe ADC operation; multiplexer operation is described in a later section.



[†]Signal internal to device

Figure 2. Timing for Conversion and Acquisition Cycles with CS and RD Toggling

13

www.ti.com

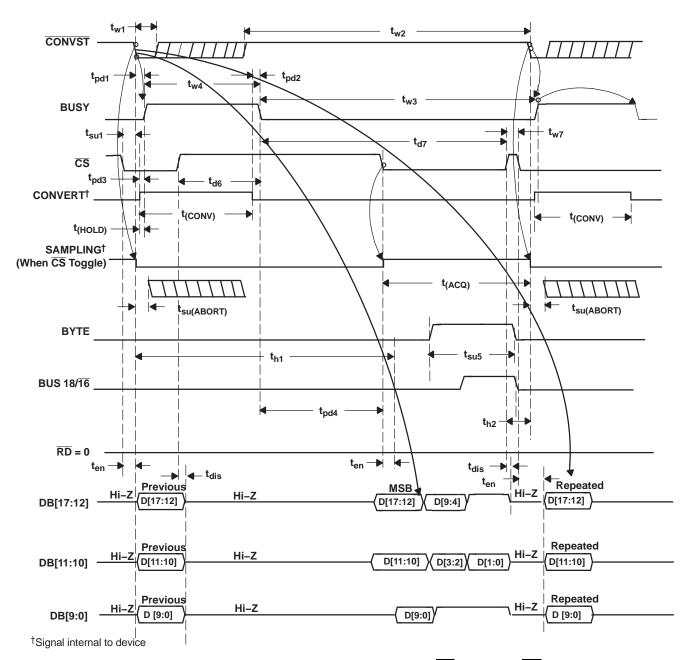
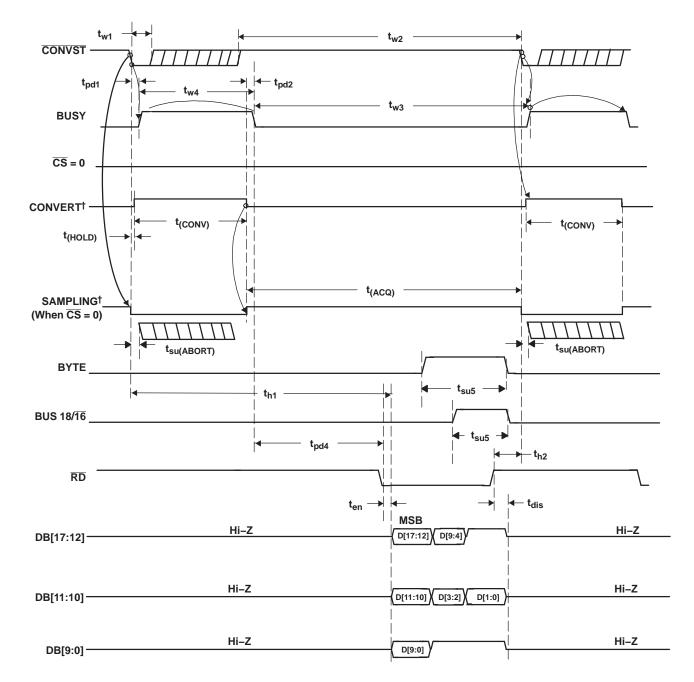


Figure 3. Timing for Conversion and Acquisition Cycles with $\overline{\text{CS}}$ Toggling, $\overline{\text{RD}}$ Tied to BDGND





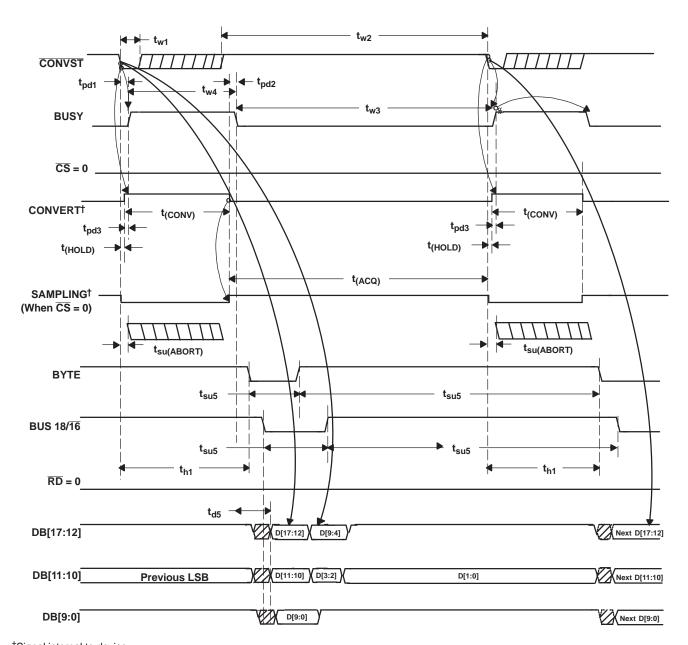
[†]Signal internal to device

Figure 4. Timing for Conversion and Acquisition Cycles With CS Tied to BDGND, RD Toggling

15



www.ti.com



[†]Signal internal to device

Figure 5. Timing for Conversion and Acquisition Cycles With $\overline{\text{CS}}$ and $\overline{\text{RD}}$ Tied to BDGND - Auto Read



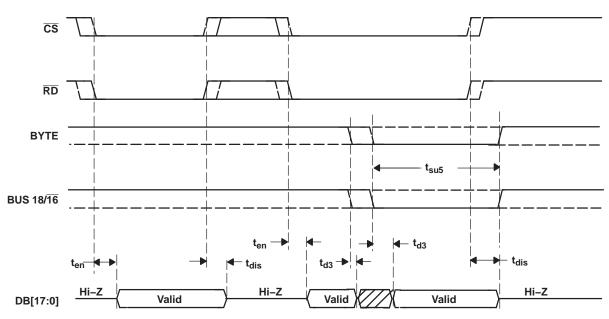


Figure 6. Detailed Timing for Read Cycles

Multiplexer: The multiplexer has two modes of sequencing namely auto sequencing and manual sequencing. Multiplexer mode selection and operation is controlled with the AUTO, C1, C2, C3, and MXCLK pins.

Auto sequencing: A logic one level on the AUTO pin selects auto sequencing mode. It is possible to select the number of channels to be scanned (always starting from channel zero) in auto sequencing mode. Pins C1 and C2 select the channel count (last channel in the auto sequence).

On every rising edge of MXCLK while C3 is at the logic zero level, the next higher channel (in ascending order) is selected. Channel selection rolls over to channel zero on the rising edge of MXCLK after channel selection reaches the *channel count* (last channel in the auto sequence selected by pins C1 and C2).

Any time during the sequence the channel sequence can be reset to channel zero. A rising edge on MXCLK while C3 is at the logic one level resets channel selection to channel zero.

CLOCK PIN CHANNEL COUNT PINS LAST CHANNEL IN SEQUENCE CHANNEL SEQUENCE MXCLK C3 C2 C1 0 0,0,0,0.. 0 0 1 0 0 0 1 0,1,0,1,.. 1 1 0 1 0 2 0,1,2,0,1,2,0... 1 0 1 1 1 3 0,1,2,3,0,1,2,3,0... Χ 1 Χ Χ $n \rightarrow 0$ (channel reset to zero) 1

Podult Folder in (s): ADS 328

Table 1. Channel Selection in Auto Mode



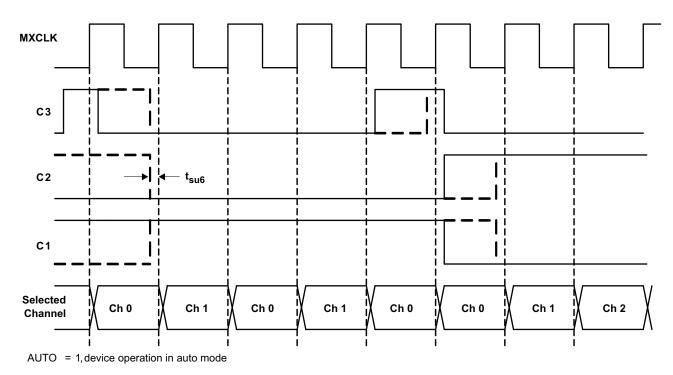


Figure 7. Multiplexer Auto Mode Timing Diagram

Manual sequencing: A logic zero level on the AUTO pin selects manual sequencing mode. Pins C1and C2 set the channel address. On the rising edge of MXCLK, the addressed channel is connected to the ADC driver input.

MODE CHANNEL ADDRESS PINS CLOCK PIN CHANNEL **MXCLK AUTO** C3 C2 C1 0 Χ 0 0 0 0 Χ 0 1 1 0 Χ 0 2 1 0 Х 1 1 3

Table 2. Channel Selection in Manual Mode

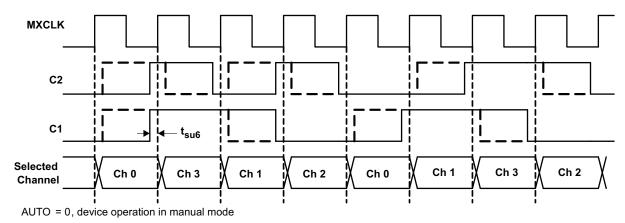
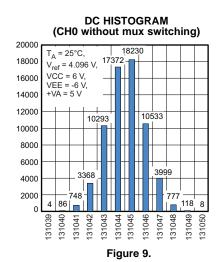


Figure 8. Multiplexer Manual Mode Timing Diagram

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS



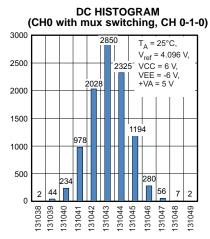


Figure 10.

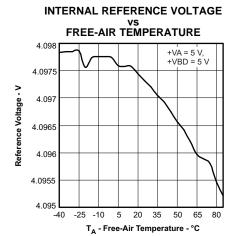


Figure 11.

INTERNAL REFERENCE VOLTAGE VS SUPPLY VOLTAGE

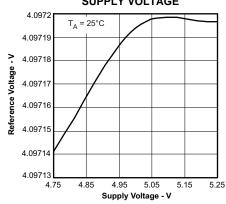


Figure 12.

ANALOG VOLTAGE (+VA) SUPPLY CURRENT (IA)

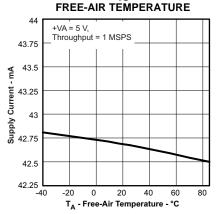


Figure 13.

SUPPLY CURRENT (IA) vs ANALOG VOLTAGE (+VA)

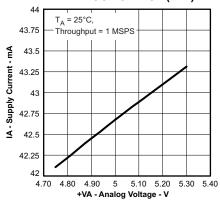


Figure 14.

ANALOG SUPPLY CURRENT vs SAMPLE RATE

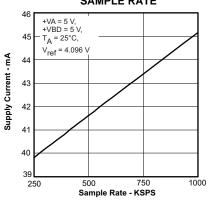


Figure 15.

OPA POSITIVE SUPPLY CURRENT (I_{CC})

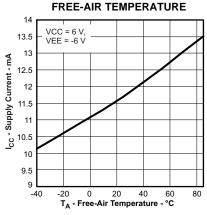


Figure 16.

P odu it Fo der link s): ADS 128

OPA POSITIVE SUPPLY CURRENT (I_{CC}) vs

OPA POSITIVE SUPPLY VOLTAGE (+VCC)

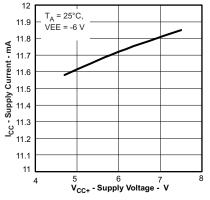


Figure 17.



TYPICAL CHARACTERISTICS (continued)

Figure 18.

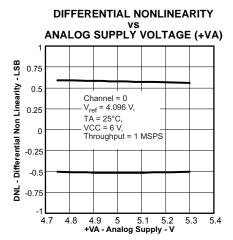
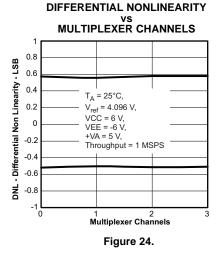


Figure 21.



OPA NEGATIVE SUPPLY CURRENT (IEE) vs OPA NEGATIVE SUPPLY VOLTAGE

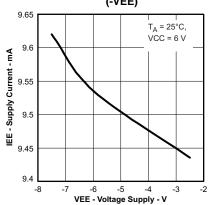


Figure 19.

DIFFERENTIAL NONLINEARITY VS REFERENCE VOLTAGE

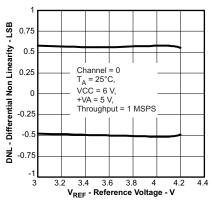


Figure 22.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

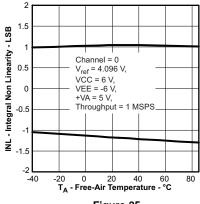


Figure 25.

DIFFERENTIAL NONLINEARITY vs

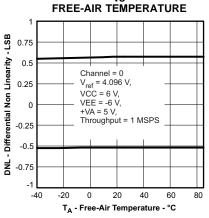


Figure 20.

DIFFERENTIAL NONLINEARITY VS OPA SUPPLY VOLTAGE (VCC)

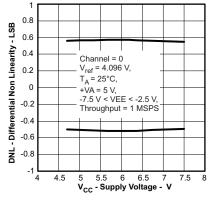


Figure 23.

INTEGRAL NONLINEARITY vs ANALOG SUPPLY VOLTAGE (+VA)

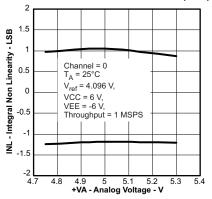


Figure 26.

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS (continued)

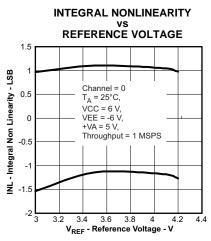


Figure 27.

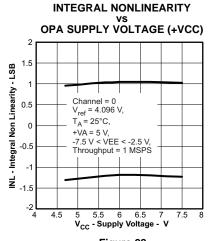


Figure 28.

FULL CHIP OFFSET ERROR

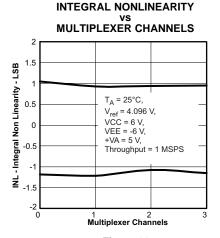


Figure 29.

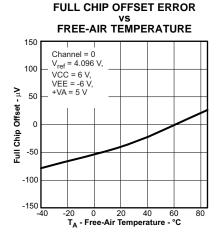


Figure 30.

FULL CHIP OFFSET ERROR

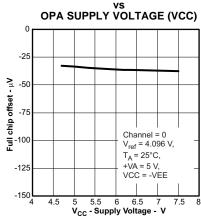
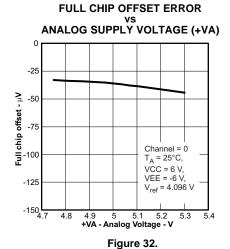


Figure 31.



r igure oz.

FULL CHIP GAIN ERROR

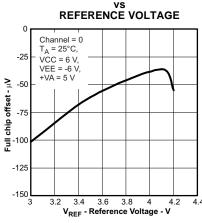


Figure 33.

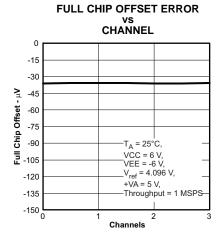


Figure 34.

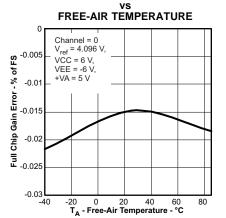
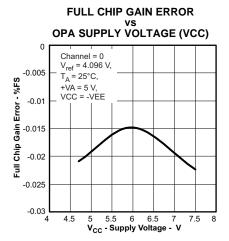


Figure 35.



TYPICAL CHARACTERISTICS (continued)





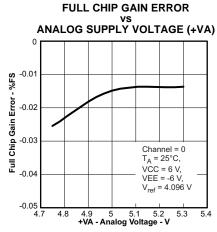


Figure 37.

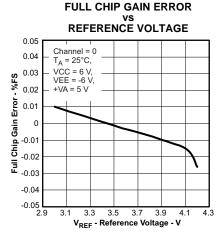


Figure 38.

TOTAL HARMONIC DISTORTION

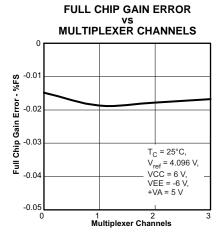


Figure 39.

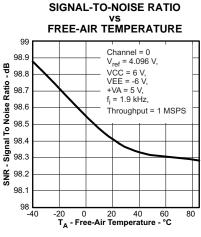


Figure 40.

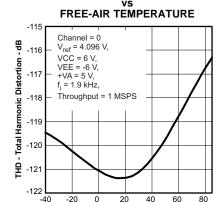


Figure 41.



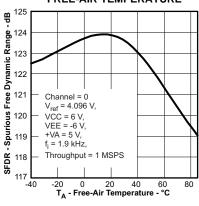


Figure 42.

EFFECTIVE NUMBER OF BITS vs FREE-AIR TEMPERATURE

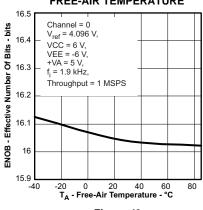


Figure 43.

SIGNAL-TO-NOISE RATIO VS ANALOG SUPPLY VOLTAGE (+VA)

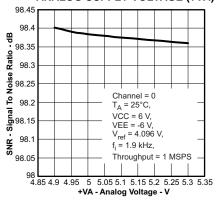
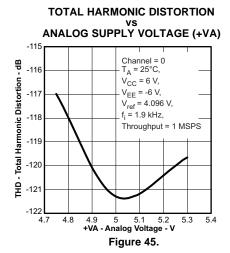


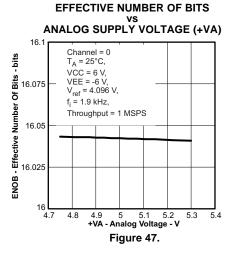
Figure 44.

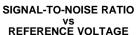
Texas Instruments

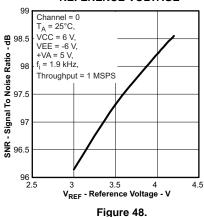
TYPICAL CHARACTERISTICS (continued)

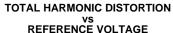


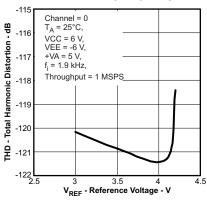
SPURIOUS FREE DYNAMIC RANGE ANALOG SUPPLY VOLTAGE (+VA) **9** 125 124 123 122 Channel = 0 <u>9</u> 121 T_A = 25°C, VCC = 6 V, Spurious 119 VEE = -6 V, V_{ref} = 4.096 V, $f_i = 1.9 \text{ kHz},$ Throughput = 1 MSPS H 118 4.9 5 5.1 5.2 +VA - Analog Voltage - V Figure 46.



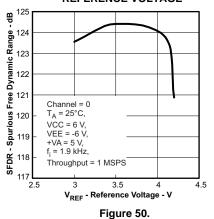




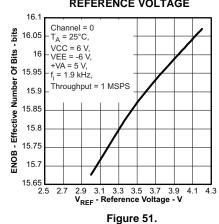




SPURIOUS FREE DYNAMIC RANGE vs REFERENCE VOLTAGE



EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE



SIGNAL-TO-NOISE RATIO

Figure 49.

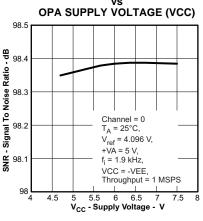


Figure 52.

TOTAL HARMONIC DISTORTION VS OPA SUPPLY VOLTAGE (VCC)

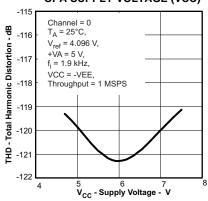


Figure 53.



TYPICAL CHARACTERISTICS (continued)

SPURIOUS FREE DYNAMIC RANGE **OPA SUPPLY VOLTAGE (VCC)** g 124 Ran 123 Dynamic 122 **8** 12 Channel = 0 **S** 120 T_A = 25°C, V_{ref} = 4.096 V. +VA = 5 V, $f_i = 1.9 \text{ kHz}$ SFDR. VCC = - VEE Throughput = 1 MSPS 117

Figure 54.

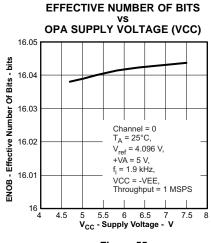


Figure 55.

SPURIOUS FREE DYNAMIC RANGE

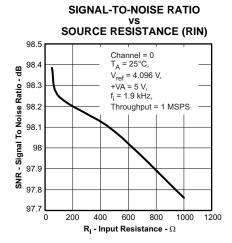


Figure 56.

TOTAL HARMONIC DISTORTION vs SOURCE RESISTANCE (RIN)

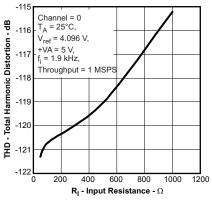


Figure 57.

vs SOURCE RESISTANCE (RIN) Dynamic Range - dB 124 122 121 121 Channel = 0 T_A = 25°C, V_{ref} = 4.096 V, +VA = 5 V. $f_i = 1.9 \text{ kHz},$ Throughput = 1 MSPS 120 - Spurious Free 119 118 SFDR-116 200 400 600 800 1000 1200 $\textbf{R}_{\textbf{I}}$ - Input Resistance - Ω

Figure 58.

SOURCE RESISTANCE (RIN)

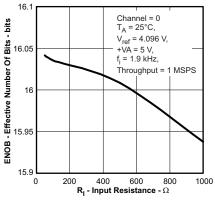
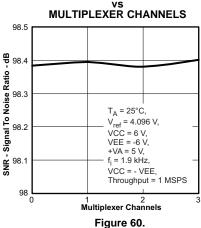
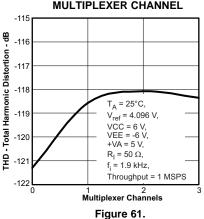


Figure 59.

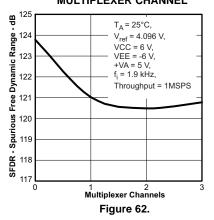
SIGNAL-TO-NOISE RATIO



TOTAL HARMONIC DISTORTION
vs
MULTIPLEXER CHANNEL

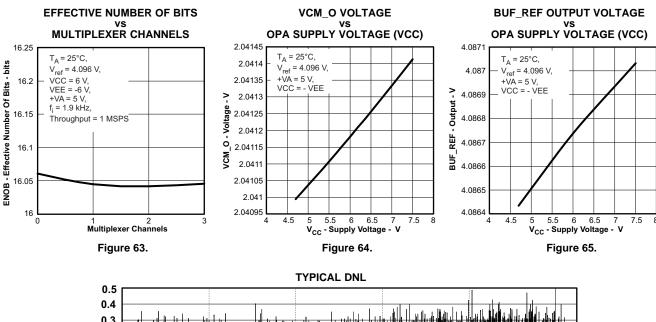


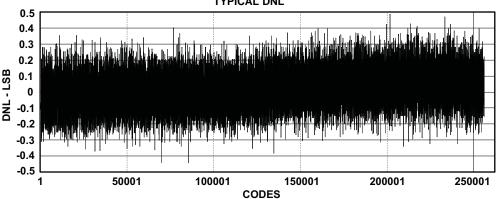
SPURIOUS FREE DYNAMIC RANGE
vs
MULTIPLEXER CHANNEL



TEXAS INSTRUMENTS

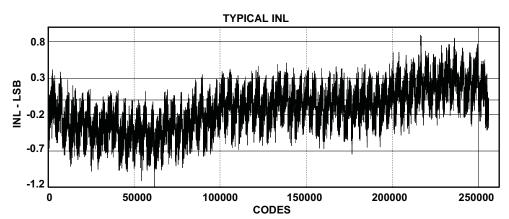
TYPICAL CHARACTERISTICS (continued)





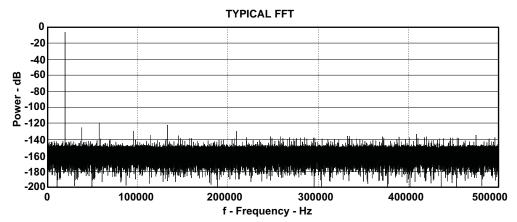
Test conditions: +VA = 5 V, +VBD = 5 V, T_A =25°C, F_s = 1 MSPS, V_{ref} = 4.096 V Figure 66.

Figure 67.



Test conditions: +VA = 5 V, +VBD = 5 V, T_A =25°C, F_S = 1 MSPS, V_{ref} = 4.096 V Figure 68.

TYPICAL CHARACTERISTICS (continued)



Test conditions: F_i = 19 kHz, F_s = 1 MSPS, V_{ref} = 4.096V, SNR = 97.8 dB, THD = 113 dB, SFDR = 115 dB Figure 69.



APPLICATION INFORMATION

As discussed before, the ADS8284 is 18-bit analog SoC that includes various blocks like a multiplexer, ADC driver, internal reference, internal reference buffer, buffered reference output, and Ref/2 output on-board. The following diagram shows the recommended analog and digital interfacing of the ADS8284.

APPLICATION DIAGRAM

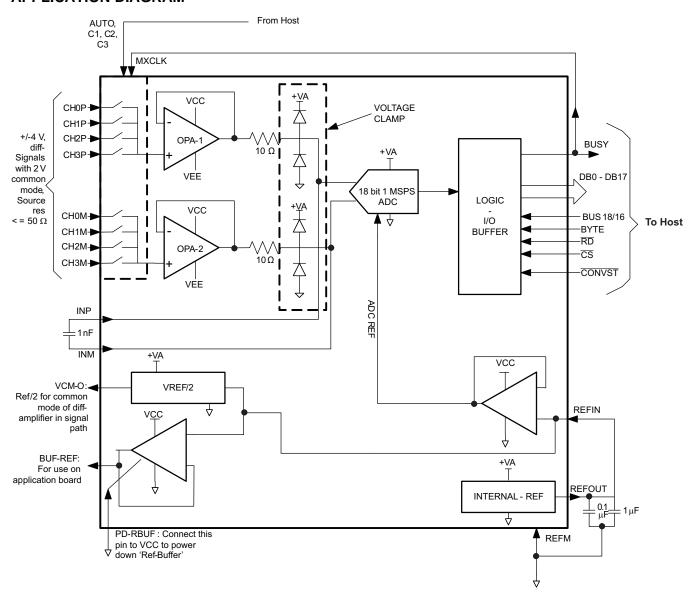
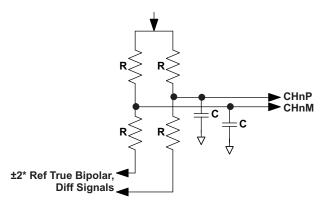


Figure 70. Analog and Digital Interface Diagram

As shown in Figure 70, the ADS8284 accepts unipolar differential analog inputs in the range of $\pm V_{ref}$ with a common-mode voltage of $V_{ref}/2$ (0 to V_{ref} at positive input and V_{ref} to 0 at negative input). An application may require the interfacing of true bipolar input signals. Figure 71 shows the conversion of bipolar input signals to unipolar differential signals.



From BUF-REF o/p of ADC (Use external buffer if current drawn by resistor network exceeds current output specification of reference buffer)



Note: Value of R depends on signal BW Use R = 1.2 k Ω for signal BW <= 10 kHz. Choose C as per signal BW, 3 dB BW (filt) = RC/2

Figure 71. Conversion of Bipolar Input Signals to Unipolar Differential Signals

MICROCONTROLLER INTERFACING

ADS8284 to 8-Bit Microcontroller Interface

Figure 72 shows a parallel interface between the ADS8284 and a typical microcontroller using an 8-bit data bus. The BUSY signal is used as a falling edge interrupt to the microcontroller.

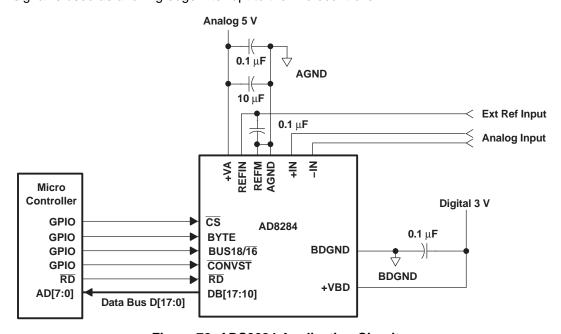


Figure 72. ADS8284 Application Circuitry

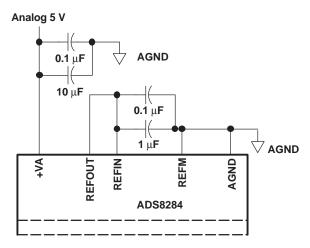


Figure 73. ADS8284 Using Internal Reference



PRINCIPLES OF OPERATION

The ADS8284 features a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution which inherently includes a sample/hold function. See Figure 72 for the application circuit for the ADS8284.

The conversion clock is generated internally. The conversion time of 650 ns is capable of sustaining a 1 MHz throughput.

The analog input voltage to ADC is provided to two input pins AINP and AINM. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8284 can operate with an external reference with a range from 3.0 V to 4.2 V. The reference voltage on the input pin 10 (REFIN) of the converter is internally buffered. A clean, low noise, well-decoupled reference voltage on this pin is required to ensure good performance of the converter. A low noise band-gap reference like the REF5040 can be used to drive this pin. A 0.1- μ F decoupling capacitor is required between REFIN and REFM pins (pin 10 and pin 9) of the converter. This capacitor should be placed as close as possible to the pins of the device. Designers should strive to minimize the routing length of the traces that connect the terminals of the capacitor to the pins of the converter. An RC network can also be used to filter the reference voltage. A 100- Ω series resistor and a 0.1- μ F capacitor, which can also serve as the decoupling capacitor can be used to filter the reference voltage.

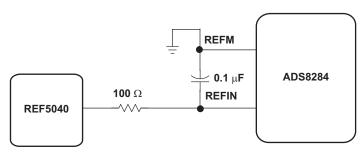


Figure 74. ADS8284 Using External Reference

The ADS8284 also has limited low pass filtering capability built into the converter. The equivalent circuitry on the REFIN input is as shown in Figure 75.

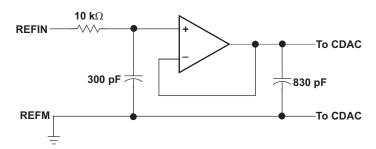


Figure 75. Simplified Reference Input Circuit

The REFM input of the ADS8284 should always be shorted to AGND. A 4.096-V internal reference is included. When the internal reference is used, pin 11 (REFOUT) is connected to pin 10 (REFIN) with an 0.1- μ F decoupling capacitor and 1- μ F storage capacitor between pin 11 (REFOUT) and pin 9 (REFM) (see Figure 73). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion (see Figure 75). Pin 11 (REFOUT) can be left unconnected (floating) if external reference is used.

TEXAS INSTRUMENTS

ANALOG INPUT

The device features an analog multiplexer, a differential, high input impedance, unity gain ADC driver, and a high performance ADC. Typically alot of care is required for driving circuit component selection and board layout for high resolution ADC driving. However an on-board ADC driver simplifies the job for the user. All that is required is to decouple AINP and AINM with a 1-nF decoupling capacitor across these two terminals as close to the device as possible. The multiplexer inputs tolerate source impedance of up to 50 Ω for specified device performance at an operating speed of 1-MSPS. This relaxes constraints on the signal conditioning circuit. In the case of true bipolar input signals, it is possible to condition them with a resister divider as shown in Figure 71. The device permits use of 1.2-k Ω resistors for the divider with effective source impedance of 600 Ω for signal bandwidth less than 10 kHz. A suitable capacitor value used to limit signal bandwidth limits noise coming from the resistor divider network. Care must be taken concerning absolute analog voltage at the multiplexer input terminals. This voltage should not exceed VCC and VEE. The clamp at the driver OPA limits the voltage applied to the ADC input.

Reading Data

The ADS8284 outputs full parallel data in straight binary format as shown in Table 3. The parallel output is active when CS and RD are both low. There is a minimal quiet zone requirement around the falling edge of CONVST. This is 50 ns prior to the falling edge of CONVST and 40 ns after the falling edge. No data read should attempted within this zone. Any other combination of CS and RD sets the parallel output to 3-state. BYTE and BUS18/16 are used for multiword read operations. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. BUS18/16 is used whenever the last two bits on the 18-bit bus is output on either bytes of the higher 16-bit bus. Refer to Table 3 for ideal output codes.

ranco er raear inpar remages ana eacpar econo								
DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY						
Full scale range	2 × (+V _{ref})	- DIGITAL OUTPUT STRAIGHT BINARY						
Least significant bit (LSB)	2 x (+V _{ref})/262144	BINARY CODE	HEX CODE					
+Full scale	(+V _{ref}) - 1 LSB	01 1111 1111 1111 1111	1FFFF					
Midscale	0 V	00 0000 0000 0000 0000	00000					
Midscale – 1 LSB	0 V – 1 LSB	11 1111 1111 1111 1111	3FFFF					
Zero	-V _{ref}	10 0000 0000 0000 0000	20000					

Table 3. Ideal Input Voltages and Output Codes

The output data is a full 18-bit word (D17-D0) on DB17-DB0 pins (MSB-LSB) if both BUS18/ $\overline{16}$ and BYTE are low.

The result may also be read on an 16-bit bus by using only pins DB17–DB2. In this case two reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 16 most significant bits (D17–D2) on pins DB17–DB2, then bringing BUS18/16 high while holding BYTE low. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB3–DB2.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB17–DB10. In this case three reads are necessary: the first as before, leaving both BUS18/16 and BYTE low and reading the 8 most significant bits on pins DB17–DB10, then bringing BYTE high while holding BUS18/16 low. When BYTE is high, the medium bits (D9–D2) appear on pins DB17–DB10. The last read is done by bringing BUS18/16 high while holding BYTE high. When BUS18/16 is high, the lower two bits (D1–D0) appear on pins DB11–DB10. The last read cycle is not necessary if only the first 16 most significant bits are of interest.

All of these multiword read operations can be performed with multiple active \overline{RD} (toggling) or with \overline{RD} held low for simplicity. This is referred to as the AUTO READ operation.

DATA READ OUT BYTE BUS18/16 **PINS PINS PINS PINS PINS** DB17-DB12 DB11-DB10 DB9-DB4 DB3-DB2 DB1-DB0 All One's D1-D0 All One's All One's All One's High High Low High All One's All One's All One's D1-D0 All One's

Podult Folder Link's):ADS 828

Table 4. Conversion Data Read Out



ADS8284



Table 4. Conversion Data Read Out (continued)

					DATA READ OUT		
BYTE	BUS18/16	PINS DB17-DB12	PINS DB11-DB10	PINS DB9-DB4	PINS DB3-DB2	PINS DB1-DB0	
	High	Low	D9-D4	D3-D2	All One's	All One's	All One's
	Low	Low	D17-D12	D11-D10	D9-D4	D3-D2	D1-D0

INSTRUMENTS



PACKAGE OPTION ADDENDUM

www.ti.com 3-Apr-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS8284IBRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8284IBRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8284IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8284IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

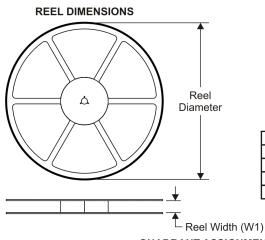
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

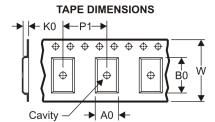
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

www.ti.com 2-Apr-2009

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8284IBRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8284IBRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8284IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8284IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2



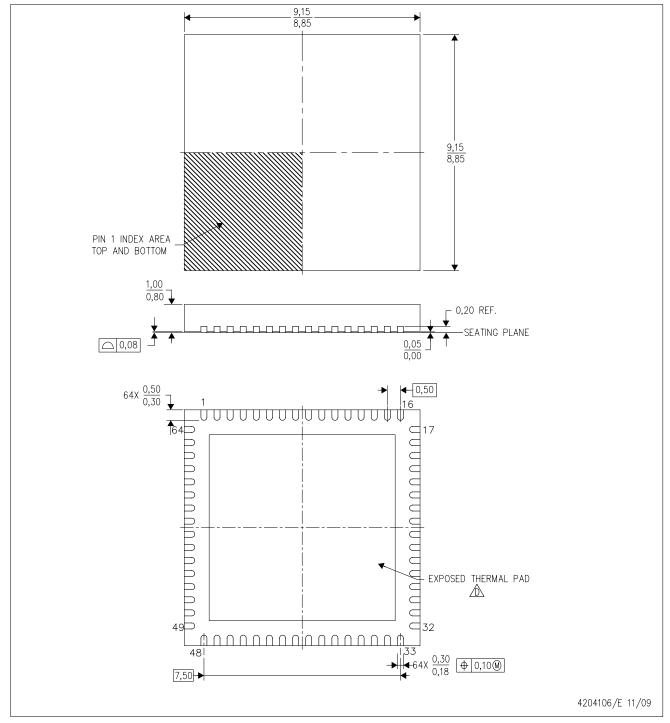
www.ti.com 2-Apr-2009



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8284IBRGCR	VQFN	RGC	64	2000	333.2	345.9	28.6
ADS8284IBRGCT	VQFN	RGC	64	250	333.2	345.9	28.6
ADS8284IRGCR	VQFN	RGC	64	2000	333.2	345.9	28.6
ADS8284IRGCT	VQFN	RGC	64	250	333.2	345.9	28.6

RGC(S-PVQFN-N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO-LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.

- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance.

 See the Product Data Sheet for details regarding the exposed thermal pad dimensions.



THERMAL PAD MECHANICAL DATA



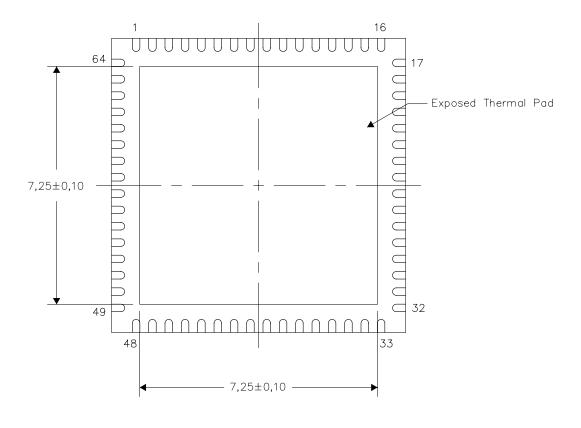
RGC (S-PVQFN-N64)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No—Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

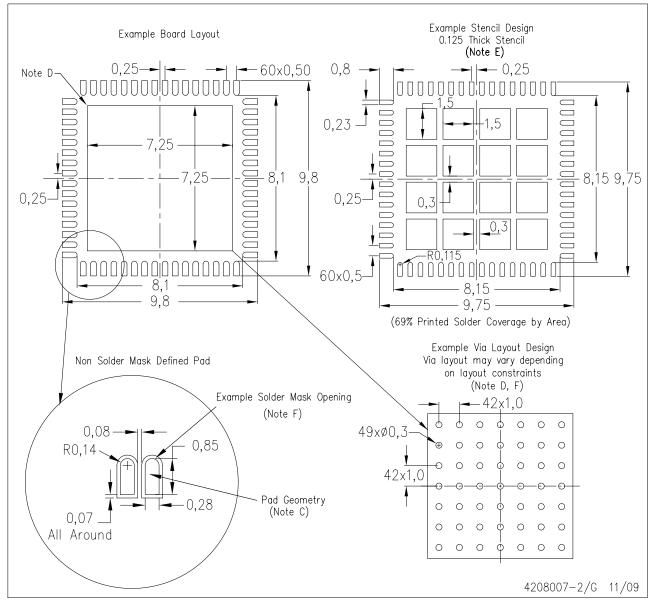


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGC (S-PVQFN-N64)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat—Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com www.ti.com.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products Applications Amplifiers amplifier.ti.com Audio www.ti.com/audio **Data Converters** dataconverter.ti.com Automotive www.ti.com/automotive **DLP® Products** www.dlp.com Communications and www.ti.com/communications Telecom DSP Computers and www.ti.com/computers dsp.ti.com Peripherals Clocks and Timers www.ti.com/clocks Consumer Electronics www.ti.com/consumer-apps Interface interface.ti.com **Energy** www.ti.com/energy Industrial www.ti.com/industrial Logic logic.ti.com Power Mgmt power.ti.com Medical www.ti.com/medical Microcontrollers microcontroller.ti.com www.ti.com/security Security **RFID** www.ti-rfid.com Space, Avionics & www.ti.com/space-avionics-defense Defense RF/IF and ZigBee® Solutions www.ti.com/lprf Video and Imaging www.ti.com/video www.ti.com/wireless-apps Wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2010, Texas Instruments Incorporated

