16-, 14-, 12-Bit, Six-Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **Family of 16-, 14-, 12-Bit, Pin- and Software-Compatible ADCs**
- **Six SAR ADCs Grouped in Three Pairs**
- **Maximum Data Rate Per Channel with Internal Conversion Clock and Reference:**
  ADS8556: 630kSPS (PAR) or 450kSPS (SER)
  ADS8557: 670kSPS (PAR) or 470kSPS (SER)
  ADS8558: 730kSPS (PAR) or 500kSPS (SER)
- **Maximum Data Rate with External Conversion Clock and Reference:**
  800kSPS (PAR) or 530kSPS (SER)
- **Pin-Selectable or Programmable Input Voltage Ranges: Up to ±12V**
- **Excellent Signal-to-Noise Performance:**
  91.5dB (ADS8556)
  85dB (ADS8557)
  73.9dB (ADS8558)
- **Programmable and Buffered Internal Reference: 0.5V to 2.5V and 0.5V to 3.0V**
- **Comprehensive Power-Down Modes:**
  Deep Power-Down (Standby Mode)
  Partial Power-Down
  Auto-Nap Power-Down
- **Selectable Parallel or Serial Interface**
- **Operating Temperature Range:**
  –40°C to +125°C
- **LQFP-64 Package**

APPLICATIONS

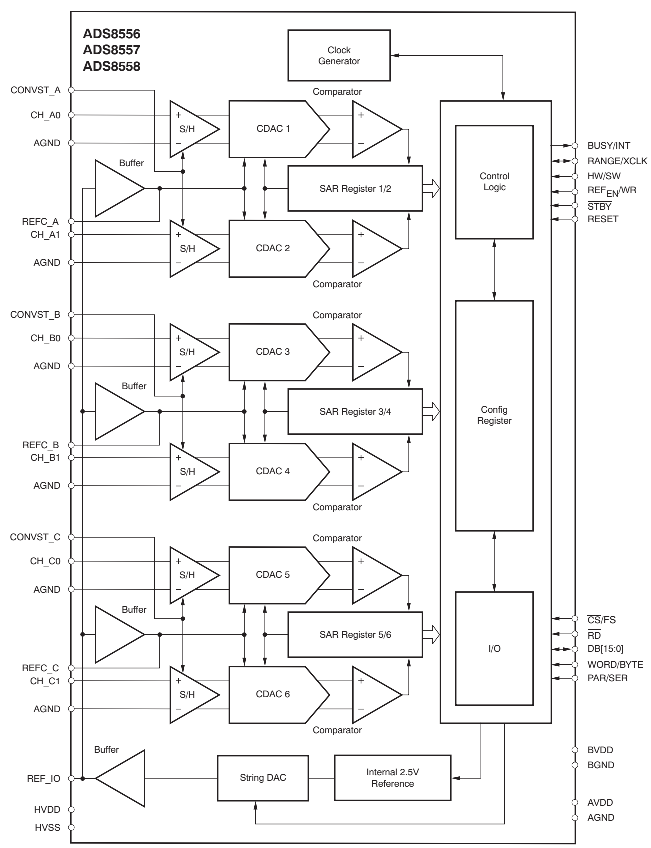
- **Power Quality Measurement**
- **Protection Relays**
- **Multi-Axis Motor Control**
- **Programmable Logic Controllers**
- **Industrial Data Acquisition**

DESCRIPTION

The ADS8556/7/8 contain six low-power, 16-, 14-, or 12-bit, successive approximation register (SAR) based analog-to-digital converters (ADCs) with true bipolar inputs. Each channel contains a sample-and-hold circuit that allows simultaneous high-speed multi-channel signal acquisition.

The ADS8556/7/8 support data rates of up to 730kSPS in parallel interface mode or up to 500kSPS if the serial interface is used. The bus width of the parallel interface can be set to eight or 16 bits. In serial mode, up to three output channels can be activated.

The ADS8556/7/8 is specified over the full industrial temperature range of –40°C to +125°C and is available in an LQFP-64 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	RESOLUTION (Bits)	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8556I	16	LQFP-64	PM	ADS8556IPM	Tray, 160
				ADS8556IPMR	Tape and Reel, 1000
ADS8557I	14	LQFP-64	PM	ADS8557IPM	Tray, 160
				ADS8557IPMR	Tape and Reel, 1000
ADS8558I	12	LQFP-64	PM	ADS8558IPM	Tray, 160
				ADS8558IPMR	Tape and Reel, 1000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		ADS8556, ADS8557, ADS8558	UNIT
Supply voltage, HVDD to AGND		–0.3 to +18	V
Supply voltage, HVSS to AGND		–18 to +0.3	V
Supply voltage, AVDD to AGND		–0.3 to +6	V
Supply voltage, BVDD to BGND		–0.3 to +6	V
Analog input voltage		HVSS – 0.3 to HVDD + 0.3	V
Reference input voltage with respect to AGND		AGND – 0.3 to AVDD + 0.3	V
Digital input voltage with respect to BGND		BGND – 0.3 to BVDD + 0.3	V
Ground voltage difference AGND to BGND		±0.3	V
Input current to all pins except supply		–10 to +10	mA
Maximum virtual junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±2000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, AVDD to AGND		4.5	5	5.5	V
Supply voltage, BVDD to BGND	Low-voltage levels	2.7	3.0	3.6	V
	5V logic levels	4.5	5	5.5	V
Input supply voltage, HVDD to AGND	Range 1 (±2 × V_{REF})	2 × V_{REF}		16.5	V
	Range 2 (±4 × V_{REF})	4 × V_{REF}		16.5	V
Input supply voltage, HVSS to AGND	Range 1 (±2 × V_{REF})	–16.5		–2 × V_{REF}	V
	Range 2 (±4 × V_{REF})	–16.5		–4 × V_{REF}	V
Reference input voltage (V_{REF})		0.5	2.5	3.0	V
Analog inputs (also see the *Analog Inputs* section)	Range 1 (±2 × V_{REF})	–2 × V_{REF}		+2 × V_{REF}	V
	Range 1 (±4 × V_{REF})	–4 × V_{REF}		+4 × V_{REF}	V
Operating ambient temperature range, T_A		–40		+125	°C

DISSIPATION RATINGS[1]

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	T_A ≤ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING	T_A = +125°C POWER RATING
LQFP-64	20.8mW/°C	2.60W	1.66W	1.35W	0.52W

(1) Based on High-K θ_{JA}.

THERMAL CHARACTERISTICS

Over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8556, ADS8557, ADS8558 MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance[1]		74		°C/W
		High-K thermal resistance[1]		48		°C/W
θ_{JC}	Junction-to-case thermal resistance			16		°C/W
P_D	Device power dissipation	ADS8556, HVDD = +15V, HVSS = –15V, AVDD = 5V, BVDD = 3V, and f_{DATA} = maximum		251.7	298.5	mW
		ADS8557, HVDD = +15V, HVSS = –15V, AVDD = 5V, BVDD = 3V, and f_{DATA} = maximum		253.2	303.0	mW
		ADS8558, HVDD = +15V, HVSS = –15V, AVDD = 5V, BVDD = 3V, and f_{DATA} = maximum		262.2	318.0	mW

(1) Modeled in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3.

ELECTRICAL CHARACTERISTICS: ADS8556

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = 630kSPS in parallel mode or 450kSPS in serial mode, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8556			UNIT
		MIN	TYP[1]	MAX	
DC ACCURACY					
Resolution			16		Bits
No missing codes		16			Bits
Integral linearity error INL	At T_A = –40°C to +85°C	–3	±1.5	3	LSB
	At T_A = –40°C to +125°C	–4	±1.5	4	LSB
Differential linearity error DNL	At T_A = –40°C to +85°C	–1	±0.75	1.5	LSB
	At T_A = –40°C to +125°C	–1	±0.75	2	LSB
Offset error		–4.0	±0.8	4.0	mV
Offset error drift			±3.5		µV/°C
Gain error	Referenced to voltage at REFIO	–0.75	±0.25	0.75	%FSR
Gain error drift	Referenced to voltage at REFIO		±6		ppm/°C
Power-supply rejection ratio PSRR	At output code FFFFh, related to AVDD		60		dB
SAMPLING DYNAMICS					
Acquisition time t_{ACQ}		280			ns
Conversion time per ADC t_{CONV}				1.26	µs
Internal conversion clock period t_{CCLK}				18.5	t_{CCLK}
				68.0	ns
Throughput rate f_{DATA}	Parallel interface, internal clock and reference			630	kSPS
	Serial interface, internal clock and reference			450	kSPS
AC ACCURACY					
Signal-to-noise ratio SNR	At f_{IN} = 10kHz, T_A = –40°C to +85°C	90	91.5		dB
	At f_{IN} = 10kHz, T_A = –40°C to +125°C	89	91.5		dB
Signal-to-noise ratio + distortion SINAD	At f_{IN} = 10kHz, T_A = –40°C to +85°C	87	89.5		dB
	At f_{IN} = 10kHz, T_A = –40°C to +125°C	86.5	89.5		dB
Total harmonic distortion[2] THD	At f_{IN} = 10kHz, T_A = –40°C to +85°C		–94	–90	dB
	At f_{IN} = 10kHz, T_A = –40°C to +125°C		–94	–89.5	
Spurious-free dynamic range SFDR	At f_{IN} = 10kHz, T_A = –40°C to +85°C	90	95		dB
	At f_{IN} = 10kHz, T_A = –40°C to +125°C	89.5	95		dB
Channel-to-channel isolation	At f_{IN} = 10kHz		100		dB
–3dB small-signal bandwidth	In 4 × V_{REF} mode		48		MHz
	In 2 × V_{REF} mode		24		MHz

(1) All values are at T_A = +25°C.
(2) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: ADS8557

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5.5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = 670kSPS in parallel mode or 470kSPS in serial mode, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8557			UNIT
			MIN	TYP(1)	MAX	
DC ACCURACY						
Resolution				14		Bits
No missing codes			14			Bits
Integral linearity error	INL		–1	±0.4	1	LSB
Differential linearity error	DNL		–1	±0.25	1	LSB
Offset error			–4	±0.8	4	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.75	±0.25	0.75	%FSR
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
Power-supply rejection ratio	PSRR	At output code FFFFh, related to AVDD		60		dB
SAMPLING DYNAMICS						
Acquisition time	t_{ACQ}		280			ns
Conversion time per ADC	t_{CONV}				1.19	µs
Internal conversion clock period	t_{CCLK}				18.5	t_{CCLK}
					64.1	ns
Throughput rate	f_{DATA}	Parallel interface, internal clock and reference			670	kSPS
		Serial interface, internal clock and reference			470	kSPS
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10kHz	84	85		dB
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10kHz	83	84		dB
Total harmonic distortion(2)	THD	At f_{IN} = 10kHz		–91	–86	dB
Spurious-free dynamic range	SFDR	At f_{IN} = 10kHz	86	92		dB
Channel-to-channel isolation		At f_{IN} = 10kHz		100		dB
–3dB small-signal bandwidth		In 4 × V_{REF} mode		48		MHz
		In 2 × V_{REF} mode		24		MHz

(1) All values are at T_A = +25°C.
(2) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: ADS8558

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = 730kSPS in parallel mode or 500kSPS in serial mode, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8558			UNIT
			MIN	TYP(1)	MAX	
DC ACCURACY						
Resolution				12		Bits
No missing codes			12			Bits
Integral linearity error	INL		–0.75	±0.2	0.75	LSB
Differential linearity error	DNL		–0.5	±0.2	0.5	LSB
Offset error			–4	±0.8	4	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.75	±0.25	0.75	%FSR
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
Power-supply rejection ratio	PSRR	At output code FFFFh, related to AVDD		60		dB
SAMPLING DYNAMICS						
Acquisition time	t_{ACQ}		280			ns
Conversion time per ADC	t_{CONV}				1.09	µs
Internal conversion clock period	t_{CCLK}				18.5	t_{CCLK}
					58.8	ns
Throughput rate	f_{DATA}	Parallel interface, internal clock and reference			730	kSPS
		Serial interface, internal clock and reference			500	kSPS
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10kHz	73	73.9		dB
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10kHz	73	73.8		dB
Total harmonic distortion(2)	THD	At f_{IN} = 10kHz		–89	–84	dB
Spurious-free dynamic range	SFDR	At f_{IN} = 10kHz	84	92		dB
Channel-to-channel isolation		At f_{IN} = 10kHz		100		dB
–3dB small-signal bandwidth		In 4 × V_{REF} mode		48		MHz
		In 2 × V_{REF} mode		24		MHz

(1) All values are at T_A = +25°C.
(2) Calculated on the first nine harmonics of the input frequency.

ELECTRICAL CHARACTERISTICS: GENERAL

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5.5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8556, ADS8557, ADS8558 MIN	TYP(1)	MAX	UNIT
ANALOG INPUT					
Bipolar full-scale range CHXX	RANGE pin/RANGE bit = 0	–4 × V_{REF}		+4 × V_{REF}	V
	RANGE pin/RANGE bit = 1	–2 × V_{REF}		+2 × V_{REF}	V
Input capacitance	Input range = ±4 × V_{REF}		10		pF
	Input range = ±2 × V_{REF}		20		pF
Input leakage current	No ongoing conversion			±1	µA
Aperture delay			5		ns
Aperture delay matching	Common CONVST for all channels		250		ps
Aperture jitter			50		ps
EXTERNAL CLOCK INPUT (XCLK)					
External clock frequency f_{XCLK}	An external reference must be used for $f_{XCLK} > f_{CCLK}$	1	18	20	MHz
External clock duty cycle		45		55	%
REFERENCE VOLTAGE OUTPUT (REF_{OUT})					
Reference voltage V_{REF}	2.5V operation, REFDAC = 0x3FF	2.485	2.5	2.515	V
	2.5V operation, REFDAC = 0x3FF at +25°C	2.496	2.5	2.504	V
	3.0V operation, REFDAC = 0x3FF	2.985	3.0	3.015	V
	3.0V operation, REFDAC = 0x3FF at +25°C	2.995	3.0	3.005	V
Reference voltage drift dV_{REF}/dT			±10		ppm/°C
Power-supply rejection ratio PSRR			73		dB
Output current I_{REFOUT}	DC current	–2		2	mA
Short-circuit current(2) I_{REFSC}			50		mA
Turn-on settling time t_{REFON}			10		ms
External load capacitance	At CREF_x pins	4.7	10		µF
	At REFIO pins	100	470		nF
Tuning range REFDAC	Internal reference output voltage range	0.2 × V_{REF}		V_{REF}	V
REFDAC resolution		10			Bits
REFDAC differential nonlinearity DNL_{DAC}		–1	±0.1	1	LSB
REFDAC integral nonlinearity INL_{DAC}		–2	±0.1	2	LSB
REFDAC offset error V_{OSDAC}	V_{REF} = 0.5V (DAC = 0x0CC)	–4	±0.65	4	LSB
REFERENCE VOLTAGE INPUT (REF_{IN})					
Reference input voltage V_{REFIN}		0.5	2.5	3.025	V
Input resistance			100		MΩ
Input capacitance			5		pF
Reference input current				1	µA
SERIAL CLOCK INPUT (SCLK)					
Serial clock input frequency f_{SCLK}		0.1		36	MHz
Serial clock period t_{SCLK}		0.0278		10	µs
Serial clock duty cycle		40		60	%
DIGITAL INPUTS(3)					
Logic family		CMOS with Schmitt-Trigger			
High-level input voltage		0.7 × BVDD		BVDD + 0.3	V
Low-level input voltage		BGND – 0.3		0.3 × BVDD	V
Input current	V_I = BVDD to BGND	–50		+50	nA
Input capacitance			5		pF

(1) All values are at T_A = +25°C.
(2) Reference output current is not limited internally.
(3) Specified by design.

ELECTRICAL CHARACTERISTICS: GENERAL (continued)

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5.5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

PARAMETER		CONDITIONS	ADS8556, ADS8557, ADS8558 MIN	TYP(1)	MAX	UNIT
DIGITAL OUTPUTS(4)						
Logic family			CMOS			
High-level output voltage		I_{OH} = 100µA	BVDD – 0.6		BVDD	V
Low-level output voltage		I_{OH} = –100µA	BGND		BGND + 0.4	V
High-impedance-state output current			–50		50	nA
Output capacitance				5		pF
Load capacitance					30	pF
POWER-SUPPLY REQUIREMENTS						
Analog supply voltage	AVDD		4.5	5.0	5.5	V
Buffer I/O supply voltage	BVDD		2.7	3.0	5.5	V
Input positive supply voltage	HVDD		5.0	10.0	16.5	V
Input negative supply voltage	HVSS		–16.5	–10.0	–5.0	V
Analog supply current(5)	IAVDD	f_{DATA} = maximum		30.0	36.0	mA
		ADS8556, f_{DATA} = 250kSPS (auto-NAP mode)		14.0	16.5	mA
		ADS8557, f_{DATA} = 250kSPS (auto-NAP mode)		14.0	17.0	mA
		ADS8558, f_{DATA} = 250kSPS (auto-NAP mode)		14.0	18.0	mA
		Auto-NAP mode, no ongoing conversion, internal conversion clock		4.0	6.0	mA
		Power-down mode		0.1	50.0	µA
Buffer I/O supply current(6)	IBVDD	f_{DATA} = maximum		0.9	2.0	mA
		f_{DATA} = 250kSPS (auto-NAP mode)		0.5	1.5	mA
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.1	10.0	µA
		Power-down mode		0.1	10.0	µA
Input positive supply current(7)	IHVDD	ADS8556, f_{DATA} = maximum		3.0	3.5	mA
		ADS8557, f_{DATA} = maximum		3.1	3.6	mA
		ADS8558, f_{DATA} = maximum		3.3	4.0	mA
		f_{DATA} = 250kSPS (auto-NAP mode)		1.6	2.0	mA
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.2	0.3	µA
		Power-down mode		0.1	10.0	µA
Input negative supply current(8)	IHVSS	ADS8556, f_{DATA} = maximum		3.6	4.0	mA
		ADS8557, f_{DATA} = maximum		3.6	4.2	mA
		ADS8558, f_{DATA} = maximum		4.0	4.8	mA
		f_{DATA} = 250kSPS (auto-NAP mode)		1.8	2.2	mA
		Auto-NAP mode, no ongoing conversion, internal conversion clock		0.2	0.25	µA
		Power-down mode		0.1	10.0	µA

(4) Specified by design.
(5) At AVDD = 5V.
(6) At BVDD = 3V, parallel mode, load capacitance = 6pF/pin.
(7) At HVDD = 15V.
(8) At HVSS = –15V.

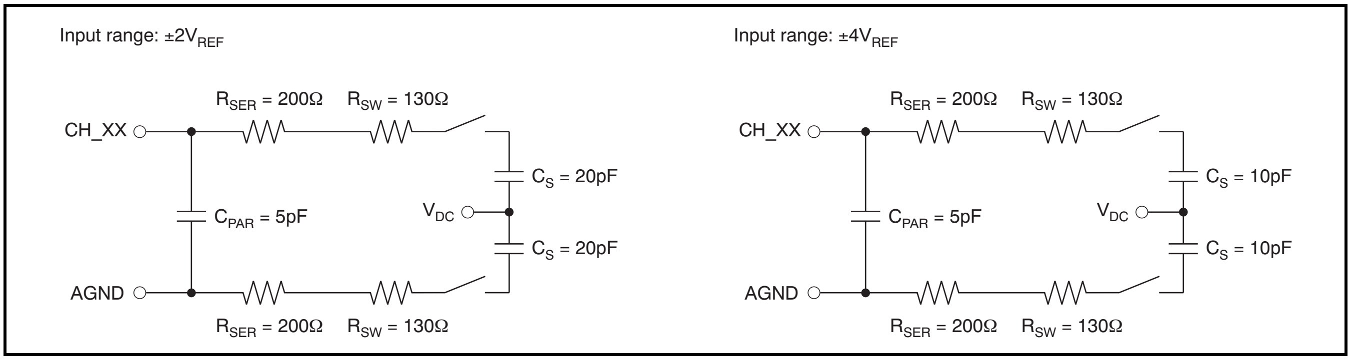
ELECTRICAL CHARACTERISTICS: GENERAL (continued)

Over recommended operating free-air temperature range of –40°C to +125°C, AVDD = 4.5V to 5.5V, BVDD = 2.7V to 5.5V, HVDD = 10V to 15V, HVSS = –15V to –10V, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8556, ADS8557, ADS8558 MIN	TYP(1)	MAX	UNIT
POWER-SUPPLY REQUIREMENTS (continued)					
Power dissipation(9)	ADS8556, f_{DATA} = maximum		251.7	298.5	mW
	ADS8557, f_{DATA} = maximum		253.2	303.0	mW
	ADS8558, f_{DATA} = maximum		262.2	318.0	mW
	ADS8556, f_{DATA} = 250kSPS (auto-NAP mode)		122.5	150.0	mW
	ADS8557, f_{DATA} = 250kSPS (auto-NAP mode)		122.5	152.5	mW
	ADS8558, f_{DATA} = 250kSPS (auto-NAP mode)		122.5	157.5	mW
	Auto-NAP mode, no ongoing conversion, internal conversion clock		26.0	38.3	mW
	Power-down mode		3.8	580.0	µW

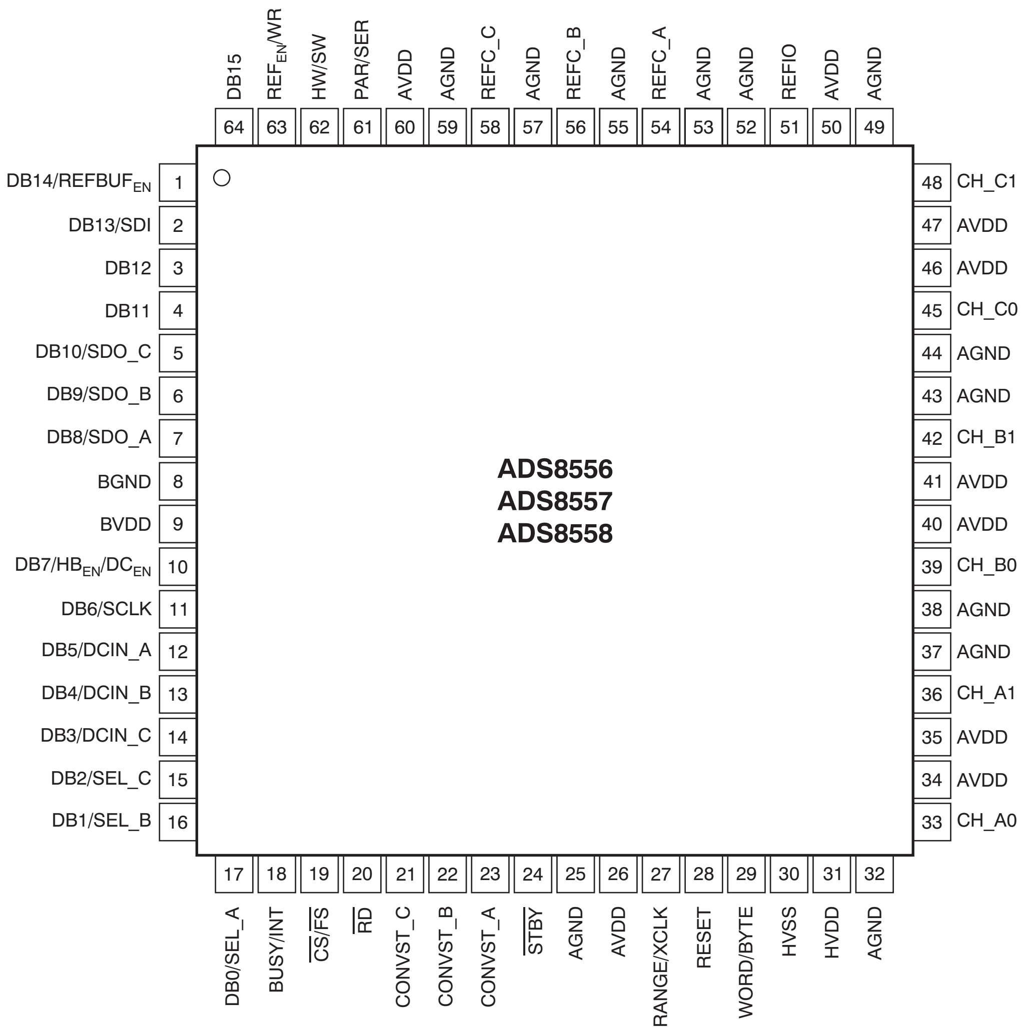
(9) At AVDD = 5V, BVDD = 3V, HVDD = 15V, and HVSS = –15V.

EQUIVALENT INPUT CIRCUITS



PIN CONFIGURATION

**PM PACKAGE
LQFP-64
(TOP VIEW)**



TERMINAL FUNCTIONS

NAME	PIN #	TYPE[(1)]	DESCRIPTION	
			PARALLEL INTERFACE (PAR/SER = 0)	SERIAL INTERFACE (PAR/SER = 1)
DB14/REFBUF$_{EN}$	1	DIO/DI	Data bit 14 input/output Output is '0' for the ADS8557/8	Hardware mode (HW/SW = 0): Reference buffers enable input. When low, all reference buffers are enabled (mandatory if internal reference is used). When high, all reference buffers are disabled. Software mode (HW/SW = 1):Connect to BGND or BVDD. The reference buffers are controlled by bit C24 (REFBUF) in control register (CR).
DB13/SDI	2	DIO/DI	Data bit 13 input/output Output is MSB for the ADS8557 and '0' for the ADS8558	Hardware mode (HW/SW = 0): Connect to BGND Software mode (HW/SW = 1): Serial data input
DB12	3	DIO	Data bit 12 input/output Output is '0' for the ADS8558	Connect to BGND
DB11	4	DIO	Data bit 11 input/output Output is MSB for the ADS8558	Connect to BGND
DB10/SDO_C	5	DIO/DO	Data bit 10 input/output	When SEL_C = 1, data output for channel C When SEL_C = 0, this pin should be tied to BGND
DB9/SDO_B	6	DIO/DO	Data bit 9 input/output	When SEL_B = 1, data output for channel B When SEL_B = 0, this pin should be tied to BGND When SEL_C = 0, data from channel C1 are also available on this output
DB8/SDO_A	7	DIO/DO	Data bit 8 input/output	Data output for channel A When SEL_C = 0, data from channel C0 are also available on this output When SEL_C = 0 and SEL_B = 0, SDO_A acts as the single data output for all channels
BGND	8	P	Buffer IO ground, connect to digital ground plane	
BVDD	9	P	Buffer IO supply, connect to digital supply (2.7V to 5.5V). Decouple with a 1µF ceramic capacitor or a combination of 100nF and 10µF ceramic capacitors to BGND.	
DB7/HB$_{EN}$/DC$_{EN}$	10	DIO/DI/DI	Word mode (WORD/BYTE = 0): Data bit 7 input/output Byte mode (WORD/BYTE = 1): High byte enable input. When high, the high byte is output first on DB[15:8]. When low, the low byte is output first on DB[15:8].	Daisy-chain enable input. When high, DB[5:3] serve as daisy-chain inputs DCIN[A:C]. If daisy-chain mode is not used, connect to BGND.
DB6/SCLK	11	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 6 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	Serial interface clock input (36MHz max)
DB5/DCIN_A	12	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 5 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	When DC$_{EN}$ = 1, daisy-chain data input for channel A When DC$_{EN}$ = 0, connect to BGND
DB4/DCIN_B	13	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 4 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	When SEL_B = 1 and DC$_{EN}$ = 1, daisy-chain data input for channel B When DC$_{EN}$ = 0, connect to BGND
DB3/DCIN_C	14	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 3 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	When SEL_C = 1 and DC$_{EN}$ = 1, daisy-chain data input for channel C When DC$_{EN}$ = 0, connect to BGND
DB2/SEL_C	15	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 2 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	Select SDO_C input. When high, SDO_C is active. When low, SDO_C is disabled.
DB1/SEL_B	16	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 1 input/output Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	Select SDO_B input. When high, SDO_B is active. When low, SDO_B is disabled.

(1) AI = analog input; AIO = analog input/output; DI = digital input; DO = digital output; DIO = digital input/output; and P = power supply.

TERMINAL FUNCTIONS (continued)

NAME	PIN #	TYPE(1)	DESCRIPTION: PARALLEL INTERFACE (PAR/SER = 0)	DESCRIPTION: SERIAL INTERFACE (PAR/SER = 1)
DB0/SEL_A	17	DIO/DI	Word mode (WORD/BYTE = 0): Data bit 0 (LSB) input/output	Select SDO_A input. When high, SDO_A is active. When low, SDO_A is disabled. Should always be high.
			Byte mode (WORD/BYTE = 1): Connect to BGND or BVDD	
BUSY/INT	18	DO	When CR bit C21 = 0 (BUSY/INT), converter busy status output. Transitions high when a conversion has been started and remains high during the entire process. Transitions low when the conversion data of all six channels are latched to the output register and remains low thereafter. In sequential mode (SEQ = 1 in the CR), the BUSY output transitions high when a conversion has been started and goes low for a single conversion clock cycle (t_{CCLK}) whenever a channel pair conversion is completed. When bit C21 = 1 (BUSY/INT in CR), interrupt output. This bit transitions high after a conversion has been completed and remains high until the conversion result has been read. The polarity of BUSY/INT output can be changed using bit C20 (BUSY L/H) in the control register.	
$\overline{\text{CS}}/\overline{\text{FS}}$	19	DI/DI	Chip select input. When low, the parallel interface is enabled. When high, the interface is disabled.	Frame synchronization. The falling edge of $\overline{\text{FS}}$ controls the frame transfer.
$\overline{\text{RD}}$	20	DI	Read data input. When low, the parallel data output is enabled. When high, the data output is disabled.	Connect to BGND
CONVST_C	21	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair C. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_C[1:0]. CONVST_C should remain high during the entire conversion cycle, otherwise both ADCs of channel C are put in partial power-down mode (see the Reset and Power-down Modes sections).	
			Software mode (HW/SW = 1): Conversion start of channel pair C in sequential mode (CR bit C23 = 1) only; connect to BGND or BVDD otherwise	
CONVST_B	22	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair B. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_B[1:0]. CONVST_B should remain high during the entire conversion cycle; otherwise, both ADCs of channel B are put into partial power-down mode (see the Reset and Power-down Modes sections).	
			Software mode (HW/SW = 1): Conversion start of channel pair B in sequential mode (CR bit C23 = 1) only; connect to BGND or BVDD otherwise	
CONVST_A	23	DI	Hardware mode (HW/SW = 0): Conversion start of channel pair A. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_A[1:0]. CONVST_A should remain high during the entire conversion cycle; otherwise, both ADCs of channel A are put into partial power-down mode (see the Reset and Power-down Modes sections).	
			Software mode (HW/SW = 1): Conversion start of all selected channels except in sequential mode (CR bit C23 = 1): Conversion start of channel pair A only	
$\overline{\text{STBY}}$	24	DI	Standby mode input. When low, the entire device is powered-down (including the internal clock and reference). When high, the device operates in normal mode.	
AGND	25, 32, 37, 38, 43, 44, 49, 52, 53, 55, 57, 59	P	Analog ground, connect to analog ground plane Pin 25 may have a dedicated ground if the difference between its potential and AGND is always kept within ±300mV.	
AVDD	26, 34, 35, 40, 41, 46, 47, 50, 60	P	Analog power supply (4.5V to 5.5V). Decouple each pin with a 100nF ceramic capacitor to AGND. Use an additional 10µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor. Pin 26 may have a dedicated power supply if the difference between its potential and AVDD is always kept within ±300mV.	
RANGE/XCLK	27	DI/DIO	Hardware mode (HW/SW = 0): Input voltage range select input. When low, the analog input range is $\pm 4V_{REF}$. When high, the analog input range is $\pm 2V_{REF}$.	
			Software mode (HW/SW = 1): External conversion clock input, if CR bit C11 (CLKSEL) is set high or internal conversion clock output, if CR bit C10 (CLKOUT_EN) is set high. If not used, connect to BVDD or BGND.	
RESET	28	DI	Reset input, active high. Aborts any ongoing conversions. Resets the internal control register to 0x000003FF. The RESET pulse should be at least 50ns long.	
WORD/BYTE	29	DI	Output mode selection input. When low, data are transferred in word mode using DB[15:0]. When high, data are transferred in byte mode using DB[15:8] with the byte order controlled by HB_{EN} pin while two accesses are required for a complete 16-bit transfer.	Connect to BGND
HVSS	30	P	Negative supply voltage for the analog inputs (–16.5V to –5V). Decouple with a 100nF ceramic capacitor to AGND placed next to the device and a 10µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor.	

TERMINAL FUNCTIONS (continued)

NAME	PIN #	TYPE(1)	DESCRIPTION: PARALLEL INTERFACE (PAR/SER = 0)	DESCRIPTION: SERIAL INTERFACE (PAR/SER = 1)
HVDD	31	P	Positive supply voltage for the analog inputs (5V to 16.5V). Decouple with a 100nF ceramic capacitor to AGND placed next to the device and a 10µF capacitor to AGND close to the device but without compromising the placement of the smaller capacitor.	
CH_A0	33	AI	Analog input of channel A0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C26 (RANGE_A) in software mode.	
CH_A1	36	AI	Analog input of channel A1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C26 (RANGE_A) in software mode.	
CH_B0	39	AI	Analog input of channel B0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C27 (RANGE_B) in software mode.	
CH_B1	42	AI	Analog input of channel B1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C27 (RANGE_B) in software mode.	
CH_C0	45	AI	Analog input of channel C0. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C28 (RANGE_C) in software mode.	
CH_C1	48	AI	Analog input of channel C1. The input voltage range is controlled by RANGE pin in hardware mode or CR bit C28 (RANGE_C) in software mode.	
REFIO	51	AIO	Reference voltage input/output (0.5V to 3.025V). The internal reference is enabled via REF_{EN}/WR pin in hardware mode or CR bit C25 (REF_{EN}) in software mode. The output value is controlled by the internal DAC (CR bits C[9:0]). Connect a 470nF ceramic decoupling capacitor between this pin and pin 52.	
REFC_A	54	AI	Decoupling capacitor for reference of channels A. Connect a 10µF ceramic decoupling capacitor between this pin and pin 53.	
REFC_B	56	AI	Decoupling capacitor for reference of channels B. Connect a 10µF ceramic decoupling capacitor between this pin and pin 55.	
REFC_C	58	AI	Decoupling capacitor for reference of channels C. Connect a 10µF ceramic decoupling capacitor between this pin and pin 57.	
PAR/SER	61	DI	Interface mode selection input. When low, the parallel interface is selected. When high, the serial interface is enabled.	
HW/SW	62	DI	Mode selection input. When low, the hardware mode is selected and part works according to the settings of external pins. When high, the software mode is selected in which the device is configured by writing into the control register.	
REF_{EN}/WR	63	DI	Hardware mode (HW/SW = 0): Internal reference enable input. When high, the internal reference is enabled (the reference buffers are to be enabled). When low, the internal reference is disabled and an external reference is applied at REFIO.	Hardware mode (HW/SW = 0): Internal reference enable input. When high, the internal reference is enabled (the reference buffers are to be enabled). When low, the internal reference is disabled and an external reference should be applied at REFIO.
			Software mode (HW/SW = 1): Write input. The parallel data input is enabled, when $\overline{CS}$ and WR are low. The internal reference is enabled by the CR bit C25 (REF_{EN}).	Software mode (HW/SW = 1): Connect to BGND or BVDD. The internal reference is enabled by CR bit C25 (REF_{EN}).
DB15	64	DIO	Data bit 15 (MSB) input/output Output is '0' for the ADS8557/8	Connect to BGND

TIMING CHARACTERISTICS

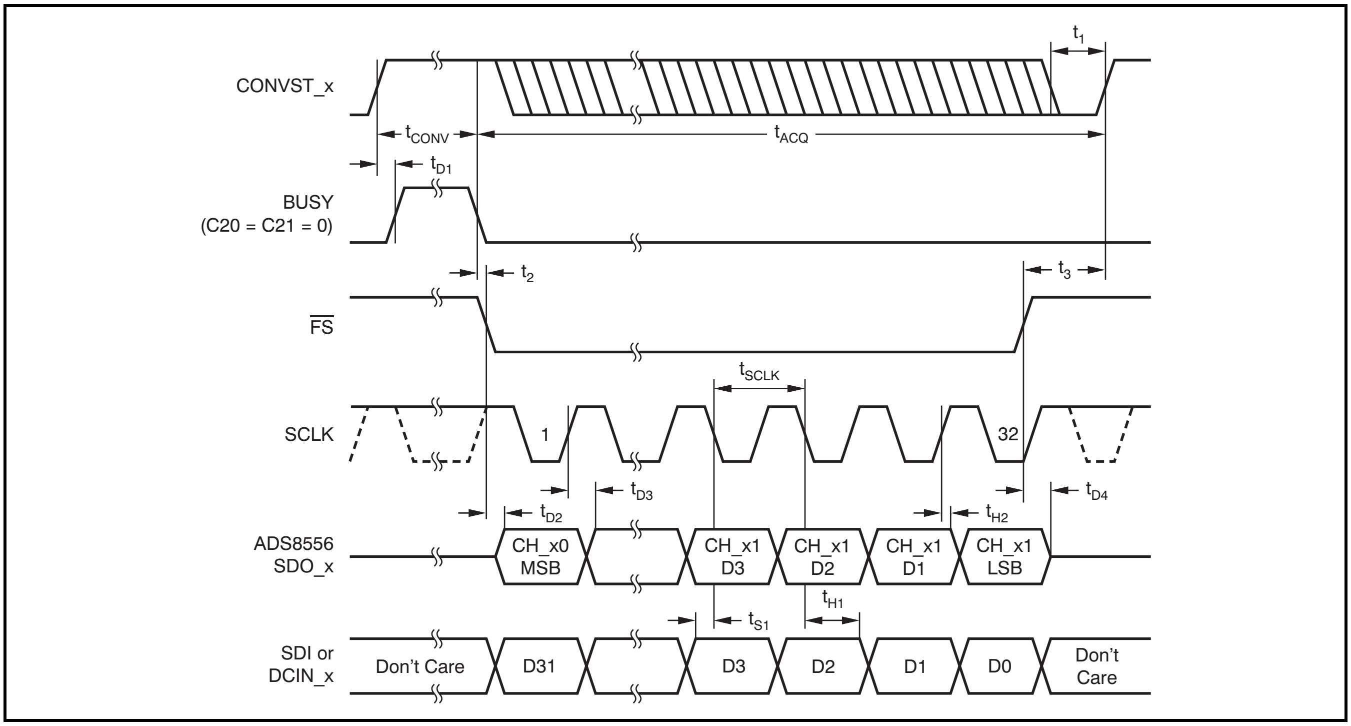


Figure 1. Serial Operation Timing Diagram (All Three SDOs Active)

Serial Interface Timing Requirements(1)

Over recommended operating free-air temperature range at –40°C to +125°C, AVDD = 5V, and BVDD = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		TEST CONDITION	ADS8556, ADS8557, ADS8558			UNIT
			MIN	TYP	MAX	
t_{ACQ}	Acquisition time		280			ns
t_{CONV}	Conversion time	ADS8556			1.26	ns
		ADS8557			1.19	ns
		ADS8558			1.09	ns
t_1	CONVST_x low time		20			ns
t_2	BUSY low to $\overline{FS}$ low time		0			ns
t_3	Bus access finished to next conversion start time	ADS8556	40			ns
		ADS8557	20			ns
		ADS8558	0			ns
t_{D1}	CONVST_x high to BUSY high delay		5		20	ns
t_{D2}	$\overline{FS}$ low to SDO_x active delay		5		12	ns
t_{D3}	SCLK rising edge to new data valid delay				15	ns
t_{D4}	$\overline{FS}$ high to SDO_x 3-state delay				10	ns
t_{H1}	Input data to SCLK falling edge hold time		5			ns
t_{H2}	Output data to SCLK rising edge hold time		5			ns
t_{S1}	Input data to SCLK falling edge setup time		3			ns
t_{SCLK}	Serial clock period		0.0278		10	µs

(1) All input signals are specified with $t_R = t_F = 1.5ns$ (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

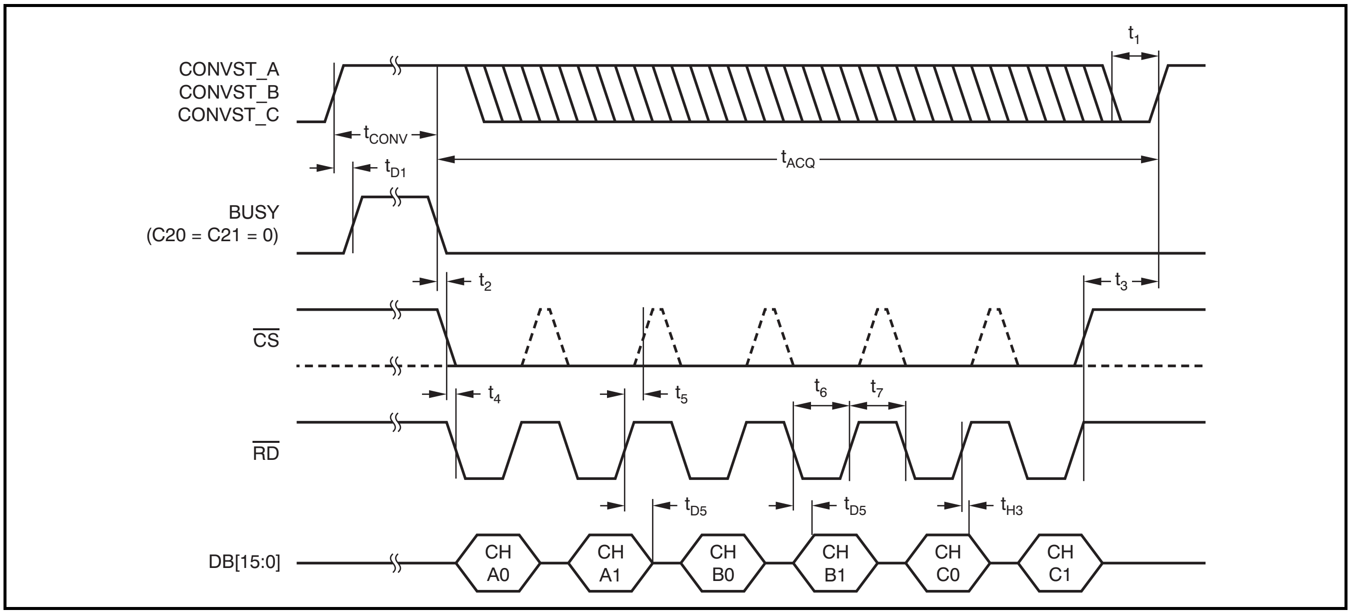


Figure 2. Parallel Read Access Timing Diagram

Parallel Interface Timing Requirements (Read Access)(1)

Over recommended operating free-air temperature range at –40°C to +125°C, AVDD = 5V, and BVDD = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		TEST CONDITION	ADS8556, ADS8557, ADS8558 MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time		280			ns
t_{CONV}	Conversion time	ADS8556			1.26	ns
		ADS8557			1.19	ns
		ADS8558			1.09	ns
t_1	CONVST_x low time		20			ns
t_2	BUSY low to $\overline{CS}$ low time		0			ns
t_3	Bus access finished to next conversion start time(2)	ADS8556	40			ns
		ADS8557	20			ns
		ADS8558	0			ns
t_4	$\overline{CS}$ low to $\overline{RD}$ low time		0			ns
t_5	$\overline{RD}$ high to $\overline{CS}$ high time		0			ns
t_6	$\overline{RD}$ pulse width		30			ns
t_7	Minimum time between two read accesses		10			ns
t_{D1}	CONVST_x high to BUSY high delay		5		20	ns
t_{D5}	$\overline{RD}$ falling edge to output data valid delay				20	ns
t_{H3}	Output data to $\overline{RD}$ rising edge hold time		5			ns

(1) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) Refer to $\overline{CS}$ signal or $\overline{RD}$, whichever occurs first.

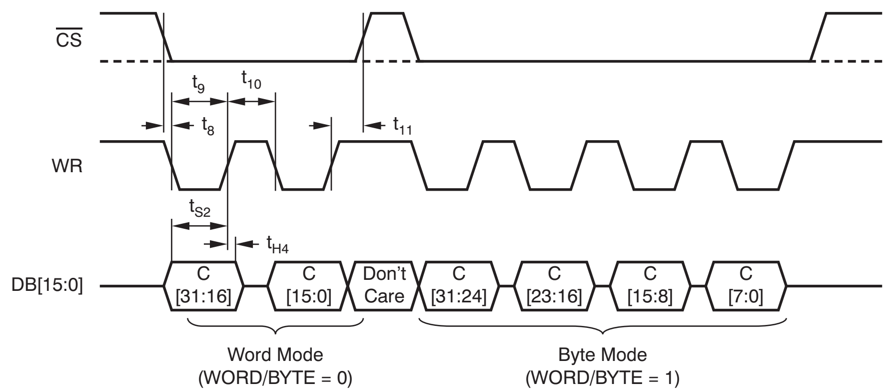


Figure 3. Parallel Write Access Timing Diagram

Parallel Interface Timing Requirements (Write Access)(1)

Over recommended operating free-air temperature range at –40°C to +125°C, AVDD = 5V, and BVDD = 2.7V to 5.5V, unless otherwise noted.

PARAMETER		ADS8556, ADS8557, ADS8558			UNIT
		MIN	TYP	MAX	
t_8	$\overline{CS}$ low to WR low time	0			ns
t_9	WR low pulse width	15			ns
t_{10}	WR high pulse width	10			ns
t_{11}	WR high to $\overline{CS}$ high time	0			ns
t_{S2}	Output data to WR rising edge setup time	5			ns
t_{H4}	Data output to WR rising edge hold time	5			ns

(1) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of BVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

TYPICAL CHARACTERISTICS

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

INL vs CODE (ADS8556 ±10V_{IN} Range)

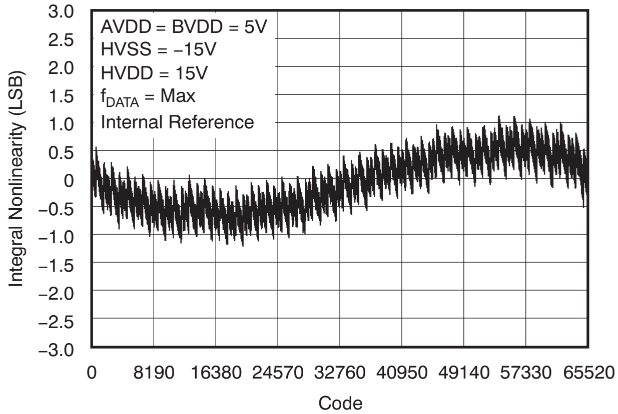


Figure 4.

INL vs CODE (ADS8556 ±5V_{IN} Range)

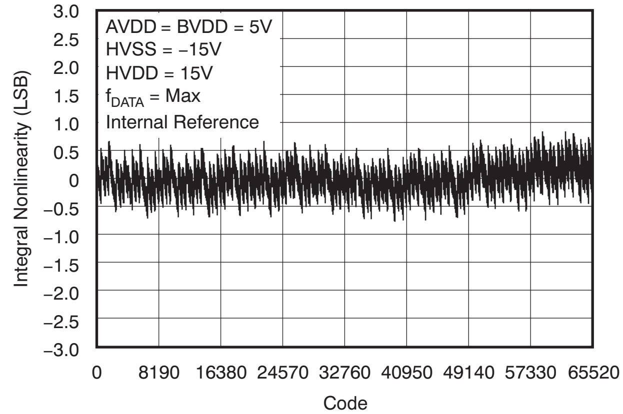


Figure 5.

DNL vs CODE (ADS8556 ±10V_{IN} Range)

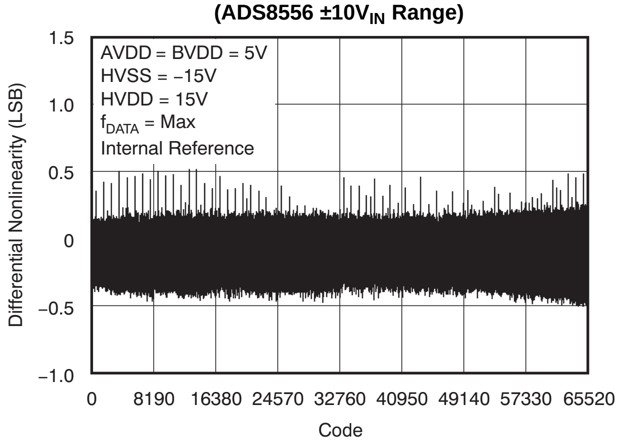


Figure 6.

DNL vs CODE (ADS8556 ±5V_{IN} Range)

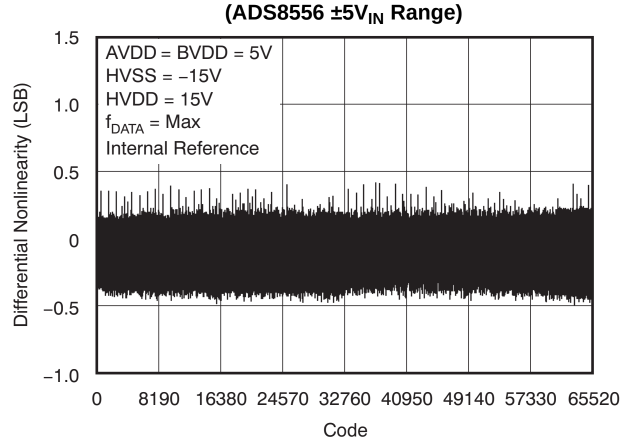


Figure 7.

INL vs CODE (ADS8557 ±10V_{IN} Range)

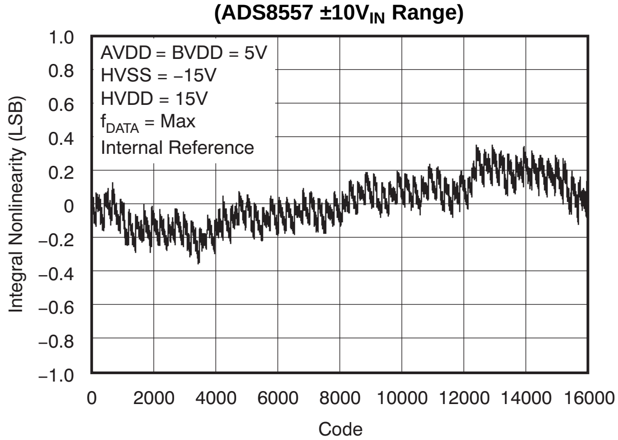


Figure 8.

INL vs CODE (ADS8557 ±5V_{IN} Range)

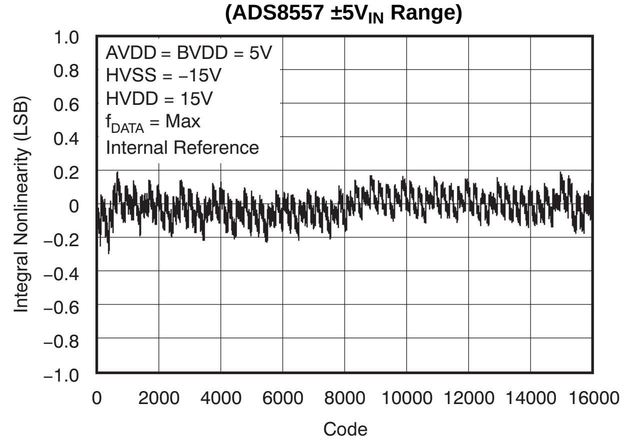


Figure 9.

TYPICAL CHARACTERISTICS (continued)

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

DNL vs CODE (ADS8557 ±10V$_{IN}$ Range)

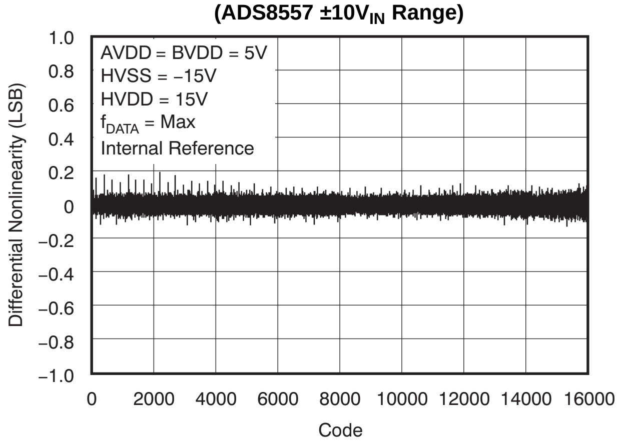


Figure 10.

DNL vs CODE (ADS8557 ±5V$_{IN}$ Range)

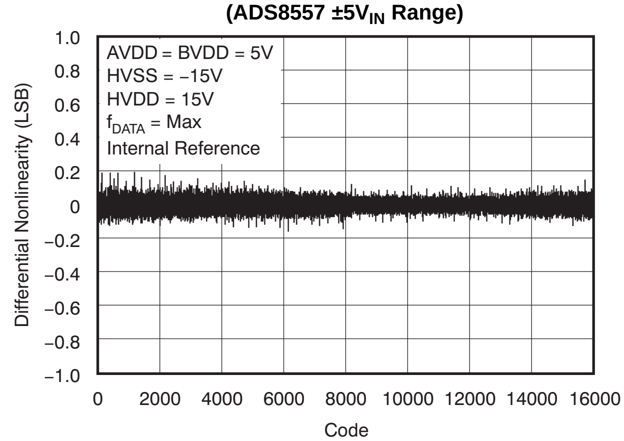


Figure 11.

INL vs CODE (ADS8558)

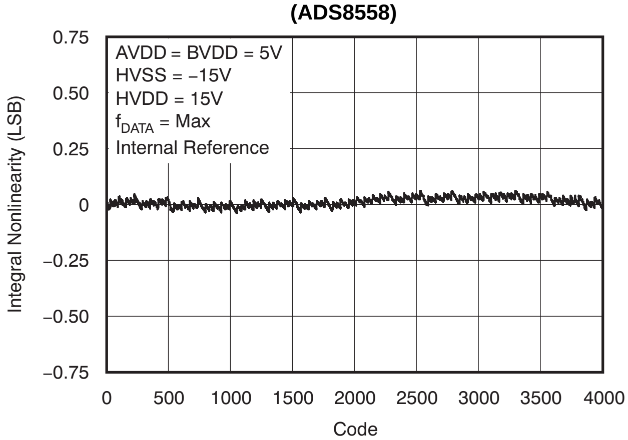


Figure 12.

DNL vs CODE (ADS8558)

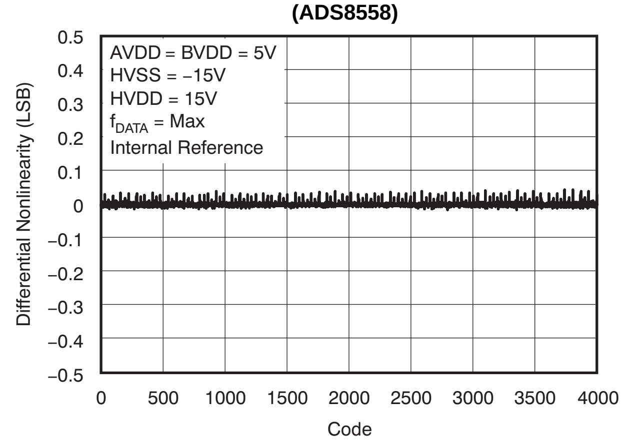


Figure 13.

OFFSET ERROR vs TEMPERATURE

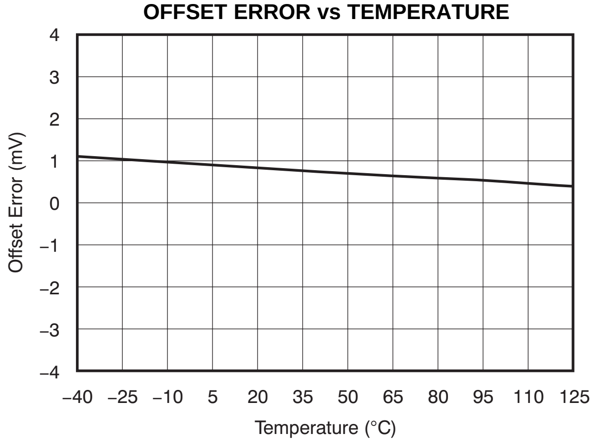


Figure 14.

GAIN ERROR vs TEMPERATURE

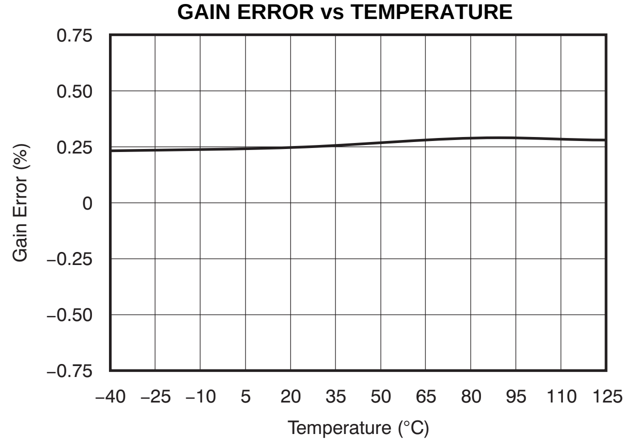


Figure 15.

TYPICAL CHARACTERISTICS (continued)

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

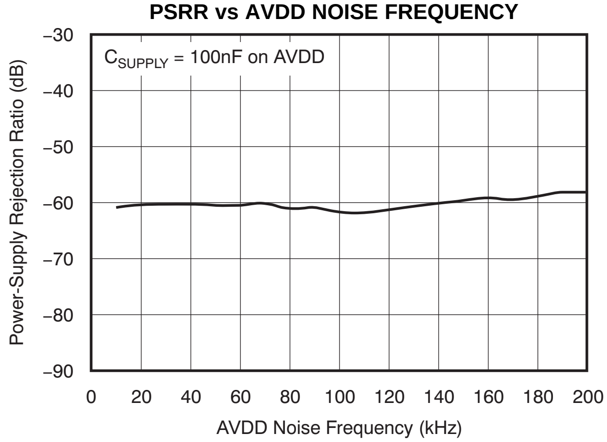


Figure 16.

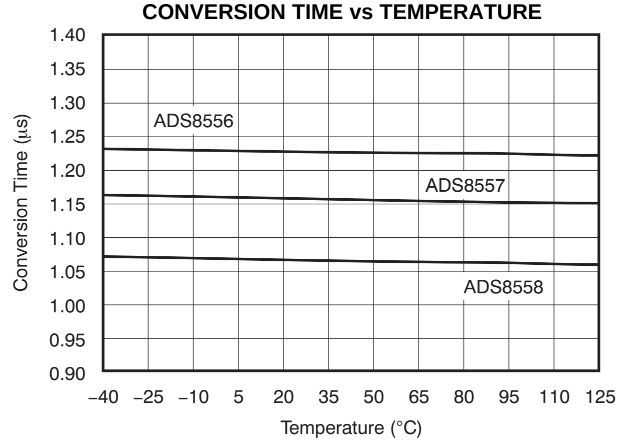


Figure 17.

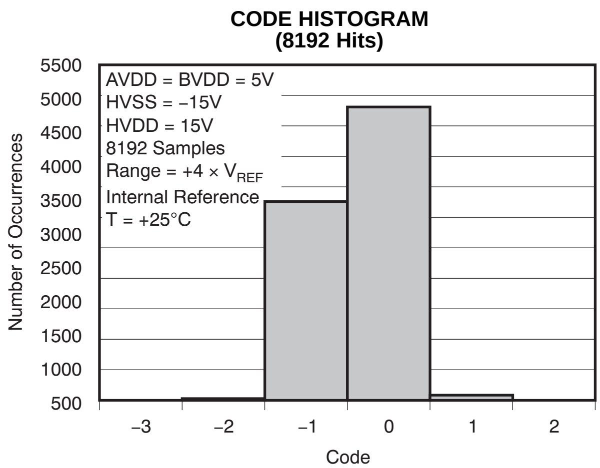


Figure 18.

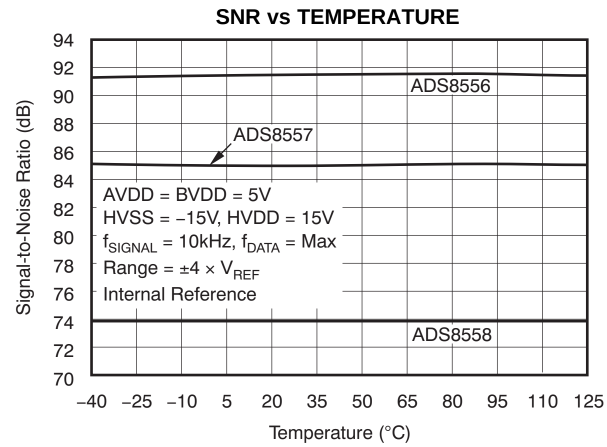


Figure 19.

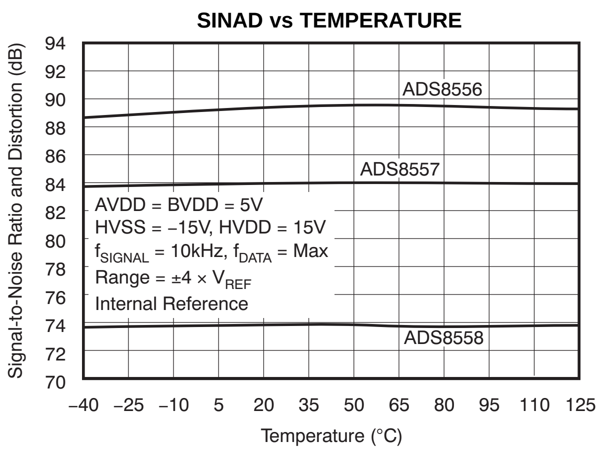


Figure 20.

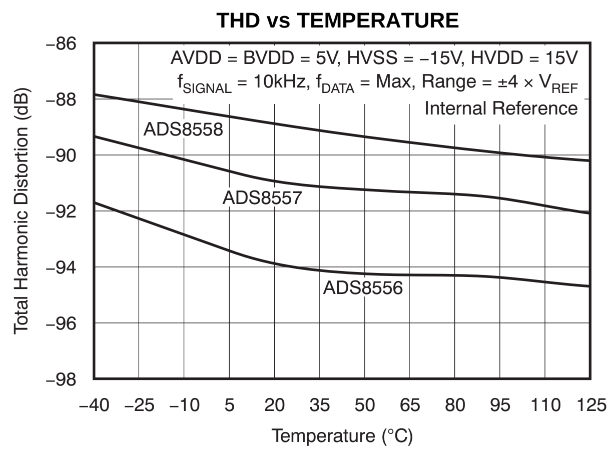


Figure 21.

TYPICAL CHARACTERISTICS (continued)

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

SFDR vs TEMPERATURE

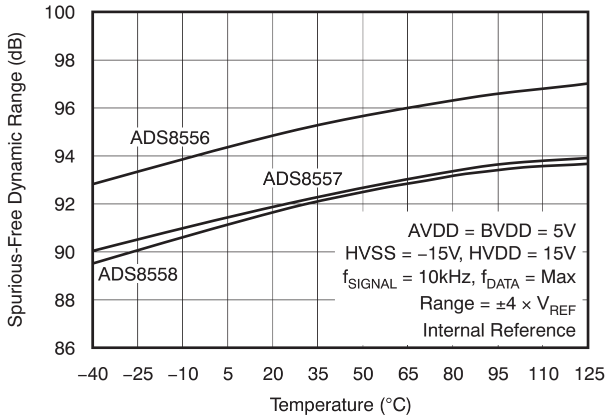


Figure 22.

FREQUENCY SPECTRUM (2048-Point FFT, f_{IN} = 10kHz, ±10V_{IN} Range)

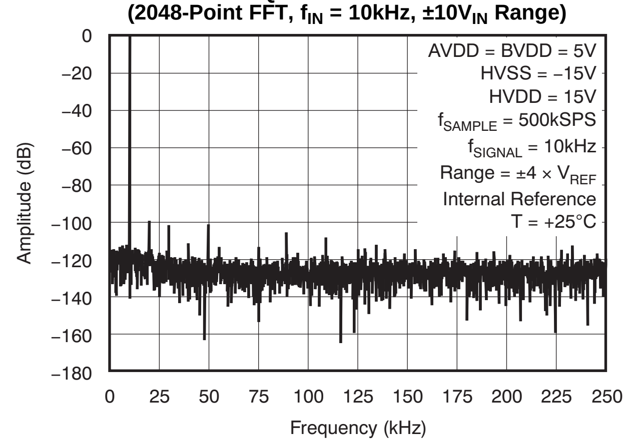


Figure 23.

FREQUENCY SPECTRUM (2048-Point FFT, f_{IN} = 10kHz, ±5V_{IN} Range)

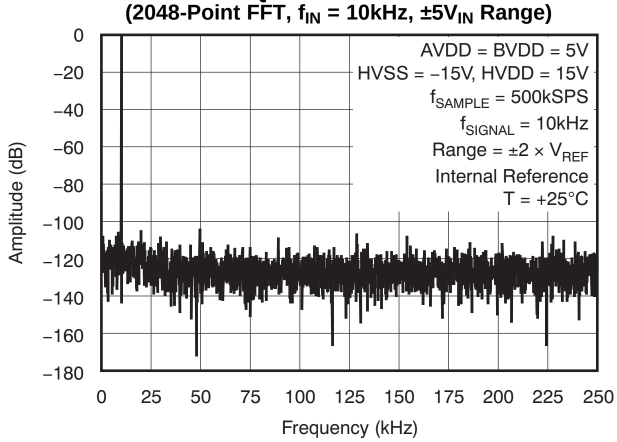


Figure 24.

CHANNEL-TO-CHANNEL ISOLATION vs INPUT NOISE FREQUENCY

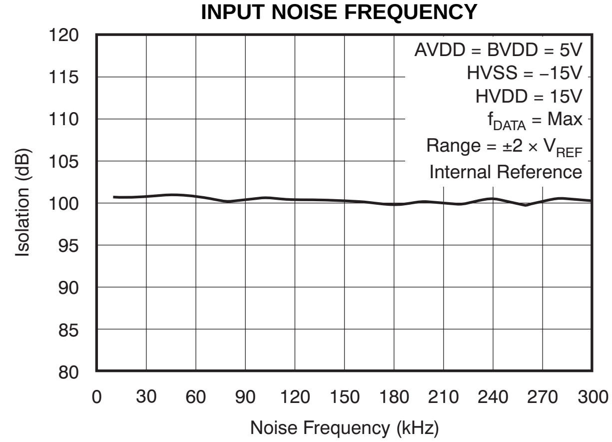


Figure 25.

INTERNAL REFERENCE VOLTAGE vs ANALOG SUPPLY VOLTAGE (2.5V Mode)

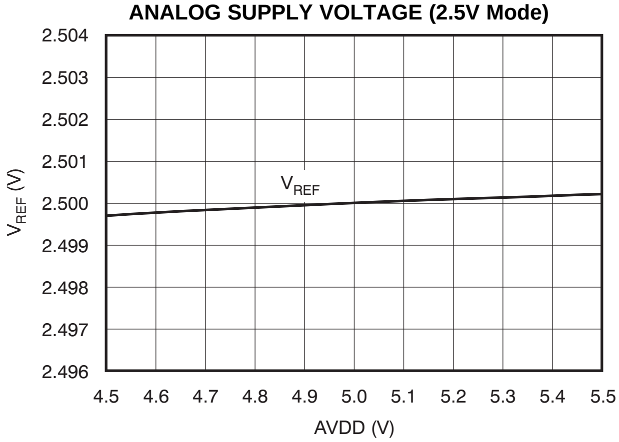


Figure 26.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (2.5V Mode)

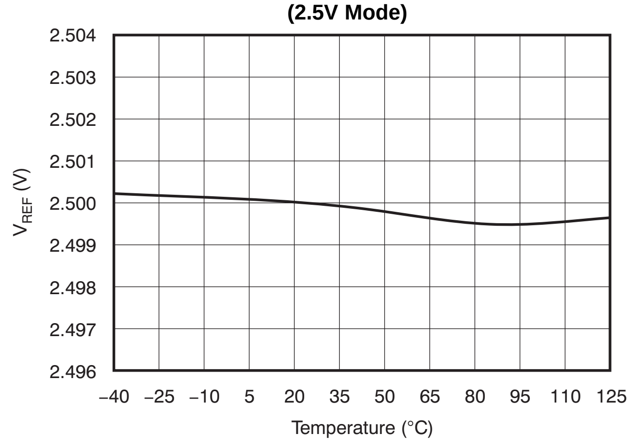


Figure 27.

TYPICAL CHARACTERISTICS (continued)

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (3.0V Mode)

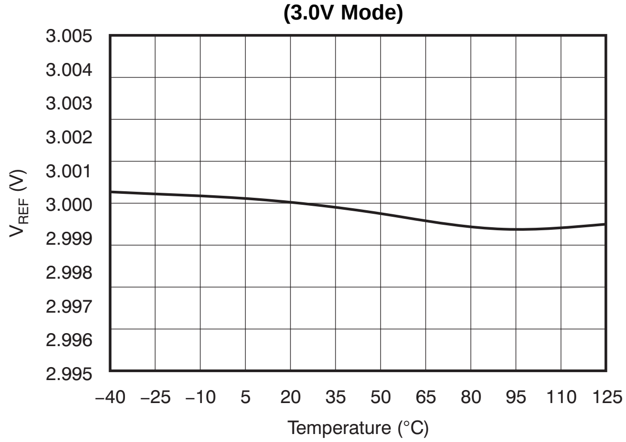


Figure 28.

ANALOG SUPPLY CURRENT vs TEMPERATURE

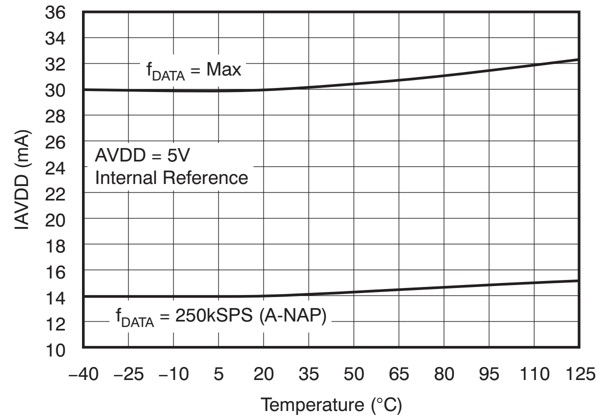


Figure 29.

ADS8556
ANALOG SUPPLY CURRENT vs DATA RATE

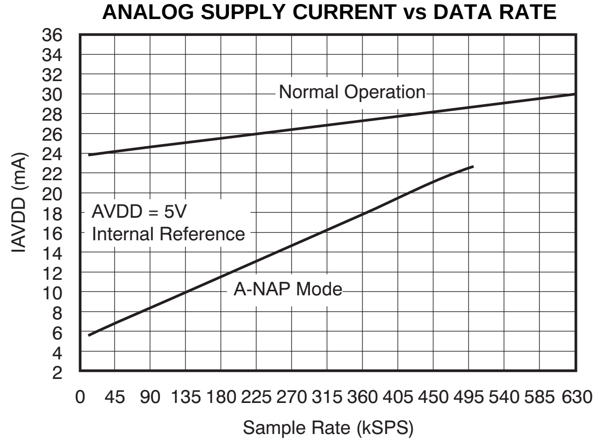


Figure 30.

BUFFER I/O SUPPLY CURRENT vs TEMPERATURE

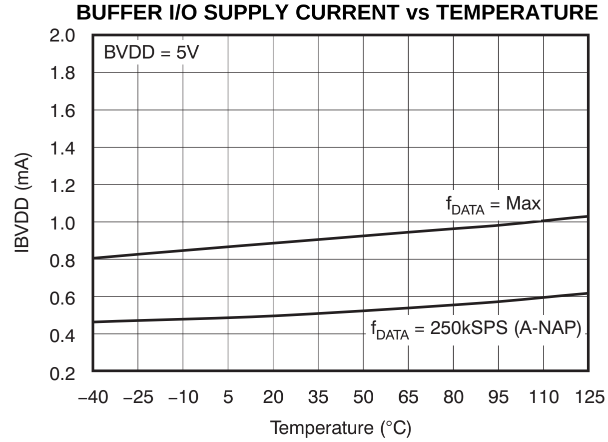


Figure 31.

ADS8556
INPUT SUPPLY CURRENT vs TEMPERATURE

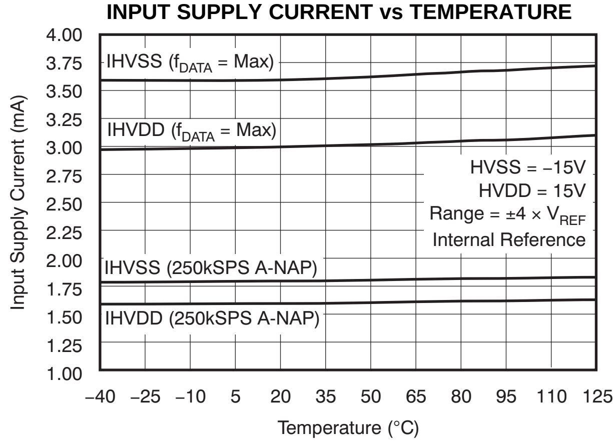


Figure 32.

ADS8556
INPUT SUPPLY CURRENT vs INPUT SUPPLY VOLTAGE

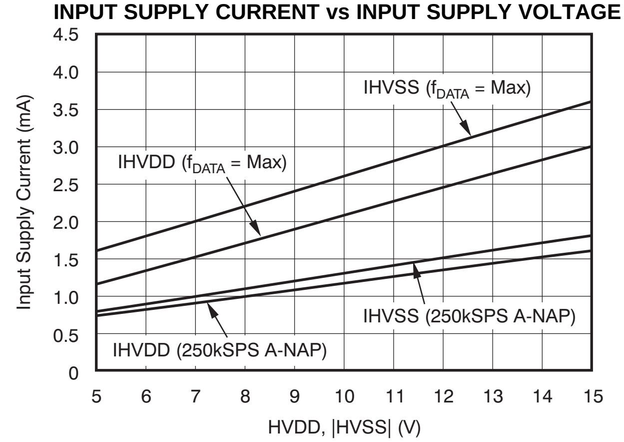


Figure 33.

TYPICAL CHARACTERISTICS (continued)

At +25°C, over entire supply voltage range, V_{REF} = 2.5V (internal), and f_{DATA} = maximum, unless otherwise noted.

ADS8556
INPUT SUPPLY CURRENT vs DATA RATE

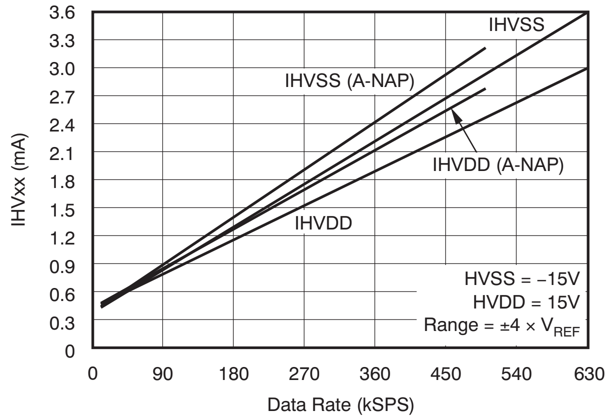


Figure 34.

GENERAL DESCRIPTION

The ADS8556/7/8 series include six 16-, 14-, and 12-bit analog-to-digital converters (ADCs) respectively that operate based on the successive approximation register (SAR) principle. The architecture is designed on the charge redistribution principle, which inherently includes a sample-and-hold function. The six analog inputs are grouped into three channel pairs. These channel pairs can be sampled and converted simultaneously, preserving the relative phase information of the signals of each pair. Separate conversion start signals allow simultaneous sampling on each channel pair: on four channels or on all six channels.

These devices accept single-ended, bipolar analog input signals in the selectable ranges of $\pm 4V_{REF}$ or $\pm 2V_{REF}$ with an absolute value of up to ±12V; see the *Analog Inputs* section.

The devices offer an internal 2.5V/3V reference source followed by a 10-bit digital-to-analog converter (DAC) that allows the reference voltage V_{REF} to be adjusted in 2.44mV or 2.93mV steps, respectively.

The ADS8556/7/8 also offer a selectable parallel or serial interface that can be used in hardware or software mode; see the *Device Configuration* section for details.

ANALOG

This section addresses the analog input circuit, the ADCs and control signals, and the reference design of the device.

Analog Inputs

The inputs and the converters are of single-ended, bipolar type. The absolute voltage range can be selected using the RANGE pin (in hardware mode) or RANGE_x bits (in software mode) in the control register (CR) to either $\pm 4V_{REF}$ or $\pm 2V_{REF}$. With the reference set to 2.5V (CR bit C18 = 0), the input voltage range can be ±10V or ±5V. With the reference source set to 3V (CR bit C18 = 1), an input voltage range of ±12V or ±6V can be configured. The logic state of the RANGE pin is latched with the falling edge of BUSY (if CR bit C20 = 0).

The input current on the analog inputs depends on the actual sample rate, input voltage, and signal source impedance. Essentially, the current into the analog inputs charges the internal capacitor array only during the sampling period (t_{ACQ}). The source of the analog input voltage must be able to charge the input capacitance of 10pF in $\pm 4V_{REF}$ mode or 20pF in $\pm 2V_{REF}$ to a 12-, 14-, 16-bit accuracy level within the acquisition time of 280ns at maximum data rate; see the Equivalent Input Circuit. During the conversion period, there is no further input current flow and the input impedance is greater than 1MΩ. To ensure a defined start condition, the sampling capacitors of the ADS8556/7/8 are pre-charged to a fixed internal voltage, before switching into sampling mode.

To maintain the linearity of the converter, the inputs should always remain within the specified range of HVSS – 0.2V to HVDD + 0.2V.

The minimum –3dB bandwidth of the driving operational amplifier can be calculated using Equation 1:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

where:

n = 16, 14, or 12; *n* is the resolution of the ADS8556/7/8

With a minimum acquisition time of t_{ACQ} = 280ns, the required minimum bandwidth of the driving amplifier is 6.7MHz for the ADS8556, 6MHz for the ADS8557, or 5.2MHz for the ADS8558. The required bandwidth can be lower if the application allows a longer acquisition time. A gain error occurs if a given application does not fulfill the bandwidth requirement shown in Equation 1.

A driving operational amplifier may not be required, if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of Equation 2:

$$R_{SOURCE} < \frac{t_{ACQ}}{C_S \ln(2) \times (n + 1)} - (R_{SER} + R_{SW}) \quad (2)$$

where:

n = 16, 14, or 12; *n* is the resolution of the ADC,

C_S = 10pF is the sample capacitor value for V_{IN} = ±4 × V_{REF} mode,

R_{SER} = 200Ω is the input resistor value,

and R_{SW} = 130Ω is the switch resistance value

With t_{ACQ} = 280ns, the maximum source impedance should be less than 2.0kΩ for the ADS8556, 2.3kΩ for the ADS8557, and 2.7kΩ for the ADS8558 in V_{IN} = $\pm 4V_{REF}$ mode or less than 0.8kΩ for the ADS8556, 1.0kΩ for the ADS8557, and 1.2kΩ for the ADS8558 in V_{IN} = $\pm 2V_{REF}$ mode. The source impedance can be higher if the application allows longer acquisition time.

Analog-to-Digital Converter (ADC)

The devices include six ADCs that operate with either an internal or an external conversion clock. The conversion time can be as low as 1.09μs with internal conversion clock (ADS8558). When an external clock and reference are used, the minimum conversion time is 925ns.

Conversion Clock

The device uses either an internally-generated or an external (XCLK) conversion clock signal (in software mode only). In default mode, the device generates an internal clock. When the CLKSEL bit is set high (bit C11 in the CR), an external conversion clock of up to 20MHz (max) can be applied on pin 27. In both cases, 18.5 clock cycles are required for a complete conversion including the pre-charging of the sample capacitors. The external clock can remain low between conversions.

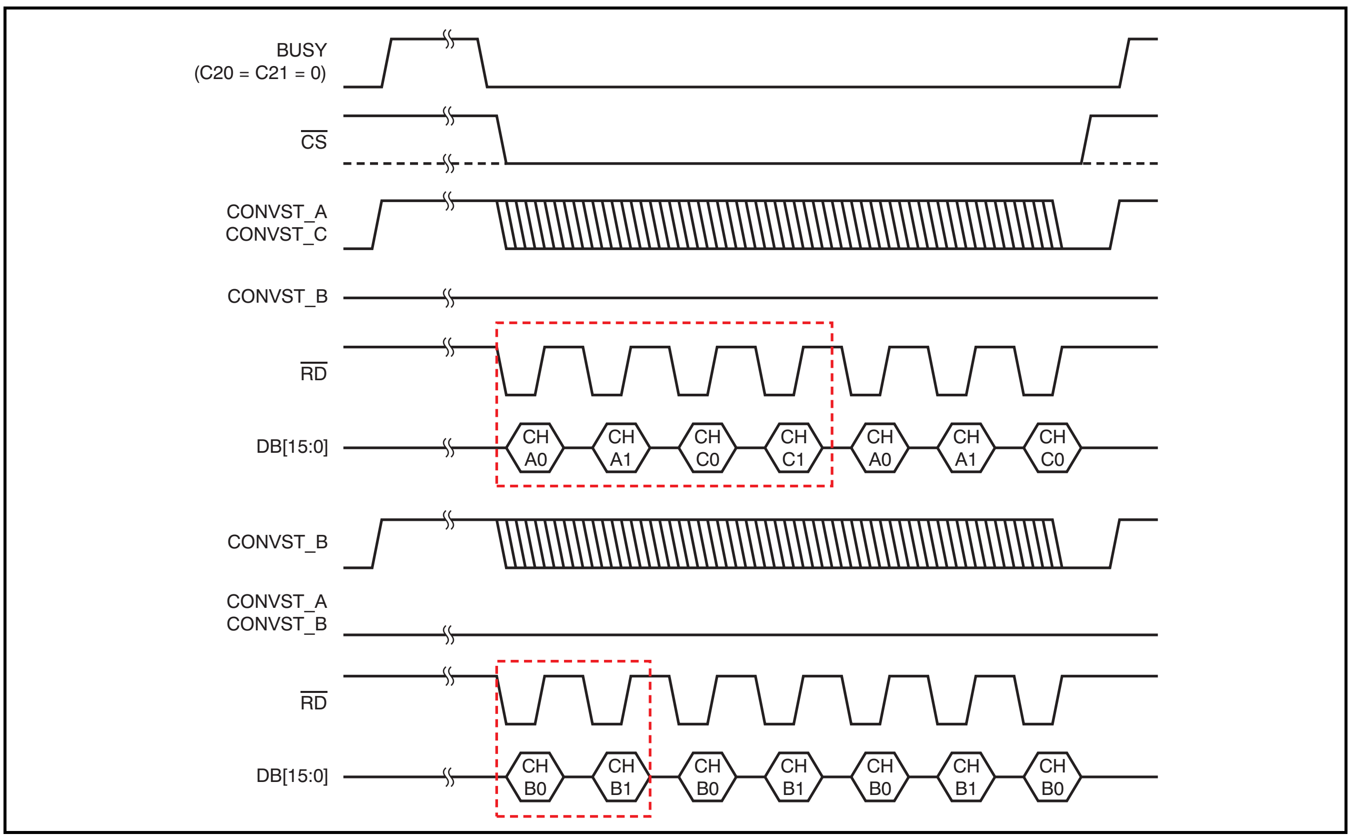
The conversion clock duty cycle should be 50%. However, the ADS8556/7/8 function properly with a duty cycle between 45% and 55%.

CONVST_x

The analog inputs of each channel pair (CH_x0/1) are held with the rising edge of the corresponding CONVST_x signal. Only in software mode (except sequential mode), CONVST_A is used for all six ADCs. The conversion automatically starts with the next edge of the conversion clock. CONVST_x should remain high during the entire conversion cycle; this is while the BUSY signal remains active. A falling edge during an ongoing conversion puts the related ADC pair into partial power-down mode (see the *Reset and Power-Down Modes* section for more details).

A conversion start must not be issued during an ongoing conversion on the same channel pair. It is allowed to initiate conversions on the other input pairs, however (see the *Sequential Mode* section for more details).

If a parallel interface is used, the behavior of the output port depends on which CONVST_x signals have been issued. Figure 35 shows examples of different scenarios.



NOTE: Boxed areas indicate the minimum required frame to acquire all data.

Figure 35. Data Output versus CONVST_x

BUSY/INT

The BUSY signal indicates if a conversion is in progress. It goes high with a rising edge of any CONVST_x signal and goes low when the output data of the last channel pair are available in the respective output register. The readout of the data can be initiated immediately after the falling edge of BUSY. A falling edge of a CONVST_x input during an ongoing conversion (when BUSY is high) powers down the corresponding ADC pair.

In sequential mode, the BUSY signal goes low only for one clock cycle. See the *Sequential Mode* section for more details.

The polarity of the BUSY/INT signal can be changed using CR bit C20.

Reference

The ADS8556/7/8 provides an internal, low-drift 2.5V reference source. To increase the input voltage range, the reference voltage can be switched to 3V mode using the VREF bit (bit C18 in the CR). The reference feeds a 10-bit string-DAC controlled by bits C[9:0] in the control register. The buffered DAC output is connected to the REFIO pin. In this way, the voltage at this pin is programmable in 2.44mV (2.92mV in 3V mode) steps and adjustable to the application needs without additional external components. The actual output voltage can be calculated using Equation 3:

$$V_{REF} = \frac{\text{Range} \times (\text{Code} + 1)}{1024} \quad (3)$$

where:

Range = the chosen maximum reference voltage output range (2.5V or 3V),

Code = the decimal value of the DAC register content

Table 1 lists some examples of internal reference DAC settings with a reference range set to 2.5V. However, to ensure proper performance, the DAC output voltage should not be programmed below 0.5V.

The buffered output of the DAC should be decoupled with a 100nF capacitor (minimum); for best performance, a 470nF capacitor is recommended. If the internal reference is placed into power-down (default), an external reference voltage can drive the REFIO pin.

The voltage at the REFIO pin is buffered with three internal amplifiers, one for each ADC pair. The output of each buffer needs to be decoupled with a 10μF capacitor between pin pairs 53 and 54, 55 and 56, and 57 and 58. The 10μF capacitors are available as ceramic 0805-SMD components and in X5R quality.

The internal reference buffers can be powered down to decrease the power dissipation of the device. In this case, external reference drivers can be connected to REFC_A, REFC_B, and REFC_C pins. With 10μF decoupling capacitors, the minimum required bandwidth can be calculated using Equation 4:

$$f_{-3dB} = \frac{\ln(2)}{2\pi \times t_{CONV}} \quad (4)$$

With the minimum t_{CONV} of 1.09μs, the external reference buffers require a minimum bandwidth of 1.02kHz.

Table 1. DAC Setting Examples (2.5V Operation)

$V_{REF\ OUT}$ (V)	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.500	204	00 1100 1100	CC
1.25	511	01 1111 1111	1FF
2.500	1023	11 1111 1111	3FF

DIGITAL

This section describes the digital control and the timing of the device in detail.

Device Configuration

Depending on the desired mode of operation, the ADS8556/7/8 can be configured using the external pins and/or the control register (CR), as shown in Table 2.

Parallel Interface

To use the device with the parallel interface, the PAR/SER pin should be held low. The maximum achievable data throughput rate using the internal clock is 630kSPS for the ADS8556, 670kSPS for the ADS8557, and 730kSPS for the ADS8558 in this case.

Access to the ADS8556/7/8 is controlled as illustrated in Figure 2 and Figure 3.

The device can either operate with a 16-bit (WORD/BYTE pin set low) or an 8-bit (WORD/BYTE pin set high) parallel interface. If 8-bit operation is used, the HB_{EN} pin selects if the low-byte (DB7 low) or the high-byte (DB7 high) is available on the data output DB[15:8] first.

Serial Interface

The serial interface mode is selected by setting the PAR/SER pin high. In this case, each data transfer starts with the falling edge of the frame synchronization input (FS). The conversion results are presented on the serial data output pins SDO_A, SDO_B, and SDO_C depending on the selections made using the SEL_x pins. Starting with the most significant bit (MSB), the output data are changed at the rising edge of SCLK, so that the host processor can read it at the following falling edge. Output data of the ADS8557 and ADS8558 maintain the 16-bit format with leading zeros.

Serial data input SDI are latched at the falling edge of SCLK.

The serial interface can be used with one, two, or three output ports. These ports are enabled with pins SEL_A, SEL_B, and SEL_C. If all three serial data output ports (SDO_A, SDO_B, and SDO_C) are selected, the data can be read with either two 16-bit data transfers or with one 32-bit data transfer. The data of channels CH_x0 are available first, followed by data from channels CH_x1. The maximum achievable data throughput rate is 450kSPS for the ADS8556, 470kSPS for the ADS8557, and 500kSPS for the ADS8558 in this case.

If the application allows a data transfer using two ports only, SDO_A and SDO_B outputs are used. The device outputs data from channel CH_A0 followed by CH_A1 and CH_C0 on SDO_A, while data from channel CH_B0 followed by CH_B1 and CH_C1 occurs on SDO_B. In this case, a data transfer of three consecutive 16-bit words or one continuous 48-bit word is supported. The maximum achievable data throughput rate is 375kSPS for the ADS8556, 390kSPS for the ADS8557, and 400kSPS for the ADS8558.

The output SDO_A is selected if only one serial data port is used in the application. The data are available in the following order: CH_A0, CH_A1, CH_B0, CH_B1, CH_C0, and, finally CH_C1. Data can be read using six 16-bit transfers, three 32-bit transfers, or a single 96-bit transfer. The maximum achievable data throughput rate is 250kSPS for the ADS8556/7 and 260kSPS for the ADS8558 in this case.

Figure 1 (the serial operation timing diagram) and Figure 36 show all possible scenarios in more detail.

Table 2. ADS8556/7/8 Configuration Settings

INTERFACE MODE	HARDWARE MODE (HW/SW = 0) CONVERSION START CONTROLLED BY SEPARATE CONVST_x PINS	SOFTWARE MODE (HW/SW = 1) CONVERSION START CONTROLLED BY CONVST_A PIN ONLY, EXCEPT IN SEQUENTIAL MODE
Parallel (PAR/SER = 0)	Configuration using pins, optionally, control bits C[22:18], C[15:13], and C[9:0]	Configuration using control register bits C[31:0] only; status of pins 27 (only if used as RANGE input) and 63 is disregarded
Serial (PAR/SER = 1)	Configuration using pins, optionally, control bits C[22:18], C[15:13], and C[9:0]; bits C[31:24] are disregarded	Configuration using control register bits C[31:0] only; status of pins 1, 27 (only if used as RANGE input), and 63 is disregarded; each access requires a control register update via SDI (see the *Serial Interface* section for details)

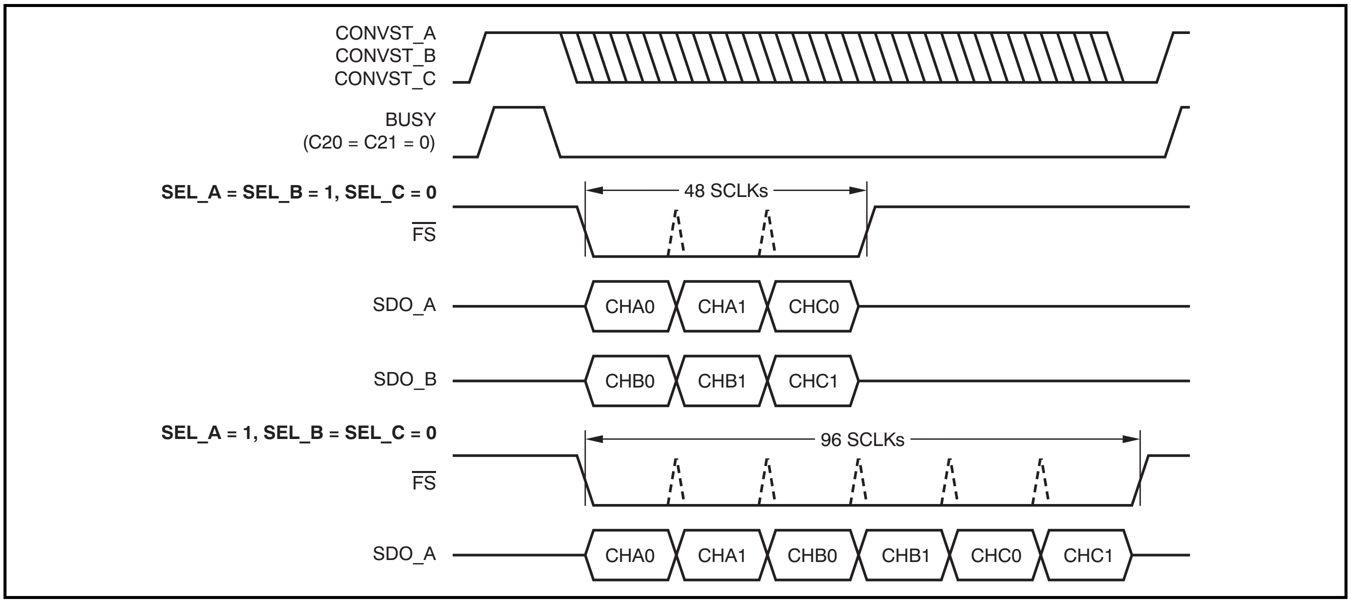


Figure 36. Serial Interface: Data Output with One or Two Active SDOs

Hardware Mode

With the HW/SW input (pin 62) set low, the device functions are controlled via the pins and, optionally, control register bits C[22:18], C[15:13], and C[9:0].

It is possible to generally use the part in hardware mode but to switch it into software mode to initialize or adjust the control register settings (for example, the internal reference DAC) and back to hardware mode thereafter.

Software Mode

When the HW/SW input is set high, the device operates in software mode with functionality set only by the control register bits (corresponding pin settings are ignored).

If parallel interface is used, an update of all control register settings is performed by issuing two 16-bit write accesses on pins DB[15:0] in word mode or four 8-bit accesses on pins DB[15:8] in byte mode (to avoid losing data, the entire sequence must be finished before starting a new conversion). $\overline{\text{CS}}$ should be held low during the two or four write accesses to completely update the configuration register. It is also possible to update only the upper eight bits (C[31:24]) using a single write access and pins DB[15:8] in both word and byte modes. In word mode, the first write access updates only the upper eight bits and stores the lower eight bits (C[23:16]) for an update that takes place with the second write access along with C[15:0].

If the serial interface is used, input data containing control register contents are required with each read access to the device in this mode (combined read/write access). For initialization purposes, all 32 bits of the register should be set (bit C16 must be set to '1' during that access to allow the update of the entire register content). To minimize switching noise on the interface, an update of the first eight bits (C[31:24]) with the remaining bits held low can be performed thereafter.

Figure 37 illustrates the different control register update options.

Control Register (CR); Default Value = 0x000003FF

The control register settings can only be changed in software mode and are not affected when switching to hardware mode thereafter. The register values are independent from input pin settings. Changes are active with the rising edge of $\overline{\text{WR}}$ in parallel interface mode or with the 32nd falling SCLK edge of the access in which the register content has been updated in serial mode. Optionally, the register can also be partially updated by writing only the upper eight bits (C[31:24]). The CR content is defined in Table 3.

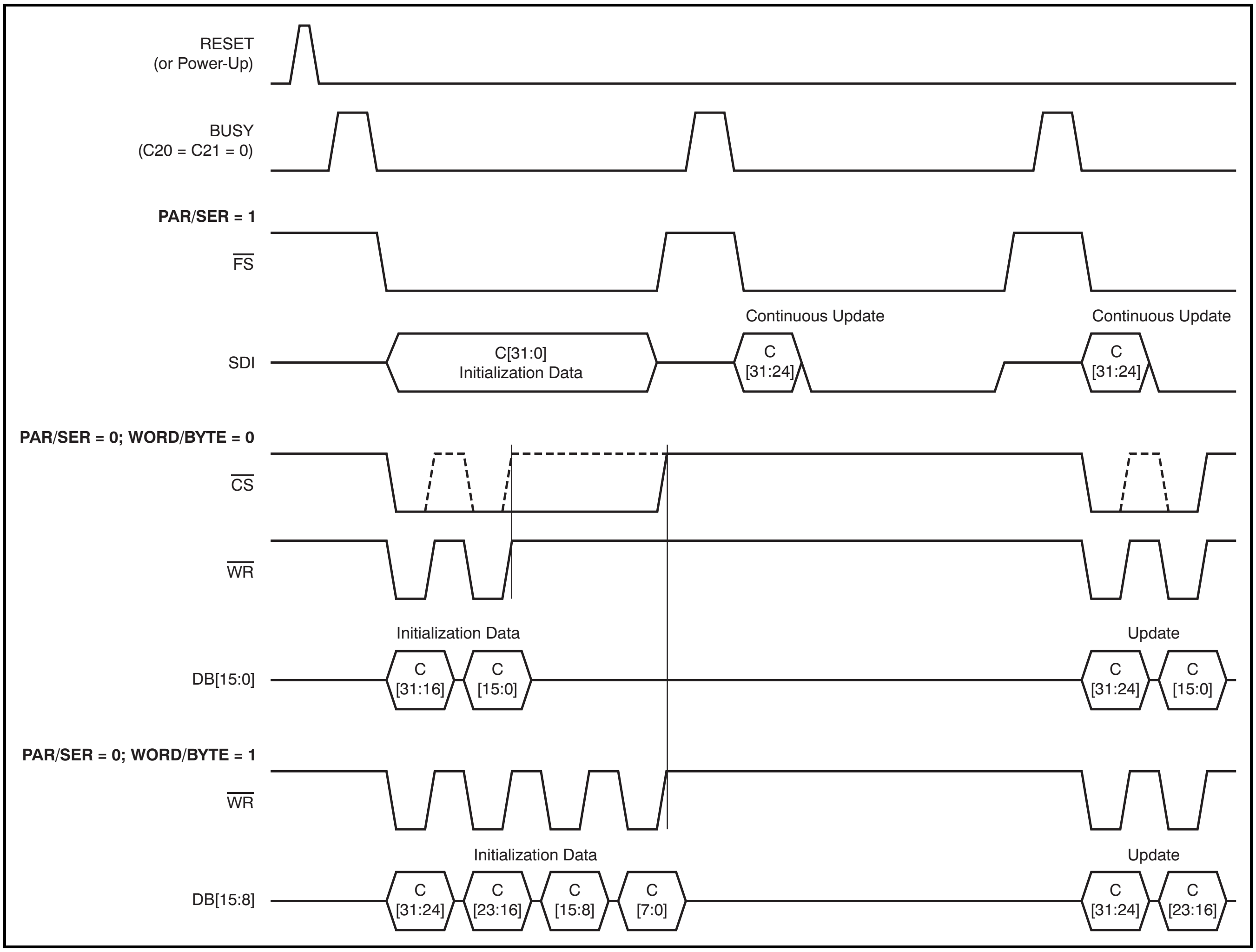


Figure 37. Control Register Update Options

Table 3. Control Register (CR)

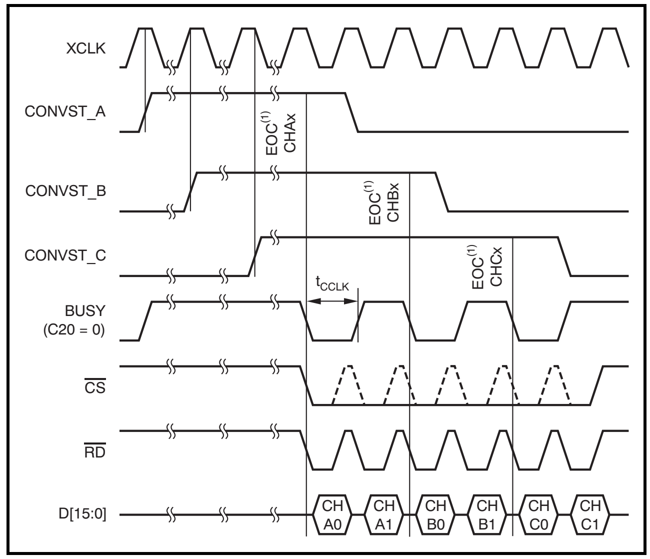
BIT	NAME	DESCRIPTION	ACTIVE IN HARDWARE MODE
C31	CH_C	0 = Channel pair C disabled for next conversion (default) 1 = Channel pair C enabled	No
C30	CH_B	0 = Channel pair B disabled for next conversion (default) 1 = Channel pair B enabled	No
C29	CH_A	0 = Channel pair A disabled for next conversion (default) 1 = Channel pair A enabled	No
C28	RANGE_C	0 = Input voltage range selection for channel pair C: $4V_{REF}$ (default) 1 = Input voltage range selection for channel pair C: $2V_{REF}$	No
C27	RANGE_B	0 = Input voltage range selection for channel pair B: $4V_{REF}$ (default) 1 = Input voltage range selection for channel pair B: $2V_{REF}$	No
C26	RANGE_A	0 = Input voltage range selection for channel pair A: $4V_{REF}$ (default) 1 = Input voltage range selection for channel pair A: $2V_{REF}$	No
C25	REF_{EN}	0 = Internal reference source disabled (default) 1 = Internal reference source enabled	No
C24	REFBUF	0 = Internal reference buffers enabled (default) 1 = Internal reference buffers disabled	No
C23	SEQ	0 = Sequential convert start mode disabled (default) 1 = Sequential convert start mode enabled (bit 11 must be '1' in this case)	No
C22	A-NAP	0 = Normal operation (default) 1 = Auto-NAP feature enabled	Yes
C21	BUSY/INT	0 = BUSY/INT pin in normal mode (BUSY) (default) 1 = BUSY/INT pin in interrupt mode (INT)	Yes
C20	BUSY L/H	0 = BUSY active high while INT active low (default) 1 = BUSY active low while INT active high	Yes
C19	Don't use	This bit is always set to '0'	—
C18	VREF	0 = Internal reference voltage: 2.5V (default) 1 = Internal reference voltage: 3V	Yes
C17	READ_EN	0 = Normal operation (conversion results available on SDO_x) (default) 1 = Control register contents output on SDO_x with next access	Yes
C16	C23:0_EN	0 = Control register bits C[31:24] update only (serial mode only) (default) 1 = Entire control register update enabled (serial mode only)	Yes
C15	PD_C	0 = Normal operation (default) 1 = Power-down for channel pair *C* enabled (bit 31 must be '0' in this case)	Yes
C14	PD_B	0 = Normal operation (default) 1 = Power-down for channel pair *B* enabled (bit 30 must be '0' in this case)	Yes
C13	PD_A	0 = Normal operation (default) 1 = Power-down for channel pair *A* enabled (bit 29 must be '0' in this case)	Yes
C12	Don't use	This bit is always '0'	—
C11	CLKSEL	0 = Normal operation with internal conversion clock (mandatory in hardware mode) (default) 1 = External conversion clock (applied through pin 27) used	No
C10	CLKOUT_EN	0 = Normal operation (default) 1 = Internal conversion clock available at pin 27	No
C9	REFDAC[9]	Bit 9 (MSB) of reference DAC value; default = 1	Yes
C8	REFDAC[8]	Bit 8 of reference DAC value; default = 1	Yes
C7	REFDAC[7]	Bit 7 of reference DAC value; default = 1	Yes
C6	REFDAC[6]	Bit 6 of reference DAC value; default = 1	Yes
C5	REFDAC[5]	Bit 5 of reference DAC value; default = 1	Yes
C4	REFDAC[4]	Bit 4 of reference DAC value; default = 1	Yes
C3	REFDAC[3]	Bit 3 of reference DAC value; default = 1	Yes
C2	REFDAC[2]	Bit 2 of reference DAC value; default = 1	Yes
C1	REFDAC[1]	Bit 1 of reference DAC value; default = 1	Yes
C0	REFDAC[0]	Bit 0 (LSB) of reference DAC value; default = 1	Yes

Daisy-Chain Mode (in Serial Mode Only)

The serial interface of the ADS8556/7/8 supports a daisy-chain feature that allows cascading of multiple devices to minimize the board space requirements and simplify routing of the data and control lines. In this case, pins DB5/DCIN_A, DB4/DCIN_B, and DB3/DCIN_C are used as serial data inputs for channels A, B, and C, respectively. Figure 39 shows an example of a daisy-chain connection of three devices sharing a common CONVST line to allow simultaneous sampling of 18 analog channels along with the corresponding timing diagram. To activate the daisy-chain mode, the DC_{EN} pin must be pulled high. As a result of the time specifications t_{S1}, t_{H1}, and t_{D3}, the maximum SCLK frequency that may be used in daisy-chain mode is 27.78MHz (assuming 50% duty cycle).

Sequential Mode (in Software Mode with External Conversion clock Only)

The three channel pairs of the ADS8556/7/8 can be run in sequential mode, with the corresponding CONVST_x signals interleaved, when an external clock is used. To activate the device in sequential mode, CR bits C11 (CLKSEL) and C23 (SEQ) must be asserted. In this case, the BUSY output indicates a finished conversion by going low (when C20 = 0) or high (when C20 = 1) for only a single conversion clock cycle in case of ongoing conversions of any other channel pairs. Figure 38 shows the behavior of the BUSY output in this mode. Each conversion start should be initiated during the high phase of the external clock, as shown in Figure 38. The minimum time required between two CONVST_x pulses in the time required to read the conversion result of a channel (pair).



(1) EOC = end of conversion (internal signal).

Figure 38. Sequential Mode Timing

Output Data Format

The data output format of the ADS8556/7/8 is binary twos complement, as shown in Table 4.

For the ADS8557, which delivers 14-bit conversion results, the leading two bits of the 16-bit frame are '0' in the serial interface mode. In parallel interface mode, the output pins DB[15:14] are held low.

Respectively, as the ADS8558 outputs 12 bits of data, the first four bits of a serial 16-bit frame are zeros, in parallel interface mode the output pins DB[15:12] are held low.

Table 4. Output Data Format

DESCRIPTION	INPUT VOLTAGE VALUE	BINARY CODE (HEXADECIMAL CODE)		
		ADS8556	ADS8557	ADS8558
Positive full-scale	$+4V_{REF}$ or $+2V_{REF}$	0111 1111 1111 1111 (7FFF)	0001 1111 1111 1111 (1FFF)	0000 0111 1111 1111 (7FF)
Midscale + 0.5LSB	V_{REF}/(2 × resolution)	0000 0000 0000 0000 (0000)	0000 0000 0000 0000 (0000)	0000 0000 0000 0000 (0000)
Midscale – 0.5LSB	$–V_{REF}$/(2 × resolution)	1111 1111 1111 1111 (FFFF)	0011 1111 1111 1111 (3FFF)	0000 1111 1111 1111 (FFF)
Negative full-scale	$–4V_{REF}$ or $–2V_{REF}$	1000 0000 0000 0000 (8000)	0010 0000 0000 0000 (2000)	0000 1000 0000 0000 (800)

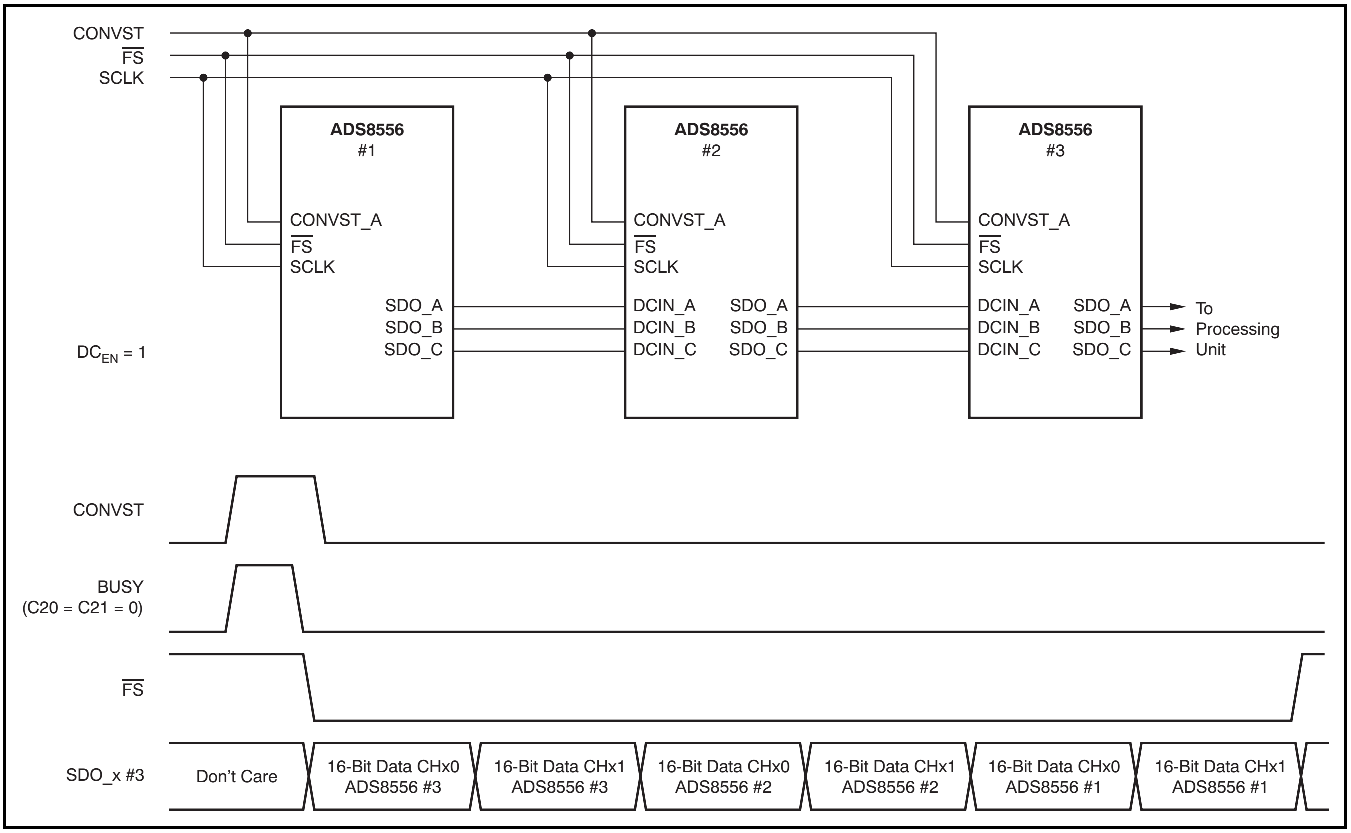


Figure 39. Example of Daisy-Chaining Three ADS8556s

Reset and Power-Down Modes

The device supports two reset mechanisms: a power-on reset (POR) and a pin-controlled reset (RESET) that can be issued using pin 28. Both the POR and RESET act as a master reset that causes any ongoing conversion to be interrupted, the control register content to be set to the default value, and all channels to be switched into sample mode.

When the device is powered up, the POR sets the device in default mode when AVDD reaches 1.5V. When the device is powered down, the POR circuit requires AVDD to remain below 125mV at least 350ms to ensure proper discharging of internal capacitors and to ensure correct behavior of the device when powered up again. If the AVDD drops below 400mV but remains above 125mV (see the *undefined zone* in Figure 40), the internal POR capacitor does not discharge fully and the device requires a pin-controlled reset to perform correctly after the recovery of AVDD.

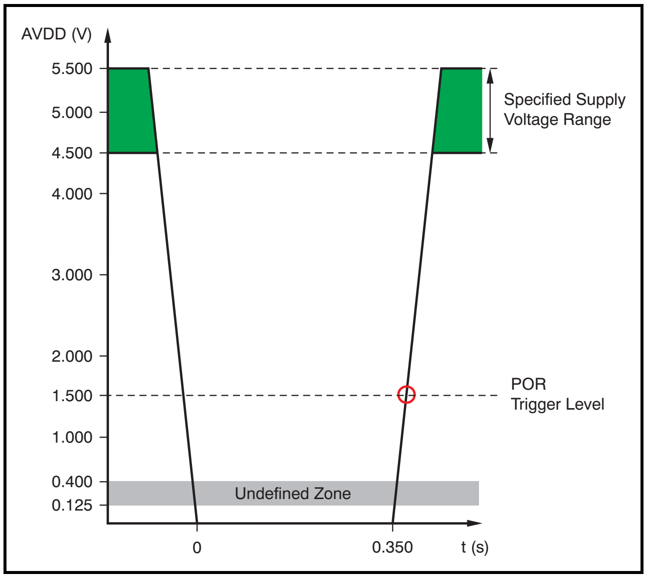


Figure 40. POR: Relevant Voltage Levels

The entire device, except the digital interface, can be powered down by pulling the STBY pin low (pin 24). As the digital interface section remains active, data can be retrieved while in stand-by mode. To power the part on again, the STBY pin must be brought high. The device is ready to start a new conversion after 10ms required to activate and settle the internal circuitry. This user-controlled approach can be used in applications that require lower data throughput rates and lowest power dissipation. The content of CR is not changed during standby mode. It is not required to perform a pin-controlled reset after returning to normal operation.

While the standby mode impacts the entire device, each device channel pair can also be individually switched off by setting control register bits C[15:13] (PD_x). When reactivated, the relevant channel pair requires 10ms to fully settle before starting a new conversion. The internal reference remains active, except all channels are powered down at the same time.

In partial power-down mode, each of the three channel pairs of the ADS8556/7/8 can be individually put into a power-saving condition that reduces the current requirement to 2mA per channel pair by bringing the corresponding CONVST_x signal low during an ongoing conversion when BUSY is high. The relevant channel pair is activated again by issuing a RESET pulse (to avoid loss of data from the active channels, this RESET pulse should be generated after retrieving the latest conversion results). The next rising edge of the CONVST_x signal should be issued at least six conversion cycle periods after the reset pulse and starts a new conversion, as shown in Figure 41. The internal reference remains active during the partial power-down mode.

The auto-NAP power-down mode is enabled by asserting the A-NAP bit (C22) in the control register. If the auto-NAP mode is enabled, the ADS8556/7/8 automatically reduce the current requirement to 6mA after finishing a conversion; thus, the end of conversion actually activates the power-down mode. Triggering a new conversion by applying a positive CONVST_x edge puts the device back into normal operation, starts the acquisition of the analog input, and automatically starts a new conversion six conversion clock cycles later. Therefore, a complete conversion cycle takes 24.5 conversion clock cycles; thus, the maximum throughput rate in auto-NAP power-down mode is reduced to a maximum of 380kSPS for the ADS8556, 395kSPS for the ADS8557, and 420kSPS for the ADS8558 in serial mode. In parallel mode, the maximum data rates are 500kSPS for the ADS8556, 530kSPS for the ADS8557, and 580kSPS for the ADS8558. The internal reference remains active during the auto-NAP mode. Table 5 compares the analog current requirements of the devices in the different modes.

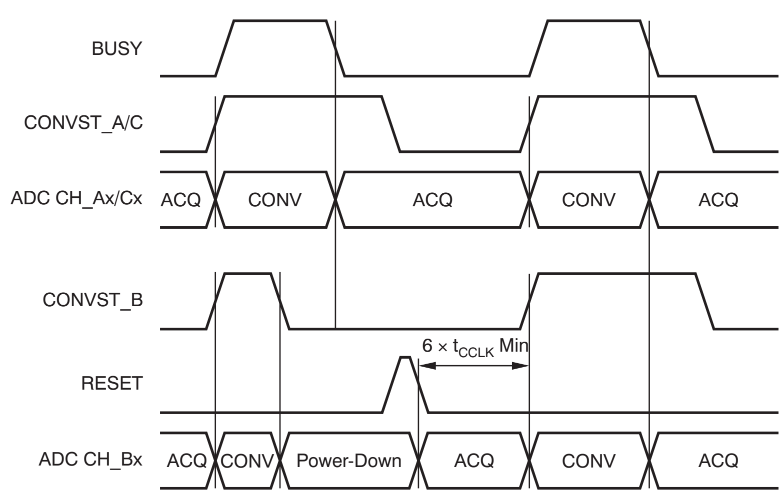


Figure 41. Partial Power-Down

Table 5. Maximum Analog Current (I_{AVDD}) Demand of the ADS8556/7/8

OPERATIONAL MODE	ANALOG CURRENT (I_{AVDD})	ENABLED BY	ACTIVATED BY	NORMAL OPERATION TO POWER-DOWN DELAY	RESUMED BY	POWER-UP TO NORMAL OPERATION DELAY	POWER-UP TO NEXT CONVERSION START TIME	DISABLED BY
Normal operation	12mA/channel pair (maximum data rate)	Power on	CONVST_x	—	—	—	—	Power off
Partial power-down of channel pair x	2mA (channel pair x)	Power on	CONVST_x low while BUSY is high	At falling edge of BUSY	RESET pulse	Immediate	6 × t_{CCLK}	Power off
Auto-NAP	6mA	A-NAP = 1 (CR bit)	Each end of conversion	At falling edge of BUSY	CONVST_x	Immediate	6 × t_{CCLK}	A-NAP = 0 (CR bit)
Power-down of channel pair x	16µA (channel pair x)	HW/SW = 1	PD_x = 1 (CR bit)	Immediate	PD_x = 0 (CR bit)	Immediate after completing register update	10ms	HW/SW = 0
Stand-by	50µA	Power on	$\overline{STBY}$ = 0	Immediate	$\overline{STBY}$ = 1	Immediate	10ms	Power off

GROUNDING

All GND pins should be connected to a clean ground reference. This connection should be kept as short as possible to minimize the inductance of this path. It is recommended to use vias connecting the pads directly to the ground plane. In designs without ground planes, the ground trace should be kept as wide as possible. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area may be used. In case of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next) to the ADC. Otherwise, even short undershoots on the digital interface lower than –300mV lead to the conduction of ESD diodes causing current flow through the substrate and degrading the analog performance.

During PCB layout, care should be taken to avoid any return currents crossing sensitive analog areas or signals.

SUPPLY

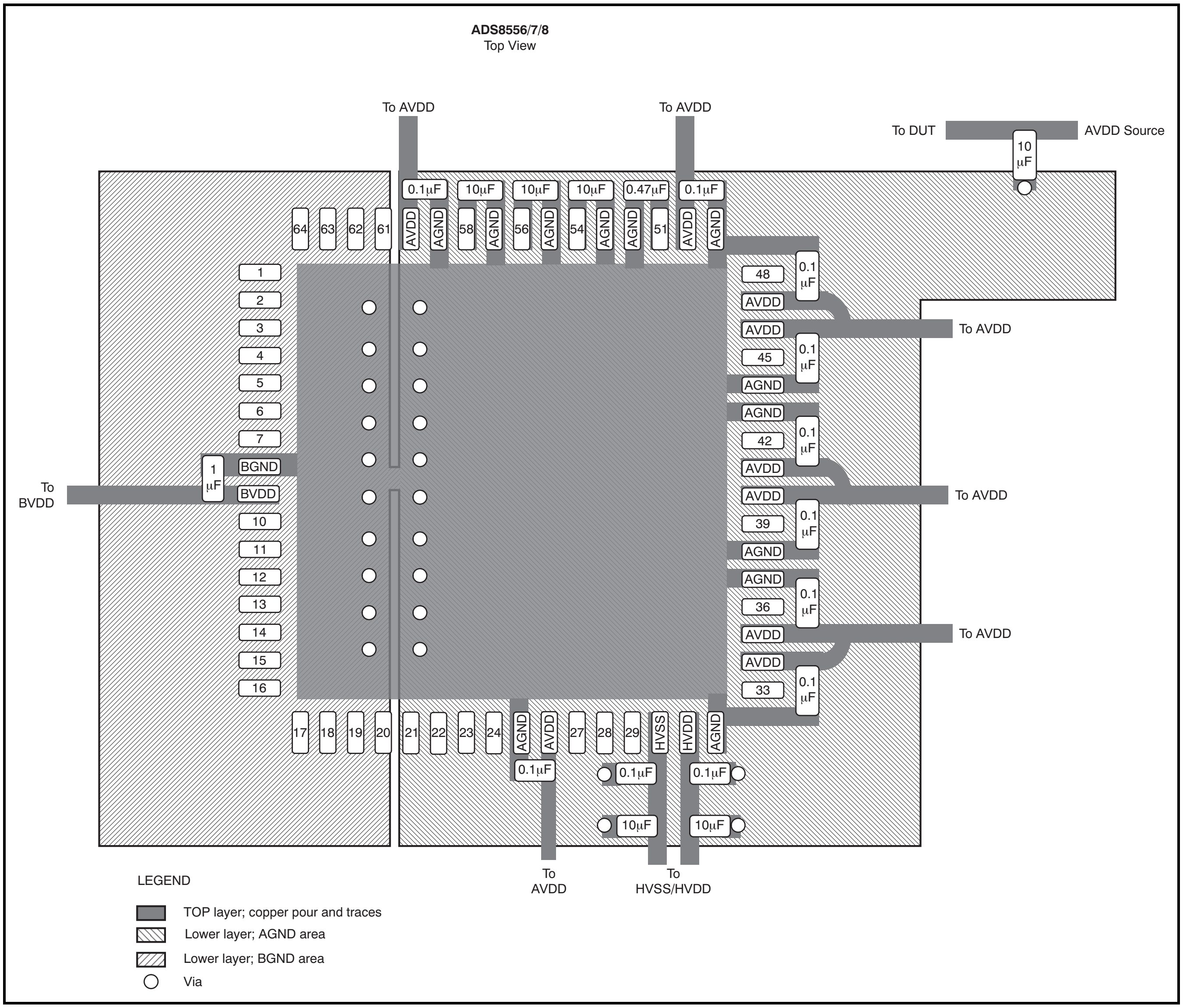
The ADS8556/7/8 require four separate supplies: the analog supply for the ADC (AVDD), the buffer I/O supply for the digital interface (BVDD), and the high-voltage supplies driving the analog input circuitry (HVDD and HVSS). Generally, there are no specific requirements with regard to the power sequencing of the device. However, when HVDD is supplied before AVDD, the internal ESD structure conducts, increasing IHVDD beyond the specified value.

The AVDD supply provides power to the internal circuitry of the ADC. It can be set in the range of 4.5V to 5.5V. Because the supply current of the device is typically 30mA, it is not possible to use a passive filter between the digital board supply of the application and the AVDD pin. A linear regulator is recommended to generate the analog supply voltage. Each AVDD pin should be decoupled to AGND with a 100nF capacitor. In addition, a single 10µF capacitor should be placed close to the device but without compromising the placement of the smaller capacitor. Optionally, each supply pin can be decoupled using a 1µF ceramic capacitor without the requirement for a 10µF capacitor.

The BVDD supply is only used to drive the digital I/O buffers and can be set in the range of 2.7V to 5.5V. This range allows the device to interface with most state-of-the-art processors and controllers. To limit the noise energy from the external digital circuitry to the device, BVDD should be filtered. A 10Ω resistor can be placed between the external digital circuitry and the device, because the current drawn is typically below 2mA (depending on the external loads). A bypass ceramic capacitor of 1µF (or alternatively, a pair of 100nF and 10µF capacitors) should be placed between the BVDD pin and pin 8.

The high-voltage supplies (HVSS and HVDD) are connected to the analog inputs. Noise and glitches on these supplies directly couple into the input signals. Place a 100nF ceramic decoupling capacitor, located as close to the device as possible, between each of pins 30, 31, and AGND. An additional 10µF capacitor is used that should be placed close to the device but without compromising the placement of the smaller capacitor.

Figure 42 shows a layout recommendation for the ADS8556/7/8 along with the proper decoupling and reference capacitor placement and connections.



(1) All 0.1µF, 0.47µF, and 1µF capacitors should be placed as close to the ADS8556/7/8 as possible.

(2) All 10µF capacitors should be close to the device but without compromising the placement of the smaller capacitors.

Figure 42. Layout Recommendation

APPLICATION INFORMATION

The minimum configuration of the ADS8556/7/8 in parallel mode is shown in Figure 43. In this case, the BUSY signal is not used while the SW generates the required signals in a timely manner. TI's OPA2211 is used as an input driver, supporting bandwidth that allows running the device at the maximum data rate.

The actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application. For highest data rate, it is recommended to use a filter capacitor value of 1nF and a series resistor of 22Ω to fulfill the settling requirements to an accuracy level of 16 bits within the acquisition time of 280ns.

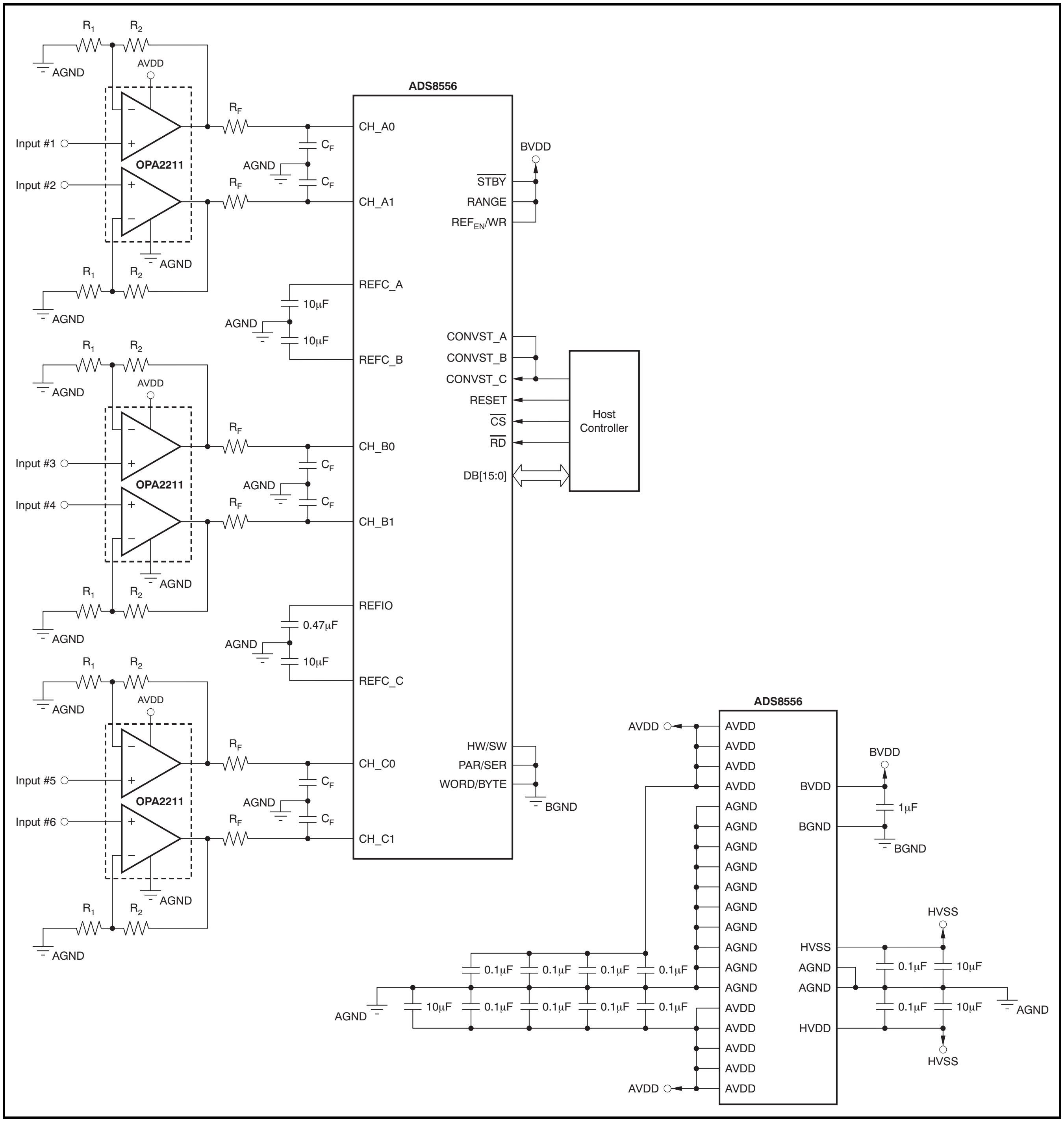


Figure 43. Minimum Configuration in Parallel Interface Mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS8556IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8556IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8557IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8557IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8558IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
ADS8558IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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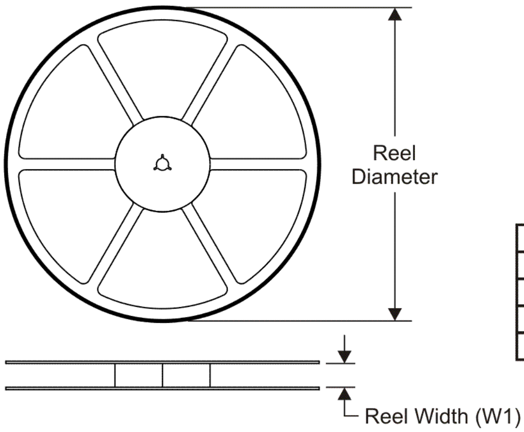
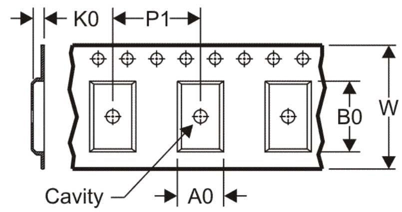
TAPE AND REEL INFORMATION

REEL DIMENSIONS

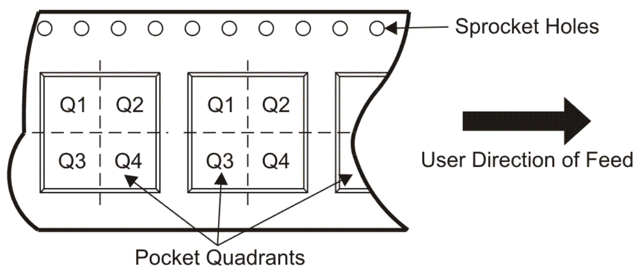


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

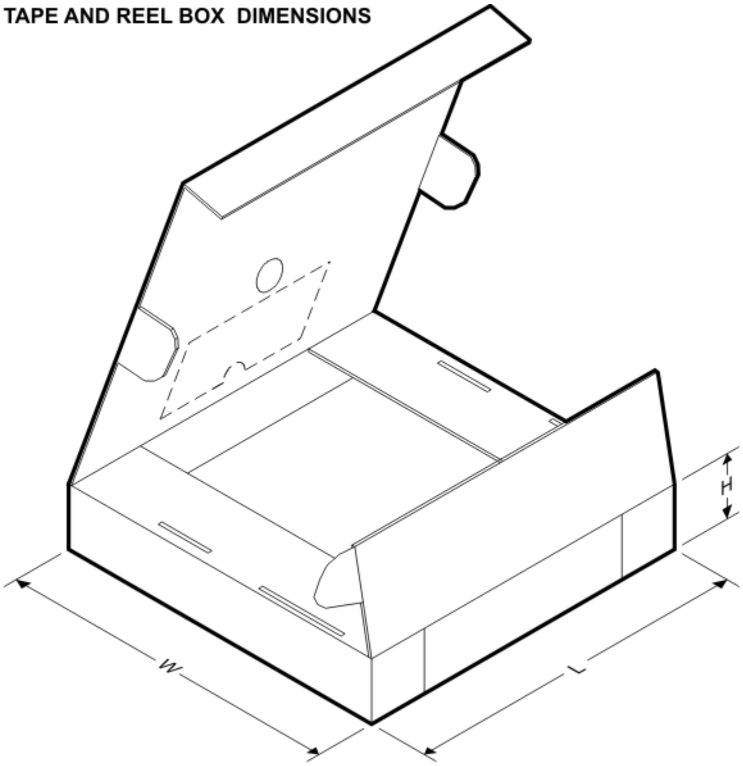
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8556IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
ADS8557IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2
ADS8558IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2

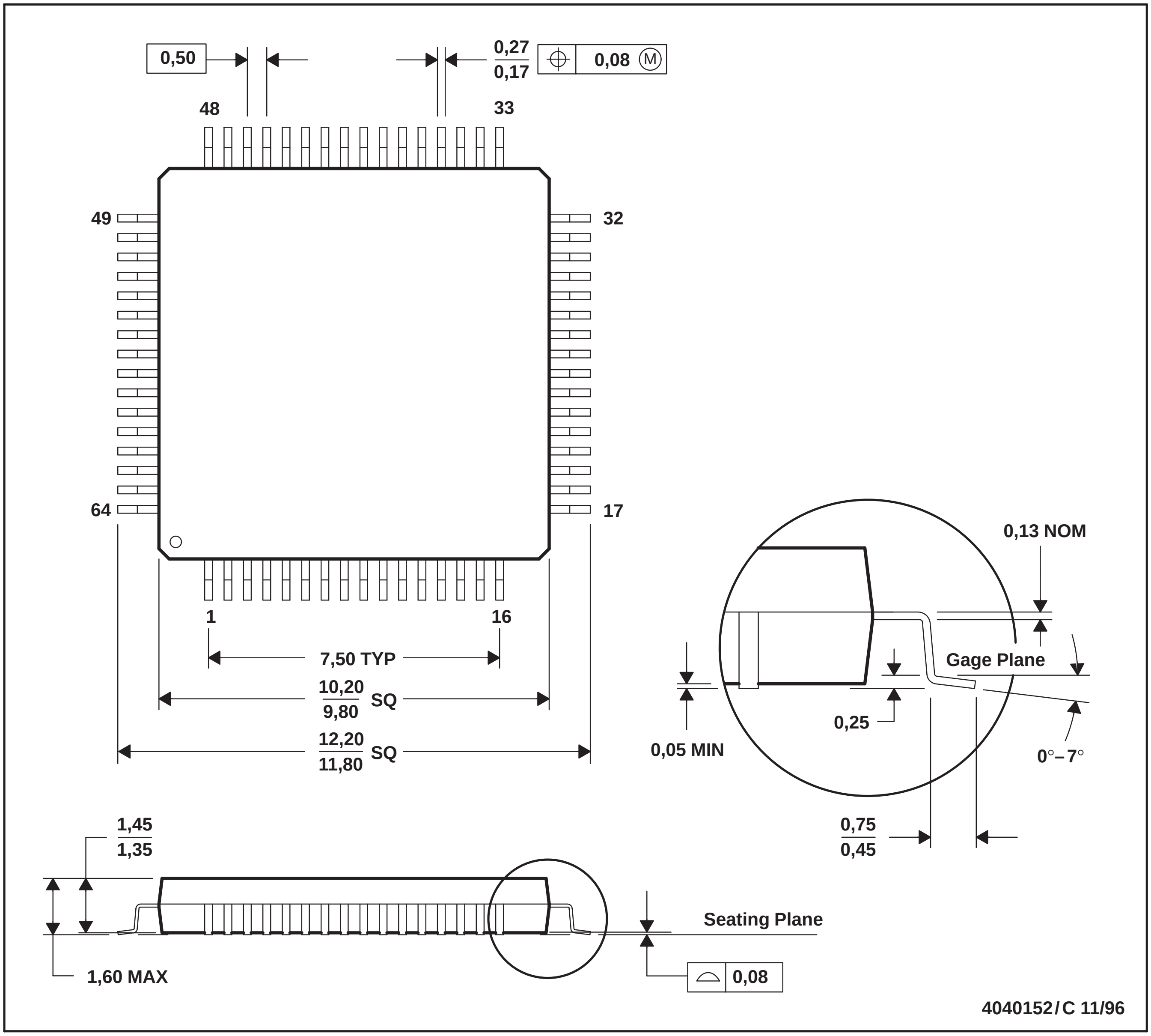
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8556IPMR	LQFP	PM	64	1000	346.0	346.0	41.0
ADS8557IPMR	LQFP	PM	64	1000	346.0	346.0	41.0
ADS8558IPMR	LQFP	PM	64	1000	346.0	346.0	41.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.