

## 2-, 3-, AND 4-CELL LITHIUM-ION OR LITHIUM-POLYMER BATTERY PROTECTION AFE

### FEATURES

- 2- 3- or 4-Cell Series Protection Control
- Can Directly Interface with the bq803x-Based Gas Gauge Family
- Watchdog and POR for the Host
- Provides Individual Cell Voltages and Battery Voltage to Battery Management Host
- Capable of Operation With 5-mΩ Sense Resistor Integrated Cell Balancing Drive
- I<sup>2</sup>C Compatible User Interface Allows Access to Battery Information
- Programmable Threshold and Delay for Overload Short Circuit in Discharge and Short Circuit in Charge

- NMOS FET Drive for Charge and Discharge FETs
- Host Control can Initiate Sleep and Ship Power Modes
- Integrated 2.5-V, 16-mA LDO
- Integrated 3.3-V, 25-mA LDO
- Supply Voltage Range from 4.5 V to 28 V
- Low Supply Current of 100 μA Typical

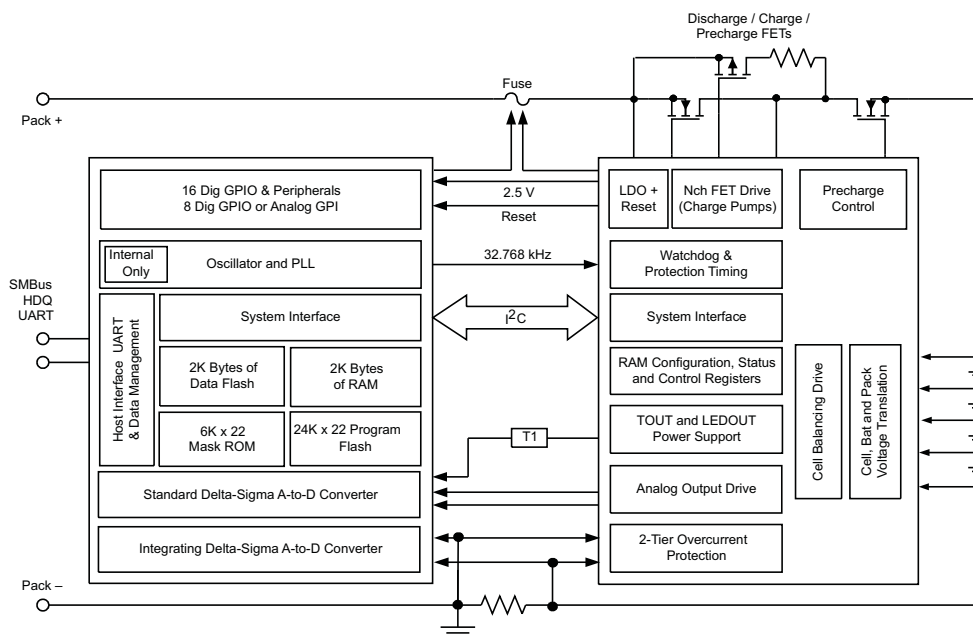
### APPLICATIONS

- Notebook Computers
- Medical and Test Equipment
- Instrumentation and Measurement Systems

### DESCRIPTION

The bq29330 is a 2-, 3-, or 4-cell lithium-ion battery pack full-protection analog front end (AFE) IC that incorporates a 2.5-V, 16-mA and 3.3-V, 25-mA low dropout regulator (LDO). The bq29330 also integrates an I<sup>2</sup>C-compatible interface to extract battery parameters such as battery voltage, individual cell voltages, and control output status. Other parameters such as current protection thresholds and delays can also be programmed into the bq29330 to increase the flexibility of the battery management system.

### SYSTEM DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION (CONTINUED)

The bq29330 provides safety protection for overload, short circuit in charge, and short circuit in discharge conditions and can also provide cell overvoltage, battery overvoltage and battery undervoltage protection with the battery management host. In overload, short circuit in charge and short circuit in discharge conditions, the bq29330 turns off the FET drive autonomously, depending on the internal configuration setting. The communications interface allows the host to observe and control the status of the bq29330, enable cell balancing, enter different power modes, set current protection levels, and set the blanking delay times.

Cell balancing of each cell can be performed via a cell bypass path integrated into the bq29330, which can be enabled via the internal control register accessible via the I<sup>2</sup>C-compatible interface. The maximum bypass current is set via an external series resistor and internal FET on resistance (typ. 400 Ω).

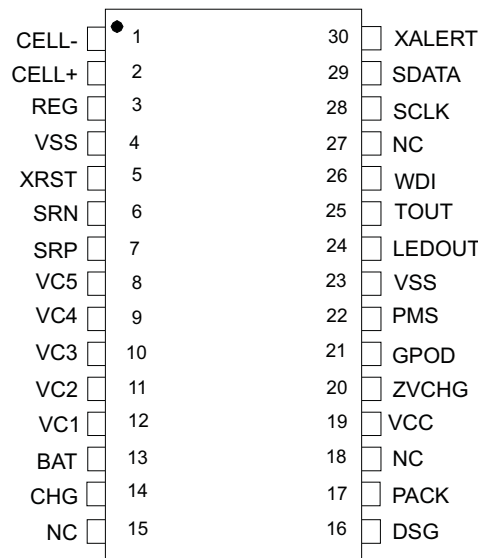
### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE
	TSSOP(DBT) <sup>(2)</sup>
-40°C to 110°C	bq29330DBT

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) The bq29330 can be ordered in tape and reel by adding the suffix R to the orderable part number, i.e., bq29330DBTR.

### PACKAGE OPTION PIN DIAGRAMS

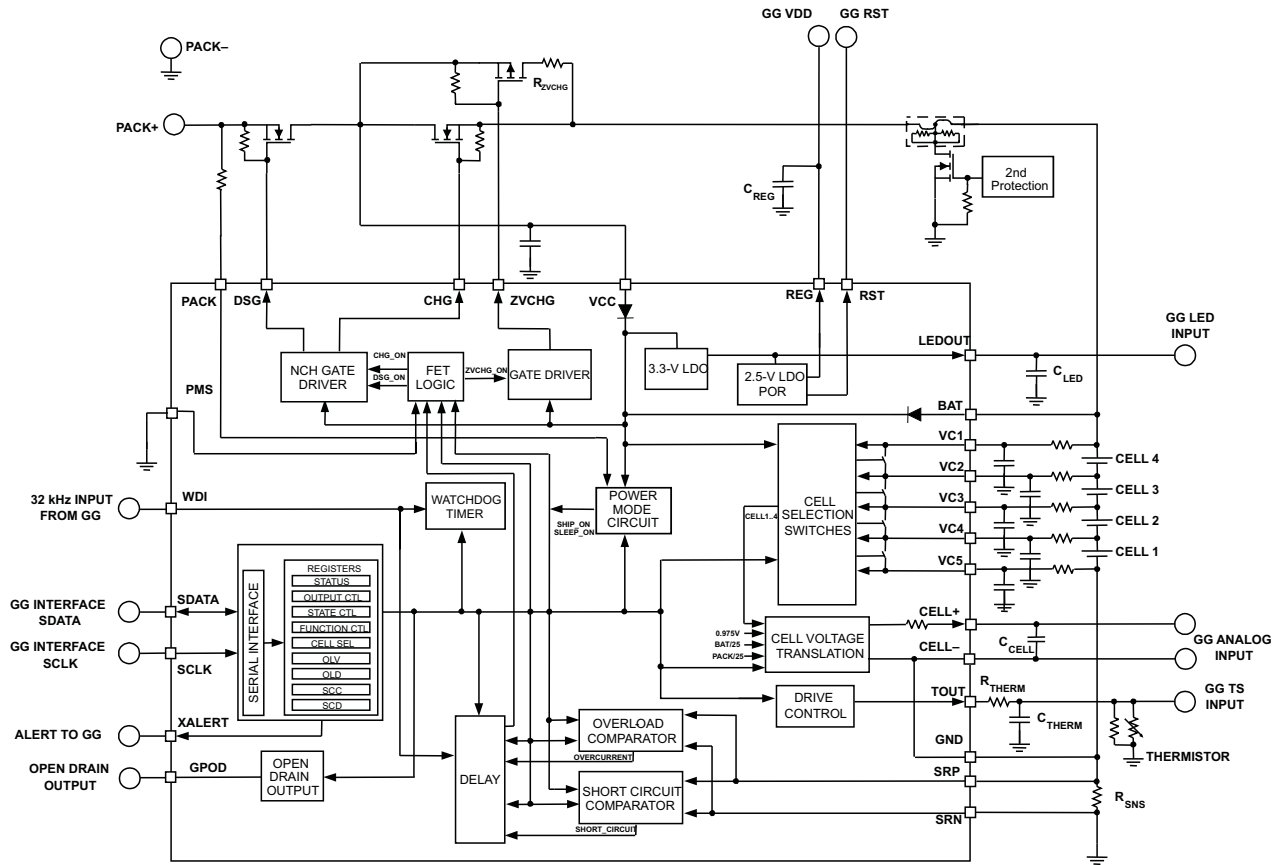
TSSOP PACKAGE  
(TOP VIEW)



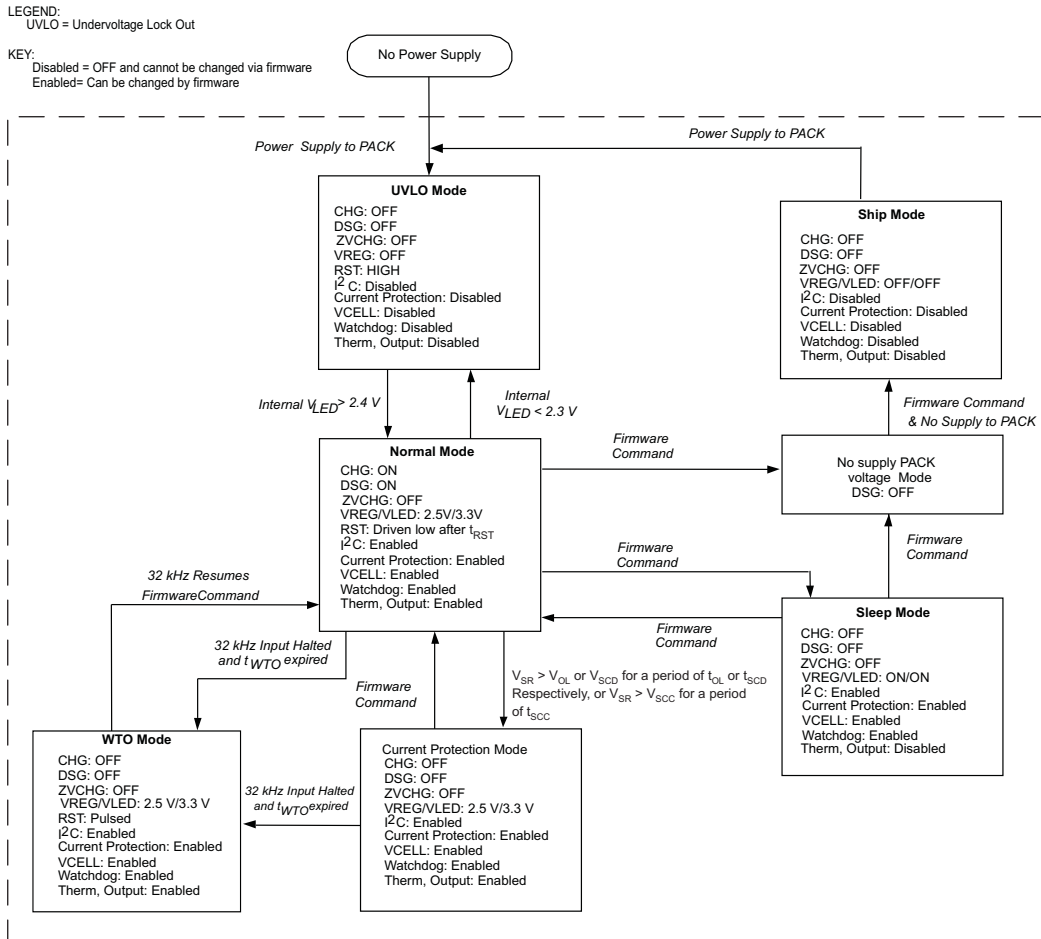
**PIN FUNCTIONS**

PIN		DESCRIPTION
NAME	DBT NO.	
CELL–	1	Output of scaled value of the measured cell voltage.
CELL+	2	Output of scaled value of the measured cell voltage.
REG	3	Integrated 2.5-V regulator output
VSS	4, 23	Power supply ground
XRST	5	Active-low output
SRN	6	Current sense terminal
SRP	7	Current sense positive terminal when charging relative to SRN; current sense negative terminal when discharging relative to SRN
VC5	8	Sense voltage input terminal for most negative cell; balance current input for least positive cell.
VC4	9	Sense voltage input terminal for least positive cell, balance current input for least positive cell, and return balance current for third most positive cell.
VC3	10	Sense voltage input terminal for third most positive cell, balance current input for third most positive cell, and return balance current for second most positive cell.
VC2	11	Sense voltage input terminal for second most positive cell, balance current input for second most positive cell, and return balance current for most positive cell.
VC1	12	Sense voltage input terminal for most positive cell, balance current input for most positive cell, and battery stack measurement input
BAT	13	Device power supply input
CHG	14	Charge pump, charge N-CH FET gate drive
DSG	16	Charge pump output, discharge N-CH FET gate drive
PACK	17	PACK positive terminal and alternative power source
VCC	19	Power supply voltage
ZVCHG	20	Connect the precharge P-CH FET drive here
GPOD	21	NCH FET open-drain output
PMS	22	Determines CHG output state on POR
LEDOUT	24	3.3-V output for LED display power supply
TOUT	25	Provides thermistor bias current
WDI	26	Digital input that provides the timing clock for the OC and SC delays and also acts as the watchdog clock.
SCLK	28	Open-drain serial interface clock with internal 10-k $\Omega$ pullup to $V_{REG}$
SDATA	29	Open-drain bidirectional serial interface data with internal 10-k $\Omega$ pullup to $V_{REG}$
XALERT	30	Open-drain output used to indicate status register changes. With internal 100-k $\Omega$ pullup to $V_{REG}$
NC	15,18,27	Not electrically connected to the IC

FUNCTIONAL BLOCK DIAGRAM



### SAFETY STATE DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		bq29330	UNIT
Supply voltage range	(VCC, BAT)	−0.3 to 34	V
Input voltage range	(VC1, VC2, VC3, VC4, PACK, PMS)	−0.3 to 34	
	(VC5)	−0.3 to 1.0	
	(SRP, SRN)	−1.0 to 1.0	
	(VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to VC5)	−0.3 to 8.5	
	(WDI, SCLK, SDATA)	−0.3 to 8.5	
Output voltage range	(DSG,CHG)	−0.3 to BAT	
	(ZVCHG)	−0.3 to 34	
	(GPOD)	−0.3 to 34	
	(TOUT, SDATA, CELL, XALERT, XRST, LEDOUT)	−0.3 to 7	
	(CELL+)	−0.3 to 7	
Current for cell balancing		10	mA
Storage temperature range, T <sub>stg</sub>		−65 to 150	°C
Lead temperature (soldering, 10 s)		300	

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground of this device except VCn-VC(n+1), where n=1, 2, 3, 4 cell voltage.

### RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage ( VCC,BAT)			4.5		25	V
V <sub>I(STARTUP)</sub>	Start up voltage (VCC,BAT)		5.5			V
V <sub>I</sub>	Input voltage range	VC1, VC2, VC3, VC4	0		VDD	V
		VC5	0		0.5	
		SRP, SRN	−0.5		0.5	
		VCn – VC(n+1), (n=1, 2, 3, 4 )	0		5.0	
		PACK, PMS			25	
V <sub>IH</sub>	Logic level input voltage	SCLK, SDATA, WDI	0.8xREG		REG	V
V <sub>IL</sub>			0		0.2xREG	
V <sub>O</sub>	Output voltage	GPOD			25	V
V <sub>O</sub>	Output voltage range	XALERT, SDATA, XRST			REG	V
		CELL+, CELL−		0.975		
	External 2.5V REG capacitor	C <sub>REG</sub>	1.0			μF
	External LEDOUT capacitor	C <sub>LED</sub>	2.2			μF
	Extend CELL output capacitor	C <sub>CELL</sub>		0.1		μF
	IOL	GPOD			1	mA
	RPACK			1		kΩ
	Input frequency	WDI		32.768		kHz
	WDI high time		2			μs
T <sub>A</sub>	Operating temperature		−25		85	°C
	Functional temperature		−40		110	°C

**ELECTRICAL CHARACTERISTICS**

<b>SUPPLY CURRENT, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math> (unless otherwise noted)</b>								
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT	
$I_{CC1}$ Supply Current 1	No load at REG, LEDOUT, TOUT, XALERT, SCLK, SDATA, ZVCHG= off, WDI = 32 kHz VMEN = on, VC5 = VC4 = VC3 = VC2 = VC1 = 0 V select VC5 = VC4 = 0 V			$T_A = 25^\circ\text{C}$	140	190	$\mu\text{A}$	
				$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$		220	$\mu\text{A}$	
$I_{CC2}$ Supply Current 2	No load at REG, LEDOUT, TOUT, XALERT, SCLK, SDATA. ZVCHG = off, WDI = 32 kHz, VMEN = off			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	105	185	$\mu\text{A}$	
$I_{(SLEEP)}$ Sleep current	CHG, DSG and ZVCHG = off, REG = on, VMEN = off, WDI no clock, SLEEP = 1			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	30	50	$\mu\text{A}$	
$I_{(SHUTDOWN)}$ Shutdown mode	CHG, DSG and ZVCHG = off, REG = off, VMEN = off, WDI no clock, VPACK = 0 V, VC1 = VC2 = VC3 = VC4 = 3.5 V			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	0.1	1	$\mu\text{A}$	
<b>2.5 V LDO, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math>, <math>I_{OUT33} = 0\ \text{mA}</math> (unless otherwise noted)</b>								
$V_{(REG)}$ Regulator output voltage	$4.5\ \text{V} < V_{CC}$ or $BAT \leq 25\ \text{V}$ , $I_{OUT25} \leq 16\ \text{mA}$			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	2.41	2.5	2.59	V
$\Delta V_{(EGTEMP)}$ Regulator output change with temperature	$V_{CC}$ or $BAT = 14\ \text{V}$ , $I_{OUT25} = 2\ \text{mA}$			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	$\pm 0.2\%$			
$\Delta V_{(REGLINE)}$ Line regulation	$5.4\ \text{V} \leq V_{CC}$ or $BAT \leq 25\ \text{V}$ , $I_{OUT25} = 2\ \text{mA}$			$T_A = 25^\circ\text{C}$	3	10	mV	
$\Delta V_{(REGLOAD)}$ Load regulation	$V_{CC}$ or $BAT = 14\ \text{V}$ , $0.2\ \text{mA} \leq I_{OUT25} \leq 2\ \text{mA}$			$T_A = 25^\circ\text{C}$	7	15	mV	
	$V_{CC}$ or $BAT = 14\ \text{V}$ , $0.2\ \text{mA} \leq I_{OUT25} \leq 16\ \text{mA}$			$T_A = 25^\circ\text{C}$	15	50	mV	
$I_{(REGMAX)}$ Current limit	$V_{CC}$ or $BAT = 14\ \text{V}$ , REG = 2 V			$T_A = 25^\circ\text{C}$	16	75	mA	
	$V_{CC}$ or $BAT = 14\ \text{V}$ , REG = 0 V			$T_A = 25^\circ\text{C}$	5	45		
<b>3.3 V LED, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1.0\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math>, <math>I_{OUT25} = 0\ \text{mA}</math> (unless otherwise noted)</b>								
$V_{O(LED)}$ Regulator output voltage	$4.5\ \text{V} < V_{CC}$ or $BAT \leq 25\ \text{V}$ , $I_{OUT33} \leq 10\ \text{mA}$			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	3	3.3	3.6	V
	$6.5\ \text{V} < V_{CC}$ or $BAT \leq 25\ \text{V}$ , $I_{OUT33} \leq 25\ \text{mA}$				3	3.3	3.6	
$\Delta V_{(LEDEMP)}$ Regulator output change with temperature	$V_{CC}$ or $BAT = 14\ \text{V}$ , $I_{OUT33} = 2\ \text{mA}$			$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	$\pm 0.2\%$			
$\Delta V_{(LEDLINE)}$ Line regulation	$5.4\ \text{V} \leq V_{CC}$ or $BAT \leq 25\ \text{V}$ , $I_{OUT33} = 2\ \text{mA}$			$T_A = 25^\circ\text{C}$	3	10	mV	
$\Delta V_{(LEDLOAD)}$ Load regulation	$V_{CC}$ or $BAT = 14\ \text{V}$ , $0.2\ \text{mA} \leq I_{OUT33} \leq 2\ \text{mA}$			$T_A = 25^\circ\text{C}$	7	15	mV	
	$V_{CC}$ or $BAT = 14\ \text{V}$ , $0.2\ \text{mA} \leq I_{OUT33} \leq 25\ \text{mA}$				40	100		
$I_{(LEDMAX)}$ Current limit	$V_{CC}$ or $BAT = 14\ \text{V}$ , REG = 3 V			$T_A = 25^\circ\text{C}$	25	125	mA	
	$V_{CC}$ or $BAT = 14\ \text{V}$ , REG = 0 V				12	50		
<b>THERMISTOR DRIVE, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math> (unless otherwise noted)</b>								
V <sub>TOUT</sub>	$I_{TOUT} = 0\ \text{mA}$				2.4	2.6	V	
$R_{DS(ON)}$	TOUT Pass-element series resistance	$I_{TOUT} = -1\ \text{mA}$ at TOUT pin, $R_{DS(ON)} = [V_{REG} - V_{OUT}(TOUT)] / 1\ \text{mA}$		$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	50	100	$\Omega$	
<b>SHUTDOWN WAKE, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math> (unless otherwise noted)</b>								
$V_{STARTUP}$	PACK Exit shutdown threshold	$V_{CC}$ or $BAT = 14\ \text{V}$ , PACK = 1.4 V				1	$\mu\text{A}$	
<b>POR, <math>T_A = 25^\circ\text{C}</math>, <math>C_{REG} = 1\ \mu\text{F}</math>, <math>C_L = 2.2\ \mu\text{F}</math>, <math>V_{CC}</math> or <math>BAT = 14\ \text{V}</math> (unless otherwise noted)</b>								
$V_{POR}$	VREGTH-				-3%	1.8	3%	V
	Hysteresis ( $V_{regth+} - V_{regth-}$ )				50	150	250	mV

**ELECTRICAL CHARACTERISTICS (Continued)**

CELL VOLTAGE MONITOR, T <sub>A</sub> = 25°C, C <sub>REG</sub> = 1 μF, C <sub>L</sub> = 2.2 μF, VCC or BAT = 14 V (unless otherwise noted)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(CELLOUT)</sub>	CELL output	V <sub>Cn</sub> - V <sub>Cn+1</sub> = 0 V, 8 V ≤ VDD ≤ 25 V	0.950	0.975	1	V
REF		V <sub>Cn</sub> - V <sub>Cn+1</sub> = 4.5 V, 8 V ≤ VDD ≤ 25 V	0.275	0.3	0.325	V
PACK		Mode <sup>(1)</sup> , 8 V ≤ VDD ≤ 25 V	-1%	0.975	1%	V
BAT		Mode [Register Address = 0x03, b1(PACK) = 1, b0(VMEN) = 1]	-2%	PACK/18	2%	V
CMRR		Common mode rejection	CELL max to CELL min	40		
V <sub>(CELLSLEW)</sub>	CELL output rise	Min to Max 10% to 90%	9			ms
K	CELL scale factor	K = {CELL output (VC5 = 0 V, VC4 = 4.5 V) -CELL output (VC5 = VC4 = 0 V)} / 4.5	0.147	0.150	0.153	
		K = {CELL output (VC2 = 13.5 V, VC1 = 18 V) -CELL output (VC2 = VC1 = 13.5 V)} / 4.5	0.147	0.150	0.153	
I <sub>(VCELLOUT)</sub>	Drive current	V <sub>Cn</sub> - V <sub>Cn+1</sub> = 0 V, V <sub>cell</sub> = 0 V, T <sub>A</sub> = -40° to 110°	12	18		μA
V <sub>(ICR)</sub>	CELL output offset error	CELL output (VC2 = 18 V, VC1 = 18 V) -CELL output (VC2 = VC1 = 0 V)		-1		mV
R <sub>(BAL)</sub>	Cell balance internal resistance	R <sub>DS(ON)</sub> for internal FET switch at V <sub>DS</sub> = 2 V	-50%	400	50%	Ω

(1) Register Address = 0x04, b2(CAL0) = b3(CAL1) = 1, Register Address = 0x03, b0(VMEN) = 1

CURRENT PROTECTION DETECTION, T <sub>A</sub> = 25°C, C <sub>REG</sub> = 1 μF, C <sub>L</sub> = 2.2 μF, VCC or BAT = 14 V (unless otherwise noted)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(OLT)</sub>	OL detection threshold voltage range, typical <sup>(1)</sup>	RSNS = 0	-50		-205	mV
		RSNS = 1	-25		-102.5	
ΔV <sub>(OLT)</sub>	OL detection threshold voltage program step	RSNS = 0		-5		mV
		RSNS = 1		-2.5		
V <sub>(SCCT)</sub>	SCC detection threshold voltage range, typical <sup>(2)</sup>	RSNS = 0	100		475	mV
		RSNS = 1	50		237.5	
ΔV <sub>(SCCT)</sub>	SCC detection threshold voltage program step	RSNS = 0		25		mV
		RSNS = 1		12.5		
V <sub>(SCDT)</sub>	SCD detection threshold voltage range, typical <sup>(3)</sup>	RSNS = 0	-100		-475	mV
		RSNS = 1	-50		-237.5	
ΔV <sub>(SCDT)</sub>	SCD detection threshold voltage program step	RSNS = 0		-25		mV
		RSNS = 1		-12.5		
V <sub>(OL(acr))</sub>	OL detection threshold voltage accuracy <sup>(1)</sup>	V <sub>OL</sub> = -25 mV (typ)	-15	-25	-35	mV
		V <sub>OL</sub> = -100 mV (typ) (RSNS = 0,1)	-90	-100	-110	
		V <sub>OL</sub> = -205 mV (typ)	-185	-205	-225	
V <sub>(SCC(acr))</sub>	SCC detection threshold voltage accuracy <sup>(2)</sup>	V <sub>SCC</sub> = 50 mV (typ)	30	50	70	mV
		V <sub>SCC</sub> = 200 mV (typ) (RSNS = 0,1)	180	200	220	
		V <sub>SCC</sub> = 475 mV (typ)	428	475	523	
V <sub>(SCD(acr))</sub>	SCD detection threshold voltage accuracy <sup>(3)</sup>	V <sub>SCD</sub> = -50 mV (typ)	-30	-50	-70	mV
		V <sub>SCD</sub> = -200 mV (typ) (RSNS = 0,1)	-180	-200	-220	
		V <sub>SCD</sub> = -475 mV (typ)	-426	-475	-523	

(1) See OLV register for setting detection threshold

(2) See SCC register for setting detection threshold

(3) See SCD register for setting detection threshold



**ELECTRICAL CHARACTERISTICS (Continued)**

FET DRIVE CIRCUIT, $T_A = 25^\circ\text{C}$ , $C_{REG} = 1\ \mu\text{F}$ , $C_L = 2.2\ \mu\text{F}$ , $V_{CC}$ or $BAT = 14\ \text{V}$ (unless otherwise noted)								
PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT	
$V_{O(FETON)}$ Output voltage, charge, and discharge FETs on	$V_{O(FETOND)} = V_{(DSG)} - V_{\text{pack}}$ VGS connect 10 M $\Omega$	$T_A = 25^\circ\text{C}$		7.5	12	15.5	V	
		$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$		8	12	16		
	$V_{O(FETONC)} = V_{(CHG)} - V_{\text{BAT}}$ VGS connect 10 M $\Omega$	$T_A = 25^\circ\text{C}$		7.5	12	15.5	V	
		$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$		8	12	16		
$V_{(ZCHG)}$ ZVCHG clamp voltage	BAT = 4.5 V			3.3	3.5	3.7	V	
$V_{O(FETOF)}$ Output voltage, charge, and discharge FETs off	VFETOND = VDSG –Vpack						0.2	V
	VFETONC = VCHG –VBAT						0.2	
$t_r$ Rise time	$C_L = 4700\ \text{pF}$	$V_{(CHG)}$ : Vpack $\geq$ Vpack+4 V		400	1000		$\mu\text{s}$	
		$V_{(DSG)}$ : VBAT $\geq$ VBAT+4 V		400	1000			
$t_f$ Fall time	$C_L = 4700\ \text{pF}$	$V_{(CHG)}$ : Vpack+VCHG (FETON) $\geq$ pack +1 V		40	200		$\mu\text{s}$	
		$V_{(DSG)}$ : VC1+ VDSG (FETON) $\geq$ VC1 +1 V		40	200			
LOGIC, $T_A = 25^\circ\text{C}$ , $C_{REG} = 1\ \mu\text{F}$ , $C_L = 2.2\ \mu\text{F}$ , $V_{CC}$ or $BAT = 14\ \text{V}$ (unless otherwise noted)								
$R_{(PUP)}$ Internal pullup resistance	XALERT		$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$	60	100	200	k $\Omega$	
	SDATA, SCLK			6	10	20		
	XRST			1	3	6		
$V_{OL}$ Low Logic level output voltage	XALERT		$T_A = -40^\circ\text{C}$ to $110^\circ\text{C}$				0.2	V
	SDATA, $I_{OUT} = 200\ \mu\text{A}$						0.4	
	GPOD, $I_{OUT} = 50\ \mu\text{A}$						0.6	
	VCC or BAT = 7 V, VREG = 1.5 V, XRST, $I_{OUT} = 200\ \mu\text{A}$						0.4	
$V_{IH}$ SCLK (hysteresis input)	Hysteresis			450			mV	

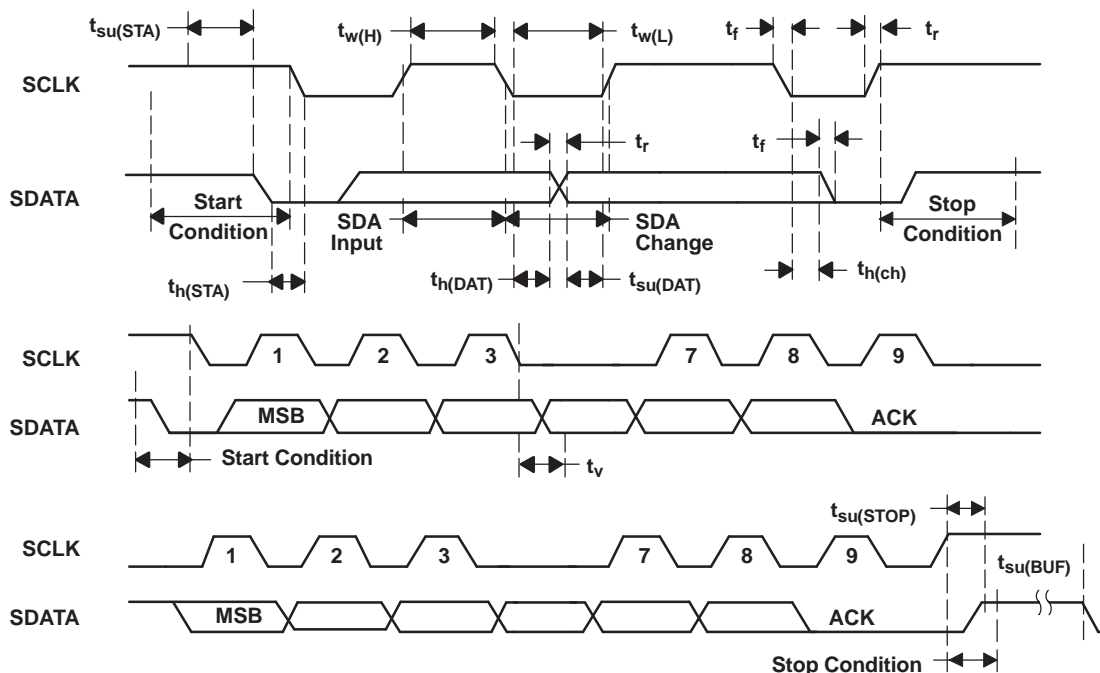
**AC ELECTRICAL CHARACTERISTICS**
 $T_A = 25^\circ\text{C}$ ,  $C_{REG} = 1\ \mu\text{F}$ ,  $C_L = 2.2\ \mu\text{F}$ ,  $V_{CC}$  or  $BAT = 14\ \text{V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{WDTINT}$ WDT start up detect time		250	500	1000	ms
$t_{WDWT}$ WDT detect time		50	100	150	$\mu\text{s}$
$t_{RST}$ XRST Active high time		100	250	560	$\mu\text{s}$

### AC TIMING REQUIREMENTS (I<sup>2</sup>C compatible serial interface)

T<sub>A</sub> = 25°C, C<sub>REG</sub> = 1 μF, VCC or BAT = 14 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
t <sub>r</sub>	SCLK, SDATA rise time		1000	ns
t <sub>f</sub>	SCLK, SDATA fall time		300	ns
t <sub>w(H)</sub>	SCLK pulse width high	4		μs
t <sub>w(L)</sub>	SCLK pulse width low	4.7		μs
t <sub>su(STA)</sub>	Setup time for start condition	4.7		μs
t <sub>h(STA)</sub>	Start condition hold time after which first clock pulse is generated	4		μs
t <sub>su(DAT)</sub>	Data setup time	250		ns
t <sub>h(DAT)</sub>	Data hold time	0		μs
t <sub>su(STOP)</sub>	Setup time for Stop condition	4		μs
t <sub>su(BUF)</sub>	Time the bus must be free before new transmission can start	4.7		μs
t <sub>v</sub>	Clock low to data out valid		900	ns
t <sub>h(CH)</sub>	Data out hold time after clock low	10		ns
f <sub>SCL</sub>	Clock frequency	0	400	kHz



## FUNCTIONAL DESCRIPTION

### LOW DROP OUTPUT REGULATOR (LEDOUT)

The inputs for this regulator can be derived from the VCC or BAT terminals. The output is a fixed voltage of typically 3.3 V with the minimum output capacitance for stable operation of 2.2  $\mu\text{F}$  and is also internally current limited. This output is used for LED drive, power supply source for REG (2.5 V) and bq29330 internal circuit. During normal operation, the regulator limits output current to typically 50 mA. Until the internal regulator circuit is correctly powered, the DSG and CHG FET drives are low (FETs = OFF).

### LOW DROP OUTPUT REGULATOR (REG)

The inputs for this regulator can be derived from the LED (3.3 V). The output is typically 2.5 V with the minimum output capacitance for stable operation of 1  $\mu\text{F}$  and is also internally current limited. During normal operation, the regulator limits output current to typically 50 mA.

### INITIALIZATION

From a shutdown situation, the bq29330 requires a voltage greater than start-up voltage ( $V_{\text{STARTUP}}$ ) applied to the PACK pin to enable its integrated regulator and provide the regulators power source. Once the REG output is stable, the power source of the regulator is switched to VCC.

After the regulator has started, it then continues to operate through the VCC input. If the VCC input is below the minimum operating range, then the bq29330 will not operate if the supply to the PACK input is removed.

If the voltage at VLED falls below about 2.3 V, the internal circuit turns off the FETs and disables all controllable functions including the REG, LEDOUT, and TOUT outputs.

The initial state of the CHG and DSG FET drive is low (OFF) and the ZVCHG FET drive is low (ON).

### OVERLOAD DETECTION

The overload detection is used to detect abnormal currents in the discharge direction. This feature is used to protect the pass FETs, cells, and any other inline components from excessive discharge current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The overload sense voltage is set in the OLV register, and delay time is set in the OLD register. The thresholds can be individually programmed from 50 mV to 205 mV in 5-mV steps with the default being 50 mV.

If the RSNS bit in the FUNCTION\_CTL register is set to 1, then the voltage threshold, programmable step size, and hysteresis is divided by 2.

### SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE DETECTION

The short current circuit in charge and short circuit in discharge detections are used to detect severe abnormal current in the charge and discharge directions, respectively. This safety feature is used to protect the pass FETs, cells, and any other inline components from excessive current conditions. The detection circuit also incorporates a blanking delay before driving the control for the pass FETs to the OFF state. The short circuit in charge threshold and delay time are set in the SCC register. The short circuit in discharge threshold and delay time are set in the SCD register. The short-circuit thresholds can be programmed from 100 mV to 475 mV in 25-mV steps.

If the RSNS bit in the FUNCTION\_CTL register is set to 1, then the voltage threshold, programmable step size, and hysteresis is divided by 2.

### OVERLOAD, SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE DELAY

The overload delay (default = 1 ms) allows the system to momentarily accept a high current condition without disconnecting the supply to the load. The delay time can be increased via the OLD register which can be programmed for a range of 1 ms to 31 ms with 2-ms steps.

The short circuit in charge and short circuit in discharge delays (default = 0  $\mu\text{s}$ ) are programmable in the SCC and SCD registers, respectively. These registers can be programmed from 0  $\mu\text{s}$  to 915  $\mu\text{s}$  with 61- $\mu\text{s}$  steps.

## OVERLOAD, SHORT CIRCUIT IN CHARGE AND SHORT CIRCUIT IN DISCHARGE RESPONSE

When an overload, short circuit in charge, or short circuit in discharge fault is detected, the FETs are turned off. The STATUS (b0...b3) register reports the details of overload, short circuit in charge or short-circuit discharge. The respective STATUS (b0...b3) bits are set to 1 and the XALERT output is triggered. This condition is latched until the STATE\_CONTROL (b7) is set and then reset. If a FET is turned on after resetting STATE\_CONTROL (b0) and the error condition is still present on the system, then the device again enters the protection response state.

## 2-, 3-, or 4-CELL CONFIGURATION

In a 2-cell configuration, VC1 and VC2 are shorted to VC3. In a 3-cell configuration, VC1 is shorted to VC2.

## CELL VOLTAGE

The cell voltage is translated to allow a system host to measure individual series elements of the battery. The series element voltage is translated to a GND-based voltage equal to  $0.15 \pm 0.003$  of the series element voltage. This provides a range from 0 to 4.5 V. The translation output is presented between CELL+ and CELL– pins of the bq29330 and is inversely proportional to the input using the following equation.

$$\text{Where, } V_{(\text{CELLOUT})} = -K \times V_{(\text{CELLIN})} + 0.975 \text{ (V)}$$

Programming CELL\_SEL (b1, b0) selects the individual series element. The CELL\_SEL (b3, b2) selects the voltage monitor mode, cell monitor, offset, etc.

## CALIBRATION OF CELL VOLTAGE MONITOR AMPLIFIER GAIN

The cell voltage monitor amplifier has an offset, and to increase accuracy, this can be calibrated.

The following procedure shows how to measure and calculate the offset as an example.

### Step 1

Set CAL1=1, CAL0=1, VMEN=1.

VREF is trimmed to 0.975 V within  $\pm 1\%$ ; measuring VREF eliminates its error.

Measure internal reference voltage VREF from VCELL directly.

$$V_{\text{REF}} = \text{measured reference voltage}$$

### Step 2

Set CAL1=0, CAL0=1, CELL1=0, CELL0=0, VMEN=1.

The output voltage includes the offset and represented by:

$$V_{\text{OUT(4-5)}} = V_{\text{REF}} + (1 + K) \times V_{\text{OS}} \text{ (V)}$$

Where K = CELL Scaling Factor

$V_{\text{OS}}$  = Offset voltage at input of the internal operational amplifier

### Step 3

Set CAL1=1, CAL0=0, CELL1=0, CELL0=0, VMEN=1.

Measure scaled REF voltage through VCELL amplifier.

The output voltage includes the scale factor error and offset and is represented by:

$$V_{(\text{OUTR})} = V_{\text{REF}} + (1 + K) \times V_{\text{OS}} - K \times V_{\text{REF}} \text{ (V)}$$

### Step 4

Calculate  $(V_{\text{OUT(4-5)}} - V_{(\text{OUTR})}) / V_{\text{REF}}$ .

The result is the actual scaling factor,  $K_{\text{ACT}}$  and is represented by:

$$K_{\text{ACT}} = (V_{\text{OUT(4-5)}} - V_{(\text{OUTR})}) / V_{\text{REF}} = (V_{\text{REF}} + (1 + K) \times V_{\text{OS}}) - (V_{\text{REF}} + (1 + K) \times V_{\text{OS}} - K \times V_{\text{REF}}) / V_{\text{REF}} = K \times V_{\text{REF}} / V_{\text{REF}} = K$$

### Step 5

Calculate the actual offset value where:

$$V_{OS(ACT)} = (V_{(OUTR)} - V_{REF}) / (1 + K_{ACT})$$

### Step 6

Calibrated cell voltage is calculated by:

$$VC_n - VC_{(n+1)} = \{ V_{REF} + (1 + K_{ACT}) \times V_{OS(ACT)} - V_{(CELLOUT)} \} / K_{ACT} = \{ V_{OUT(4-5)} - V_{(CELLOUT)} \} / K_{ACT}$$

To seek greater accuracy, it is better to measure  $V_{OS(ACT)}$  for each cell voltage.

Set CAL1=0, CAL0=0, CELL1=0, CELL0=1, VMEN=1.

Set CAL1=0, CAL0=0, CELL1=1, CELL0=0, VMEN=1.

Set CAL1=0, CAL0=0, CELL1=1, CELL0=1, VMEN=1.

Measure  $V_{OUT(3-4)}$ ,  $V_{OUT(2-3)}$ ,  $V_{OUT(1-2)}$ ,

$$VC4 - VC5 = \{ V_{OUT(4-5)} - V_{(CELLOUT)} \} / K_{ACT}$$

$$VC3 - VC4 = \{ V_{OUT(3-4)} - V_{(CELLOUT)} \} / K_{ACT}$$

$$VC2 - VC3 = \{ V_{OUT(2-3)} - V_{(CELLOUT)} \} / K_{ACT}$$

$$VC1 - VC2 = \{ V_{OUT(1-2)} - V_{(CELLOUT)} \} / K_{ACT}$$

## BATTERY PACK AND BATTERY STACK MEASUREMENTS

The PACK (battery pack) and VC1 (battery stack) inputs can be translated to the CELL+, CELL– outputs of the bq29330 through control bits in the FUNCTION\_CONTROL register. If PACK is set, then the input at the PACK is divided by 18 and presented at the CELL+, CELL– outputs. If the BAT bit is set, then the input to VC1 is divided by 18 and presented at the CELL+, CELL– outputs. If setting both bits at the same time, VC1 is presented at the CELL+, CELL– outputs.

## CELL BALANCE CONTROL

The cell balance control allows a small bypass path to be controlled for any one series element. The purpose of this bypass path is to reduce the current into any one cell during charging to bring the series elements to the same voltage. Series resistors placed between the input pins and the positive series element nodes control the bypass current value. Individual series element selection is made using bits 4 through 7 of CELL\_SEL register.

Series input resistors between 500  $\Omega$  and 1 k $\Omega$  are recommended for effective cell balancing.

## XALERT (XALERT)

XALERT is driven Low, when WDF, OL, SCC, or SCD OC are detected. To clear XALERT, toggle (from 0, set to 1, then reset to 0) STATE\_CONTROL, LTCLR (bit 7), then read the STATUS register.

## THERMISTOR DRIVE CIRCUIT (TOUT)

The TOUT pin can be enabled to drive a thermistor from REG. The typical thermistor resistance is 10 k $\Omega$  at 25°C. The default state for this is OFF to conserve power. The maximum output impedance is 100  $\Omega$ . TOUT is enabled in FUNCTION\_CONTROL register (bit 3).

## GENERAL PURPOSE OPEN DRAIN DRIVE CIRCUIT (GPOD)

The General Purpose Open Drain output has 1-mA current source drive with a maximum output voltage of 25 V. The OD output is enabled or disabled by OUTPUT\_CONTROL register (bit 4) and has a default state of OFF.

### LATCH CLEAR (LTCLR)

When a protection fault occurs, the state is latched. To clear the fault flag, toggle (from 0, set 1, then reset to 0) the LTCLR bit in the STATE\_CONTROL register (bit 7). The OL, SCC, SCD, and WDF bits are unlatched by this function. The FETs can now be controlled by programming the OUTPUT\_CONTROL register, and the XALERT output can be cleared by reading the STATUS register.

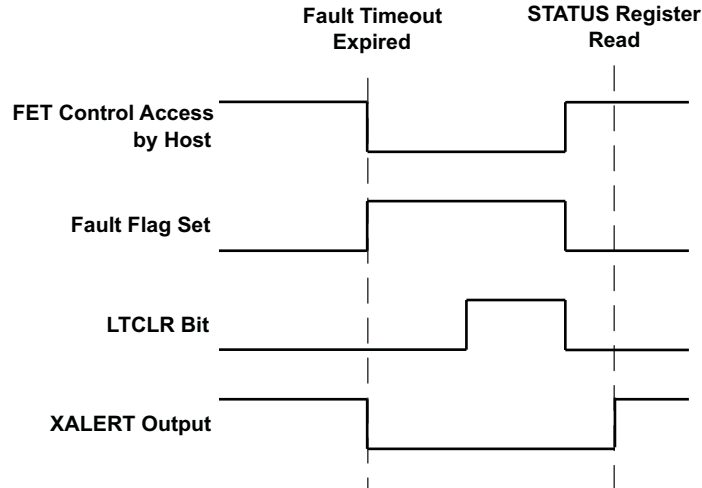


Figure 1. LTCLR and XLAERT Clear Timing

### POR and WATCHDOG RESET (XRST)

The XRST pin is activated by activation of the REG output. This holds the host in reset for the duration of the  $t_{RST}$  period, allowing the VREG to stabilize before the host is released from reset. When the regulator power is down, XRST is active below the regulator's voltage of 1.8 V. Also, when a watchdog fault is detected, the XRST is also activated to ensure a valid reset of the battery management host.

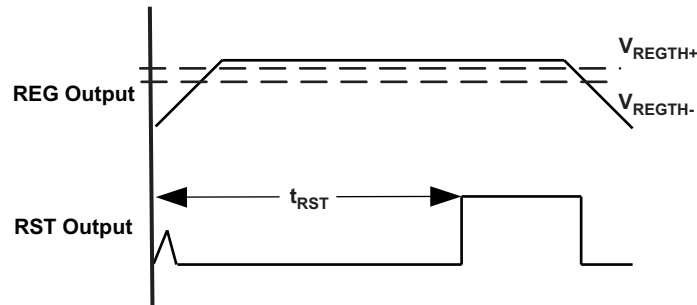


Figure 2. XRST Timing Chart – Power Up and Power Down

### WATCHDOG INPUT (WDI)

The WDI input is required as a time base for delay timing when determining fault detection and is used as part of the system watchdog.

Initially, the watchdog monitors the host oscillator start-up; if there is no response from the host within  $t_{WDINT}$  of  $t_{RST}$  expiring, then the bq29330 turns CHG, DSG, and ZVCHG FETs off. It then activates the XRST output in an attempt to reset the host.

Once the watchdog has been started during this wake-up period, it monitors the host for an oscillation stop condition which is defined as a period of  $t_{WDWT}$  where no clock input is received. If an oscillator stop condition is identified, then the watchdog turns the CHG, DSG, and ZVCHG FETs off. The bq29330 then activates the XRST output in an attempt to reset the host.

If the host clock oscillation is started after the reset, the bq29330 still has the WDF flag set until it is cleared. See the LTCLR section for further details on clearing the fault flags.

During Sleep mode, the watchdog function is not disabled.

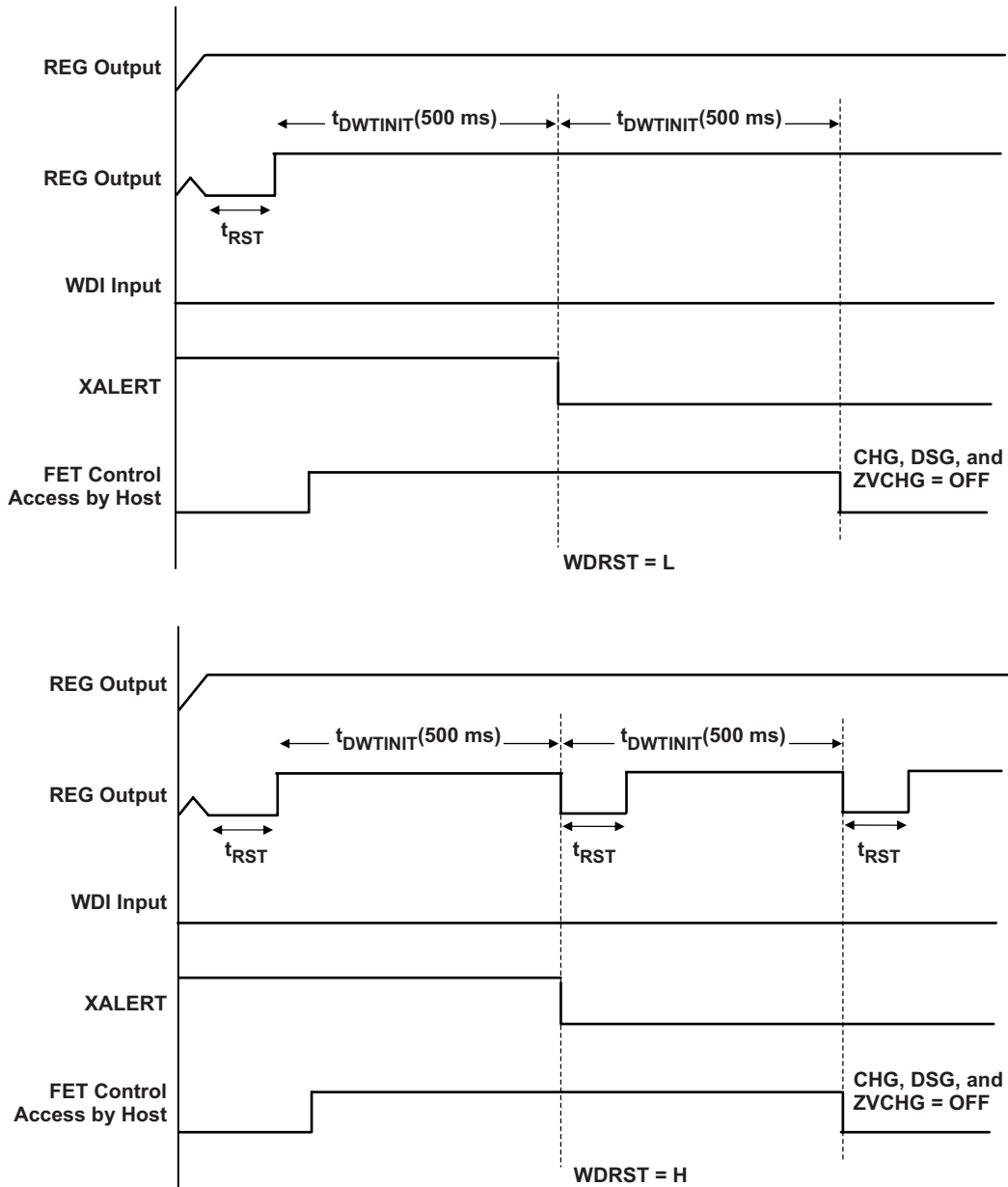


Figure 3. Watchdog Timing Chart – WDI Fault at Start-up

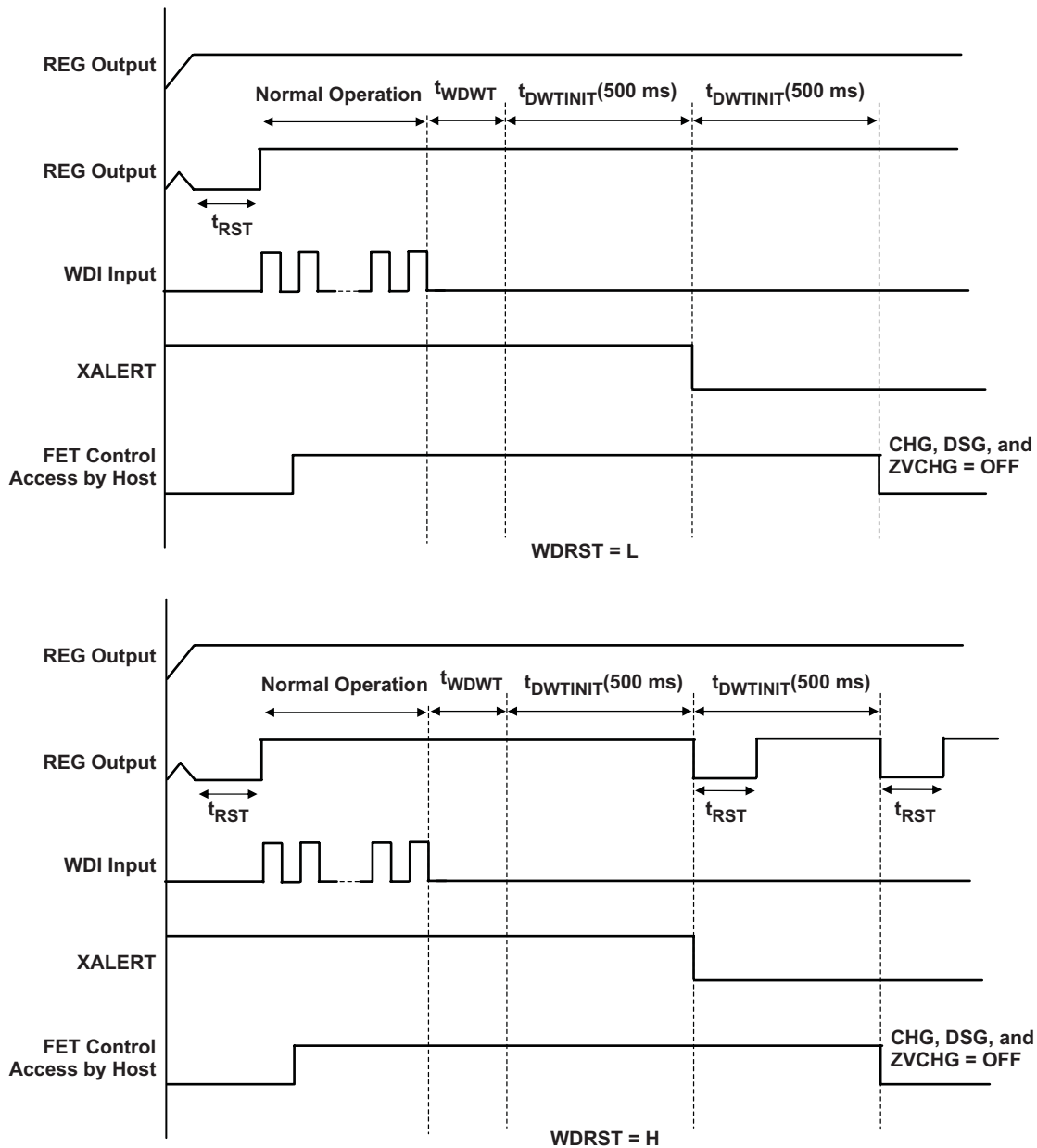


Figure 4. Watchdog Timing Chart – WDI Fault After Startup

### DSG and CHG NCH FET DRIVER CONTROL

The bq29330 drives either the DSG or CHG FET off if an OL, SCC, or SCD safety threshold is breached depending on the current direction. The host can force any FET on or off only if the bq29330 integrated protection control allows.

The default-state of the FET drive is off. A host can control the FET drive by programming OUTPUT\_CONTROL (b2..b0), where b0 is used to control the discharge FET, b1 is used to control the charge FET, and b2 is used to control the ZVCHG FET. These controls are only valid when not in the initialized state. The CHG drive FET can be powered by PACK and the DSG FET can be powered by BAT.

When the bq29330 powers down, the NCH FET drivers power down to GND causing the FETs to turn off.



## PRECHARGE AND 0 V CHARGING

The bq29330 supports both a charger that has a precharge mode and one that does not. The bq29330 also supports charging even when the battery falls to 0 V. In order to charge, the charge FET (CHG) must be turned on to create a current path. When the  $V_{BAT}$  is  $\sim 0$  V, the  $V_{(PACK)}$  is as low as the battery voltage. In this case, the supply voltage for the device is too low to operate.

## POWER MODES

The bq29330 has three power modes, normal, sleep, and ship. The following table outlines the operational functions during these power modes.

**Table 1. Outlines the Operational Functions**

POWER MODE	TO ENTER POWER MODE	TO EXIT POWER MODE	MODE DESCRIPTION
Normal	STATE_CONTROL, SLEEP( b0) = 0 and STATE_CONTROL, SHIP ( b1) = 0		The battery is in normal operation with protection, power management and battery monitoring functions available and operating.  The supply current of this mode varies as the host can enable and disable various power management features.
Sleep	STATE_CONTROL, SLEEP( b0) = 1 and STATE_CONTROL, SHIP ( b1) = 0	STATE_CONTROL, SLEEP( b0) = 0	CHG, DSG, and ZVCHG OFF, OL, SCC, and SCD function is disabled.  Cell AMP, GPOD , CELL BAL, and WDF is not disabled
Ship	STATE_CONTROL, SHIP ( b1) = 1 and supply at the PACK < $V_{WAKE}$	Supply voltage to PACK Supply	The bq29330 is completely shut down as in the sleep mode. In addition, the REG output is disabled, I <sup>2</sup> C interface is powered down, and memory is not valid.

## VOLTAGE BASED EXIT FROM SHUTDOWN

If a voltage greater than  $V_{STARTUP}$  is applied to the PACK pin, then the bq29330 exits shutdown and enters normal mode.

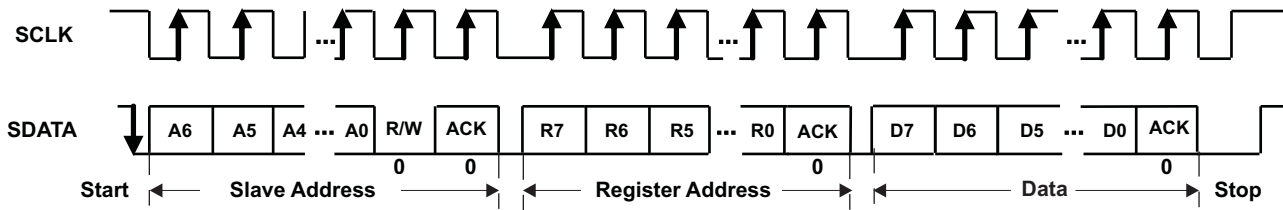
## COMMUNICATIONS

The I<sup>2</sup>C-compatible serial communications provides read and write access to the bq29330 data area. The data is clocked via separate data (SDATA) and clock (SCLK) pins. The bq29330 acts as a slave device and does not generate clock pulses. Communication to the bq29330 can be provided from GPIO pins or an I<sup>2</sup>C supporting port of a host system controller. The slave address for the bq29330 is 7 bits, and the value is 0100 000 (0x20).

	(MSB) I2C Address +R/W bit (LSB)						
	(MSB) I2C Address (0x20) (LSB)						
Write	0	1	0	0	0	0	0
Read							1

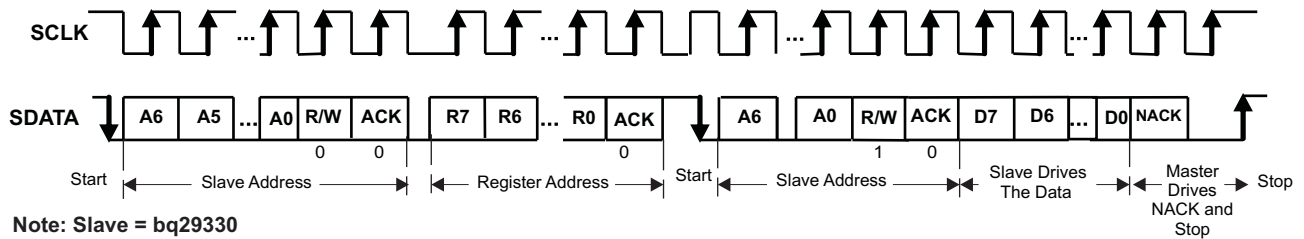
The bq29330 does NOT have the following functions compatible with the I<sup>2</sup>C specification.

- The bq29330 is always regarded as a slave.
- The bq29330 does not support the General Code of the I<sup>2</sup>C specification, and therefore will not return an ACK but may return a NACK.
- The bq29330 does not support the Address Auto Increment, which allows continuous reading and writing.
- The bq29330 will allow data to be written or read from the same location without re-sending the location address.



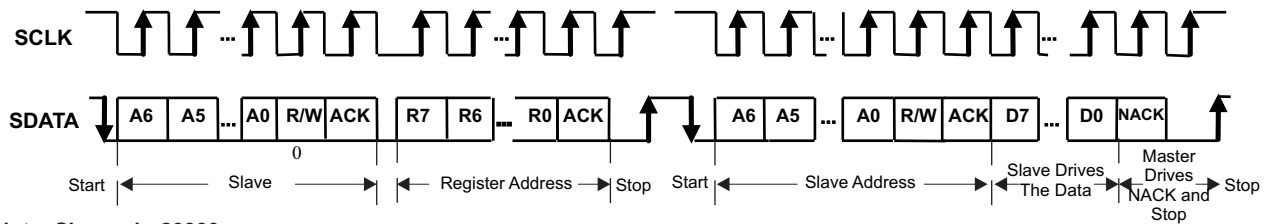
Note: Slave = bq29330

Figure 5. I<sup>2</sup>C-Bus Write to bq29330



Note: Slave = bq29330

Figure 6. I<sup>2</sup>C-Bus Read from bq29330: Protocol A



Note: Slave = bq29330

Figure 7. I<sup>2</sup>C-Bus Read from bq29330: Protocol B

**REGISTER MAP**

The bq29330 has nine addressable registers. These registers provide status, control, and configuration information for the battery protection system.

NAME	ADDR	TYPE	DESCRIPTION
STATUS	0x00	R	Status register
OUTPUT_CONTROL	0x01	R/W	Output pin control from system host and external pin status
STATE_CONTROL	0x02	R/W	State control
FUNCTION_CONTROL	0x03	R/W	Function control
CELL_SEL	0x04	R/W	Battery cell select for cell translation and balance bypass and select mode for calibration
OLV	0x05	R/W	Overload voltage threshold
OLD	0x06	R/W	Overload delay time
SCC	0x07	R/W	Short circuit in charge current threshold voltage and delay
SCD	0x08	R/W	Short circuit in discharge current threshold voltage and delay

NAME	ADDR	TYPE	BIT MAP							
			B7	B6	B5	B4	B3	B2	B1	B0
STATUS	0x00	R	0	0	0	ZV	WDF	OL	SCC	SCD
OUTPUT_CONTROL	0x01	R/W	0	0	PMS_CHG	GPOD	XZV	CHG	DSG	LTCLR
STATE_CONTROL	0x02	R/W	0	0	0	RSNS	WDRST	WDDIS	SHIP	SLEEP
FUNCTION_CONTROL	0x03	R/W	0	0	0	0	TOUT	BAT	PACK	VMEN
CELL_SEL	0x04	R/W	CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0
OLV	0x05	R/W	0	0	0	OLV4	OLV3	OLV2	OLV1	OLV0
OLD	0x06	R/W	0	0	0	0	OLD3	OLD2	OLD1	OLD0
SCC	0x07	R/W	SCCD3	SCCD2	SCCD1	SCCD0	SCCV3	SCCV2	SCCV1	SCCV0
SCD	0x08	R/W	SCDD3	SCDD2	SCDD1	SCDD0	SCDV3	SCDV2	SCDV1	SCDV0

**STATUS: Status register**

STATUS REGISTER (0x00)							
7	6	5	4	3	2	1	0
0	0	0	ZV	WDF	OL	SCC	SCD

The STATUS register provides information about the current state of the bq29330.

STATUS b0 (SCD): This bit indicates a short circuit in discharge condition.

0 = Voltage below the short circuit in discharge threshold (default).

1 = Voltage greater than or equal to the short circuit in discharge threshold.

STATUS b1 (SCC): This bit indicates a short circuit in charge condition in the charge direction.

0 = Voltage below the short circuit in charge threshold (default).

1 = Voltage greater than or equal to the short circuit in charge threshold.

STATUS b2 (OL): This bit indicates an overload condition.

0 = Voltage less than or equal to the overload threshold (default).

1 = Voltage greater than overload threshold.

STATUS b3 (WDF): This bit indicates a watchdog fault condition has occurred.

0 = 32-kHz oscillation is normal (default).

1 = 32-kHz oscillation stopped or not started, and the watchdog has timed out.

STATUS b4 (ZV): This bit indicates ZVCHG output is clamped.

0 = ZVCHG pin is not clamped (default).

1 = ZVCHG pin is clamped.

STATUS b5, b6, b7: Reserved

**OUTPUT\_CONTROL : Output control register**

OUTPUT_CONTROL REGISTER (0x01)							
7	6	5	4	3	2	1	0
0	0	PMS_CHG	GPOD	XZV	CHG	DSG	LTCLR

The OUTPUT\_CONTROL register controls the outputs of the bq29330 and can show the state of the external pin corresponding to the control.

OUTPUT\_CONTROL b0 (LTCLR): When a fault is latched, this bit releases the fault latch when toggled from 0 to 1 and back to 0 (default =0).

0 = (default)

0->1 ->0 clears the fault latches, allowing STATUS to be cleared on its next read.

OUTPUT\_CONTROL b1 (DSG): This bit controls the external discharge FET.

- 0 = Discharge FET is off and is controlled by the system host (default).
- 1 = Discharge FET is on, and the bq29330 is in normal operating mode.

OUTPUT\_CONTROL b2 (CHG): This bit controls the external charge FET.

- 0 = Charge FET is off, and is controlled by the system host (default).
- 1 = Charge FET is on, and the bq29330 is in normal operating mode.

OUTPUT\_CONTROL b3(ZV): This bit enables or disables the precharge function.

- 0 = ZVCHG FET is on, and is controlled by the system host (default).
- 1 = ZVCHG FET is off, and the bq29330 is in normal operating mode.

OUTPUT\_CONTROL b4 (GPOD): This bit enables or disables the GPOD output.

- 0 = GPOD is high impedance (default).
- 1 = GPOD output is active (GND).

OUTPUT\_CONTROL b5 (PMS\_CHG): This bit enables the CHG output for 0-V charge, when PMS terminal is connected to Pack.

- 0 = CHG FET is off (When PMS = GND, default).
- 1 = CHG FET is on by connecting CHG and PACK terminal. (When PMS = PACK, default)

#### STATE\_CONTROL : State control register

STATE_CONTROL REGISTER (0x02)							
7	6	5	4	3	2	1	0
0	0	0	RSNS	WDRST	WDDIS	SHIP	SLEEP

The STATE\_CTL register controls the outputs of the bq29330 and can be used to clear certain states.

STATE\_CONTROL b0 (SLEEP): This bit is used to enter the sleep power mode.

- 0 = bq29330 exits sleep mode (default).
- 1 = bq29330 enters the sleep mode.

STATE\_CONTROL b1 (SHIP): This bit is used to enter the ship power mode when Pack supply voltage is not applied.

- 0 = bq29330 in normal mode (default)
- 1 = bq29330 enters ship mode when pack voltage is removed.

STATE\_CONTROL b2 (WDDIS): This bit is used to enable the watchdog timer.

- 0 = Watchdog timer enabled (default)
- 1 = Watchdog timer disabled

STATE\_CONTROL b3 (WDRST): This bit is used to enable the reset for GC, when watchdog timer is active.

- 0 = Reset output is disabled, when watchdog timer is active (default).
- 1 = 2 Times reset output is enabled, when watchdog timer is active.

STATE\_CONTROL b4 (RSNS): This bit sets the OL, SCC, and SCD thresholds into a range suitable for a low sense resistor value by dividing the OLV, SCCV, and SCDV selected voltage thresholds by 2.

- 0 = Current protection voltage threshold as programmed (default)
- 1 = Current protection voltage thresholds divided by 2 as programmed

STATE\_CONTROL b6..7 (0): These bits are not used and should be set to 0.

**FUNCTION\_CONTROL : Function control register**

FUNCTION_CTL REGISTER (0x03)							
7	6	5	4	3	2	1	0
0	0	0	0	TOUT	BAT	PACK	VMEN

The FUNCTION\_CONTROL register enables and disables features of the bq29330.

**FUNCTION\_CONTROL b0 (VMEN):** This bit enables or disables the cell and battery voltage monitoring function.

- 0 = Disable voltage monitoring (default). CELL output is pulled down to GND level.
- 1 = Enable voltage monitoring.

**FUNCTION\_CONTROL b1 (PACK):** This bit is used to translate the PACK input to the CELL+, CELL– pins when VMEN = 1. The PACK input voltage is divided by 18 and is presented on CELL+, CELL– pins regardless of the CELL\_SEL register settings.

- 0 = CELL\_SEL (b0, b1) settings determine CELL+, CELL– output when VMEN = 1 (default).
- 1 = PACK input translated to CELL output regardless of CELL\_SEL (b0, b1) selection when VMEN=1

**FUNCTION\_CTL b2 (BAT):** This bit is used to translate the BAT input to the CELL+, CELL– pins when VMEN=1. The VC5 input voltage is divided by 18 and is presented on CELL+, CELL– regardless of the CELL\_SEL register settings.

- 0 = CELL\_SEL (b0, b1) settings determine CELL+, CELL– output when VMEN = 1 (default).
- 1 = BAT input translated to CELL+, CELL– output regardless of CELL\_SEL (b0, b1) selection when VMEN = 1

This bit priority is higher than PACK(b1).

**FUNCTION\_CONTROL b3 (TOUT):** This bit controls the power to the thermistor.

- 0 = Thermistor power is off (default)
- 1 = Thermistor power is on

**CELL\_SEL : Cell select register**

CELL_SEL REGISTER (0x04)							
7	6	5	4	3	2	1	0
CB3	CB2	CB1	CB0	CAL1	CAL0	CELL1	CELL0

This register determines cell selection for voltage measurement and translation, cell balancing, and the operational mode of the cell voltage monitoring.

**CELL\_SEL b0-b1 (CELL0–CELL1):** These two bits select the series cell for voltage measurement translation.

CELL1	CELL0	SELECTED CELL
0	0	VC4-VC5, Bottom series element (default)
0	1	VC4-VC3, Second lowest series element
1	0	VC3-VC2, Second highest series element
1	1	VC1-VC2, Top series element

CELL\_SEL b2-b3 (CAL1, CAL0): These bits determine the mode of the voltage monitor block

CAL1	CAL0	SELECTED MODE
0	0	Cell translation for selected cell (default)
0	1	Offset measurement for selected cell
1	0	Monitor the VREF value for gain calibration
1	1	Monitor the $V_{REF}$ directly value for gain calibration, bypassing the translation circuit

CELL\_SEL b4-b7 (CB0 – CB3): These 4 bits select the series cell for cell balance bypass path.

CELL\_SEL b4 (CB0): This bit enables or disables the bottom series cell balance charge bypass path.

0 = Disable bottom series cell balance charge bypass path (default)

1 = Enable bottom series cell balance charge bypass path

CELL\_SEL b5 (CB1): This bit enables or disables the second lowest series cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

CELL\_SEL b6 (CB2): This bit enables or disables the second highest cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

CELL\_SEL b7 (CB3): This bit enables or disables the highest series cell balance charge bypass path.

0 = Disable series cell balance charge bypass path (default)

1 = Enable series cell balance charge bypass path

#### OLV: Overload Voltage threshold register

OLV REGISTER (0x05)							
7	6	5	4	3	2	1	0
0	0	0	OLV4	OLV3	OLV2	OLV1	OLV0

OLV (b4-b0): These four bits select the value of the overload threshold with a default of 0000.

OLV (b5-b7): These bits are not used and should be set to 0.

OLV (b4-b0) configuration bits with corresponding voltage threshold <sup>(1)</sup>							
0x00	–0.050 V	0x08	–0.090 V	0x10	–0.130 V	0x18	–0.170 V
0x01	–0.055 V	0x09	–0.095 V	0x11	–0.135 V	0x19	–0.175 V
0x02	–0.060 V	0x0a	–0.100 V	0x12	–0.140 V	0x1a	–0.180 V
0x03	–0.065 V	0x0b	–0.105 V	0x13	–0.145 V	0x1b	–0.185 V
0x04	–0.070 V	0x0c	–0.110 V	0x14	–0.150 V	0x1c	–0.190 V
0x05	–0.075 V	0x0d	–0.115 V	0x15	–0.155 V	0x1d	–0.195 V
0x06	–0.080 V	0x0e	–0.120 V	0x16	–0.160 V	0x1e	–0.200 V
0x07	–0.085 V	0x0f	–0.125 V	0x17	–0.165 V	0x1f	–0.205 V

(1) If RSNS bit is FUNCTION\_CONTROL = 1, then the corresponding voltage threshold is divided by 2.

**OLD: Overload Delay time configuration register**

OLD REGISTER (0x07)							
7	6	5	4	3	2	1	0
0	0	0	0	OLD3	OLD2	OLD1	OLD0

OLD(b3-b0): These four bits select the value of the delay time for overload with a default of 0000.

0x00	1 ms	0x04	9 ms	0x08	17 ms	0x0c	25 ms
0x01	3 ms	0x05	11 ms	0x09	19 ms	0x0d	27 ms
0x02	5 ms	0x06	13 ms	0x0a	21 ms	0x0e	29 ms
0x03	7 ms	0x07	15 ms	0x0b	23 ms	0x0f	31 ms

**SCC : Short Circuit In Charge configuration register**

SCC REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCCD3	SCCD2	SCCD1	SCCD0	SCCV3	SCCV2	SCCV1	SCCV0

This register selects the short circuit in charge voltage threshold and delay.

SCCV (b3-b0) : These lower nibble bits select the value of the short circuit in charge voltage threshold with 0000 as the default.<sup>(1)</sup>

0x00	0.100 V	0x04	0.200 V	0x08	0.300 V	0x0c	0.400 V
0x01	0.125 V	0x05	0.225 V	0x09	0.325 V	0x0d	0.425 V
0x02	0.150 V	0x06	0.250 V	0x0a	0.350 V	0x0e	0.450 V
0x03	0.175 V	0x07	0.275 V	0x0b	0.375 V	0x0f	0.475 V

(1) If RSNS bit is FUNCTION\_CTL = 1, then the corresponding voltage threshold is divided by 2.

SCCD (b7-b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the short circuit in charge voltage threshold for longer than this period turns off the CHG and DSG outputs. 0000 is the default.

0x00	0 $\mu$ s	0x04	244 $\mu$ s	0x08	488 $\mu$ s	0x0c	732 $\mu$ s
0x01	61 $\mu$ s	0x05	305 $\mu$ s	0x09	549 $\mu$ s	0x0d	793 $\mu$ s
0x02	122 $\mu$ s	0x06	366 $\mu$ s	0x0a	610 $\mu$ s	0x0e	854 $\mu$ s
0x03	183 $\mu$ s	0x07	427 $\mu$ s	0x0b	671 $\mu$ s	0x0f	915 $\mu$ s

**SCD : Short Circuit In Discharge configuration register**

SCD REGISTER (0x08)							
7	6	5	4	3	2	1	0
SCDD3	SCDD2	SCDD1	SCDD0	SCDV3	SCDV2	SCDV1	SCDV0

This register selects the short circuit in discharge voltage threshold and delay.

SCDV(b3-b0) : These lower nibble bits select the value of the short circuit in discharge voltage threshold with 0000 as the default.<sup>(1)</sup>

0x00	-0.100 V	0x04	-0.200 V	0x08	-0.300 V	0x0c	-0.400 V
0x01	-0.125 V	0x05	-0.225 V	0x09	-0.325 V	0x0d	-0.425 V
0x02	-0.150 V	0x06	-0.250 V	0x0a	-0.350 V	0x0e	-0.450 V
0x03	-0.175 V	0x07	-0.275 V	0x0b	-0.375 V	0x0f	-0.475 V

(1) If RSNS bit is FUNCTION\_CTL = 1, then the corresponding voltage threshold is divided by 2.

SCCD (b7-b4): These upper nibble bits select the value of the short circuit in charge delay time. Exceeding the Short Circuit in charge voltage threshold for longer than this period will turn off the CHG and DSG outputs. 0000 is the default.

0x00	0 $\mu$ s	0x04	244 $\mu$ s	0x08	488 $\mu$ s	0x0c	732 $\mu$ s
0x01	61 $\mu$ s	0x05	305 $\mu$ s	0x09	549 $\mu$ s	0x0d	793 $\mu$ s
0x02	122 $\mu$ s	0x06	366 $\mu$ s	0x0a	610 $\mu$ s	0x0e	854 $\mu$ s
0x03	183 $\mu$ s	0x07	427 $\mu$ s	0x0b	671 $\mu$ s	0x0f	915 $\mu$ s

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
BQ29330DBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ29330DBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ29330DBTR	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ29330DBTRG4	ACTIVE	TSSOP	DBT	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29330DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29330DBTR	TSSOP	DBT	30	2000	346.0	346.0	33.0

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