PowerLAN™ Master Gateway Battery Management Controller With PowerPump™ Cell Balancing Technology

Check for Samples: bq78PL116

FEATURES

- **bq78PL116 Designed for Managing 3- to 16-Series-Cell Battery Systems**
  - **Support for LCD and Electronic Paper Displays or EPDs**
  - **Configurable for 11-A, 26-A, or 110-A Operating Currents**
- **Systems With More Than Four Series Cells Require External bq76PL102 Dual-Cell Monitors**
- **SmartSafety Features:**
  - **Prevention: Optimal Cell Management**
  - **Diagnosis: Improved Sensing of Cell Problems**
  - **Fail Safe: Detection of Event Precursors**
- **Rate-of-Change Detection of All Important Cell Characteristics:**
  - **Voltage**
  - **Impedance**
  - **Cell Temperature**
- **PowerPump Technology Transfers Charge Efficiently From Cell to Cell During All Operating Conditions, Resulting in Longer Run Time and Cell Life**
  - **Includes User-Configurable PowerPump Cell-Balancing Modes**
- **High-Resolution 18-Bit Integrating Delta-Sigma Coulomb Counter for Precise Charge-Flow Measurements and Gas Gauging**
- **Multiple Independent Δ-Σ ADCs: One-per-Cell Voltage, Plus Separate Temperature, Current, and Safety**
- **Simultaneous, Synchronous Measurement of Pack Current and Individual Cell Voltages**
- **Very Low Power Consumption**
  - **< 300 μA Active, < 185 μA Standby, < 85 μA Ship, and < 1 μA Undervoltage Shutdown**
- **Accurate, Advanced Temperature Monitoring of Cells and MOSFETs With up to 4 Sensors**
- **Fail-Safe Operation of Pack Protection Circuits: Up to Three Power MOSFETs and One Secondary Safety Output (Fuse)**
- **Fully Programmable Voltage, Current, Balance, and Temperature-Protection Features**
- **External Inputs for Auxiliary MOSFET Control**
- **Smart Battery System 1.1 Compliant via SMBus**

APPLICATIONS

- **Portable Medical Instruments and Test Equipment**
- **Mobility Devices (E-Bike)**
- **Uninterruptible Power Supplies and Hand-Held Tools**

DESCRIPTION

The bq78PL116 master gateway battery controller is part of a complete Li-Ion control, monitoring, and safety solution designed for large series cell strings.

The bq78PL116 along with bq76PL102 PowerLAN™ dual-cell monitors provide complete battery-system control, communications, and safety functions for a structure of three up to 16 series cells. This PowerLAN system provides simultaneous, synchronized voltage and current measurements using one A/D per-cell technology. This eliminates system-induced noise from measurements and allows the precise, continuous, real-time calculation of cell impedance under all operating conditions, even during widely fluctuating load conditions.

PowerPump technology transfers charge between cells to balance their voltage and capacity. Balancing is possible during all battery modes: charge, discharge, and rest. Highly efficient charge-transfer circuitry nearly eliminates energy loss while providing true real-time balance between cells, resulting in longer run-time and improved cycle life.

ADVANCE INFORMATION

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Temperature is sensed by up to 4 external sensors and one on-chip sensor. This permits accurate temperature monitoring of each cell individually. Firmware is then able to compensate for the temperature-induced effects on capacity, impedance, and OCV on a cell-by-cell basis, resulting in superior charge/ discharge and balancing control.

External MOSFET control inputs provide user- definable direct hardware control over MOSFET states. Smart control prevents excessive current through MOSFET body diodes. Auxiliary inputs can be used for enhanced safety and control in large multicell arrays.

The bq78PL116 is completely user-configurable, with parametric tables in flash memory to suit a variety of cell chemistries, operating conditions, safety controls, and data reporting needs. It is easily configured using the supplied bqWizard™ graphical user interface (GUI). The device is fully programmed and requires no algorithm or firmware development.

The bq78PL116 pin functions of LED1/SEG1–LED5/SEG5, PSH/BP/TP, and FIELD support LED, LCD, and electronic paper displays (EPDs). The user can configure the bq78PL116 for the desired display type.

ADVANCE INFORMATION

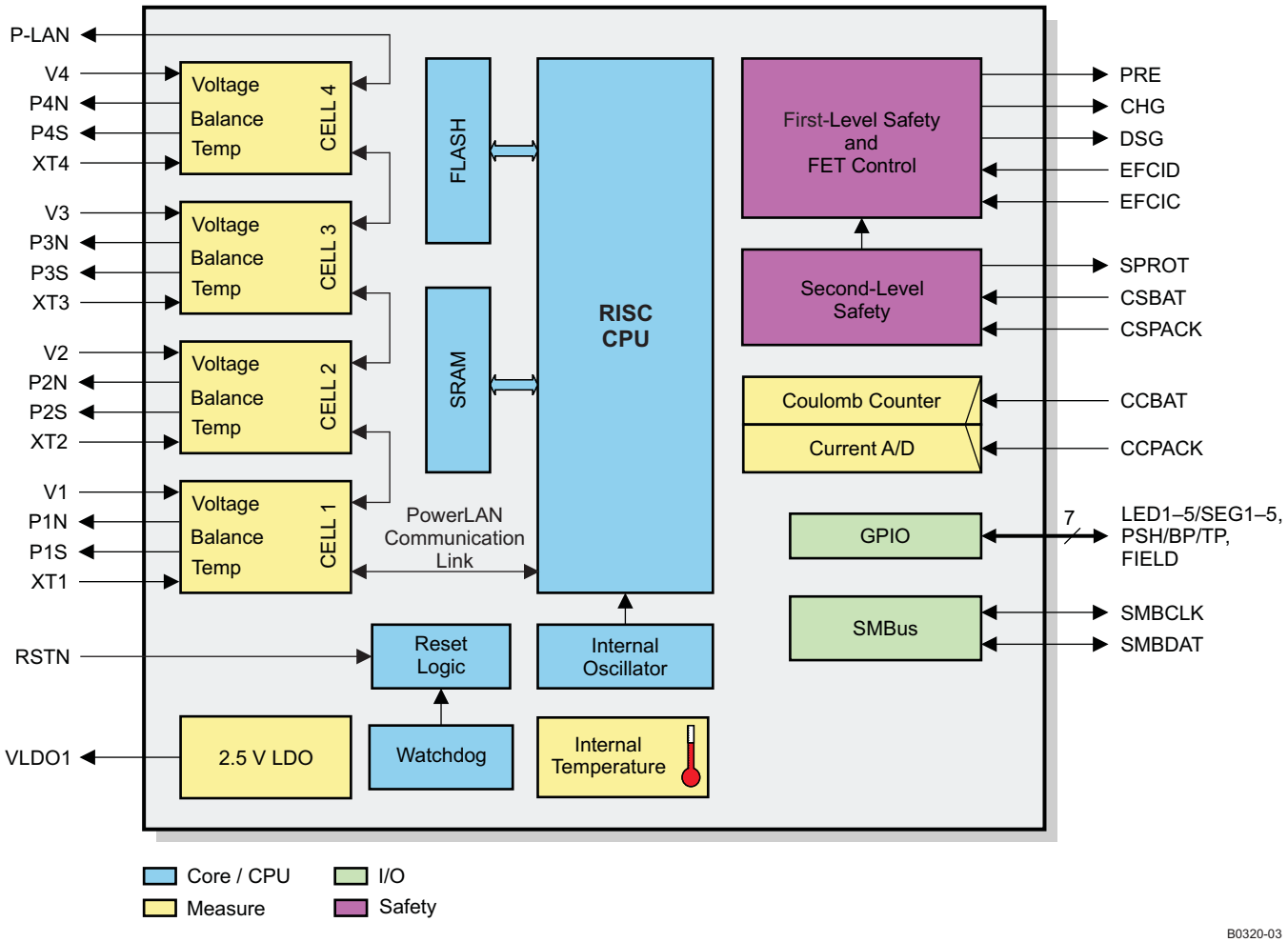


Figure 1. BQ78PL116 Internal Block Diagram

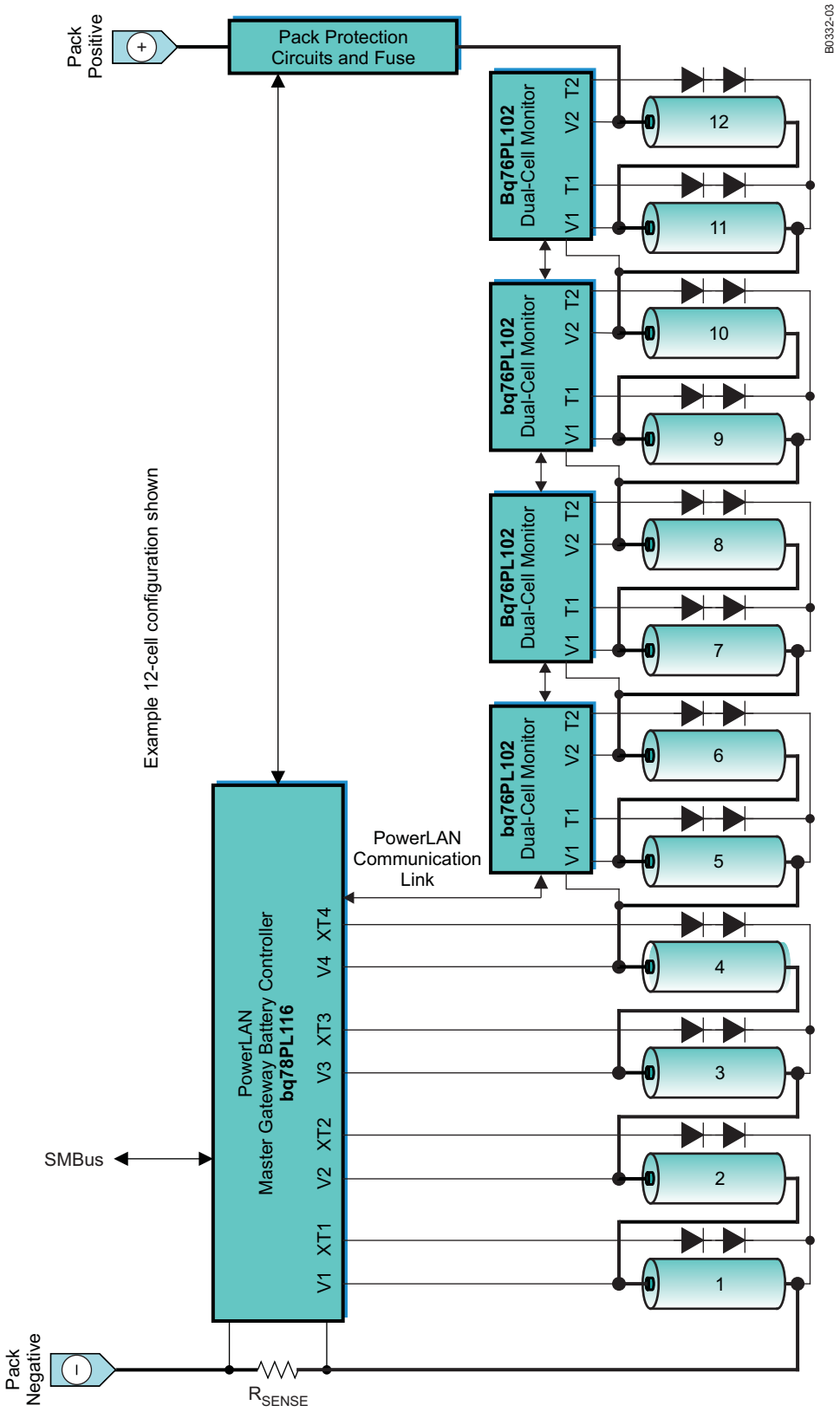


Figure 2. Example bq78PL116 System Implementation (12 Cells)

ADVANCE INFORMATION

Table 1. ORDERING INFORMATION

Product	Cell Configuration(1)	Package	Package Designator	Temperature Range	Ordering Number	Quantity, Transport Media
bq78PL116	3 to 16 series cells	QFN-48, 7-mm × 7-mm	RGZ	–40°C to 85°C	bq78PL116RGZT	250, tape and reel
					bq78PL116RGZR	2500, tape and reel

(1) For configurations consisting of more than four series cells, additional bq76PL102 parts must be used.

AVAILABLE OPTIONS

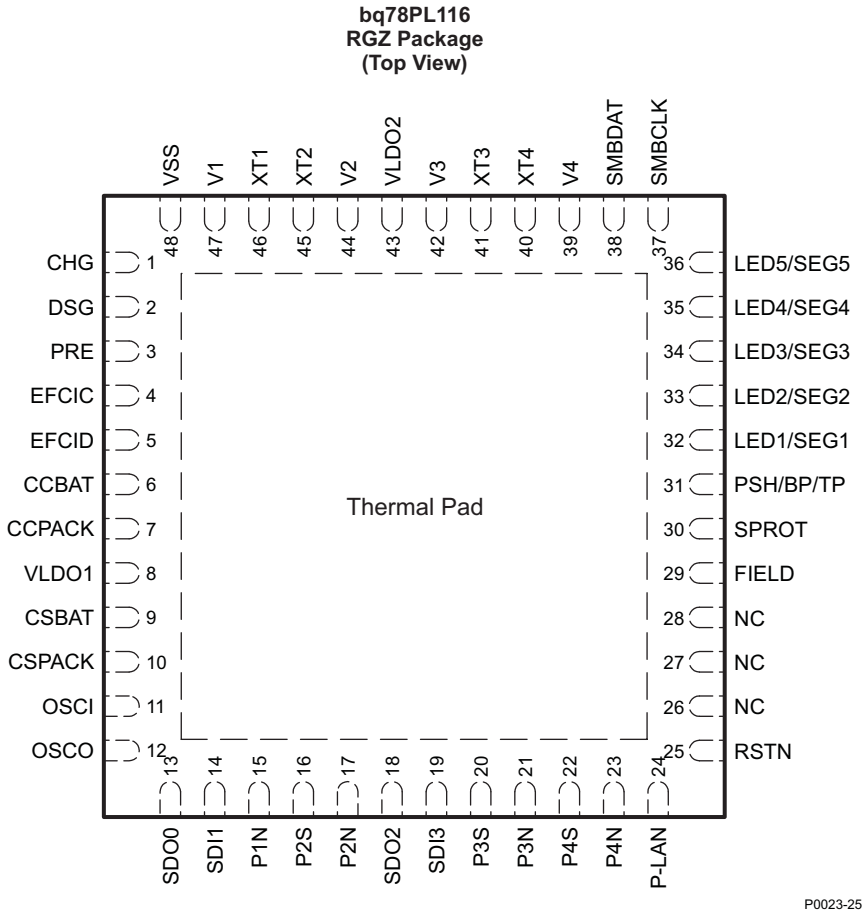


Figure 3. bq78PL116 Pinout

bq78PL116 TERMINAL FUNCTIONS

NAME	NO.	TYPE	DESCRIPTION
CCBAT	6	IA	Coulomb counter input (sense resistor), connect to battery negative
CCPACK	7	IA	Coulomb counter input (sense resistor), connect to pack negative
CHG	1	O	Charge MOSFET control (active-high, low opens MOSFET)
CSBAT	9	IA	Current sense input (safety), connect to battery negative
CSPACK	10	IA	Current sense input (safety), connect to pack negative
DSG	2	O	Discharge MOSFET control (active-high, low opens MOSFET)
EFCIC	4	I	External charge MOSFET control input
EFCID	5	I	External discharge MOSFET control input
FIELD	29	O	EPD field segment

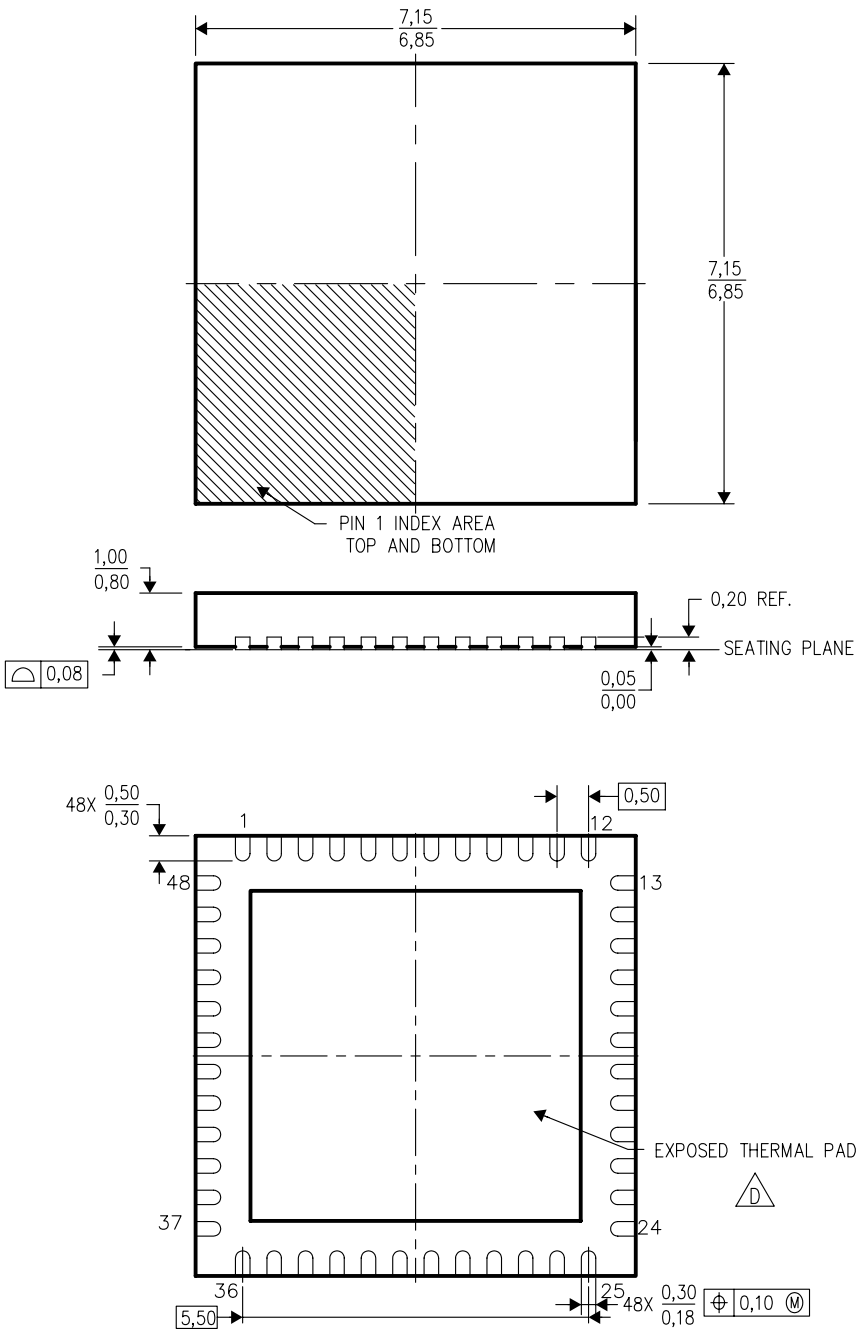
ADVANCE INFORMATION

bq78PL116 TERMINAL FUNCTIONS (continued)

NAME	NO.	TYPE	DESCRIPTION
LED1/SEG1	32	O	LED1 – open-drain, active-low, LCD and EPD segment 1
LED2/SEG2	33	O	LED2 – open-drain, active-low, LCD and EPD segment 2
LED3/SEG3	34	O	LED3 – open-drain, active-low, LCD and EPD segment 3
LED4/SEG4	35	O	LED4 – open-drain, active-low, LCD and EPD segment 4
LED5/SEG5	36	O	LED5 – open-drain, active-low, LCD and EPD segment 5
N/C	26, 27	IO	Connect 1-MΩ resistor to VSS
N/C	28	O	No connect
OSCI	11	I	External oscillator input (no connect, internal oscillator used)
OSCO	12	O	External oscillator output (no connect, internal oscillator used)
P1N	15	O	Charge-balance gate drive, cell 1 north
P2N	17	O	Charge-balance gate drive, cell 2 north
P2S	16	O	Charge-balance gate drive, cell 2 south
P3N	21	O	Charge-balance gate drive, cell 3 north
P3S	20	O	Charge-balance gate drive, cell 3 south
P4N	23	O	Charge-balance gate drive, cell 4 north
P4S	22	O	Charge-balance gate drive, cell 4 south
P-LAN	24	IO	PowerLAN I/O to external bq76PL102 nodes
PRE	3	O	Precharge MOSFET control (active-high)
PSH/BP/TP	31	IO	Pushbutton detect for LED display, LCD backplane, EPD top plane and charge pump
RSTN	25	I	Device reset, active-low
SDI1	14	I	Connect to SDO0 via a capacitor
SDI3	19	I	Internal PowerLAN connection – connect to SDO2 through a 0.01-μF capacitor
SDO0	13	O	Requires 100-kΩ pullup resistor to VLDO1
SDO2	18	O	Internal PowerLAN connection – connect to SDI3 through a 0.01-μF capacitor
SMBCLK	37	IO	SMBus clock signal
SMBDAT	38	IO	SMBus data signal
SPROT	30	O	Secondary protection output, active-high (FUSE)
V1	47	IA	Cell-1 positive input
V2	44	IA	Cell-2 positive input
V3	42	IA	Cell-3 positive input
V4	39	IA	Cell-4 positive input
VLDO1	8	P	Internal LDO-1 output, bypass with 10-μF capacitor to VSS
VLDO2	43	P	Internal LDO-2 output, bypass with 10-μF capacitor to V2
VSS	48	IA	Cell-1 negative input
XT1	46	IA	External temperature-sensor-1 input
XT2	45	IA	External temperature-sensor-2 input
XT3	41	IA	External temperature-sensor-3 input
XT4	40	IA	External temperature-sensor-4 input
–	–	P	Thermal pad. Connect to VSS

ADVANCE INFORMATION

RGZ (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

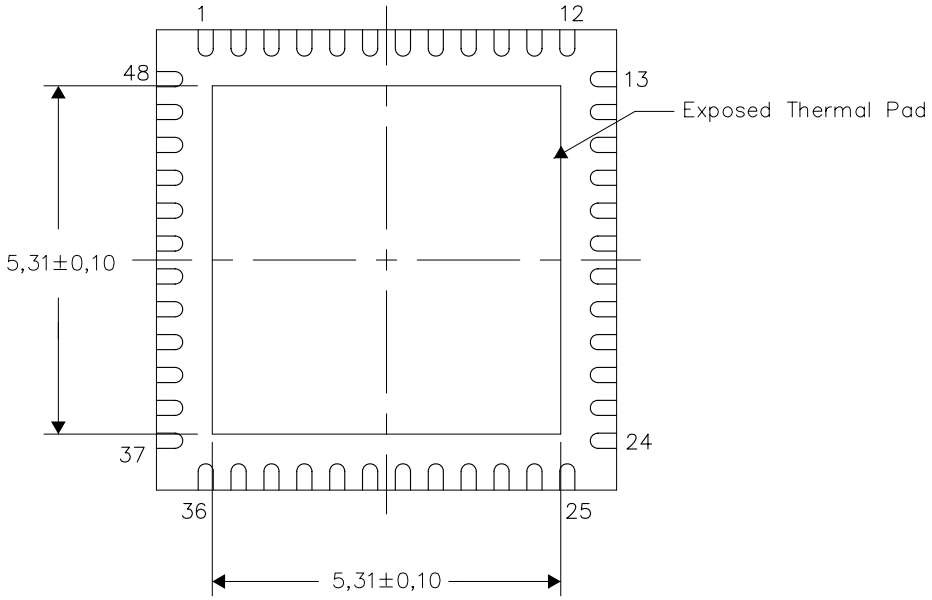
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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